freescale semiconductor

TWR-MEM

User's Manual

Rev. 1.2

Contents

1 Overview **4**

2 Reference Documents **4**

3 Hardware Features **5**

3.1 Power Supply 5
3.2 Serial Flash 5
3.3 MRAM 5
3.4 SD Card 5
3.5 CompactFlash 6
3.6 CPLD 6
3.7 Elevator Connections 8

4 Jumper Table **10**

4.1 Mechanical Form Factor 11

Revision History

Revision	Date	Changes
1.0	Jan, 2010	Initial Release
1.1	Feb 9, 2010	Corrections to SPI Flash, CPLD, and MRAM part numbers
1.2	April 20, 2010	Correction to default setting of J16

1 Overview

The Tower Memory Module (TWR-MEM) adds external memory and expansion I/O card support to the Tower System. It can be used with a wide variety of Tower Processor Modules with an SPI and/or external bus interface (EBI).

The TWR-MEM features a Serial Flash device, MRAM device, SD™ Card slot, and CompactFlash® slot. A CPLD is used to interface between the external bus interface (memory bus) of the host processor and the CompactFlash slot. This CPLD can also be used to prototype custom interfaces. A block diagram for the TWR-MEM is shown in the figure below.

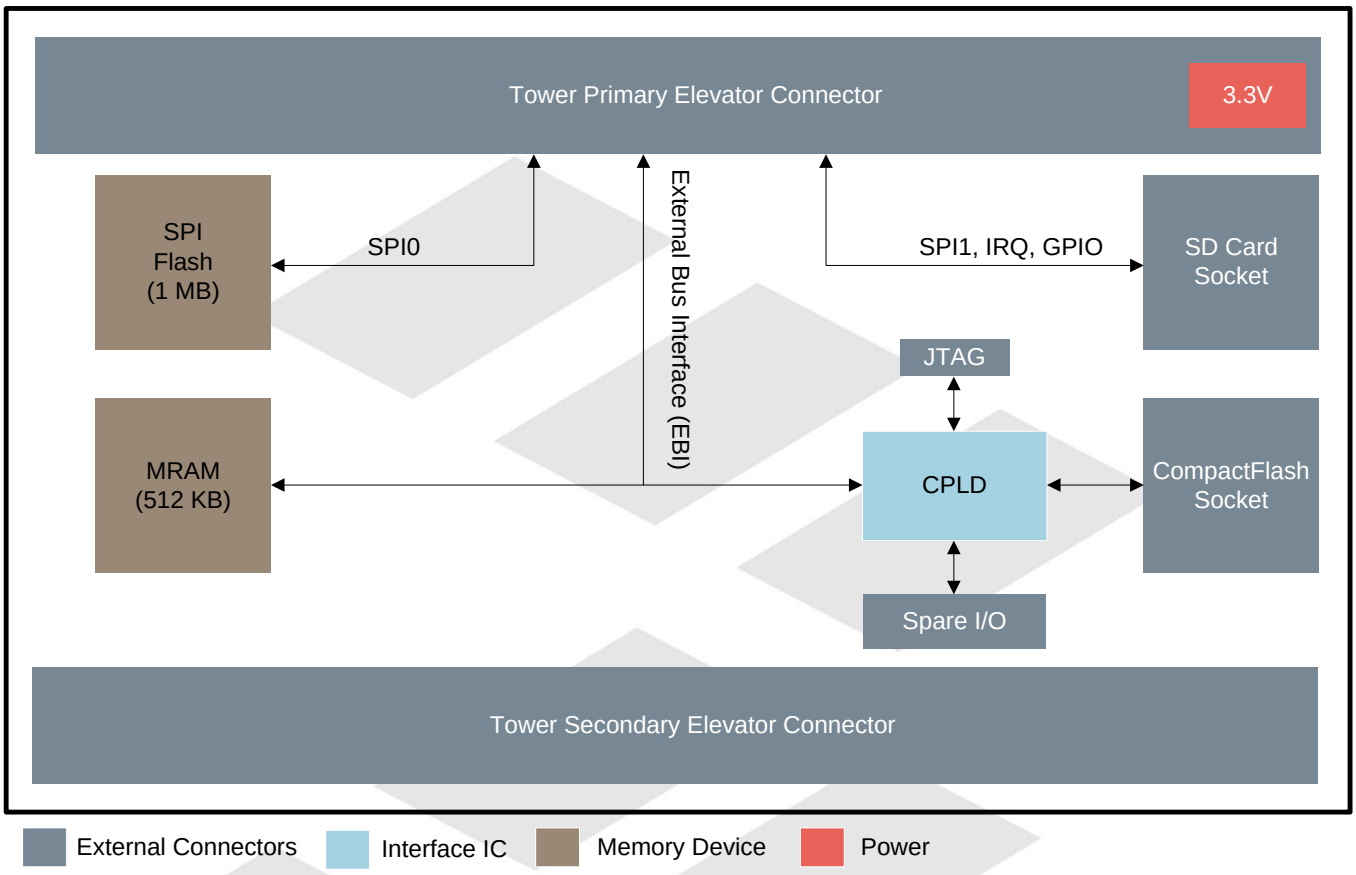

Figure 1. TWR-MEM Block Diagram

2 Reference Documents

The documents listed below should be referenced for more information on the Freescale Tower system and the TWR-MEM. Refer to http://www.freesale.com/tower for the latest revision of all Tower documentation.

- *TWR-MEM Schematics*
- *TWR-MEM Quick Start Guide*
- *Altera Max II CPLD Datasheet (EPM240GT100C3N)*
- *Altera Max II CPLD Product Website*
- *Everspin 4Mb MRAM Datasheet (MR2A16ACYS35)*
- *Atmel SPI Flash Datasheet (AT26DF081A-SU)*

3 Hardware Features

This section provides more details about the features and functionality of the TWR-MEM.

3.1 Power Supply

The TWR-MEM is powered from a source in an assembled Tower System via the 3.3V supply on the Primary Elevator Connector.

3.2 Serial Flash

An 8 Megabit (1 Mbyte) SPI Serial Flash is connected to the SPI0 interface of the Primary Elevator Connector. There are several configuration options that are controllable by jumper options J4 and J14. Refer to Table 3 "TWR-MEM Jumper Table "for details.

3.3 MRAM

An Everspin 512 Kbyte (256K x 16) magnetoresistive random access memory (MRAM) is connected to the External Bus Interface on the Primary Elevator Connector. The MRAM provides an SRAM compatible interface with non-volatile data.

There are a few configurable options on the MRAM interface controlled by shunt jumpers. Removing the shunt jumper on J10 allows the EBI chip-select, EBI_CS0_b, to be isolated from the MRAM to avoid conflicts with other EBI devices on the TWR-MEM (e.g. the CPLD/Compact Flash interface) or another Tower Module. EBI_CS0_b is connected to the MRAM's select signal by default. However, if EBI_CS0_b is selected to control the CPLD/Compact Flash interface (using J16), the shunt on J10 should be removed to avoid selecting both the MRAM and CPLD at the same time.

Additionally the MRAM can be write-protected by removing the shunt jumper on J15. This will isolate the MRAM's write-enable signal and the pull-device device will drive the signal to the read-only mode.

Refer to Table 3 for all of the configurable options on the TWR-MEM interfaces.

3.4 SD Card

The Tower System defines a Secure Digital interface as shown in Table 1. The SD Card interface is multiplexed over the SPI1 signals and four GPIOs such that the host can communicate with the SD memory or I/O (SDIO) card in the SD Card slot using the SPI mode or the one- or four-bit SD mode.

The TWR-MEM SD Card interface implements several configuration options to make it as flexible as possible. Refer to Table 3 for a complete list of the options.

When using SPI mode to communicate with the SD Card interface, the SPI chip-select can be configured using J3 to select between SPI1_CS1 and SPI1_CS0.

The SD Card Detect signal can be connected to IRQ_A and/or IRQ_H by placing a jumper shunt on J12[3:4] and/or J12[1:2], respectively. This will allow the host controller to monitor the presence of an SD memory or I/O card.

Table 1. Tower System SD Card Interface Pinout

Elevator Pin #	Name	Group	Description	I/O
B7	SDHC_CLK / SPI1_CLK	SDHC / SPI 1	SDHC or SPI Clock	O
B8	SDHC_D3 / SPI1_CS1_b	SDHC / SPI 1	SDHC Chip Select / Data or SPI Chip Select	O
B9	SDHC_D3 / SPI1_CS0_b	SDHC / SPI 1	SDHC Chip Select / Data or SPI Chip Select	O
B10	SDHC_CMD / SPI1_MOSI	SDHC / SPI 1	SDHC Command or SPI Master Out / Slave In	O
B11	SDHC_D0 / SPI1_MISO	SDHC / SPI 1	SDHC Data or SPI Master In / Slave Out	I
B22	GPIO2 / SDHC_D1	GPIO / SDHC	General Purpose I/O or SDHC Data	I/O
B52	GPIO5 / SD_CARD_DET	GPIO / SDHC	General Purpose I/O	I/O
A10	GPIO8 / SDHC_D2	GPIO / SDHC	General Purpose I/O or SDHC Data	I/O
A11	GPIO7 / SD_WP_DET	GPIO / SDHC	General Purpose I/O or SD Function	I/O

3.5 CompactFlash

The CompactFlash slot on the TWR-MEM can accept Type I (3.3mm thick) CF cards or PC Cards in the CompactFlash form factor. The CompactFlash slot is connected to the External Bus Interface (EBI) on the Primary Elevator Connector. An 8-bit data bus is implemented using EBI_D[7:0]. The necessary address and control signals are routed from the EBI and through a CPLD. This allows for the implementation of any glue logic that may be required depending on the protocol of the EBI of the host controller. Refer to Section 3.6 for details on the CPLD.

3.6 CPLD

TWR-MEM features an Altera Max II CPLD. Its primary purpose is to provide any interface logic required between the EBI and the CompactFlash slot. However, many of the IOs of the CPLD are also brought out to expansion headers for easy access when the CPLD is reprogrammed by the user for alternate purposes. Consult the schematics for details on the pinouts of the CPLD including the J7 and J9 expansion connectors.

The default program for the CPLD connects a ColdFire Flexbus interface to the CompactFlash slot. This implementation is very simple. However, other EBI protocols may require more advanced interface logic. A portion of the default CPLD program code is shown in Figure 2 below.

```
// connect reset directly
assign cf_reset = ~reset;

// connect cf_we and flexbus rw_b
assign cf_we = rw_b;

// connect cs directly
assign cf_ce = cs;

// connect directly oe for (active - zero during read)
assign cf_oe = oe;

// connect first 11 addr bytes directly on output
assign cf_address = address[10:0];

// connect addr bit n.12 directly on reg cf pin
assign cf_reg = address[12];

// card detection
always @(cf_cd) begin
        if (~cf_cd[0] & ~cf_cd[1]) begin
                data_reg  = 8'b11100101; // card is connected send (229 dec)
        end else begin
                data_reg  = 8'b10101101; // card is not connected (173 dec)
        end
end

// addr n.13 is used for card detecting
assign data = (~cs & ~oe & address[13])  ? data_reg : 8'bz;
```

Figure 2. Default CPLD Code Listing

The default CPLD code source and programmable image are available on the TWR-MEM tool support page (start at http://www.freescale.com/tower).

The CPLD can be reprogrammed using a JTAG interface cable via the standard JTAG connector, J5. In addition, J6 provides a means to connect GPIO signals from the Primary Elevator Connector to the JTAG signals on the CPLD so that a host controller can “bit-bang” the JTAG protocol (see Altera’s *AN 586: Porting the Jam STAPL and Jam STAPL Byte Code Players to an Embedded System*).

Refer to Altera’s Max II CPLD product website for complete CPLD documentation including getting started guides, free development tools and application examples.

3.7 Elevator Connections

The TWR-MEM features two expansion card-edge connectors that interface to Elevator boards in a Tower System: the Primary and Secondary Elevator connectors. The Primary Elevator connector, comprised of sides A and B, is utilized by the TWR-MEM, while the Secondary Elevator connector only makes connections to ground (GND). Table 2 provides the pinout for the Primary Elevator Connector. An "X" in the "Used" column indicated that there is a connection from the TWR-MEM to that pin on the Elevator connector. An "X" in the "Jmp" column indicates that a jumper is available that can configure or isolate the connection from the Elevator connector.

Table 2. TWR-MEM Primary Elevator Connector Pinout

TWR-MEM Primary Connector									
Pin	Name	Usage	Used	Jmp	Pin	Name	Usage	Used	Jmp
B1	**5V**				A1	**5V**			
B2	**GND**	**Ground**	X		A2	**GND**	**Ground**	X	
B3	**3.3V**	**3.3V Power**	X		A3	**3.3V**	**3.3V Power**	X	
B4	ELE_PS_SENSE				A4	**3.3V**	**3.3V Power**	X	
B5	**GND**	**Ground**	X		A5	**GND**	**Ground**	X	
B6	**GND**	**Ground**	X		A6	**GND**	**Ground**	X	
B7	SDHC_CLK / SPI1_CLK	SD Clock	X		A7	SCL0			
B8	SDHC_D3 / SPI1_CS1_b	SD Chip Select / Data3	X	X	A8	SDA0			
B9	SDHC_D3 / SPI1_CS0_b	SD Chip Select / Data3	X	X	A9	GPIO9 / CTS1	JTAG3 /	X	X
B10	SDHC_CMD / SPI1_MOSI	SD MOSI / Command	X		A10	GPIO8 / SDHC_D2	JTAG4 /	X	X
B11	SDHC_D0 / SPI1_MISO	SD MISO / Data0	X		A11	GPIO7 / SD_WP_DET	SD WP Detect	X	X
B12	ETH_COL				A12	ETH_CRS			
B13	ETH_RXER				A13	ETH_MDC			
B14	ETH_TXCLK				A14	ETH_MDIO			
B15	ETH_TXEN				A15	ETH_RXCLK			
B16	ETH_TXER				A16	ETH_RXDV			
B17	ETH_TXD3				A17	ETH_RXD3			
B18	ETH_TXD2				A18	ETH_RXD2			
B19	ETH_TXD1				A19	ETH_RXD1			
B20	ETH_TXD0				A20	ETH_RXD0			
B21	GPIO1 / RTS1	JTAG2	X	X	A21	SSI_MCLK			
B22	GPIO2 / SDHC_D1	SD Data1	X	X	A22	SSI_BCLK			
B23	GPIO3	JTAG1	X	X	A23	SSI_FS			
B24	CLKIN0				A24	SSI_RXD			
B25	CLKOUT1	CPLD GCLK3 (FB_CLK)	X	X	A25	SSI_TXD			
B26	**GND**	**Ground**	X		A26	**GND**	**Ground**	X	
B27	AN7				A27	AN3			
B28	AN6				A28	AN2			
B29	AN5				A29	AN1			
B30	AN4				A30	AN0			
B31	**GND**	**Ground**	X		A31	**GND**	**Ground**	X	
B32	DAC1				A32	DAC0			

TWR-MEM Primary Connector									
Pin	Name	Usage	Used	Jmp	Pin	Name	Usage	Used	Jmp
B33	TMR3				A33	TMR1			
B34	TMR2				A34	TMR0	CPLD GCLK2	X	
B35	GPIO4				A35	GPIO6			
B36	**3.3V**	**3.3V Power**	X		A36	**3.3V**	**3.3V Power**	X	
B37	PWM7				A37	PWM3			
B38	PWM6				A38	PWM2			
B39	PWM5				A39	PWM1			
B40	PWM4				A40	PWM0			
B41	CANRX0				A41	RXD0			
B42	CANTX0				A42	TXD0			
B43	1WIRE				A43	RXD1			
B44	SPI0_MISO	Serial Flash MISO	X		A44	TXD1			
B45	SPI0_MOSI	Serial Flash MOSI	X		A45	GPIO10			
B46	SPI0_CS0_b	Serial Flash Chip Select	X	X	A46	GPIO11			
B47	SPI0_CS1_b	Serial Flash Chip Select	X	X	A47	GPIO12			
B48	SPI0_CLK	Serial Flash Clock	X		A48	GPIO13			
B49	**GND**	**Ground**	X		A49	**GND**	**Ground**	X	
B50	SCL1				A50	GPIO14			
B51	SDA1				A51	GPIO15			
B52	GPIO5 / SD_CARD_DET	SD Detect	X	X	A52	GPIO16			
B53	USB0_DP_PDOWN				A53	GPIO17			
B54	USB0_DM_PDOWN				A54	USB0_DM			
B55	IRQ_H	SD Detect	X	X	A55	USB0_DP			
B56	IRQ_G				A56	USB0_ID			
B57	IRQ_F				A57	USB0_VBUS			
B58	IRQ_E				A58	TMR7			
B59	IRQ_D				A59	TMR6			
B60	IRQ_C				A60	TMR5			
B61	IRQ_B				A61	TMR4			
B62	IRQ_A	SD Detect	X	X	A62	RSTIN_b			
B63	EBI_ALE / EBI_CS1_b	CPLD Address Latch	X	X	A63	RSTOUT_b	CPLD Reset	X	
B64	EBI_CS0_b	CPLD / MRAM Chip Select	X	X	A64	CLKOUT0	CPLD GCLK3 (FB_CLK)	X	X
B65	**GND**	**Ground**	X		A65	**GND**	**Ground**	X	
B66	EBI_AD15	CPLD / MRAM	X		A66	EBI_AD14	CPLD / MRAM	X	
B67	EBI_AD16	CPLD / MRAM	X		A67	EBI_AD13	CPLD / MRAM	X	
B68	EBI_AD17	CPLD / MRAM	X		A68	EBI_AD12	CPLD / MRAM	X	
B69	EBI_AD18	CPLD / MRAM	X		A69	EBI_AD11	CPLD / MRAM	X	
B70	EBI_AD19	CPLD	X		A70	EBI_AD10	CPLD / MRAM	X	
B71	EBI_R/W_b	CPLD / MRAM	X	X	A71	EBI_AD9	CPLD / MRAM	X	
B72	EBI_OE_b	CPLD / MRAM	X		A72	EBI_AD8	CPLD / MRAM	X	
B73	EBI_D7	CPLD / MRAM	X		A73	EBI_AD7	CPLD / MRAM	X	
B74	EBI_D6	CPLD / MRAM	X		A74	EBI_AD6	CPLD / MRAM	X	
B75	EBI_D5	CPLD / MRAM	X		A75	EBI_AD5	CPLD / MRAM	X	
B76	EBI_D4	CPLD / MRAM	X		A76	EBI_AD4	CPLD / MRAM	X	
B77	EBI_D3	CPLD / MRAM	X		A77	EBI_AD3	CPLD / MRAM	X	

TWR-MEM Primary Connector									
Pin	Name	Usage	Used	Jmp	Pin	Name	Usage	Used	Jmp
B78	EBI_D2	CPLD / MRAM	X		A78	EBI_AD2	CPLD / MRAM	X	
B79	EBI_D1	CPLD / MRAM	X		A79	EBI_AD1	CPLD / MRAM	X	
B80	EBI_D0	CPLD / MRAM	X		A80	EBI_AD0	CPLD / MRAM	X	
B81	**GND**	**Ground**	X		A81	**GND**	**Ground**	X	
B82	**3.3V**	**3.3V Power**	X		A82	**3.3V**	**3.3V Power**	X	

4 Jumper Table

There are several jumpers provided for isolation, configuration, and feature selection. Refer to the following table for details. The default installed jumper settings are shown in *__bold__*.

Table 3. TWR-MEM Jumper Table

Jumper	Option	Setting	Description
J1	CPLD GCLK3 Selection	***1-2***	Connect GCLK3 to Tower CLKOUT1 (B25)
		2-3	Connect GCLK3 to Tower CLKOUT0 (A64)
J2	SD Card SPI Mode Select Pull Option	1-2	Pull-up on SD_D3 / SS (SPI Mode Select)
		2-3	Pull-down on SD_D3 / SS (SPI Mode Select)
		OFF	No pull resistor applied
J3	SD Card SPI Mode Chip-Select	***1-2***	Connect SD_D3 / SS to SPI1_CS0 (B9)
		2-3	Connect SD_D3 / SS to SPI1_CS1 (B8)
J4	Serial Flash Configuration Options	***1-2***	Connect Serial Flash Chip-Select to SPI CS selected by J14
		2-3	Enable Serial Flash Write Protect
		5-6	Connect Serial Flash HOLD signal to Tower GPIO5 (B52)
J6	JTAG / GPIO Connections	1-2	Connect GPIO8 (A10) to CPLD JTAG TMS signal
		3-4	Connect GPIO9 (A9) to CPLD JTAG TDO signal
		5-6	Connect GPIO1 (B21) to CPLD JTAG TDI signal
		7-8	Connect GPIO3 (B23) to CPLD JTAG TCK signal
J10	MRAM Chip-Select Isolation	***ON***	Connect EBI_CS0 to MRAM Chip-Select
		OFF	Disconnect EBI_CS0 from MRAM Chip-Select
J11	CPLD Flexbus CS0 Isolation	***ON***	Connect EBI_CS0 to CPLD pin 48
		OFF	Disconnect EBI_CS0 from CPLD
J12	SD Card Configuration Options	***1-2***	Connect SD Card Detect to IRQH (B55)
		3-4	Connect SD Card Detect to IRQA (B62)
		5-6	Connect SD_D1 to GPIO2 (B22)
		7-8	Connect SD_D2 to GPIO8 (A10)
		9-10	Apply pull-up to SD_CMD/MOSI
		11-12	Apply pull-up to SD_D0/MISO
J13	SD Card Write Protect Detect Isolation	***ON***	Connect SD Card Write Protect Detect to Tower GPIO7 (A11)
		OFF	Disconnect SD Card Write Protect Detect from Tower

Jumper	Option	Setting	Description
J14	Serial Flash Chip-Select	***1-2***	Connect Serial Flash Chip-Select to SPI0_CS0 (B46)
		2-3	Connect Serial Flash Chip-Select to SPI0_CS1 (B47)
J15	MRAM Write Protect	***ON***	Normal MRAM operation (R/W)
		OFF	Write protect MRAM
J16	CPLD Chip-Select Selection	1-2	Use EBI_CS0 as CPLD chip-select (pin 50)
		2-3	Use EBI_CS1 as CPLD chip-select (pin 50)

4.1 Mechanical Form Factor

The TWR-MEM is designed for the Freescale Tower System and complies with the mechanical specification as described in *Freescale Tower Mechanical Specification*.