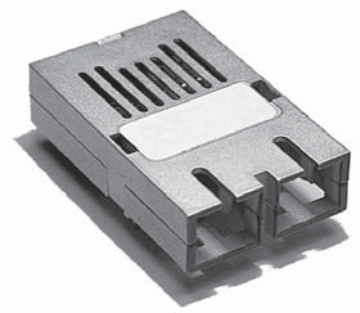
HFBR-5208xxxZ

1 x 9 Fiber Optic Transceivers for 622 Mb/s ATM/SONET/SDH Applications

Data Sheet



Description

General

The HFBR-5208xxxZ (multimode transceiver) from Avago allow the system designer to implement a range of solutions for ATM/SONET STS-12/SDH STM-4 applications.

The overall Avago transceiver consists of three sections: the transmitter and receiver optical subassemblies, an electrical subassembly and the mezzanine package housing which incorporates a duplex SC connector receptacle.

Transmitter Section

The transmitter section of the HFBR-5208xxxZ consists of a 1300 nm LED in an optical subassembly (OSA) which mates to the multimode fiber cable. The OSA's are driven by a custom, silicon bipolar IC which converts differential PECL logic signals (ECL referenced to a +5 V supply) into an analog LED drive current.

Receiver Section

The receiver contains an InGaAs PIN photodiode mounted together with a custom, silicon bipolar transimpedance preamplifier IC in an OSA. This OSA is mated to a custom, silicon bipolar circuit providing post amplification and quantization and optical signal detection.

The custom, silicon bipolar circuit includes a Signal Detect circuit which provides a PECL logic high state output upon detection of a usable input optical signal level. This single-ended PECL output is designed to drive a standard PECL input through normal 50 W PECL load.

Features

- Links of 500 m with 62.5/125 µm multimode fiber (MMF) from 155-622 Mb/s
- RoHS compliant
- Compliant with ATM forum 622.08 Mb/s physical layer specification (AF-PHY-0046.000)
- Compliant with ANSI broadband ISDN - physical layer specification T1.646-1995 and T1.646a-1997
- HFBR-5208xxxZ is compliant with ANSI network to customer installation interfaces - synchronous optical NETwork (SONET) physical media dependent specification: multimode fiber T1.416.01-1998
- Industry-standard multi-sourced 1 x 9 mezzanine package style
- Single +5 V power supply operation and PECL logic interfaces
- Wave solder and aqueous wash process compatible

Applications

- General purpose low-cost MMF links at 155 to 650 Mb/s
- ATM 622 Mb/s MMF links from switch-to-switch or switch-to-server in the end-user premise
- Private MMF interconnections at 622 Mb/s SONET STS-12/SDH STM-4 rate

Applications Information

Typical BER Performance of HFBR-5208xxxZ Receiver versus Input Optical Power Level

The HFBR-5208xxxZ transceiver can be operated at Bit-Error-Ratio conditions other than the required BER = 1 x 10^{-10} of the 622 MBd ATM Forum 622.08 Mb/s Physical Layer Standard and the ANSI T1.646a. The typical trade-off of BER versus Relative Input Optical Power is shown in Figure 1. The Relative Input Optical Power in dB is referenced to the Input Optical Power parameter value in the Receiver Optical Characteristics table. For better BER condition than 1 x 10^{-10}, more input signal is needed (+dB). For example, to operate the HFBR-5208xxxZ at a BER of 1 x 10^{-12}, the receiver will require an input signal approximately 0.6 dB higher than the -26 dBm level required for 1 x 10^{-10} operation, i.e. -25.4 dBm.

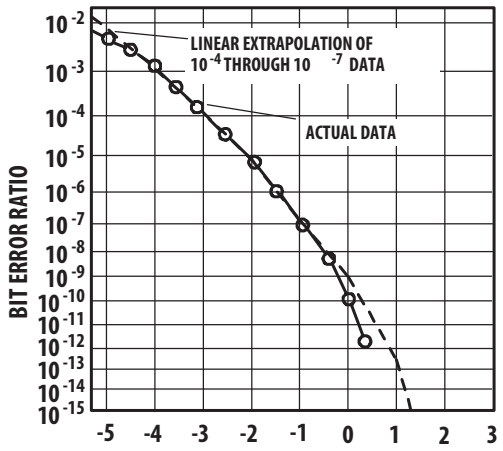


Figure 1. Relative Input Optical Power - dBm Average.

An informative graph of a typical, short fiber transceiver link per-formance can be seen in Figure 2. This figure is useful for designing short reach links with time-based jitter requirements. This figure indicates Relative Input Optical Power versus Sampling Time Position within the receiver output data eye-opening. The given curves are at a constant bit-error-ratio (BER) of 10^{-10} for four different signaling rates, 155 MBd, 311 MBd, 622 MBd and 650 MBd. These curves, called "tub" diagrams for their shape, show the amount of data eye-opening time-width for various receiver input optical power levels. A wider data eye-opening provides more time for the clock recovery circuit to operate within without creating errors. The deeper the tub is indicates less input optical power is needed to operate the receiver at the same BER condition. Generally, the wider and deeper the tub is the better. The Relative Input Optical Power amount (dB) is referenced to the absolute level (dBm avg.) given in the Receiver Optical Characteristics table. The 0 ns sampling time position for this Figure 2 refers to the center of the Baud interval for the particular signaling rate. The Baud interval is the reciprocal of the signaling rate in MBd. For example, at 622 MBd the Baud interval is 1.61 ns, at 155 MBd the Baud interval is 6.45 ns. Test conditions for this tub diagram are listed in Figure 2.

The HFBR-5208xxxZ receiver input optical power requirements vary slightly over the signaling rate range of 20 MBd to 700 MBd for a constant bit-error-ratio (BER) of 10^{-10} condition. Figure 3 illustrates the typical receiver relative input optical power varies by $\leq$0.7 dB over this full range. This small sensitivity variation allows the optical budget to remain nearly constant for designs that make use of the broad signaling rate range of the HFBR-5208xxxZ. The curve has been normalized to the input optical power level (dBm avg.) of the receiver for 622 MBd at center of the Baud interval with a BER of 10^{-10}. The data patterns that can be used at these signaling rates should be, on average, balanced duty factor of 50%. Momentary excursions of less or more data duty factor than 50% can occur, but the overall data pattern must remain balanced. Unbalanced data duty factor will cause excessive pulse-width distortion, or worse, bit errors. The test conditions are listed in Figure 3.

Recommended Circuit Schematic

When designing the HFBR-5208xxxZ circuit interface, there are a few fundamental guidelines to follow. For example, in the Recommended Circuit Schematic, Figure 4, the differential data lines should be treated as 50 ohm Microstrip or stripline transmission lines. This will help to minimize the parasitic inductance and capacitance effects. Proper termination of the differential data signal will prevent reflections and ringing which would compromise the signal fidelity and generate unwanted electrical noise. Locate termination at the received signal end of the transmission line. The length of these lines should be kept short and of equal length to prevent pulse-width distortion from occurring. For the high-speed signal lines, differential signals should be used, not single-ended signals. These differential signals need to be loaded symmetrically to prevent unbalanced currents from flowing which will cause distortion in the signal.

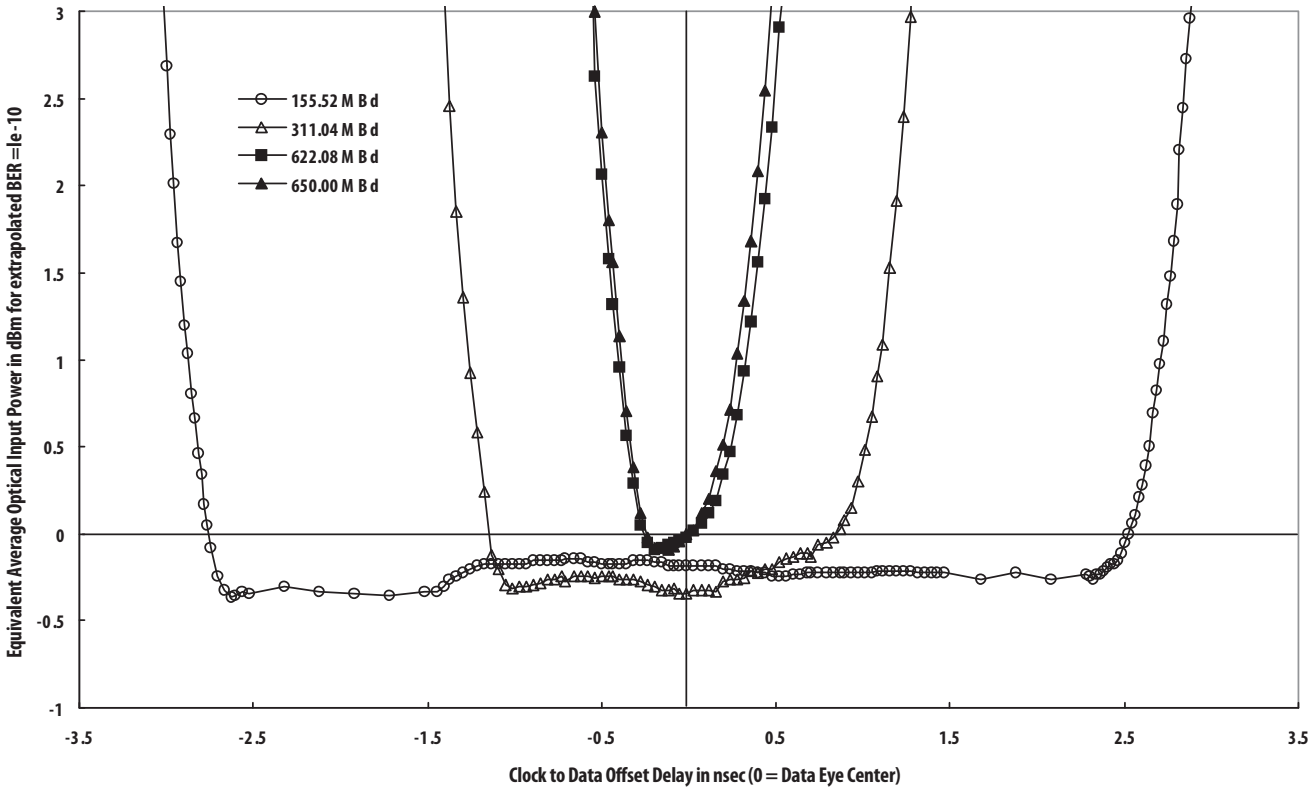


Figure 2. HFBR-5208xxMZ Relative Input Optical Power as a function of sampling time position. Normalized to center of Baud interval at 622 MBd. Test Conditions +25°C, 5.25 V, PRBS 2^{23}-1, optical $\tau_r/\tau_f = 0.9$ ns with 3 m of 62.5 µm MMF.

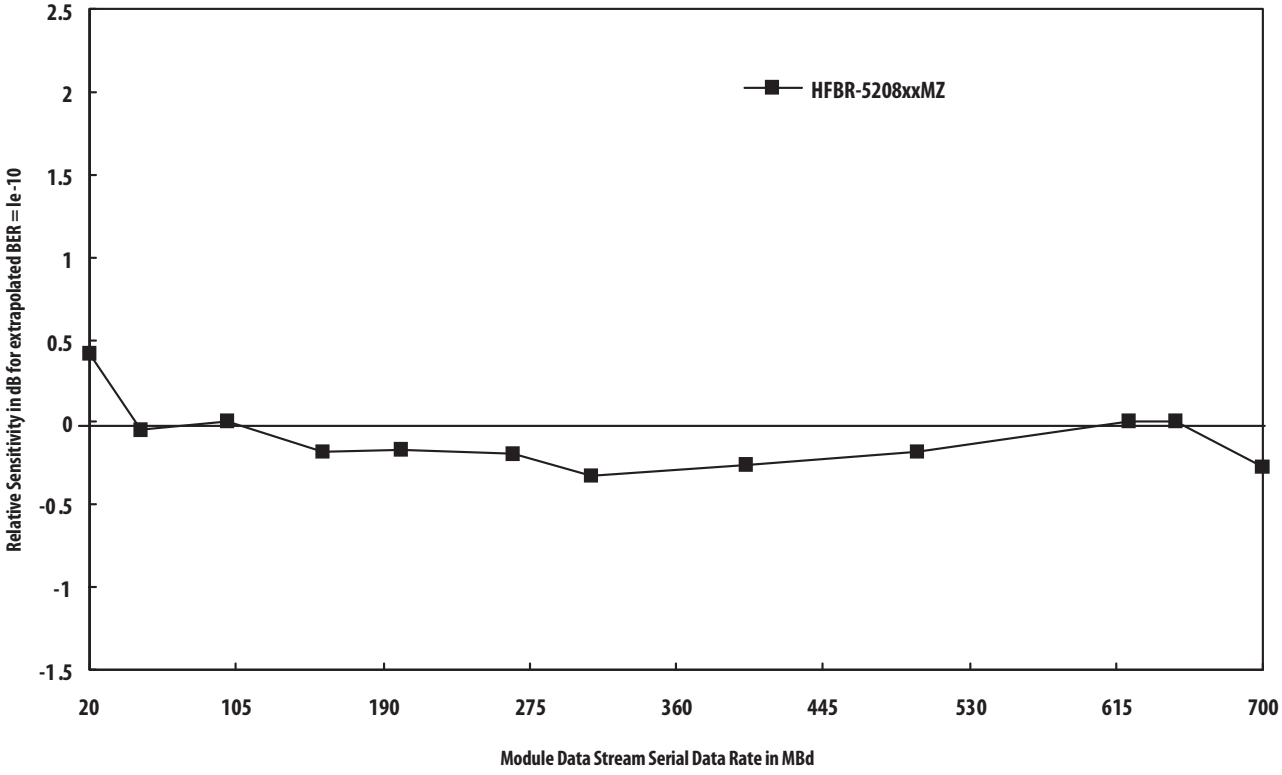


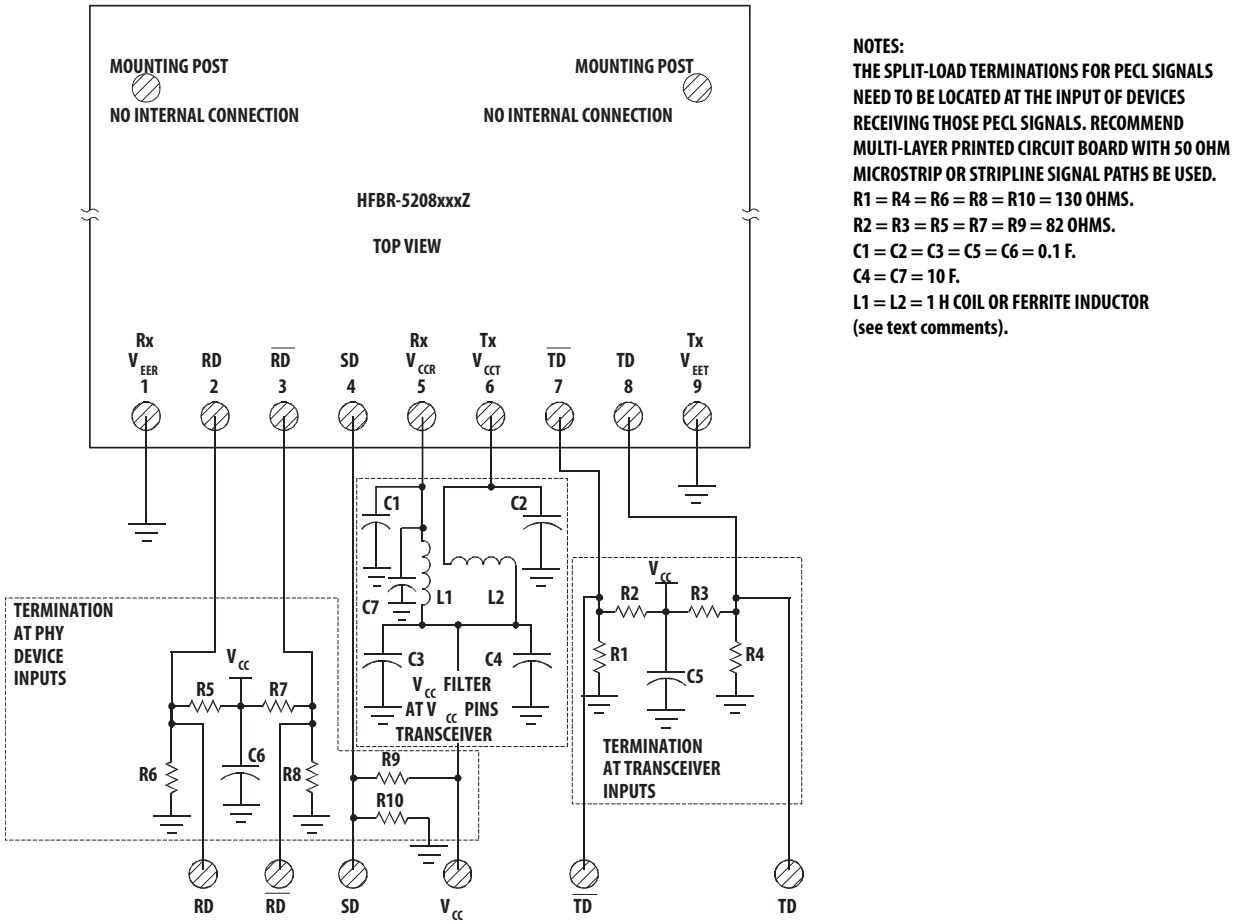
Figure 3. Relative Input Optical Power as a function of data rate normalized to center of Baud interval at 622 MBd. Test Conditions +25°C, 5.25 V, PRBS 2^{23}-1, optical $\tau_r/\tau_f = 0.9$ ns with 3 m of MMF or SMF.

Maintain a solid, low inductance ground plane for returning signal currents to the power supply. Multilayer plane printed circuit board is best for distribution of V_{CC}, returning ground currents, forming transmission lines and shielding. Also, it is important to suppress noise from influencing the fiber-optic transceiver per-formance, especially the receiver circuit. Proper power supply filtering of V_{CC} for this transceiver is accomplished by using the recommended separate filter circuits shown in Figure 4. These filter circuits suppress V_{CC} noise of 100 mV peak-to-peak or less over a broad frequency range. This prevents receiver sensitivity degradation . It is recommended that surface-mount components be used. Use tantalum capacitors for the 10 µF capacitors and monolithic, ceramic bypass capacitors for the 0.1 µF capacitors. Also, it is recommended that a surface-mount coil inductor of 1 µH be used. Ferrite beads can be used to replace the coil inductors when using quieter V_{CC} supplies, but a coil inductor is recommended over a ferrite bead to provide low-frequency noise filtering as well. Coils with a low, series dc resistance (<0.7 ohms) and high, self-resonating frequency are recommended. All power supply components need to be placed physically next to the V_{CC} pins of the receiver and transmitter. Use a good, uniform ground plane with a minimum number of holes to provide a low-inductance ground current return path for the signal and power supply currents.

Although the front mounting posts make contact with the metallized housing, these posts should not be relied upon to provide adequate electrical connection to the plated housing. It is recommended to either connect these front posts to chassis ground or allow them to remain unconnected. These front posts should not be connected to signal ground.

Figure 5 shows the recommended board layout pattern.

In addition to these recommendations, Avago Technologies Application Engineering staff is available for consulting on best layout practices with various vendors' serializer/deserializer, clock recovery/generation integrated circuits.



NOTES:
THE SPLIT-LOAD TERMINATIONS FOR PECL SIGNALS NEED TO BE LOCATED AT THE INPUT OF DEVICES RECEIVING THOSE PECL SIGNALS. RECOMMEND MULTI-LAYER PRINTED CIRCUIT BOARD WITH 50 OHM MICROSTRIP OR STRIPLINE SIGNAL PATHS BE USED.
R1 = R4 = R6 = R8 = R10 = 130 OHMS.
R2 = R3 = R5 = R7 = R9 = 82 OHMS.
C1 = C2 = C3 = C5 = C6 = 0.1 F.
C4 = C7 = 10 F.
L1 = L2 = 1 H COIL OR FERRITE INDUCTOR (see text comments).

Figure 4. Recommended Circuit Schematic for dc Coupling (at +5 V) between Optical Transceiver and Physical Layer IC

Reference Design

Avago has developed a reference design for multimode ATM-SONET/SDH applications shown in Figure 6. This reference design uses a Vitesse Semiconductor Inc.'s VSC8117 clock recovery/clock generation/serializer/deserializer integrated circuit and a PMC-Sierra Inc. PM5355 framer IC. Application Note 1178 documents the design, layout, testing and performance of this reference design. Gerber files, schematic and application note are available from the Avago Fiber-Optics Components' web site at the URL of **http://www.avagotech.com.**

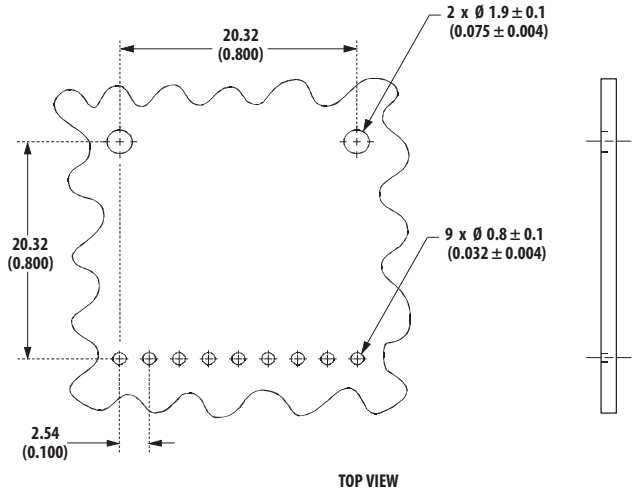


Figure 5. Recommended Board Layout Pattern

Operation in -5.2 V Designs

For applications that require -5.2 V dc power supply level for true ECL logic circuits, the HFBR-5208xxxZ transceiver can be operated with a V_{CC} = 0 V dc and a V_{EE} = -5.2 V dc. This transceiver is not specified with an operating, negative power supply voltage. The potential compromises that can occur with use of -5.2 V dc power are that the absolute voltage states for V_{OH} and V_{OL} will be changed slightly due to the 0.2 V difference in supply levels. Also, noise immunity may be compromised for the HFBR-5208xxxZ trans-ceiver because the ground plane is now the V_{CC} supply point. The suggested power supply filter circuit shown in the Recommended Circuit Schematic figure should be located in the V_{EE} paths at the transceiver supply pins. Direct coupling of the differential data signal can be done between the HFBR-5208xxxZ transceiver and the standard ECL circuits. For guaranteed -5.2 V dc operation, contact your local Avago Component Field Sales Engineer for assistance.

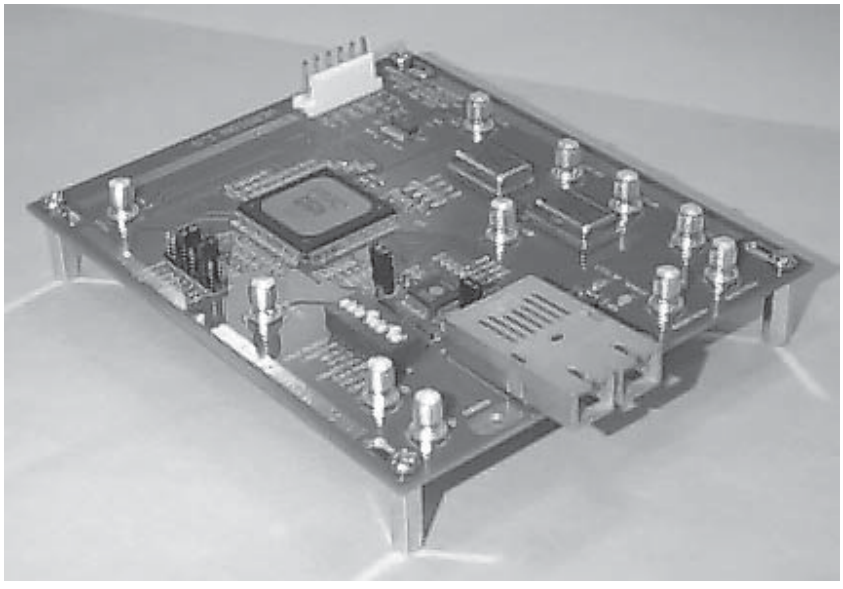


Figure 6. 622.08 Mb/s OC-12 ATM-SONET/SDH Reference Design Board

Electromagnetic Interference (EMI)

One of a circuit board designer's foremost concerns is the control of electromagnetic emissions from electronic equipment. Success in controlling generated Electromagnetic Interference (EMI) enables the designer to pass a governmental agency's EMI regulatory standard; and more importantly, it reduces the possibility of interference to neighboring equipment. There are three options available for the HFBR-5208xxxZ with regard to EMI shielding for providing the designer with a means to achieve good EMI performance. The EMI performance of an enclosure using these transceivers is dependent on the chassis design. Avago encourages using standard RF suppression practices and avoiding poorly EMI-sealed enclosures. In addition, Avago advises that for the best EMI performance, the metalized case must be connected to chassis ground using one of the shield options.

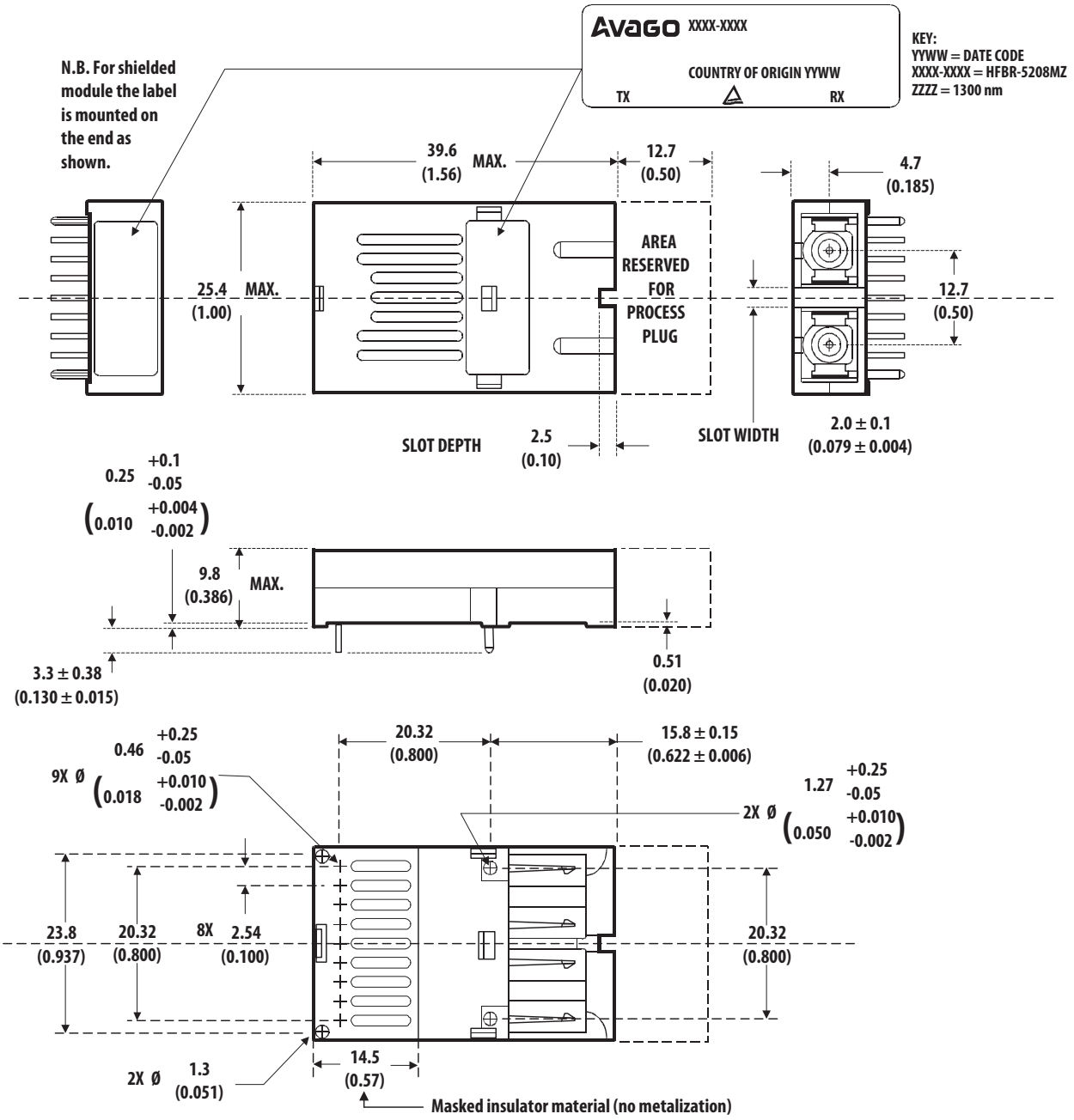
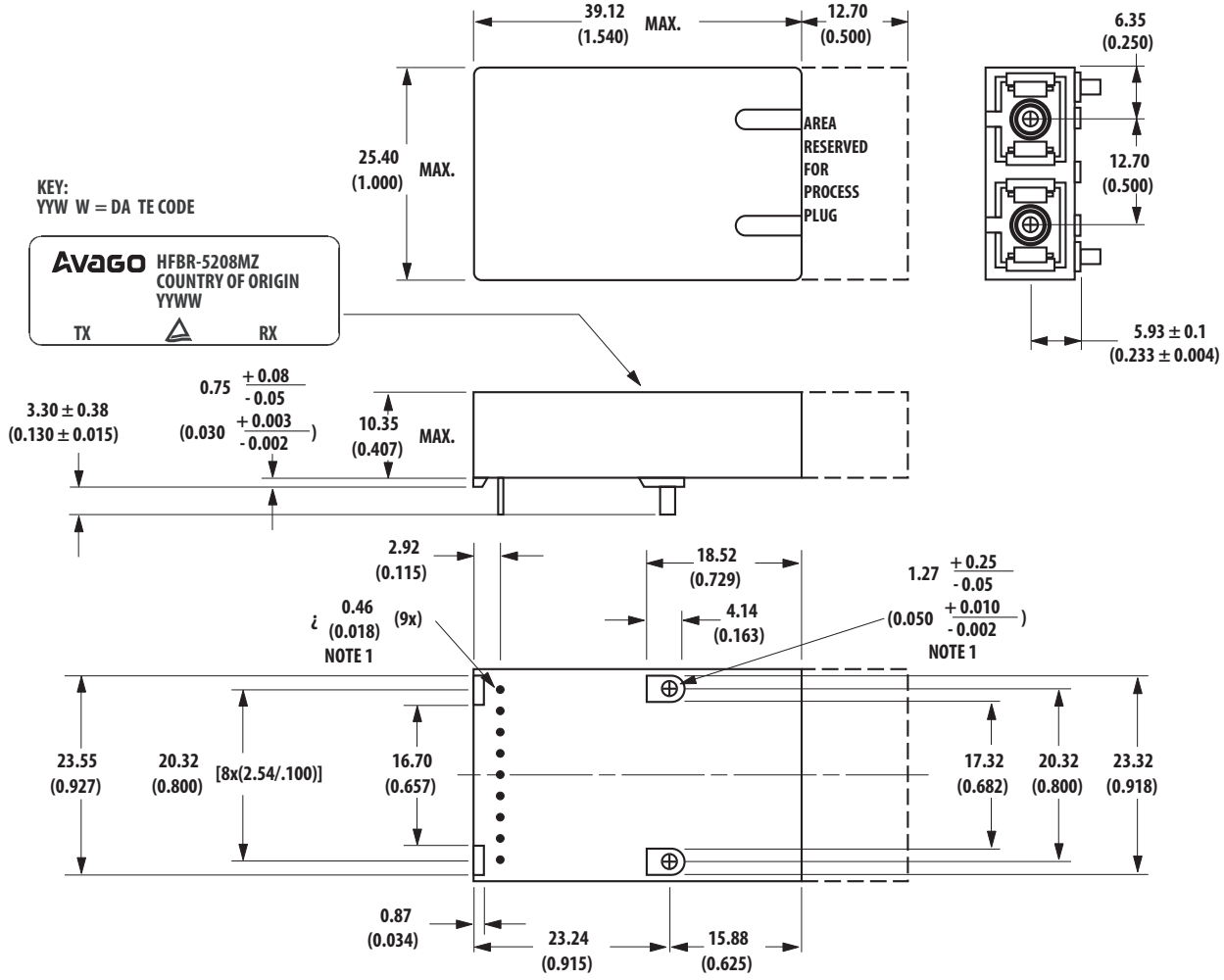


Figure 7a. Package Outline Drawing for HFBR-5208xxxZ



NOTE 1: PHOSPHOR BRONZE IS THE BASE MATERIAL FOR THE POSTS & PINS.
FOR LEAD-FREE SOLDERING, THE SOLDER POSTS HAVE TIN COPPER OVER
NICKEL PLATING, AND THE ELECTRICAL PINS HAVE PURE TIN OVER NICKEL PLATING.

DIMENSIONS ARE IN MILLIMETERS (INCHES).

Figure 7b. Package Outline Drawing for HFBR-5208MZ

An un-shielded option, shown in Figure 7a is available for the HFBR-5208xxxZ fiber optic transceiver. This unit is intended for applications where EMI is either not an issue for the designer, or the unit resides in a highly-shielded enclosure.

The first shielded option, option EM, is for applications where the position of the transceiver module will extend outside the equipment enclosure. The metallized plastic package and integral external metal shield of the transceiver helps locally to terminate EM fields to the chassis to prevent their emissions outside the enclosure. This metal shield contacts the panel or enclosure on the inside of the aperture on all but the bottom side of the shield and provides a good RF connection to the panel. This option can accommodate various panel or enclosure thicknesses, i.e. 1.02 mm (.04 in) min to 2.54 mm (0.1 in) max. The reference plane for this panel thickness variation is from the front surface of the panel or enclosure. The recommended length for protruding the HFBR-5208EMZ transceiver beyond the front surface of the panel or enclosure is 6.35 mm (0.25 in) . With this option, there is flexibility of positioning the module to fit the specific need of the enclosure design. (See Figure 8 for the mechanical drawing dimensions of this shield.)

The second shielded option, option FM, is for applications that are designed to have a flush mounting of the module with respect to the front of the panel or enclosure. The flush-mount design accommodates a large variety of panel thickness, i.e. 1.02 mm (.04 in) min to 2.54 mm (0.1 in) max. Note the reference plane for the flush-mount design is the interior side of the panel or enclosure. The recommended distance from the centerline of the transceiver front solder posts to the inside wall of the panel is 13.82 mm (0.544 in) . This option contacts the inside panel or enclosure wall on all four sides of this metal shield. (See Figure 10 for the mechanical drawing dimensions of this shield.)

Both shielded design options connect only to the equipment chassis and not to the signal or logic ground of the circuit board within the equipment closure. The front panel aperture dimensions are recommended in Figures 9 and 11. When layout of the printed circuit board is done to incorporate these metal-shielded transceivers, keep the area on the printed circuit board directly under the external metal shield free of any components and circuit board traces. For additional EMI performance advantage, use duplex SC fiber-optic connectors that have low metal content inside the connector. This lowers the ability of the metal fiber-optic connectors to couple EMI out through the aperture of the panel or enclosure.

Recommended Solder and Wash Process

The HFBR-5208xxxZ is compatible with industry-standard wave or hand solder processes.

HFBR-5000 Process Plug

The HFBR-5208xxxZ transceiver is supplied with a process plug, the HFBR-5000, for protection of the optical ports with the Duplex SC connector receptacle. This process plug prevents contamination during wave solder and aqueous rinse as well as during handling, shipping or storage. It is made of high-temperature, molded, sealing material that will withstand +85°C and a rinse pressure of 110 lb/in^2.

Recommended Solder Fluxes and Cleaning/Degreasing Chemicals

Solder fluxes used with the HFBR-5208xxxZ fiber-optic transceiver should be water-soluble, organic solder fluxes. Some recommended solder fluxes are Lonco 3355-11 from London Chemical West, Inc. of Burbank, CA, and 100 Flux from Alpha-metals of Jersey City, NJ or equivalent fluxes from other companies.

Recommended cleaning and degreasing chemicals for the HFBR-5208xxxZ are alcohols (methyl, isopropyl, isobutyl), aliphatics (hexane, heptane) and other chemicals, such as soap solution or naphtha. Do not use partially halogenated hydrocarbons for cleaning/degreasing. Examples of chemicals to avoid are 1,1.1 trichloroethane, ketones (such as MEK), acetone, chloroform, ethyl acetate, methylene dichloride, phenol, methylene chloride or N methylpyrolldone.

Regulatory Compliance

These transceiver products are intended to enable commercial system designers to develop equipment that complies with the various regulations governing certification of Information Technology Equipment. See the Regulatory Compliance Table for details. Additional information is available from your Avago sales representative.

Electrostatic Discharge (ESD)

There are two design cases in which immunity to ESD damage is important.

The first case is during handling of the transceiver prior to mounting it on the circuit board. It is important to use normal ESD handling precautions for ESD sensitive devices. These precautions include using grounded wrist straps, work benches, and floor mats in ESD controlled areas, etc.

The second case to consider is static discharges to the exterior of the equipment chassis containing the transceiver parts. To the extent that the duplex SC connector receptacle is exposed to the outside of the equipment chassis, it may be subject to whatever ESD system level test criteria that the equipment is intended to meet.

Electromagnetic Interference (EMI)

Most equipment designs utilizing these high-speed transceivers from Avago will be required to meet the requirements of FCC in the United States, CENELEC EN55022 (CISPR 22) in Europe and VCCI in Japan.

The HFBR-5208xxxZ EMI has been characterized with a chassis enclosure to demonstrate the robustness of the parts. Performance of a system containing these transceivers will vary depending on the individual chassis design.

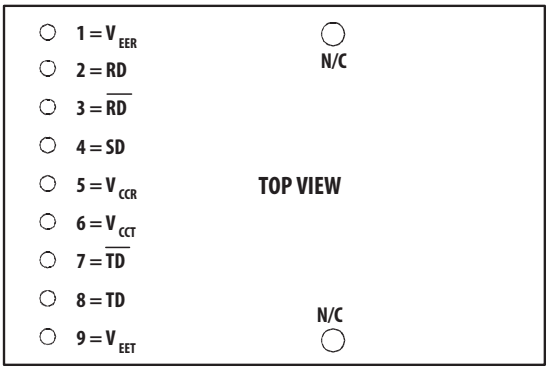
Immunity

Equipment utilizing these transceivers will be subject to radio-frequency electromagnetic fields in some environments. These transceivers, with their integral shields, have been characterized without the benefit of a normal equipment chassis enclosure and the results are reported below. Performance of a system containing these transceivers within a well- designed chassis is expected to be better than the results of these tests without a chassis enclosure.

Regulatory Compliance - Targeted Specifications

Feature	Test Method	Performance
Electrostatic Discharge (ESD)	MIL-STD-883F Method 3015.7	Class 1 (>1000 V) - Human Body Model
	RADIEC-61000-4-2	Products of this design typically withstand 25 kV without damage.
Electromagnetic Interference (EMI)	FCC Class B CENELEC EN55022 Class B (CISPR 22B) VCCI Class 2	Margins are dependant on customer board and chassis design.
Immunity	Variation of IEC 61000-4-3	Typically show no measurable effect from a 10 V/m field swept from 26 to 1000 MHz applied to the transceiver when mounted to a circuit card without a chassis enclosure.
Eye Safety	IEC 825-1 Class 1	LED Class 1
Component Recognition	Underwriters Laboratories and Canadian Standards Association Joint Component Recognition for Information Technology Equipment including Electrical Business Equipment	UL File#: E173874

The HFBR-5208xxxZ LED are classified as IEC 825-1 Accessible Emission Limit (AEL) Class 1. AEL Class 1 are considered eye safe.



N/C = NO INTERNAL CONNECTION (MOUNTING POSTS) - CONNECT TO CHASSIS GROUND OR LEAVE FLOATING, DO NOT CONNECT TO SIGNAL GROUND.

Table 1. Pinout Table

Pin	Symbol	Functional Description
Mounting Studs		The mounting studs are provided for transceiver mechanical attachment to the circuit boards, they are embedded in the metalized plastic housing and are not connected to the transceiver internal circuit. They should be soldered into plated-through holes on the printed circuit board and not connected to signal ground.
1	V_{EER}	Receiver Signal GroundDirectly connect this pin to receiver signal ground plane. Receiver V_{EER} and transmitter V_{EET} can connect to a common circuit board ground plane.
2	RD+	Receiver Data Out Terminate this high-speed, differential, PECL output with standard PECL techniques at the follow-on device input pin.
3	RD-	Receiver Data Out Bar Terminate this high-speed, differential, PECL output with standard PECL techniques at the follow-on device input pin.
4	SD	Signal Detect Normal input optical signal levels to the receiver result in a logic "1" output (V_{OH}).Low input optical signal levels to the receiver result in a fault condition indication shown by a logic "0" output (V_{OL}).If Signal Detect output is not used, leave it open-circuited.This Signal Detect output can be used to drive a PECL input on an upstream circuit, such as, Signal Detect input or Loss of Signal-bar.
5	V_{CCR}	Receiver Power Supply Provide +5 V dc via the recommended receiver V_{CCR} power supply filter circuit.Locate the power supply filter circuit as close as possible to the V_{CCR} pin.
6	V_{CCT}	Transmitter Power Supply Provide +5 V dc via the recommended transmitter V_{CCT} power supply filter circuit.Locate the power supply filter circuit as close as possible to the V_{CCT} pin.
7	TD-	Transmitter Data In Bar Terminate this high-speed, differential, Transmitter Data input with standard PECL techniques at the transmitter input pin.
8	TD+	Transmitter Data InTerminate this high-speed, differential, Transmitter Data input with standard PECL techniques at the transmitter input pin.
9	V_{EET}	Transmitter Signal GroundDirectly connect this pin to the transmitter signal ground plane. Transmitter V_{EET} and receiver V_{EER} can connect to a common circuit board ground plane.

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause catastrophic damage to the device. Limits apply to each parameter in isolation, all other parameters having values within the recommended operating conditions. It should not be assumed that limiting values of more than one parameter can be applied to the product at the same time. Exposure to the absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Storage Temperature	T_S	-40		+85	°C	
Lead Soldering Temperature	T_{SOLD}			+260	°C	
Lead Soldering Time	t_{SOLD}			10	sec.	
Supply Voltage	V_{CC}	-0.5		6.0	V	
Data Input Voltage	V_I	-0.5		V_{CC}	V	
Transmitter Differential Input Voltage	V_D			1.6	V	1
Output Current	I_D			50	mA	
Relative Humidity	RH	0		95	%	

Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Ambient Operating Temperature	T_A	0		+70	°C	
Ambient Operating Temperature	T_A	-40		+85	°C	
Supply Voltage	V_{CC}	4.75		5.25	V	
Power Supply Rejection	PSR		100		mV p-p	2
Transmitter Data Input Voltage - Low	V_{IL}-V_{CC}	-1.810		-1.475	V	3
Transmitter Data Input Voltage - High	V_{IH}-V_{CC}	-1.165		-0.880	V	3
Transmitter Differential Input Voltage	V_D	0.3		1.6	V	
Data Output Load	R_{DL}		50		W	4
Signal Detect Output Load	R_{SDL}		50		W	4

Notes:

1. This is the maximum voltage that can be applied across the Differential Transmitter Data Inputs without damaging the ESD protection circuit.
2. Tested with a 100 mV p-p sinusoidal signal in the frequency range from 500 Hz to 1 MHz imposed on the V_{CC} supply with the recommended power supply filter in place, see Figure 4. Typically less than a 0.5 dB change in sensitivity is experienced.
3. Compatible with 10K, 10KH and 100K ECL and PECL output signals.
4. The outputs are terminated to V_{CC} - 2 V.

HFBR-5208xxxZ Family, 1300 nm LED

Transmitter Electrical Characteristics

(T_A = 0°C to +70°C, V_{CC} = 4.75 to 5.25 V. Typical @+25°C, 5 V)

(T_A = -40°C to +85°C, V_{CC} = 4.75 to 5.25 V. Typical @+25°C, 5 V for A specification part)

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Supply Current	I_{CCT}		155	200	mA	1
Power Dissipation	P_{DIST}		0.75	1.05	W	
Data Input Current - Low	I_{IL}	-350			µA	
Data Input Current -High	I_{IH}			350	µA	

Receiver Electrical Characteristics

(T_A = 0°C to +70°C, V_{CC} = 4.75 to 5.25 V. Typical @+25°C, 5 V)

(T_A = -40°C to +85°C, V_{CC} = 4.75 to 5.25 V. Typical @+25°C, 5 V for A specification part)

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Supply Current	I_{CCR}		112	177	mA	
Power Dissipation	P_{DISR}		0.37	0.77	W	2
Data Output Voltage - Low	V_{OL} - V_{CC}	-1.950	-1.82	-1.620	V	3
Data Output Voltage - High	V_{OH} - V_{CC}	-1.045	-0.94	-0.740	V	3
Data Output Rise Time	t_R	0.2	0.3	0.51	ns	4
Data Output Fall Time	t_F	0.2	0.3	0.51	ns	4
Signal Detect Output Voltage - Low	V_{OL} - V_{CC}	-1.950	-1.82	-1.620	V	3
Signal Detect Output Voltage - High	V_{OH} - V_{CC}	-1.045	-0.94	-0.740	V	3
Signal Detect Assert Reaction Time(Off to On)	t_{SDA}		35	100	µs	5
Signal Detect Deassert Reaction Time (On to Off)	t_{SDD}		60	350	µs	6

Notes:

1. The I_{CC} value is held nearly constant to minimize unwanted electrical noise from being generated and conducted or emitted to neighboring circuitry.
2. Power dissipation value is the power dissipated in the receiver itself. It is calculated as the sum of the products of V_{CC} and I_{CC} minus the sum of the products of the output voltages and load currents.
3. These outputs are compatible with 10K, 10KH and 100K ECL and PECL inputs.
4. These are 20% - 80% values.
5. The Signal Detect output will change from logic "V_{OL}" to "V_{OH}" within 100 µs of a step transition in input optical power from no light to -26 dBm.
6. The Signal Detect output will change from logic "V_{OH}" to "V_{OL}" within 350 µs of a step transition in input optical power from -26 dBm to no light.

Transmitter Optical Characteristics

(T_A = 0°C to +70°C, V_{CC} = 4.75 to 5.25 V. Typical @+25°C, 5 V)

(T_A = -40°C to +85°C, V_{CC} = 4.75 to 5.25 V. Typical @+25°C, 5 V for A specification part)

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Output Optical Power 62.5/125 µm. NA = 0.275 fiber	P_O (BOL) P_O (EOL)	-19.5 -20	-17	-14 -14	dBm avg.	
Output Optical Power 50/125 µm. NA = 0.20 fiber	P_O (BOL) P_O (EOL)		-21.5 -22	-14 -14	dBm avg.	7
Output Optical Power at Logic "0" State	P_O ("0")		-60		dBm avg.	
Optical Extinction Ratio	ER	10	46		dB	
Center Wavelength	lc	1270	1330	1380	nm	
Spectral Width - FWHM	s		136	200	nm	8
Optical Rise Time	t_R		0.7	1.25	ns	9
Optical Fall Time	t_F		0.9	1.25	ns	9
Overshoot			0	25	%	
Systematic Jitter Contributed by the Transmitter	SJ		0.04	0.23	ns p-p	
Random Jitter Contributed by the Transmitter	RJ		0.0	0.10	ns p-p	

Notes:

7. The Output Optical Power is measured with the following conditions:
   - 1 meter of fiber with cladding modes removed.
   - The input electrical signal is a 12.5 MHz square wave.
   - The Beginning of Life (BOL) to End of Life (EOL) degradation is less than 0.5 dB.
8. The relationship between FWHM and RMS values for spectral width can be derived from the assumption of a Gaussian-shaped spectrum which results in RMS = FWHM/2.35.
9. These are 10-90% values.

Receiver Optical Characteristics

(T_A = 0°C to +70°C, V_{CC} = 4.75 to 5.25 V. Typical @+25°C, 5 V)
(T_A = -40°C to +85°C, V_{CC} = 4.75 to 5.25 V. Typical @+25°C, 5 V for A specification part)

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Minimum Input Optical Power at window edge	P_{IN} MIN (W)		-29.0	-26	dBm avg.	10 Fig 2
Minimum Input Optical Power at eye center	P_{IN} MIN (C)		-30.5		dBm avg.	10 Fig 2,3
Input Optical Power Maximum	P_{IN} MAX	-14	-11		dBm avg.	10
Input Operating Wavelength	l	1270		1380	nm	
Systematic Jitter Contributed by the Receiver	SJ		0.1	0.30	ns p-p	
Random Jitter Contributed by the Receiver	RJ		0.25	0.48	ns p-p	
Signal Detect - Asserted	P_A	P_D +1.0 dB	-30.5	-28	dBm avg.	
Signal Detect - Deasserted	P_D	-45	-33.7		dBm avg.	
Signal Detect - Hysteresis	P_A - P_D	1.0	3.2	5	dB	

Notes:

10. This specification is intended to indicate the performance of the receiver section of the transceiver when the input power ranges from the minimum level (with a window time-width) to the maximum level. Over this range the receiver is guaranteed to provide output data with a Bit Error Ratio (BER) better than or equal to 1 x 10^{-10}

- At the Beginning of Life (BOL)
- Over the specified operating temperature and voltage ranges
- Input is at 622.08 Mbd, 2^{23}-1 PRBS data pattern with 72 "1"s and 72 "0"s inserted per the CCITT (now ITU-T) recommendation G.958 Appendix 1.
- Receiver worst-case output data eye-opening (window time-width) is measured by applying worst-case input systematic (SJ) and randomjitter (RJ). The worst-case maximum input SJ = 0.5 ns peak-to-peak and the RJ = 0.15 ns peak-to-peak per ANSI T1.646a standard. Since the input (transmitter) random jitter contribution is very small and difficult to produce exactly, only the maximum systematic jitter is produced and used for testing the receiver. The corresponding receiver test window time-width must meet the requirement of 0.31 ns or larger. This worst-case test window time-width results from the following jitter equation: Minimum Test Window Time-Width = Baud Interval - Tx SJ max. - Rx SJ max. - Rx RJ max.
  espectively, Minimum Test Window Time-Width = 1.608 ns - 0.50 ns - 0.30 ns - 0.48 ns = 0.328 ns.
  This is a test method that is within practical test error of the worst-case 0.31 ns limit.
- Input optical rise and fall times (10% - 90%) are 0.7 ns and 0.9 ns respectively.
- Transmitter operating with a 622.08 MBd, 311.04 MHz square wave input signal to simulate any cross talk present between the transmitter and receiver sections of the transceiver.

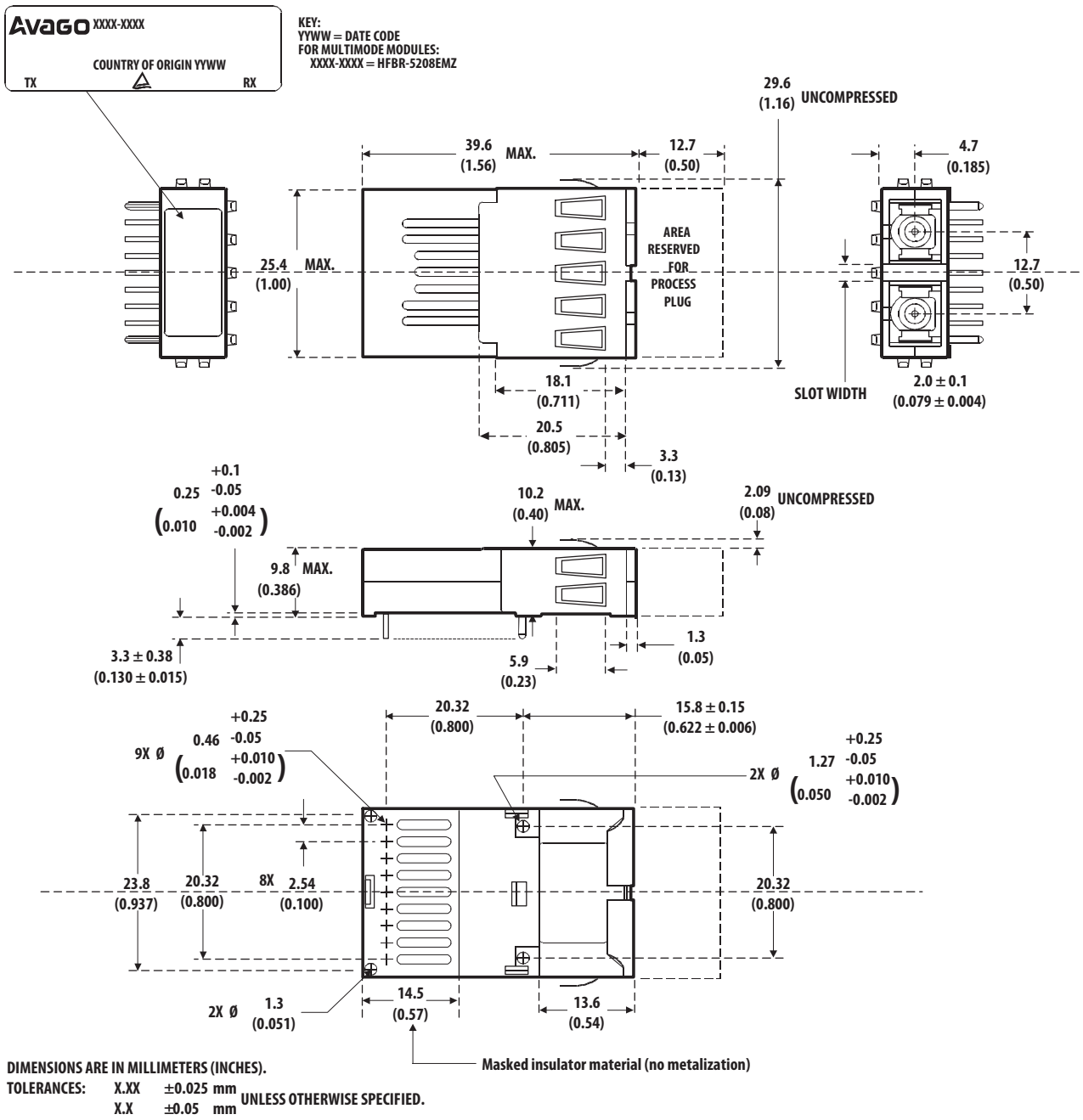
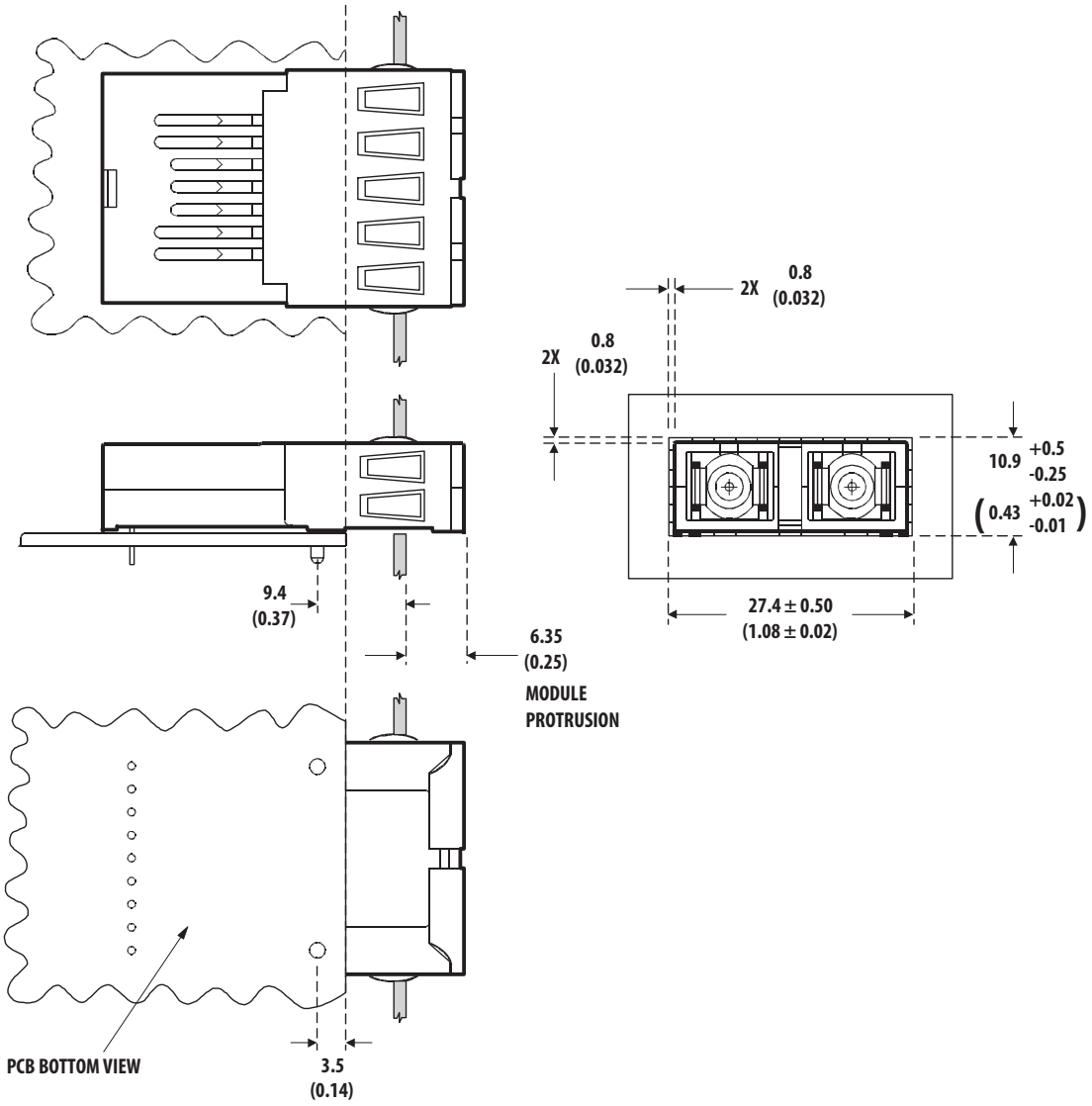


Figure 8. Package Outline for HFBR-5208EMZ



DIMENSIONS ARE IN MILLIMETERS (INCHES).
TOLERANCES: X.XX ±0.025 mm UNLESS OTHERWISE SPECIFIED.
X.X ±0.05 mm

Figure 9. Suggested Module Positioning and Panel Cut-out for HFBR-5208EMZ

Ordering Information

1300 nm LED (temperature range 0°C to +70°C)

HFBR-5208MZ	No shield, metallized housing.
HFBR-5208EMZ	Extended/protruding shield, metallized housing.

1300 nm LED (temperature range -40°C to +85°C)

HFBR-5208AMZ	No shield, metallized housing.
HFBR-5208AEMZ	Extended/protruding shield, metallized housing.

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

AV02-2549EN - February 9, 2012