19-3209; Rev 1; 2/09

EVALUATION KIT AVAILABLE

Low-Power Audio/Video Switch for Dual SCART Connectors

MAX9598

General Description

The MAX9598 dual SCART matrix routes audio and video signals between a set-top box decoder chip and two external SCART connectors under I²C control. Operating from a 3.3V supply and a 12V supply, the MAX9598 consumes 70mW during quiescent operation and 471mW during average operation when driving typical signals into typical loads. Video input detection, video load detection, and a 1.7mW low-power mode facilitate the design of low-power set-top boxes.

The MAX9598 audio section contains a buffered crosspoint to route audio inputs to audio outputs. The DirectDrive® output amplifiers create a $2V_{RMS}$ full-scale audio signal biased around ground, eliminating the need for bulky output capacitors and reducing click-and-pop noise. The zero-cross detection circuitry also further reduces clicks and pops by enabling audio sources to switch only during a zero-crossing.

The MAX9598 video section contains a buffered crosspoint to route video inputs to video outputs. The standard-definition video signals from the set-top box decoder chip are lowpass filtered to remove out-of-bandwidth artifacts.

The MAX9598 also supports slow-switching and fast-switching signals. An interrupt signal from the MAX9598 informs the microcontroller (µC) when the system status has changed.

The MAX9598 is available in a compact 40-pin thin QFN package and is specified over the 0°C to +70°C commercial temperature range.

DirectDrive is a registered trademark of Maxim Integrated Products, Inc.

Features

- **70mW Quiescent Power Consumption**
- **1.7mW Low-Power Mode Consumption**
- **0.1mW Shutdown Consumption**
- **Clickless/Popless, DirectDrive Audio**
- **Video Input Detection**
- **Video Load Detection**
- **Video Reconstruction Filter with 10MHz Passband and 52dB Attenuation at 27MHz**
- **3.3V and 12V Supply Voltages**

Applications

Set-Top Boxes

TVs

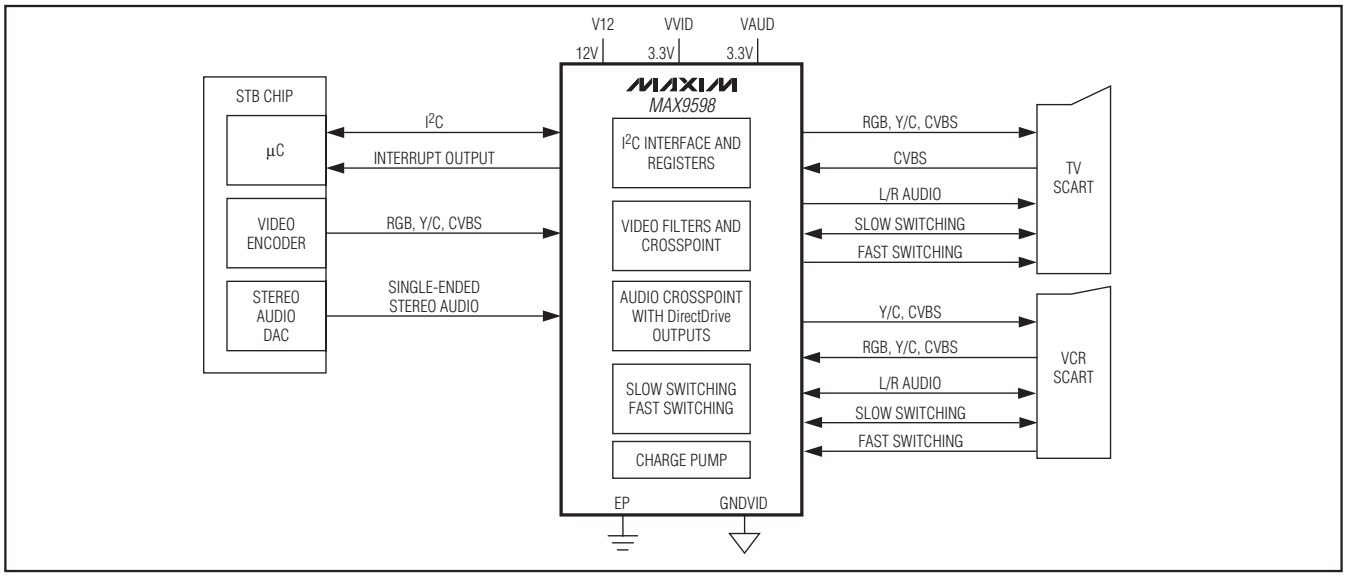
DVD Players

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9598CTL+	0°C to +70°C	40 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

System Block Diagram



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Low-Power Audio/Video Switch for Dual SCART Connectors

ABSOLUTE MAXIMUM RATINGS

VVID to GNDVID .....-0.3V to +4V
V12 to EP .....-0.3V to +14V
VAUD to EP .....-0.3V to +4V
EP to GNDVID .....-0.1V to +0.1V
All Video Inputs, VCRIN_FS to GNDVID .....-0.3V to +4V
All Audio Inputs to EP.....-1V to (EP + 1V)
SDA, SCL, DEV_ADDR, $\overline{INT}$ to GNDVID .....-0.3V to +4V
TV_SS, VCR_SS to EP .....-0.3V to (V12 + 0.3V)
Current
All Video/Audio Inputs.....±20mA
C1P, C1N, CPVSS.....±50mA
Output Short-Circuit Current Duration
All Video Outputs, TVOUT_FS to VVID, GNDVID...Continuous
Audio Outputs to VAUD, EP.....Continuous
TV_SS, VCR_SS to V12, EP.....Continuous
Continuous Power Dissipation (T_A = +70°C)
40-Pin Thin QFN
(derate 26.3mW/°C above +70°C).....2105.3mW
Operating Temperature Range .....0°C to +70°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V12 = 12V, VVID = VAUD = 3.3V, V_{GNDVID} = V_{EP} = 0V, no load, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Video Supply Voltage Range	VVID	Inferred from video PSRR test at 3V and 3.6V		3	3.3	3.6	V
Audio Supply Voltage Range	VAUD	Inferred from audio PSRR test at 3V and 3.6V		3	3.3	3.6	V
V12 Supply Voltage Range	V12	Inferred from slow-switching levels		11.4	12	12.6	V
VVID Quiescent Supply Current	I_{VID_Q}	Normal operation (Note 2), with all video outputs enabled and muted			18.2	30	mA
		Low-power mode			500	1000	µA
		Shutdown			18.4	32	
VAUD Quiescent Supply Current	I_{AUD_Q}	Normal operation (Note 2)			2.7	6	mA
		Shutdown			12	25	µA
V12 Quiescent Supply Current	I_{12_Q}	Normal operation (Note 2)	POR state		3	100	µA
			Slow-switching output sets to medium level		475		
		Shutdown			0.25	10	
VIDEO CHARACTERISTICS							
DC-COUPLED INPUT							
Input Voltage Range	V_{IN}	R_L = 75Ω to GNDVID or 150Ω to VVID/2, inferred from gain test	VVID = 3V		1.15		V_{P-P}
			VVID = 3.135V			1.2	
			VVID = 3.3V		1.3		
Input Current	I_{IN}	V_{IN} = 0.3V			1	5	µA
Input Resistance	R_{IN}				300		kΩ
AC-COUPLED INPUT							
Sync-Tip Clamp Level	V_{CLP}	Sync-tip clamp		-13	-3.5	+6	mV
Sync Crush		Sync-tip clamp, percentage reduction in sync pulse ($0.3V_{P-P}$), guaranteed by input clamping current measurement				2	%

ELECTRICAL CHARACTERISTICS (continued)

(V12 = 12V, VVID = VAUD = 3.3V, V_{GNDVID} = V_{EP} = 0V, no load, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Clamping Current		Sync-tip clamp, V_{IN} = 0.3V		1	2	µA
Maximum Input Source Resistance				300		Ω
Bias Voltage	V_{BIAS}	Bias circuit	0.57	0.60	0.63	V
Input Resistance		Bias circuit		10		kΩ
DC CHARACTERISTICS						
DC Voltage Gain	Av	Guaranteed by output-voltage swing	1.95	2	2.05	V/V
DC Gain Mismatch Between R, G, and B Outputs		Guaranteed by output-voltage swing of TV_R/C_OUT, TV_G_OUT, and TV_B_OUT; first input signal set is VCR_R/C_IN, VCR_G_IN, and VCR_B_IN; second signal set is ENC_R/C_IN, ENC_G_IN, and ENC_B_IN	-2		+2	%
Output Level		Sync-tip clamp (V_{IN} = V_{CLP})	0.19	0.30	0.40	V
		Bias circuit	1.35	1.50	1.62	
Output-Voltage Swing		Sync-tip clamp, measured at output, VVID = 3V, V_{IN} = V_{CLP} to (V_{CLP} +1.15V), R_L = 150Ω to VVID/2, R_L = 75Ω to GNDVID		2.3		V_{P-P}
		Measured at output, VVID = 3.135V, V_{IN} = V_{CLP} to (V_{CLP} +1.2V), R_L = 150Ω to VVID/2, R_L = 75Ω to GNDVID	2.34	2.40	2.46	
		Bias circuit, measured at output, VVID = 3V, V_{IN} = (V_{BIAS} - 0.575V) to (V_{BIAS} + 0.575V), R_L = 150Ω to VVID/2, R_L = 75Ω to GNDVID		2.3		
		Measured at output, VVID = 3.135V, V_{IN} = (V_{BIAS} - 0.6V) to (V_{BIAS} + 0.6V), R_L = 150Ω to VVID/2, R_L = 75Ω to GNDVID	2.34	2.40	2.46	
Output Short-Circuit Current				100		mA
Output Resistance	R_{OUT}			0.5		Ω
Output Leakage Current		Output disabled (load detection not active)			10	µA
Power-Supply Rejection Ratio		3V ≤ VVID ≤ 3.6V	50			dB
AC CHARACTERISTICS						
Filter Passband Flatness		V_{OUT} = $2V_{P-P}$, f = 100kHz to 10MHz		-1		dB
Filter Attenuation		V_{OUT} = $2V_{P-P}$, attenuation is referred to 100kHz, f = 11MHz		3		dB
		V_{OUT} = $2V_{P-P}$, attenuation is referred to 100kHz, f = 27MHz		52		
		V_{OUT} = $2V_{P-P}$, attenuation is referred to 100kHz, f = 54MHz		55		
Slew Rate		V_{OUT} = $2V_{P-P}$, no filter in video path		60		V/µs
Settling Time		V_{OUT} = $2V_{P-P}$, settle to 0.1% (Note 3)		400		ns
Differential Gain	DG	5-step modulated staircase, f = 4.43MHz		0.15		%
Differential Phase	DP	5-step modulated staircase, f = 4.43MHz		0.6		Degrees
2T Pulse-to-Bar K Rating		2T = 200ns, bar time is 18µs; the beginning 2.5% and the ending 2.5% of the bar time are ignored		0.3		K%

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ELECTRICAL CHARACTERISTICS (continued)

(V12 = 12V, VVID = VAUD = 3.3V, V_{GNDVID} = V_{EP} = 0V, no load, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
2T Pulse Response		2T = 200ns		0.2		K%
2T Bar Response		2T = 200ns, bar time is 18µs; the beginning 2.5% and the ending 2.5% of the bar time are ignored		0.2		K%
Nonlinearity		5-step staircase		0.1		%
Group Delay Distortion		100kHz ≤ f ≤ 5MHz, outputs are $2V_{P-P}$		11		ns
Glitch Impulse Caused by Charge-Pump Switching		Measured at outputs		100		pVs
Peak Signal-to-RMS Noise		100kHz ≤ f ≤ 5MHz		70		dB
Power-Supply Rejection Ratio		f = 100kHz, $100mV_{P-P}$		42		dB
Output Impedance		f = 5MHz		2		Ω
Video Crosstalk		f = 4.43MHz		-46		dB
Reverse Isolation		VCR SCART inputs to encoder inputs, full-power mode with VCR being looped through to TV, f = 4.43MHz		92		dB
Pulldown Resistance		Enable VCR_R/C_OUT pulldown through I^2C interface		4.6	7.5	Ω
AUDIO CHARACTERISTICS						
Voltage Gain		V_{IN} = -0.707V to +0.707V	3.95	4	4.05	V/V
Gain Mismatch		V_{IN} = -0.707V to +0.707V	-1.5		+1.5	%
Flatness		f = 20Hz to 20kHz, $0.25V_{RMS}$ input		0.006		dB
Frequency Bandwidth		$0.25V_{RMS}$ input, frequency where output is -3dB referenced to 1kHz		230		kHz
Capacitive Drive		No sustained oscillations, 75Ω series resistor on output		300		pF
Input Resistance		V_{IN} = -0.707V to +0.707V		10		MΩ
Input Bias Current		V_{IN} = 0V			500	nA
Input Signal Amplitude		f = 1kHz, THD < 1%		0.5		V_{RMS}
Output DC Level		No input signal, V_{IN} grounded	-3		+3	mV
Signal-to-Noise Ratio		f = 1kHz, $0.25V_{RMS}$ input, 20Hz to 20kHz		97		dB
Total Harmonic Distortion Plus Noise		R_L = 3.33kΩ, f = 1kHz, $0.25V_{RMS}$ input		0.0014		%
		R_L = 3.33kΩ, f = 1kHz, $0.5V_{RMS}$ input		0.001		
Output Impedance		f = 1kHz		0.4		Ω
Power-Supply Rejection Ratio		DC	75	100		dB
		f = 1kHz		90		
Mute Suppression		f = 1kHz, $0.25V_{RMS}$ input		110		dB
Audio Crosstalk		f = 1kHz, $0.25V_{RMS}$ input		92		dB

ELECTRICAL CHARACTERISTICS (continued)

(V12 = 12V, VVID = VAUD = 3.3V, V_{GNDVID} = V_{EP} = 0V, no load, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VIDEO-TO-AUDIO INTERACTION						
Crosstalk		Video input: f = 15kHz, $1V_{P-P}$ signal, Audio input: f = 15kHz, $0.5V_{RMS}$ signal		92		dB
CHARGE PUMP						
Switching Frequency				580		kHz
FAST SWITCHING						
Input Low					0.4	V
Input High Level			1			V
Input Current					10	µA
Output Low Voltage		I_{OL} = 0.5mA			0.1	V
Output High Voltage		I_{OH} = 0.5mA	VVID - 0.1			V
Output Resistance				7		Ω
Rise Time		143Ω to GNDVID		12		ns
Fall Time		143Ω to GNDVID		10		ns
SLOW SWITCHING						
Input Low Voltage					2	V
Input Medium Voltage			4.5		7	V
Input High Voltage			9.5			V
Input Current				70	100	µA
Output Low Voltage		10kΩ to EP, 11.4V ≤ V12 ≤ 12.6V			1.5	V
Output Medium Voltage		10kΩ to EP, 11.4V ≤ V12 ≤ 12.6V	5		6.5	V
Output High Voltage		10kΩ to EP, 11.4V ≤ V12 ≤ 12.6V	10			V
DIGITAL INTERFACE						
Input High Voltage	V_{IH}		0.7 x VVID			V
Input Low Voltage	V_{IL}				0.3 x VVID	V
Input Hysteresis	V_{HYS}			0.06 x VVID		V
Input Leakage Current	I_{IH}, I_{IL}		-1		+1	µA
Input Capacitance				6		pF
Input Current		0.1VVID < SDA < 3.3V, 0.1VVID < SCL < 3.3V, I/O pins of fast-mode devices must not obstruct the SDA and SCL lines if V+ is switched off	-10		+10	µA
Output Low Voltage SDA	V_{OL}	I_{SINK} = 6mA			0.4	V
Serial Clock Frequency	f_{SCL}		0		400	kHz
Bus Free Time Between a STOP and a START Condition	t_{BUF}		1.3			µs
Hold Time, (Repeated) START Condition	$t_{HD, STA}$		0.6			µs

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ELECTRICAL CHARACTERISTICS (continued)

(V12 = 12V, VVID = VAUD = 3.3V, V_{GNDVID} = V_{EP} = 0V, no load, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

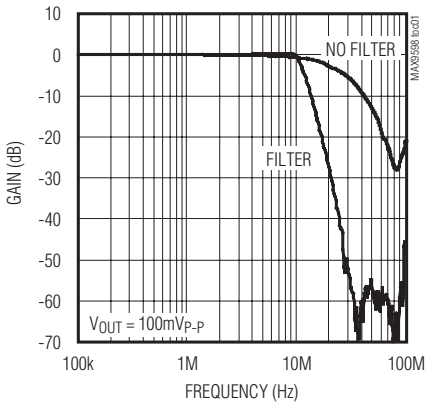
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Low Period of the SCL Clock	t_{LOW}		1.3			µs
High Period of the SCL Clock	t_{HIGH}		0.6			µs
Setup Time for a Repeated START Condition	$t_{SU, STA}$		0.6			µs
Data Hold Time	$t_{HD, DAT}$	(Note 4)	0		0.9	µs
Data Setup Time	$t_{HD, DAT}$		100			ns
Fall Time of SDA Transmitting	t_F	I_{SINK} ≤ 6mA, C_B = total capacitance of one bus line in pF, t_R and t_F measured between 0.3VVID and 0.7VVID, C_B ≤ 400pF		100		ns
Setup Time for STOP Condition	$t_{SU, STO}$		0.6			µs
Pulse Width of Spike Suppressed	t_{SP}	Input filters on the SDA and SCL inputs suppress noise spikes less than 50ns	0		50	ns
OTHER DIGITAL I/O						
DEV_ADDR Low Level					0.3 x VVID	V
DEV_ADDR High Level			0.7 x VVID			V
DEV_ADDR Input Current			-1		+1	µA
Interrupt Output Low Voltage		I_{OL} = 0.5mA			0.1	V
Interrupt Output Leakage Current		$\overline{INT}$ high impedance			10	µA

Note 1: All devices are 100% production tested at T_A = +25°C. Specifications over temperature limits are guaranteed by design.
Note 2: Normal operation mode is the POR state.
Note 3: The settling time is measured from the 50% of the input swing to the 0.1% of the final value of the output.
Note 4: A master device must provide a hold time of at least 300ns for the SDA signal (referred to V_{IL} of the SCL signal) in order to bridge the undefined region of SCL's falling edge.

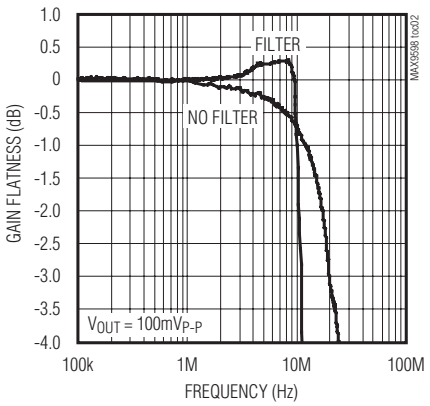
Typical Operating Characteristics

(VVID = VAUD = 3.3V, V12 = 12V, V_{GNDVID} = V_{EP} = 0V, video load is 150Ω to GNDVID, audio load is 10kΩ to EP, T_A = +25°C, unless otherwise noted.)

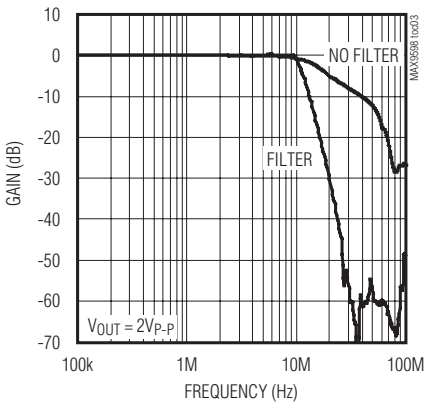
VIDEO SMALL-SIGNAL GAIN vs. FREQUENCY



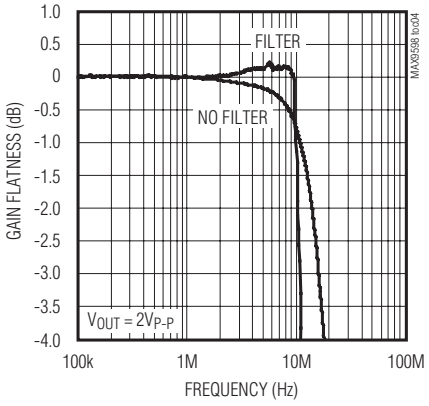
VIDEO SMALL-SIGNAL GAIN FLATNESS vs. FREQUENCY



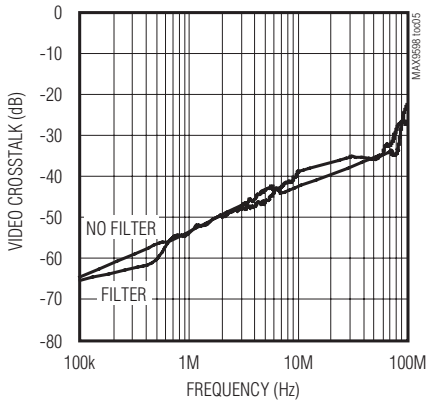
VIDEO LARGE-SIGNAL GAIN vs. FREQUENCY



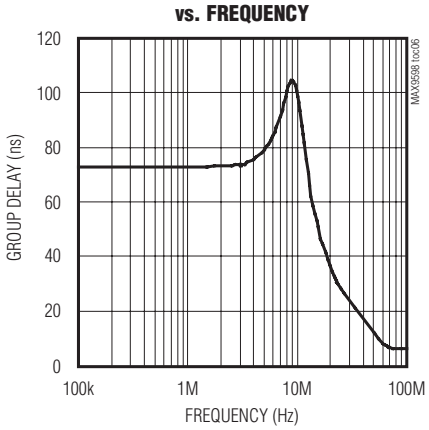
VIDEO LARGE-SIGNAL GAIN FLATNESS vs. FREQUENCY



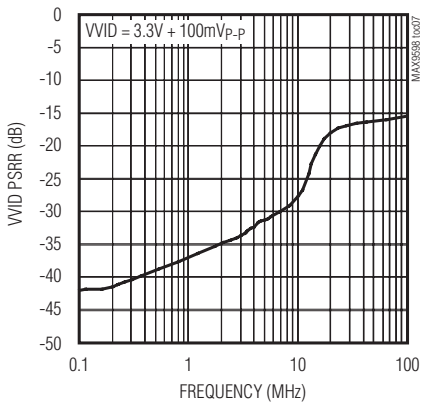
VIDEO CROSSTALK vs. FREQUENCY



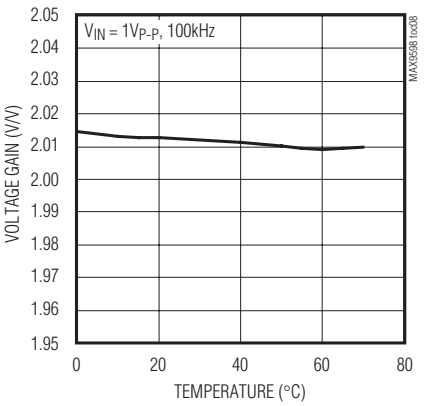
GROUP DELAY vs. FREQUENCY



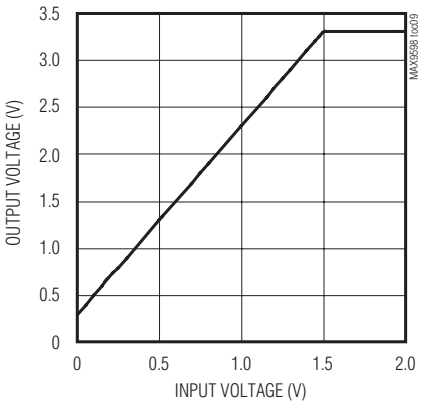
VVID POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



VIDEO VOLTAGE GAIN vs. TEMPERATURE



VIDEO OUTPUT VOLTAGE vs. INPUT VOLTAGE

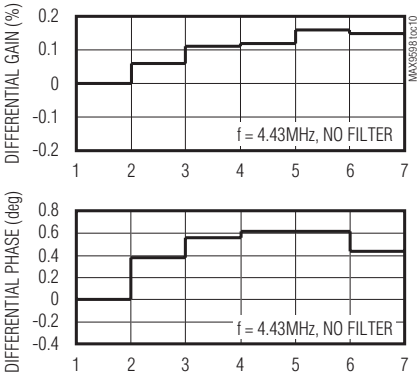


Low-Power Audio/Video Switch for Dual SCART Connectors

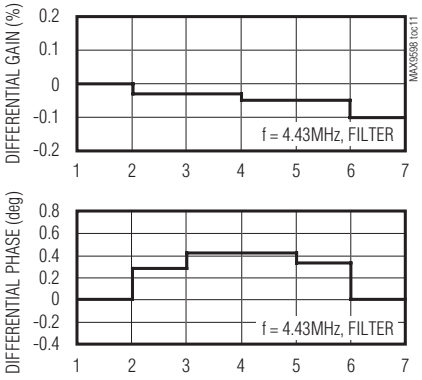
Typical Operating Characteristics (continued)

(VVID = VAUD = 3.3V, V12 = 12V, V_{GNDVID} = V_{EP} = 0V, video load is 150Ω to GNDVID, audio load is 10kΩ to EP, T_A = +25°C, unless otherwise noted.)

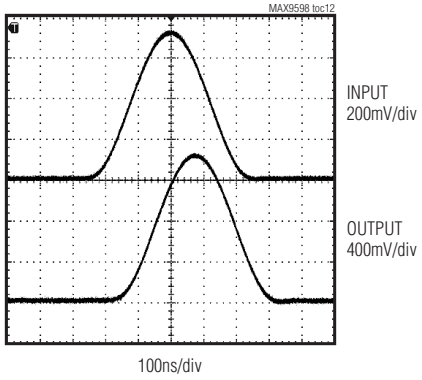
DIFFERENTIAL GAIN AND PHASE



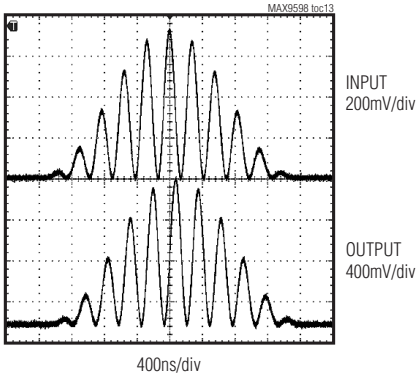
DIFFERENTIAL GAIN AND PHASE



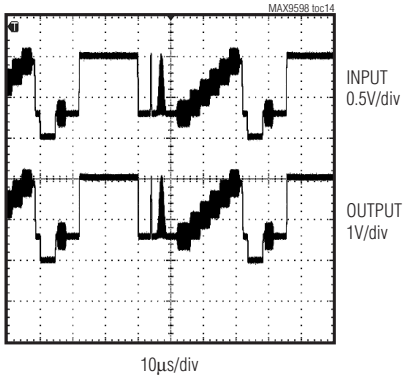
2T RESPONSE



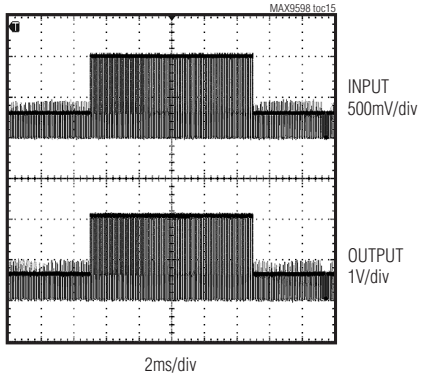
12.5T RESPONSE



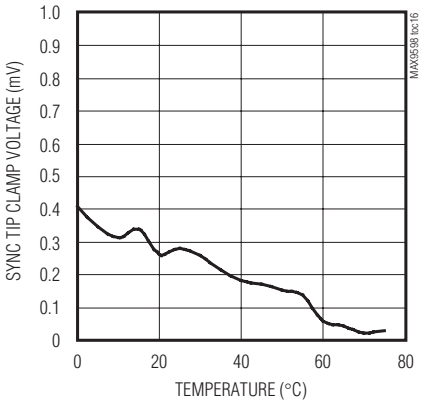
NTC-7 VIDEO TEST SIGNAL



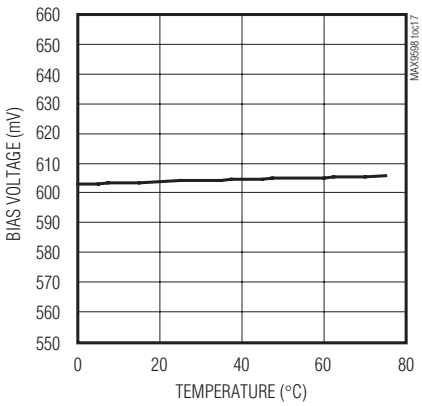
FIELD SQUARE-WAVE RESPONSE



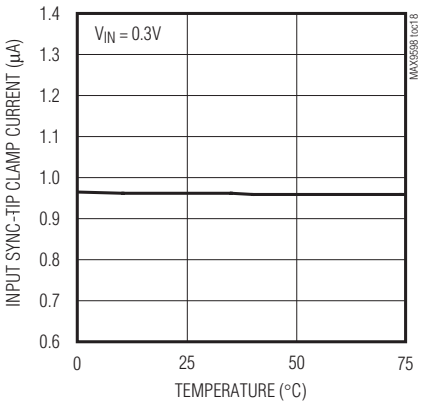
SYNC TIP CLAMP VOLTAGE vs. TEMPERATURE



BIAS VOLTAGE vs. TEMPERATURE



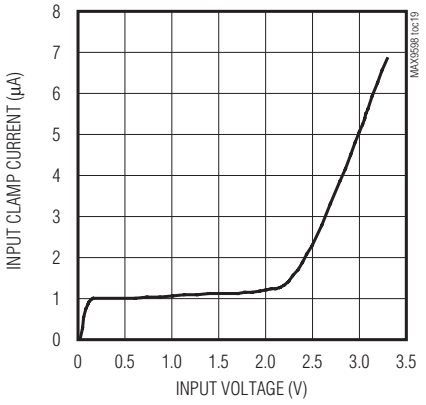
INPUT SYNC-TIP CLAMP CURRENT vs. TEMPERATURE



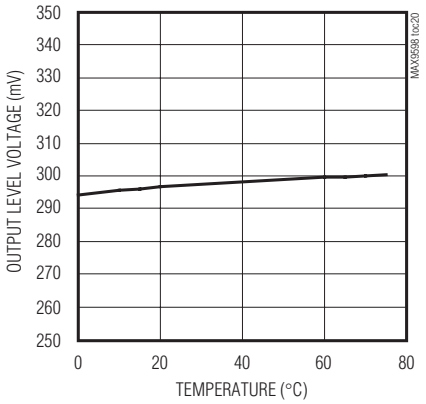
Typical Operating Characteristics (continued)

(VVID = VAUD = 3.3V, V12 = 12V, V_{GNDVID} = V_{EP} = 0V, video load is 150Ω to GNDVID, audio load is 10kΩ to EP, T_A = +25°C, unless otherwise noted.)

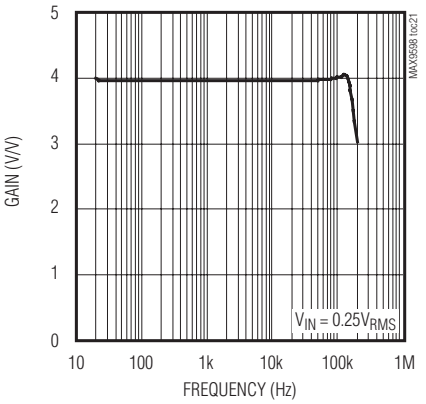
INPUT CLAMP CURRENT vs. INPUT VOLTAGE



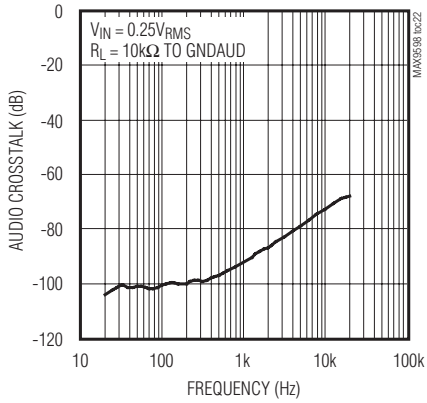
OUTPUT LEVEL VOLTAGE vs. TEMPERATURE



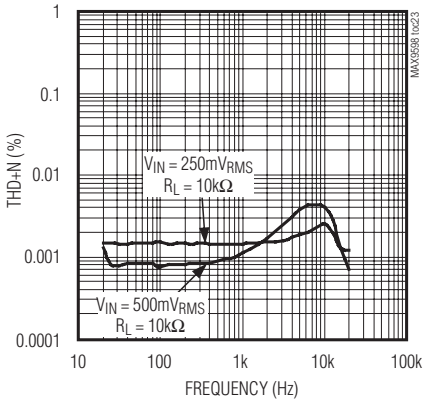
AUDIO LARGE-SIGNAL FREQUENCY RESPONSE vs. GAIN



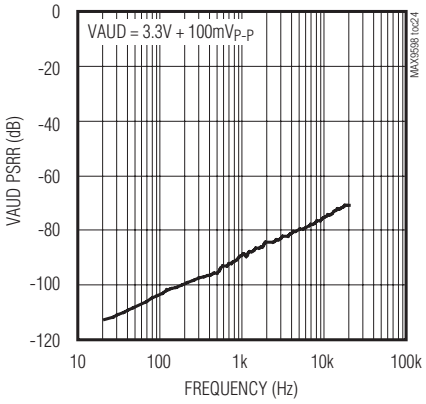
AUDIO CROSSTALK vs. FREQUENCY



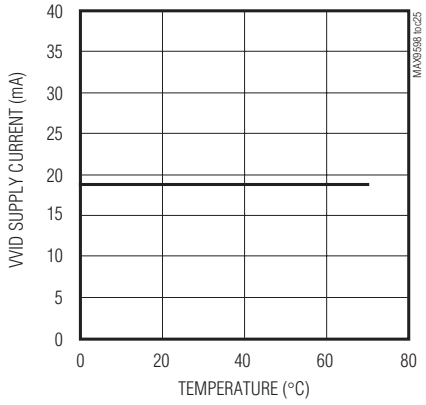
AUDIO TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



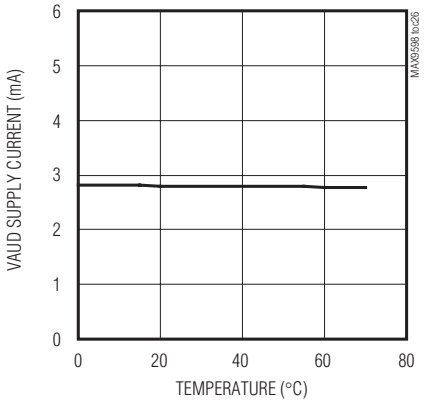
VAUD POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



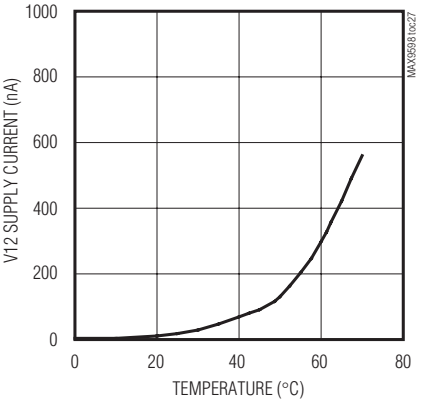
VVID SUPPLY CURRENT vs. TEMPERATURE



VAUD SUPPLY CURRENT vs. TEMPERATURE



V12 SUPPLY CURRENT vs. TEMPERATURE



Low-Power Audio/Video Switch for Dual SCART Connectors

Pin Description

PIN	NAME	FUNCTION
1	SDA	Bidirectional, I²C Data I/O. Output is open drain and tolerates up to 3.6V.
2	SCL	I²C Clock Input
3	DEV_ADDR	Device Address Set Input. Connect DEV_ADDR to GNDVID, VVID, SDA or SCL. See Table 3.
4	$\overline{INT}$	Interrupt Output. This is an open-drain output that pulls down to GNDVID to indicate a change in the VCR slow-switching input, the activity status of the composite video inputs, or the load status of the composite video outputs.
5	VAUD	Audio Supply. Connect to a 3.3V supply. Bypass with a 10µF aluminum electrolytic capacitor in parallel with a 0.1µF ceramic capacitor to EP.
6	C1P	Charge-Pump Flying Capacitor Positive Terminal. Connect a 1µF capacitor from C1P to C1N.
7	C1N	Charge-Pump Flying Capacitor Negative Terminal. Connect a 1µF capacitor from C1P to C1N.
8	CPVSS	Charge-Pump Negative Power Supply. Bypass CPVSS with a 1µF ceramic capacitor to EP.
9	ENC_INL	Encoder Left-Channel Audio Input
10	ENC_INR	Encoder Right-Channel Audio Input
11	VCR_INL	VCR SCART Left-Channel Audio Input
12	VCR_INR	VCR SCART Right-Channel Audio Input
13	TV_OUTL	TV SCART Left-Channel Audio Output
14	VCR_OUTL	VCR SCART Left-Channel Audio Output
15	VCR_OUTR	VCR SCART Right-Channel Audio Output
16	TV_OUTR	TV SCART Right-Channel Audio Output
17	TV_SS	TV SCART Bidirectional Slow-Switch Signal
18	V12	+12V Supply. Bypass V12 with a 0.1µF capacitor to EP.
19	VCR_SS	VCR SCART Bidirectional Slow-Switch Signal
20	TVOUT_FS	TV SCART Fast-Switching Logic Output
21	VCRIN_FS	VCR SCART Fast-Switching Input
22	ENC_B_IN	Encoder Blue Video Input
23	ENC_G_IN	Encoder Green Video Input
24	VCR_B_IN	VCR SCART Blue Video Input
25	VCR_G_IN	VCR SCART Green Video Input
26	TV_B_OUT	TV SCART Blue Video Output
27	TV_G_OUT	TV SCART Green Video Output
28	GNDVID	Video Ground
29	VCR_R/C_IN	VCR SCART Red/Chroma Video Input
30	VVID	Video and Digital Supply. Connect to a +3.3V supply. Bypass with a parallel 1µF and 0.1µF ceramic capacitor to GNDVID. VVID also serves as a digital supply for the I²C interface.

Pin Description (continued)

PIN	NAME	FUNCTION
31	ENC_C_IN	Encoder Chroma Video Input
32	ENC_R/C_IN	Encoder Red/Chroma Video Input
33	TV_R/C_OUT	TV SCART Red/Chroma Video Output
34	VCR_R/C_OUT	VCR SCART Red/Chroma Video Output
35	VCR_Y/CVBS_OUT	VCR SCART Luma/Composite Video Output
36	TV_Y/CVBS_OUT	TV SCART Luma/Composite Video Output
37	VCR_Y/CVBS_IN	VCR SCART Luma/Composite Video Input
38	TV_Y/CVBS_IN	TV SCART Luma/Composite Video Input
39	ENC_Y_IN	Encoder Luma Video Input
40	ENC_Y/CVBS_IN	Encoder Luma/Composite Video Input
EP	EP	Exposed Pad. The exposed pad is the internal ground for the audio amplifiers and charge pump. A low-impedance connection between ground and EP is required for proper isolation.

Detailed Description

The MAX9598 represents Maxim's third generation of SCART[1] audio/video (A/V) switches. Under I^2C control, these devices route audio, video, and control information between the set-top box decoder chip and two SCART connectors. The audio signals are left audio and right audio. The video signals are composite video with blanking and sync (CVBS) and component video (red, green, blue). S-video (Y/C) can be transported across the SCART interface if CVBS is reassigned to luma (Y) and red is reassigned to chroma (C). Support for S-video is optional. The slow-switch signal and the fast-switch signal carry control information. The slow-switch signal is a 12V, trilevel signal that indicates whether the picture aspect ratio is 4:3 or 16:9 or causes the television to use an internal A/V source such as an antenna. The fast-switch signal indicates whether the television should display CVBS or RGB signals.

CVBS, left audio, and right audio are full duplex. All the other signals are half duplex. Therefore, one device on the link must be designated as the transmitter and the other device must be designated as the receiver.

The low-power consumption and the advanced monitoring functions of the MAX9598 enable the creation of lower power set-top boxes, televisions, and DVD players. Unlike competing SCART ICs, the audio and video circuits of the MAX9598 operate entirely from 3.3V rather than from 5V and 12V. Only the slow-switch circuit of the MAX9598 requires a 12V supply. The MAX9598 also has circuits that detect activity on the CVBS inputs, loads on the CVBS outputs, and the level of the slow-switch signals. The $\overline{INT}$ signal informs the µC if there are any changes so that the µC can intelligently decide whether to power up or power down the equipment.

In addition, the MAX9598 has DirectDrive audio circuitry to eliminate click-and-pop noise. With DirectDrive, the DC bias of the audio line outputs is always at ground, no matter whether the MAX9598 is being powered up or powered down. Conventional audio line output drivers that operate from a single supply require series AC-coupling capacitors. During power-up, the DC bias on the AC-coupling capacitor moves from ground to a positive voltage, and during power-down, the opposite occurs. The changing DC bias usually causes an audible transient.

[1] ***SCART*** *(from Syndicat des Constructeurs d'Appareils Radiorécepteurs et Téléviseurs) is a French-originated standard and associated 21-pin connector for connecting audio-visual equipment together. The official standard for SCART is CENELEC document number EN 50049-1. From Wikipedia.*

Low-Power Audio/Video Switch for Dual SCART Connectors

Audio Section

The audio circuit is essentially a stereo, 2x2, nonblocking, audio crosspoint with output drivers. The encoder (stereo audio DAC) and the VCR are the two input sources, and the two outputs go to the TV SCART connector and the VCR SCART connector. See Figure 1.

The integrated charge pump inverts the +3.3V supply to create a -3.3V supply. The audio circuit operates from bipolar supplies so the audio signal is always biased to ground.

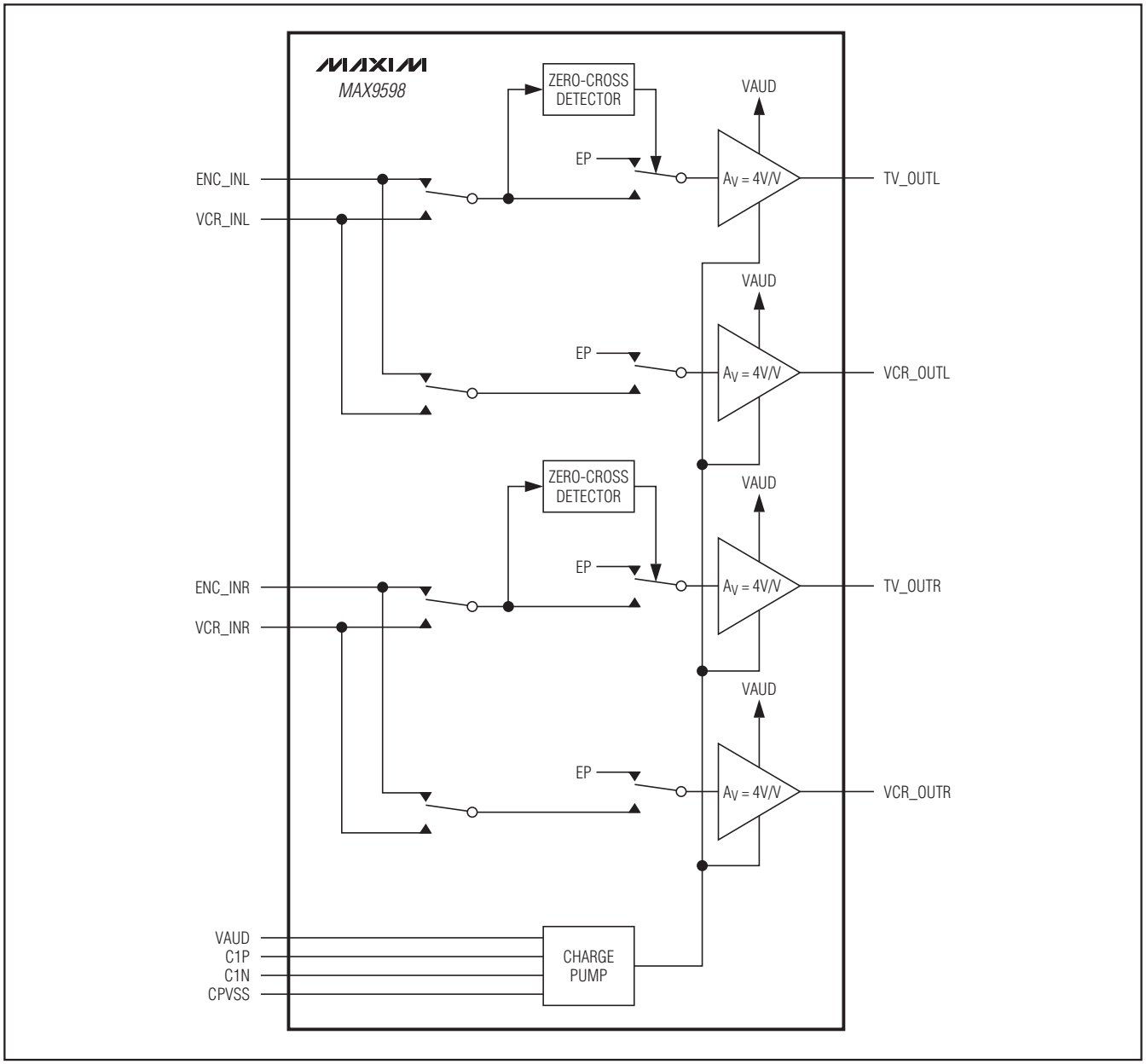


Figure 1. MAX9598 Audio Section Functional Diagram

Clickless Switching

The TV audio channel incorporates a zero-crossing detect (ZCD) circuit that minimizes click noise due to abrupt signal level changes that occur when switching between audio signals at an arbitrary moment.

To implement the zero-crossing function when switching audio signals, set the ZCD bit high (Audio Control Register 00h, bit 6). Then set the mute bit high (Audio Control Register, 00h, bit 0). Next, wait for a sufficient period of time for the audio signal to cross zero. This period is a function of the audio signal path's low-frequency 3dB corner (f_{L3dB}). Thus, if f_{L3dB} = 20Hz, the time period to wait for a zero-crossing detect is 1/20Hz or 50ms.

After the wait period, select a new audio source for the TV audio channel by writing to bits 1 and 0 of the TV Audio Control Register (01h). Finally, clear mute (Audio Control Register, 00h, bit 0) but leave ZCD (Audio Control Register, 00h, bit 6) high. The MAX9598 switches the signal out of mute at the next zero crossing. See Tables 10 and 11.

Audio Outputs

The MAX9598 audio output amplifiers feature Maxim's DirectDrive architecture, thereby eliminating the need for output-coupling capacitors required by conventional single-supply audio line drivers. An internal charge pump inverts the positive supply (VAUD), creating a negative supply (CPVSS). The audio output amplifiers operate from these bipolar supplies with their outputs biased about audio ground (Figure 2). The benefit of this audio ground bias is that the amplifier outputs do not have a DC component. The DC-blocking capacitors required with conventional audio line drivers are unnecessary, conserving board space, reducing system cost, and improving frequency response.

Conventional single-supply audio line drivers have their outputs biased about a nominal DC voltage (typically half the supply) for maximum dynamic range. Large coupling capacitors are needed to block this DC bias. Clicks and pops are created when the coupling capacitors are charged during power-up and discharged during power-down.

The MAX9598 features a low-noise charge pump that requires only two small ceramic capacitors. The 580kHz switching frequency is well beyond the audio range and does not interfere with audio signals. The switch drivers feature a controlled switching speed that minimizes noise on the video outputs generated by turn-on and turn-off transients.

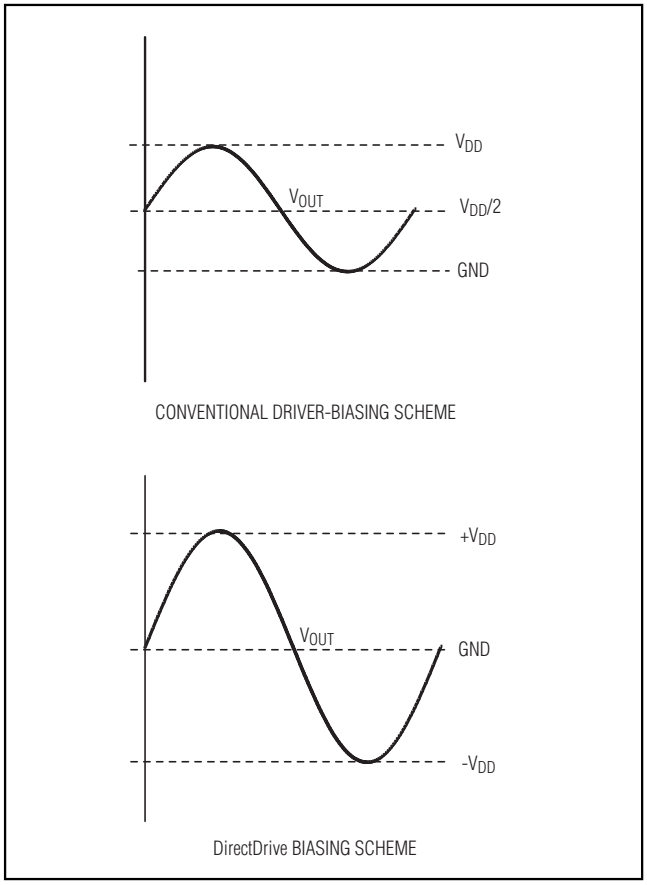


Figure 2. Conventional Driver Output Waveform vs. MAX9598 Output Waveform

The SCART standard specifies $2V_{RMS}$ as the full-scale for audio signals. As the audio circuits process $0.5V_{RMS}$ full-scale audio signals internal to the MAX9598, the gain-of-4 output amplifiers restore the audio signals to a full scale of $2V_{RMS}$.

To select which audio input source is routed to the TV SCART connector, write to bits 1 and 0 of the TV Audio Control Register (01h). To select which audio input source is routed to the VCR SCART connector, write to bits 3 and 2 of the TV Audio Control Register (01h). The power-on default is for the TV and VCR audio outputs to be muted (the inputs of the output amplifiers are connected to audio ground). See Tables 8 and 11.

Video Section

The video circuit routes different video formats between the set-top box decoder, the TV SCART connector, and the VCR SCART connector. It also routes slow-switch and fast-switch control information. See Figure 3.

Low-Power Audio/Video Switch for Dual SCART Connectors

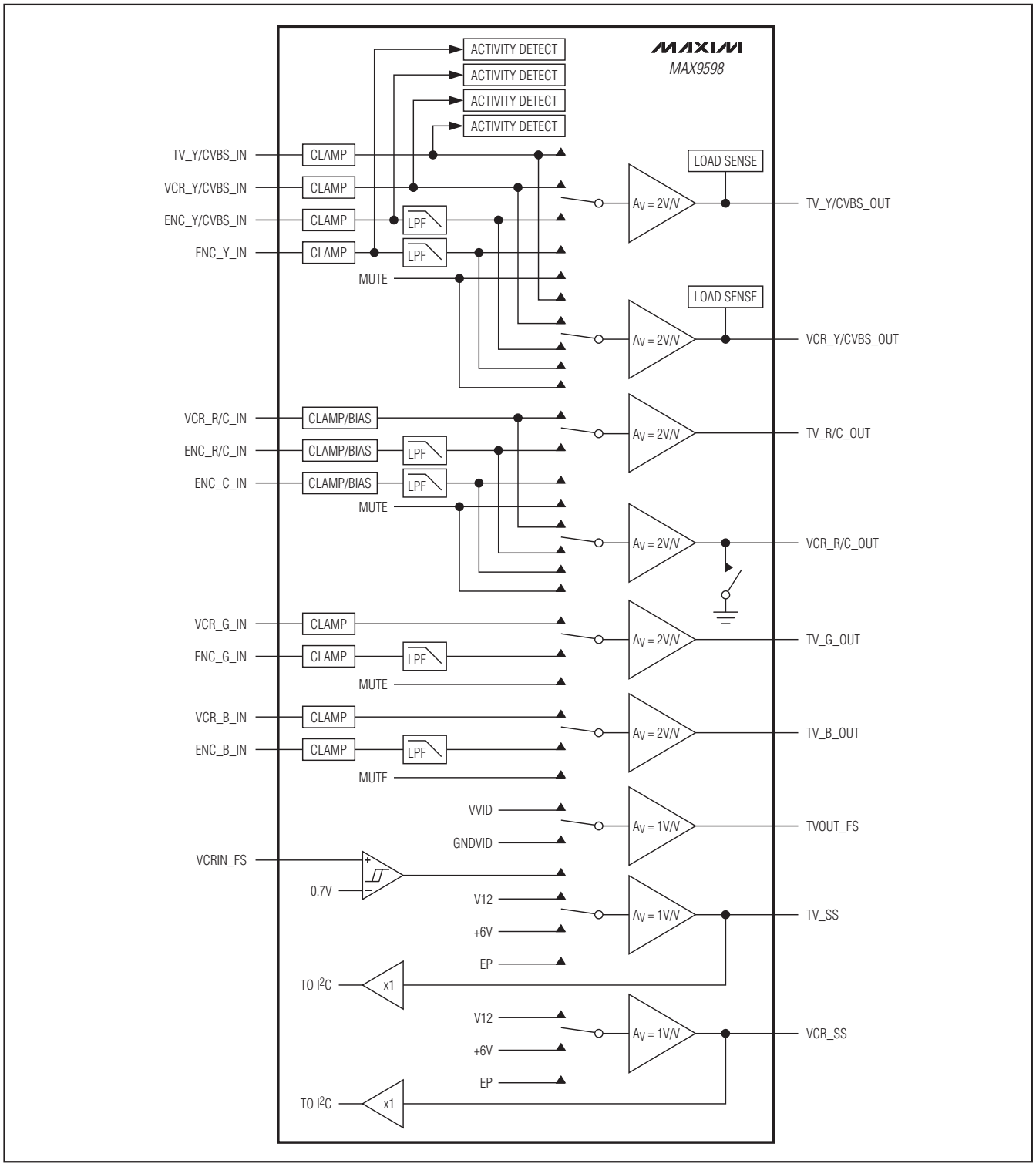


Figure 3. MAX9598 Video Section Functional Diagram

Video Inputs

Whether the incoming video signal is AC-coupled or DC-coupled into the MAX9598 depends upon the origin, format, and voltage range of the video signal. Table 1 below shows the recommended connections. Always AC-couple an external video signal through a 0.1µF capacitor because its voltage is not well defined (see the *Typical Application Circuit*). For example, the video transmitter circuit might have a different ground than the video receiver, thereby level shifting the DC bias. The 60Hz power line "hum" might cause the video signal to slowly change DC bias.

Internal video signals that are between 0 and 1V can be DC-coupled. Most video DACs generate video signals between 0 and 1V because the video DAC sources current into a ground-referenced resistor. For the minority of video DACs that generate video signals between 2.3V and 3.3V because the video DAC sinks current from a VVID-referenced resistor, AC-couple the video signal to the MAX9598.

The MAX9598 restores the DC level of incoming, AC-coupled video signals with either transparent sync-tip clamps or bias circuits. When using an AC-coupled input, the transparent sync-tip clamp automatically clamps the input signal minimum to ground, preventing it from going lower. A small current of 1µA pulls down on the input to prevent an AC-coupled signal from drifting outside the input range of the part. Use sync-tip clamps with CVBS, RGB, and luma signals.

The transparent sync-tip clamp is "transparent" when the incoming video signal is DC-coupled and at or above ground. Under such conditions, the clamp never activates. Therefore, the outputs of video DACs that typically generate signals between 0 and 1V can be directly connected to the MAX9598 inputs.

The bias circuit accepts AC-coupled chroma, which is a subcarrier with the color information modulated onto it. The bias voltage of the bias circuits is 600mV.

ENC_R/C_IN and VCR_R/C_IN can receive either a red video signal or a chroma video signal. Set the input configuration by writing to bits 7 and 3 of the VCR Video Input Control Register (08h). See Tables 8 and 14.

The MAX9598 also has video input detection. When activated, activity detect circuits check if sync is present on incoming CVBS signals. If so, then there is a valid video signal. Read bits 0, 2, 4, and 5 of the Video Activity Status Register (0Fh) to determine the status of the CVBS inputs. See Table 19.

Video Reconstruction Filter

The video DAC outputs of the set-top box decoder chip need to be lowpass-filtered to reject the out-of-band noise. The MAX9598 integrates 6th-order, Butterworth filters. The filter passband (±1dB) is typically 10MHz, and the attenuation at 27MHz is 52dB. The filters are suited for standard-definition video.

Video Outputs

The video output amplifiers can both source and sink load current, allowing output loads to be DC- or AC-coupled. The amplifier output stage needs around 300mV of headroom from either supply rail. For video signals with a sync pulse, the sync tip will typically be at 300mV, as shown in Figure 4. For a chroma signal, the blank level will typically be at 1.5V, as shown in Figure 5.

Table 1. Recommended Coupling for Incoming Video Signals and Input Circuit Configuration. (Use a 0.1µF Capacitor to AC-Couple a Video Signal into the MAX9598)

VIDEO ORIGIN	FORMAT	VOLTAGE RANGE (V)	COUPLING	INPUT CIRCUIT CONFIGURATION
External	CVBS	Unknown	AC	Transparent Sync Tip Clamp
External	RGB	Unknown	AC	Transparent Sync Tip Clamp
External	Y	Unknown	AC	Transparent Sync Tip Clamp
External	C	Unknown	AC	Bias Circuit
Internal	CVBS	0 to 1	DC	Transparent Sync Tip Clamp
Internal	R, G, B	0 to 1	DC	Transparent Sync Tip Clamp
Internal	Y, C	0 to 1	DC	Transparent Sync Tip Clamp
Internal	Y, Pb, Pr	0 to 1	DC	Transparent Sync Tip Clamp
Internal	CVBS	2.3 to 3.3	AC	Transparent Sync Tip Clamp
Internal	R, G, B	2.3 to 3.3	AC	Transparent Sync Tip Clamp
Internal	Y	2.3 to 3.3	AC	Transparent Sync Tip Clamp
Internal	C	2.3 to 3.3	AC	Bias Circuit

Low-Power Audio/Video Switch for Dual SCART Connectors

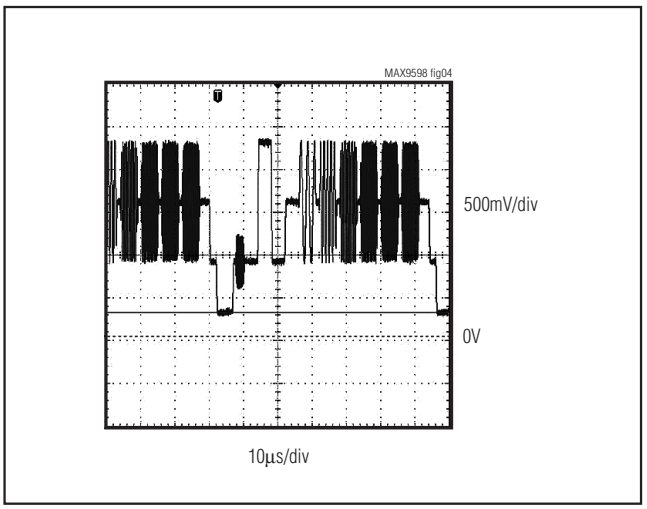


Figure 4. MAX9598 Video Output with CVBS Signal (Multiburst Video Test Signal Shown)

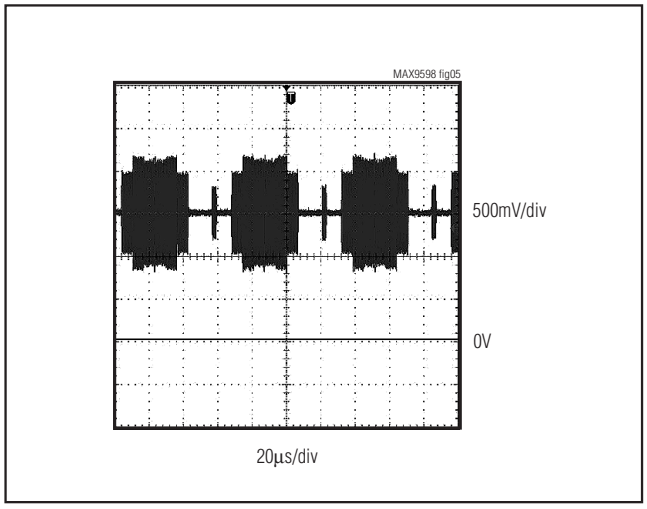


Figure 5. MAX9598 Video Output with Chroma (C) Signal (75% Color Bar Video Test Signal Shown)

If the supply voltage is greater than 3.135V (5% below a 3.3V supply), each amplifier can drive two DC-coupled video loads to ground. If the supply is less than 3.135V, each amplifier can drive only one DC-coupled or AC-coupled video load.

The SCART standard allows for video signals to have a superimposed DC component within 0 to 2V. Therefore, most video signals are DC-coupled at the output. In the unlikely event that the video signal needs to be AC-coupled, the coupling capacitors should be 220µF or greater in order to keep the highpass filter formed by the 37.5Ω equivalent resistance of the video transmission line to a corner frequency of 4.8Hz or below in order to keep it well below the 25Hz frame rate of the PAL standard.

The CVBS outputs have load sense circuits. If enabled, each load sense circuit checks for a load eight times per second by connecting an internal 15kΩ pullup resistor to the output for 1ms. If the output is pulled up, then no load is present. If the output stays low, then a load is connected. Read bits 1 and 3 to determine load status. See Table 19.

The selection of video sources that are sent to the TV SCART connector are controlled by bits 0 to 4 of the TV Video Input Control Register (06h) while the selection of video sources that are sent to the VCR SCART connector are controlled by bits 0 to 2 of the VCR Video Input Control Register (08h). See Tables 8, 12, and 14. The video outputs can be enabled or disabled by bits 2 to 7 of the Output Enable Register (0Dh). See Table 16.

Slow Switching

The MAX9598 supports the IEC 933-1, Amendment 1, trilevel slow switching that selects the aspect ratio for the display (TV). Under I²C control, the MAX9598 sets the slow-switching output voltage level. Table 2 shows the valid input levels of the slow-switching signal and the corresponding operating modes of the display device.

Two bidirectional ports are available for slow-switching signals for the TV and VCR. The slow-switching input status is continuously read and stored in the Status Register (0Eh). The slow-switching outputs can be set to a logic level or high impedance by writing to the TV Video Output Control Register (07h) and the VCR Video Output Control Register (09h). When enabled, $\overline{INT}$ becomes active low if the voltage level changes on TV_SS or VCR_SS. See Tables 8, 13, 15 and 18.

Table 2. Slow-Switching Modes

SLOW-SWITCHING SIGNAL VOLTAGE (V)	MODE
0 to 2	Display device uses an internal source such as a built-in tuner to provide a video signal
4.5 to 7.0	Display device uses a video signal from the SCART connector and sets the display to 16:9 aspect ratio
9.5 to 12.6	Display device uses a signal from the SCART connector and sets the display to 4:3 aspect ratio

Fast Switching

The fast-switching signal was originally used to switch between CVBS and RGB signals on a pixel-by-pixel basis so that on-screen display (OSD) information could be inserted. Since modern set-top box decoder chips have integrated OSD circuitry, there is no need to create OSD information using the older technique. Now, the fast-switching signal is just used to switch between CVBS and RGB signal sources.

Set the source of the fast-switching signal by writing to bits 4 and 3 of the TV Video Output Control Register (07h). The fast switching signal to the TV SCART connector can be enabled or disabled by bit 1 of the Output Enable Register (0Dh). See Tables 8, 13, and 16.

I²C Serial Interface

The MAX9598 features an I²C/SMBus™-compatible, 2-wire serial interface consisting of a serial data line (SDA) and a serial clock line (SCL). SDA and SCL facilitate communication between the MAX9598 and the master at clock rates up to 400kHz. Figure 6 shows the 2-wire interface timing diagram. The master generates SCL and initiates data transfer on the bus. A master device writes data to the MAX9598 by transmitting a START (S) condition, the proper slave address with the R/$\overline{W}$ bit set to 0, followed by the register address and then the data word. Each transmit sequence is framed by a START (S) and a STOP (P) condition. Each word transmitted to the MAX9598 is 8 bits long and is followed by an acknowledge clock pulse. A master reads from the MAX9598 by transmitting the slave address with the R/$\overline{W}$ bit set to 0, the register address of the register to be read, a REPEATED START (Sr) condition, the slave address with the R/$\overline{W}$ bit set to 1, followed by a series of SCL pulses. The MAX9598 transmits data on SDA in sync with the master-generated SCL pulses. The master acknowledges receipt of each byte of data. Each read sequence is framed by a START (S) or REPEATED START (Sr) condition, an acknowledge or a not acknowledge, and a STOP (P) condition. SDA operates as both an input and an open-drain output. A pullup resistor, typically greater than 500Ω, is required on the SDA bus. SCL operates as only an input. A pullup resistor, typically greater than 500Ω, is required on SCL if there are multiple masters on the bus, or if the master in a single-master system has an open-drain SCL output. Series resistors in line with SDA and SCL are optional. Series resistors protect the digital inputs of the MAX9598 from high-voltage spikes on the bus lines, and minimize crosstalk and undershoot of the bus signals.

Bit Transfer

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals (see the *START and STOP Conditions* section). SDA and SCL idle high when the I²C bus is not busy.

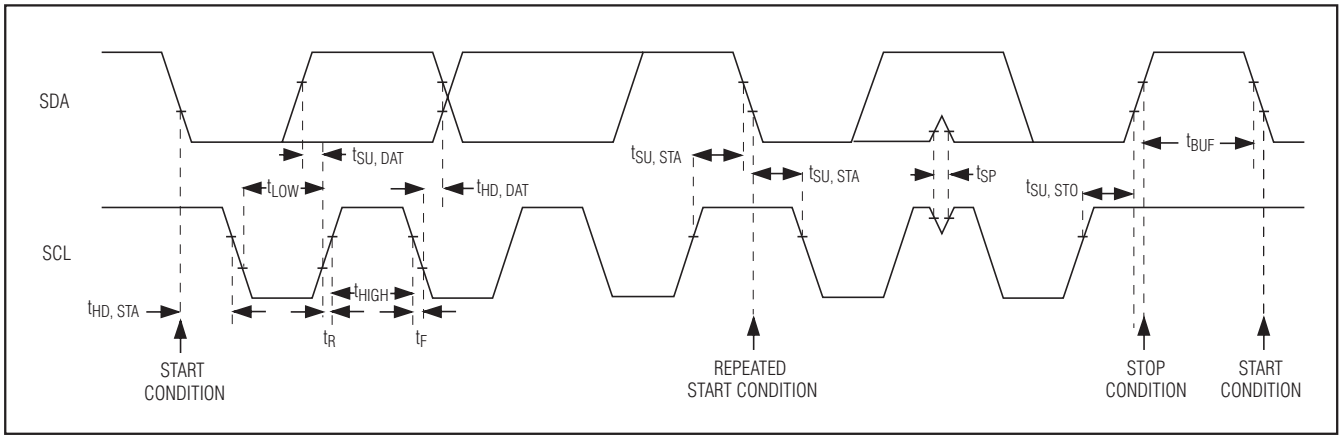


Figure 6. I²C Serial-Interface Timing Diagram

SMBus is a trademark of Intel Corporation.

Low-Power Audio/Video Switch for Dual SCART Connectors

START and STOP Conditions

SDA and SCL idle high when the bus is not in use. A master initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high (Figure 7). A START condition from the master signals the beginning of a transmission to the MAX9598. The master terminates transmission, and frees the bus, by issuing a STOP condition. The bus remains active if a REPEATED START condition is generated instead of a STOP condition.

Early STOP Conditions

The MAX9598 recognizes a STOP condition at any point during data transmission except if the STOP condition occurs in the same high pulse as a START condition. For proper operation, do not send a STOP condition during the same SCL high pulse as the START condition.

Slave Address

The slave address is defined as the 7 MSBs (most significant bits) followed by the R/$\overline{W}$ (read/write) bit. Set the R/$\overline{W}$ bit to 1 to configure the MAX9598 to read mode. Set the R/$\overline{W}$ bit to 0 to configure the MAX9598 to write mode. The slave address is always the first byte of information sent to the MAX9598 after a START or a REPEATED START condition. The MAX9598 slave address is configurable with DEV_ADDR. Table 3 shows the possible slave addresses for the MAX9598.

Acknowledge

The acknowledge bit (ACK) is a clocked 9th bit that the MAX9598 uses to handshake receipt of each byte of data when in write mode (see Figure 8). The MAX9598 pulls down SDA during the entire master-generated 9th clock pulse if the previous byte is successfully received. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master may retry communication. The master pulls down SDA during the 9th clock cycle to acknowledge receipt of data when the MAX9598 is in read mode. An acknowledge is sent by the master after each read byte to allow data transfer to continue. A not acknowledge is sent when the master reads the final byte of data from the MAX9598, followed by a STOP condition.

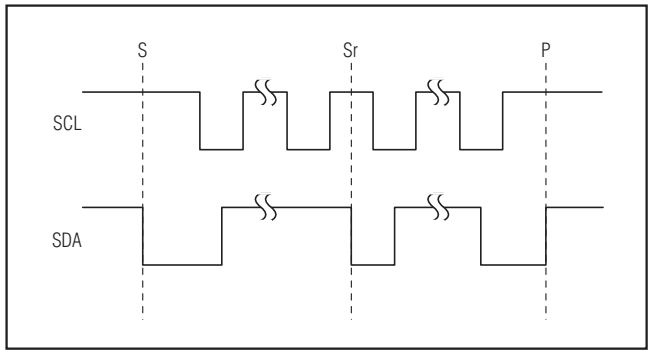


Figure 7. START, STOP, and REPEATED START Conditions

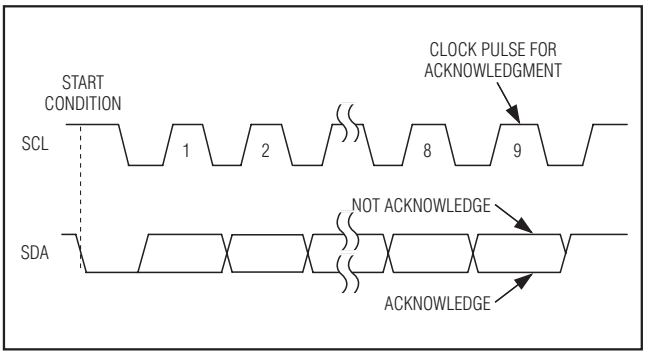


Figure 8. Acknowledge

Table 3. Slave Address

DEV_ADDR	B7	B6	B5	B4	B3	B2	B1	B0	WRITE ADDRESS (hex)	READ ADDRESS (hex)
GNDVID	1	0	0	1	0	1	0	R/$\overline{W}$	94h	95h
VVID	1	0	0	1	0	1	1	R/$\overline{W}$	96h	97h
SCL	1	0	0	1	1	0	0	R/$\overline{W}$	98h	99h
SDA	1	0	0	1	1	0	1	R/$\overline{W}$	9Ah	9Bh

Write Data Format

A write to the MAX9598 consists of transmitting a START condition, the slave address with the R/$\overline{W}$ bit set to 0, one data byte to configure the internal register address pointer, 1 or more data bytes, and a STOP condition. Figure 9 illustrates the proper frame format for writing 1 byte of data to the MAX9598. Figure 10 illustrates the frame format for writing n bytes of data to the MAX9598.

The slave address with the R/$\overline{W}$ bit set to 0 indicates that the master intends to write data to the MAX9598. The MAX9598 acknowledges receipt of the address byte during the master-generated ninth SCL pulse.

The second byte transmitted from the master configures the MAX9598's internal register address pointer. The pointer tells the MAX9598 where to write the next byte of data. An acknowledge pulse is sent by the MAX9598 upon receipt of the address pointer data.

The third byte sent to the MAX9598 contains the data that will be written to the chosen register. An acknowledge pulse from the MAX9598 signals receipt of the data byte. The address pointer autoincrements to the next register address after each received data byte. This autoincrement feature allows a master to write to sequential register address locations within one continuous frame. The master signals the end of transmission by issuing a STOP condition.

Read Data Format

The master presets the address pointer by first sending the MAX9598's slave address with the R/$\overline{W}$ bit set to 0 followed by the register address after a START condition. The MAX9598 acknowledges receipt of its slave address and the register address by pulling SDA low during the ninth SCL clock pulse. A REPEATED START condition is then sent followed by the slave address with the R/$\overline{W}$ bit set to 1. The MAX9598 transmits the contents of the specified register. Transmitted data is valid on the rising edge of the master-generated serial clock (SCL). The address pointer autoincrements after each read data byte. This autoincrement feature allows all registers to be read sequentially within one continuous frame. A STOP condition can be issued after any number of read data bytes. If a STOP condition is issued followed by another read operation, the first data byte to be read will be from the register address location set by the previous transaction and not 00h and subsequent reads will autoincrement the address pointer until the next STOP condition. Attempting to read from register addresses higher than 01h results in repeated reads from a dummy register containing FFh data. The master acknowledges receipt of each read byte during the acknowledge clock pulse. The master must acknowledge all correctly received bytes except the last byte. The final byte must be followed by a not acknowledge from the master and then a STOP condition. Figures 11 and 12 illustrate the frame format for reading data from the MAX9598.

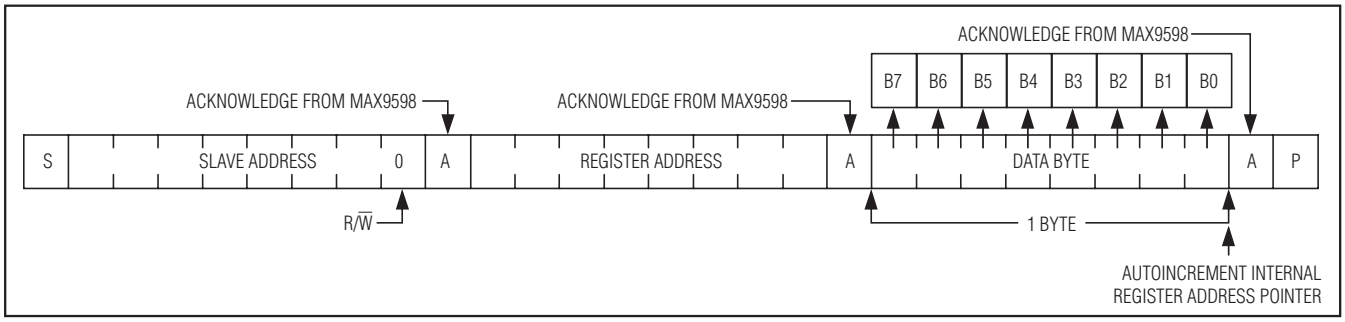


Figure 9. Writing a Byte of Data to the MAX9598

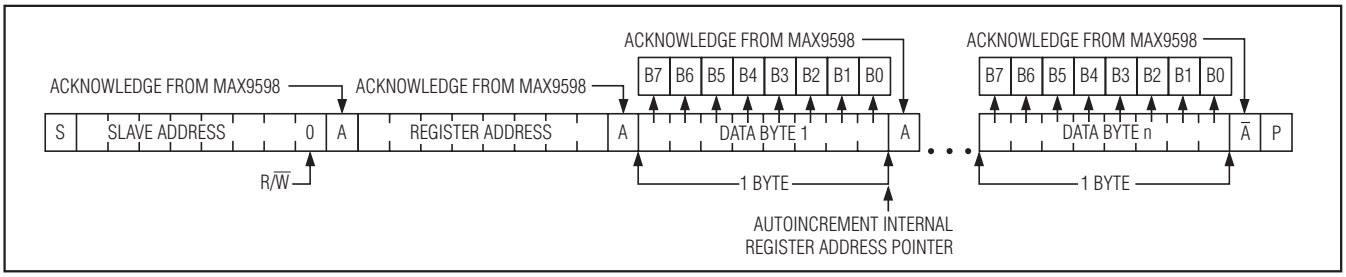


Figure 10. Writing n Bytes of Data to the MAX9598

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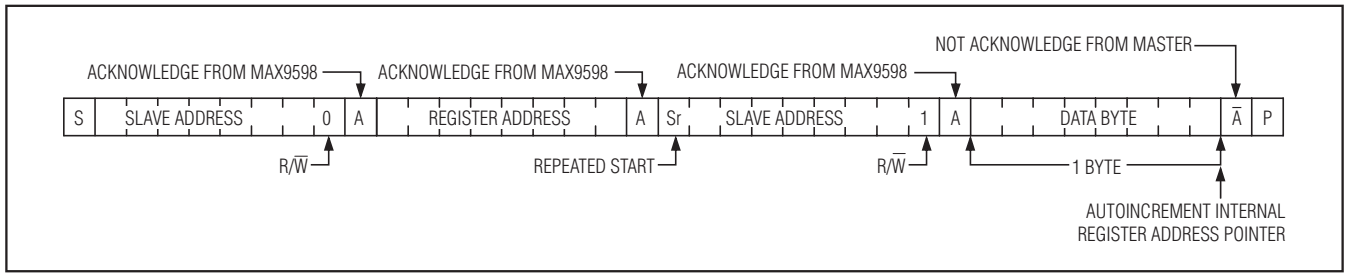

Figure 11. Reading 1 Indexed Byte of Data from the MAX9598

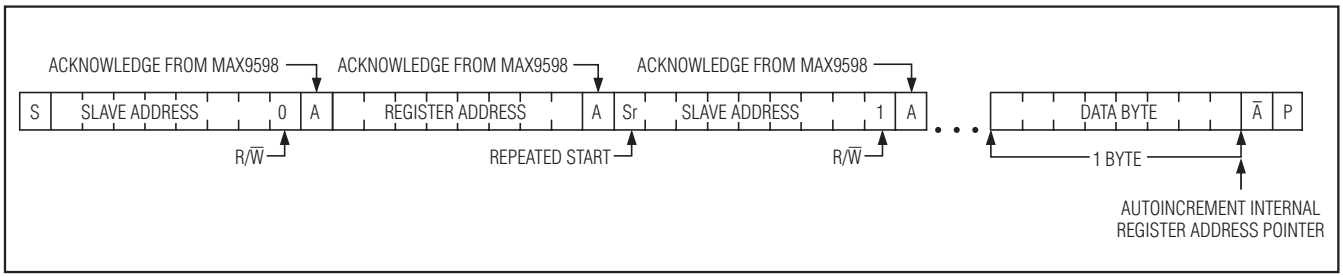

Figure 12. Reading n Bytes of Indexed Data from the MAX9598

Interrupt Output

When interrupt is enabled in modes 1 and 2 (see the *Operating Modes* section), $\overline{INT}$, which is an open-drain output, pulls low under the following conditions: slow-switch signals change value, CVBS input signals are detected or disappear, and CVBS output loads are added or removed.

When interrupt is enabled in mode 3, $\overline{INT}$ pulls low only when the slow-switch signal changes value.

Enable $\overline{INT}$ by writing a 1 into bit 4 of register 01h. See Table 11.

The interrupt can be cleared by reading register 0Eh and 0Fh.

Applications Information

Audio Inputs

The maximum full-scale audio signal that can be applied to the audio inputs is $0.5V_{RMS}$ biased at ground. The recommended application circuit to attenuate and bias an incoming audio signal is shown in Figure 13.

The audio path has a gain of 4V/V so that the full scale of the audio output signal is $2V_{RMS}$. If less than $2V_{RMS}$ full scale is desired at the audio outputs, then the full scale of the audio input signal should be proportionately decreased below $0.5V_{RMS}$.

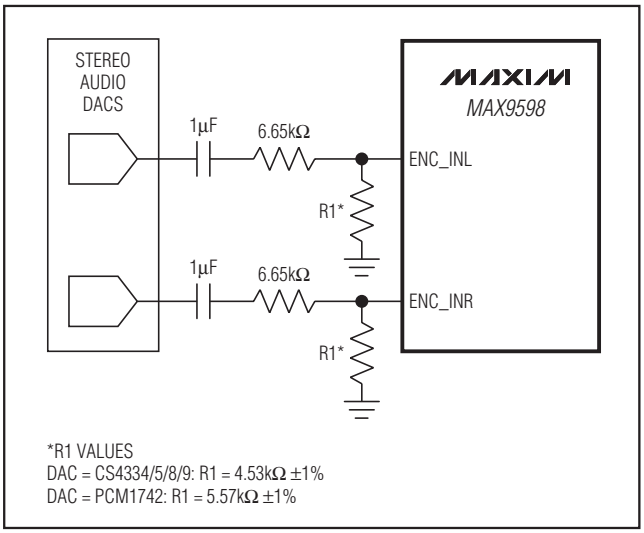

Figure 13. Application Circuit to Connect Audio Source to Audio Inputs (1µF Capacitor Connected to the Ground-Referenced Resistors Biases the Audio Signal at Ground, Resistors Attenuate the Audio Signal)

Operating Modes

The MAX9598 has four operating modes, which can be set by writing to bits 6 and 7 of register 10h. See Table 17.

Table 4. Register Settings for Looping VCR Signals to the TV

DESCRIPTION	REGISTER	BIT								COMMENTS
		7	6	5	4	3	2	1	0	
Loop VCR signals to the TV	00h	Default								
	01h	0	0	0	1	1	1	0	1	
	06h	0	0	0	0	1	0	1	0	
	07h	0	0	0	1	0	0	x	x	(Note 5)
	08h	x	0	0	0	x	1	1	1	(Note 6)
	09h	0	0	0	0	0	1	1	0	
	0Dh	0	0	1	1	1	1	1	1	
	10h	1	0	0	0	0	0	0	0	

Note 5: TV slow-switch output (bits 1 and 0) should be the same as VCR slow-switch input.
Note 6: User has to set bits 7 and 3 appropriately depending upon whether signal is red or chroma.

Shutdown

All circuitry is shut down in the MAX9598 except for the I²C interface, which is designed with static CMOS logic.

Except for register 10h, which sets the operating mode, the values in all the other I²C registers are preserved while entering, during, and leaving shutdown mode.

Low-Power Mode

Put the MAX9598 into low-power mode during standby. Everything is shut down except for the slow-switching circuits, CVBS input detection, CVBS load detection, and I²C interface. If interrupt is enabled, then $\overline{INT}$ will go active low whenever the slow-switch signal changes; a CVBS signal appears or disappears; or a CVBS load appears or disappears. The µC in the set-top box can then decide whether to change the MAX9598 to full-power mode and loop VCR signals to the TV.

Before entering low-power mode, the slow-switch signals should be set to high impedance.

Except for registers 0Eh, 0Fh, and 10h, the value in all of the other I²C registers are preserved while entering, during, and leaving low-power mode. The values in registers 0Eh and 0Fh might change in low-power mode because they provide status on the slow switch signals, CVBS input, and CVBS outputs. The value in register 10h changes while entering or leaving low-power mode because bits 6 and 7 set the operating mode.

Full-Power Mode with Video Input Detection and Video Load Detection

In this mode, the MAX9598 is fully on. If interrupt is enabled, then $\overline{INT}$ will go active low whenever the slow-switch signal changes; a CVBS signal appears or disappears; or a CVBS load appears or disappears. The µC can decide whether to change the routing configuration or operating mode of the MAX9598.

Full-Power Mode Without Video Input Detection and Video Load Detection

This mode is similar to the above mode except that video input detection and video load detection are not active. If interrupt is enabled, then $\overline{INT}$ will go active low only when the slow-switch signal changes.

Table 5. Quiescent Power Consumption

OPERATING MODE	POWER CONSUMPTION (mW)
Shutdown.	0.1
Low-power mode with slow switching, CVBS input video detection, and video load detection active only. Audio circuitry is off.	1.7
Full-power mode WITH input video detection and video load detection active.	71
Full-power mode WITHOUT input video detection and video load detection active (power-on default).	70

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Table 6. Average Power Consumption

OPERATING MODE	POWER CONSUMPTION (mW)
Full-power mode WITH input video detection and video load detection active.	471
Full-power mode WITHOUT input video detection and video load detection active (power-on default).	470

Table 7. Conditions for Average Power Consumption Measurement

PIN	NAME	TYPE	SIGNAL	LOAD
5	VAUD	Supply	3.3V	N/A
9	ENC_INL	Input	$0.25V_{RMS}$, 1kHz	N/A
10	ENC_INR	Input	$0.25V_{RMS}$, 1kHz	N/A
11	VCR_INL	Input	None	N/A
12	VCR_INR	Input	None	N/A
13	TV_OUTL	Output	$1V_{RMS}$, 1kHz	10kΩ to ground
14	VCR_OUTL	Output	$1V_{RMS}$, 1kHz	10kΩ to ground
15	VCR_OUTR	Output	$1V_{RMS}$, 1kHz	10kΩ to ground
16	TV_OUTR	Output	$1V_{RMS}$, 1kHz	10kΩ to ground
17	TV_SS	Output	12V	10kΩ to ground
18	V12	Supply	12V	N/A
19	VCR_SS	Input	0	N/A
20	TVOUT_FS	Output	3.3V	150Ω to ground
21	VCRIN_FS	Input	0	N/A
22	ENC_B_IN	Input	50% flat field	N/A
23	ENC_G_IN	Input	50% flat field	N/A
24	VCR_B_IN	Input	None	N/A
25	VCR_G_IN	Input	None	N/A
26	TV_B_OUT	Output	50% flat field	150Ω to ground
27	TV_G_OUT	Output	50% flat field	150Ω to ground
28	GNDVID	Supply	0	N/A
29	VCR_R/C_IN	Input	None	N/A
30	VVID	Supply	3.3V	N/A
31	ENC_C_IN	Input	None	N/A
32	ENC_R/C_IN	Input	50% flat field	N/A
33	TV_R/C_OUT	Output	50% flat field	150Ω to ground
34	VCR_R/C_OUT	Output	50% flat field	150Ω to ground
35	VCR_Y/CVBS_OUT	Output	50% flat field	150Ω to ground
36	TV_Y/CVBS_OUT	Output	50% flat field	150Ω to ground
37	VCR_Y/CVBS_IN	Input	None	N/A
38	TV_Y/CVBS_IN	Input	None	N/A
39	ENC_Y_IN	Input	None	N/A
40	ENC_Y/CVBS_IN	Input	50% flat field	N/A

Power Consumption

The quiescent power consumption and average power consumption of the MAX9598 are very low because of 3.3V operation and low-power circuit design. Quiescent power consumption is defined when the MAX9598 is operating without loads and without any audio or video signals. Table 5 shows the quiescent power consumption in all four operating modes.

Average power consumption is defined when the MAX9598 drives typical signals into typical loads. Table 6 shows the average power consumption in full-power mode and Table 7 shows the input and output conditions.

S-Video

The MAX9598 supports S-video from the set-top box to the TV, set-top box to the VCR, and VCR to the set-top box. S-video was not included in the original SCART specifications but was added afterwards. As a consequence, the luma (Y) signal of S-video shares the same SCART pin as the CVBS signal. Likewise, the chroma (C) signal shares the same SCART pin as the red signal. The pins that can carry both CVBS and luma have Y/CVBS in their names, and the pins that can carry red and chroma have R/C in their names.

Now, the Y/CVBS signals are full duplex while the R/C signals are half duplex. Therefore, S-video is limited to being half duplex. The MAX9598 has to transmit a chroma signal and receive a chroma signal on the same SCART pin, but not at the same time. The 75Ω resistor connected to VCR_R/C_OUT must act as a back termination resistor when the MAX9598 is transmitting chroma signal and as an input termination resistor when it is receiving a chroma signal. Figure 14 shows how the MAX9598 transmits a chroma signal to the VCR SCART connector while Figure 15 shows how the MAX9598 receives a chroma from the VCR SCART connector.

Write a 0 into bit 2 of register 09h to open the pulldown switch at VCR_R/C_OUT. To close the pulldown switch, write a 0 into bit 6 of register 0Dh to turn off the output amplifier, and then write a 1 into bit 2, register 09h. See Tables 15 and 16.

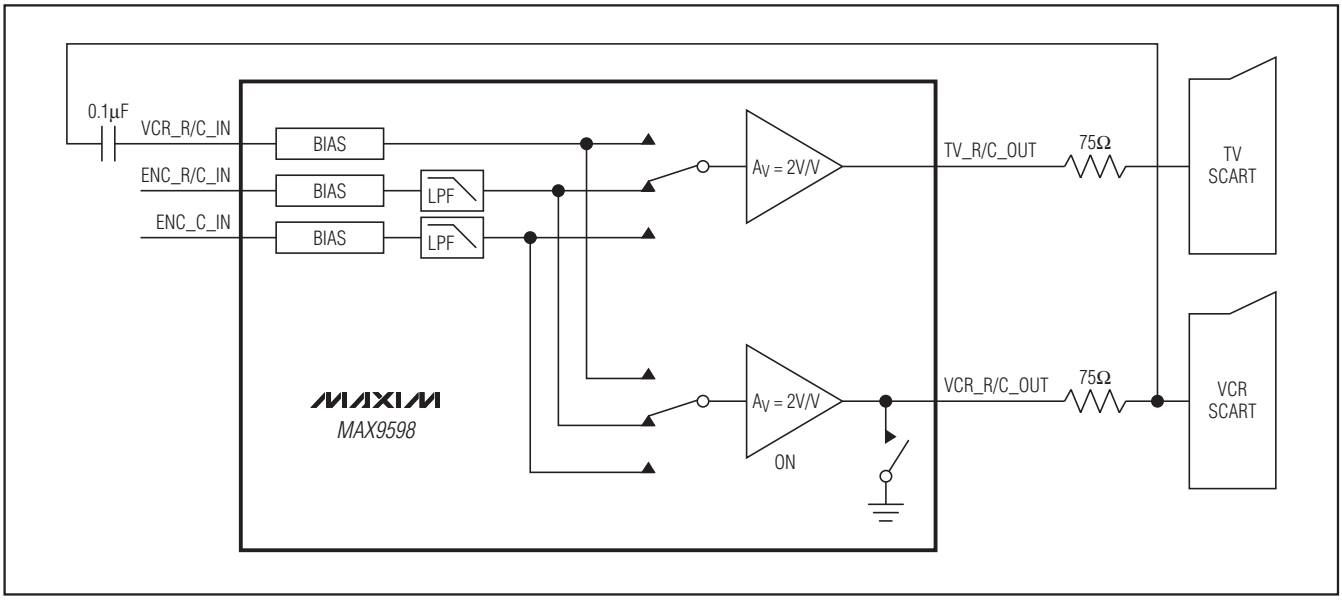

Figure 14. Gain-of-2 Amplifier on VCR_R/C_OUT Outputs Chroma Signal to VCR SCART Connector (Note the Pulldown Switch on VCR_R/C_OUT Is Open)

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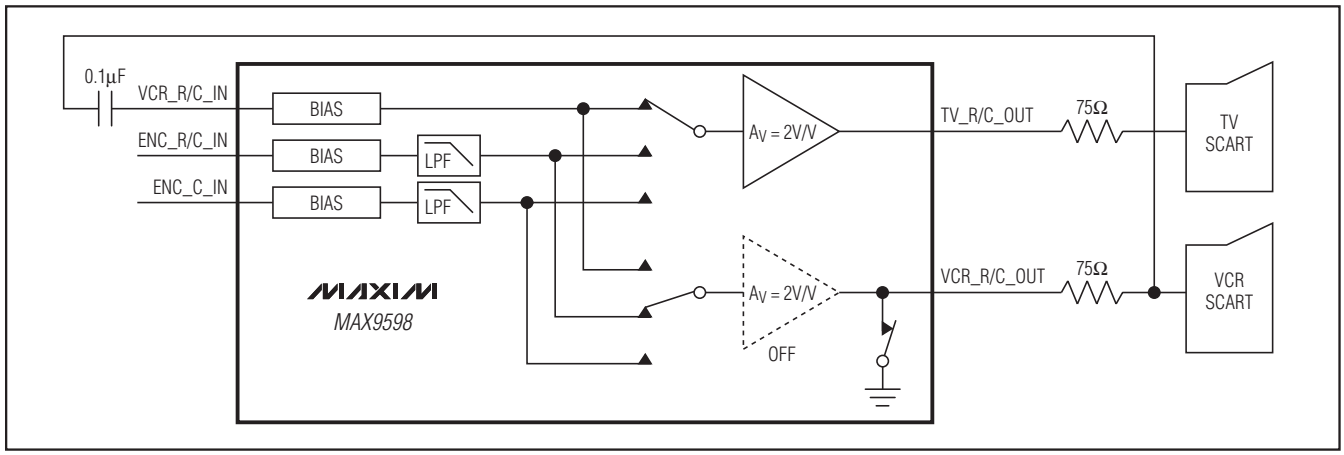

Figure 15. VCR_R/C_IN Receives a Chroma Signal from the VCR SCART Connector. Notice that the Pulldown Switch on VCR_R/C_OUT Is Closed and that the Gain-of-2 Amplifier is Off. The Chroma Signal from VCR SCART IS Looped Through to the TV SCART in the Above Configuration.

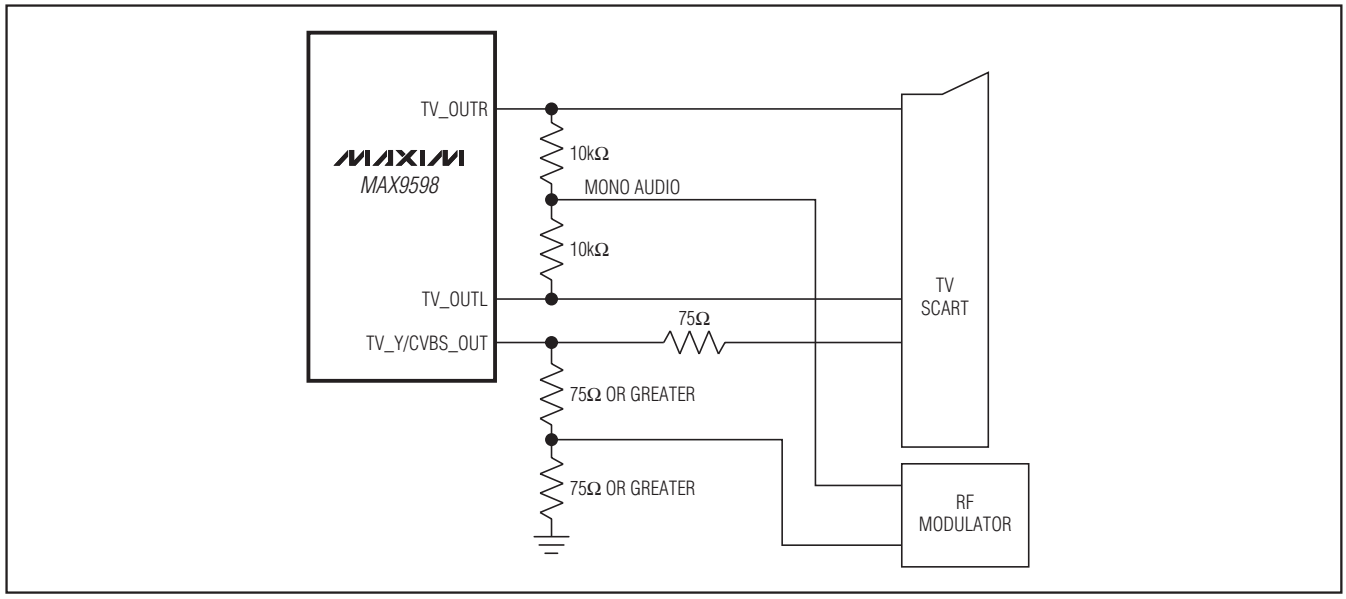

Figure 16. Application Circuit to Connect CVBS and Mono Audio from TV SCART to RF Modulator

Interfacing to an RF Modulator

If the set-top box modulates CVBS and mono audio onto an RF carrier (for example, channel 3), then a simple application circuit can provide the needed signals (see Figure 16). A 10kΩ resistor summer circuit between TV_OUTR and TV_OUTL creates the mono audio signal. The resistor-divider to ground on TV_Y/CVBS_OUT creates a video signal with normal amplitude. The unique feature of the MAX9598 that facilitates this application circuit is that the audio and video output amplifiers of the MAX9598 can drive multiple loads if VAUD and VVID are both greater than 3.135V.

Floating-Chassis Discharge Protection and ESD

Some set-top boxes have a floating chassis problem in which the chassis is not connected to earth ground. As a result, the chassis can charge up to 500V. When a SCART cable is connected to the SCART connector, the charged chassis can discharge through a signal pin. The equivalent circuit is a 2200pF capacitor charged to

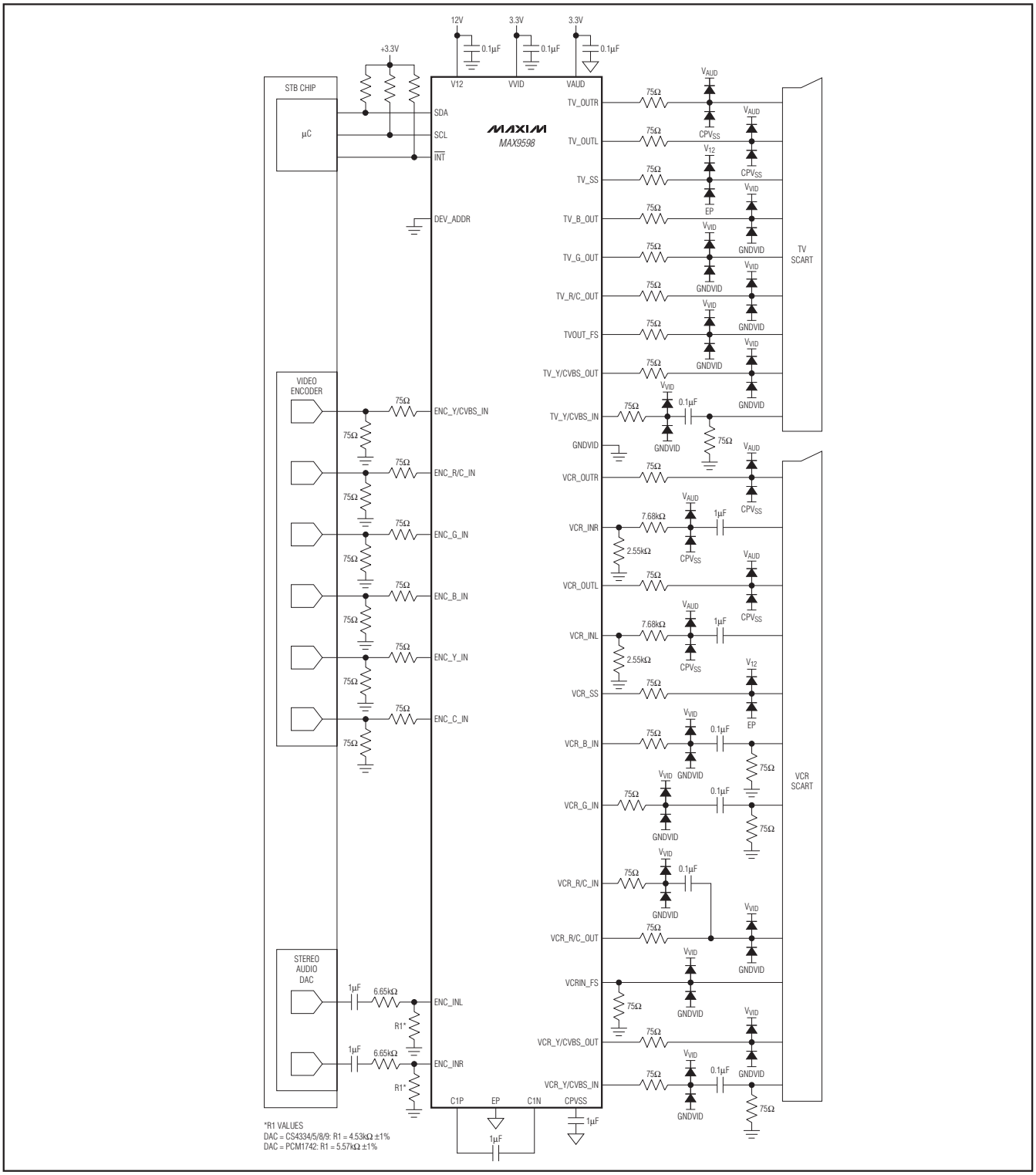

Figure 17. Application Circuit to Connect Series Resistors and External ESD Protection Diodes at MAX9598 Outputs

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311V connected through less than 0.1Ω to a signal pin. The MAX9598 is soldered on the PCB when it experiences such a discharge. Therefore, the current spike flows through both external and internal ESD protection devices and is absorbed by the supply bypass capacitors, which have high capacitance and low ESR.

To better protect the MAX9598 against excess voltages during the cable discharge condition or ESD events, add series resistors to all inputs and outputs to the SCART connector if series resistors are not already present in the application circuit. Also add external ESD protection diodes (for example, BAV99) on all inputs and outputs to the SCART connector.

Power-Supply Bypassing

The MAX9598 features single 3.3V and 12V supply operation and requires no negative supply. The 12V supply, V12 is for the SCART switching function. For V12, place a 0.1µF bypass capacitor as close as possible. Connect all VAUD pins together to 3.3V and bypass with a 10µF electrolytic capacitor in parallel with a 0.1µF ceramic capacitor to audio ground. Bypass each VVID to video ground with a 0.1µF ceramic capacitor.

Using a Digital Supply

The MAX9598 was designed to operate from noisy digital supplies. The high PSRR (49dB at 100kHz) allows the MAX9598 to reject the noise from the digital power supplies (see the *Typical Operating Characteristics*). If the digital power supply is very noisy and stripes appear on the television screen, increase the supply bypass capacitance. An additional, smaller capacitor in parallel with the main bypass capacitor can reduce digital supply noise because the smaller capacitor has lower equivalent series resistance (ESR) and equivalent series inductance (ESL).

Layout and Grounding

For optimal performance, use controlled-impedance traces for video signal paths and place input termination resistors and output back-termination resistors

Table 8. Data Format for Write Mode

REGISTER ADDRESS (HEXADECIMAL)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
00h	Not used	ZCD	Not used					TV audio output mute
01h	Not used	Not used	Not used	Interrupt enable	VCR audio selection		TV audio selection	
02h	Not used							
03h	Not used							
04h	Not used							
05h	Not used							
06h	Not used	Not used		TV G and B video switch		TV video switch		
07h	Not used	Not used	Not used	Set TV fast switching		Not used	Set TV slow switching	
08h	VCR_R/C_IN Clamp	Not used	Not used	Not used	ENC_R/C_IN clamp	VCR video switch		
09h	Not used	Not used	Not used	Not used	Not used	VCR_R/C_ OUT ground	Set VCR slow switching	
0Ah	Not used							
0Bh	Not used							
0Ch	Not used							
0Dh	VCR_Y/CVBS_OUT enable	VCR_R/C_ OUT enable	TV_R/C_ OUT enable	TV_G_OUT enable	TV_B_OUT enable	TV_Y/CVBS_ OUT enable	TVOUT_FS enable	Not used
10h	Operating mode		Not used					

Table 9. Data Format for Read Mode

REGISTER ADDRESS (HEXADECIMAL)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0Eh	Not used	Power-on reset	Not used		VCR slow-switch input status		TV slow-switch input status	
0Fh	Not used		ENC_Y_IN input video detection	ENC_Y/CVBS_IN input video detection	VCR CVBS output load	VCR CVBS input video detection	TV CVBS output load	TV CVBS input video detection

Table 10. Register 00h: Audio Control

DESCRIPTION	BIT								COMMENTS
	7	6	5	4	3	2	1	0	
TV Audio Mute								0	Off
								1	On (power-on default)
Zero-Crossing Detector		0							Off
		1							On (power-on default)

Table 11. Register 01h: TV Audio Control

DESCRIPTION	BIT								COMMENTS
	7	6	5	4	3	2	1	0	
Input Source for TV Audio							0	0	Encoder audio
							0	1	VCR audio
							1	0	Not used
							1	1	Mute (power-on default)
Input Source for VCR Audio					0	0			Encoder audio
					0	1			VCR audio
					1	0			Not used
					1	1			Mute (power-on default)
Interrupt Enable				0					Disabled (power-on default)
				1					Enabled

close to the MAX9598. Avoid routing video traces parallel to high-speed data lines.

The MAX9598 provides separate ground connections for video and audio supplies. For best performance, use separate ground planes for each of the ground returns and connect all ground planes together at a single point. Refer to the MAX9598 Evaluation Kit for a proven PCB layout example.

If the MAX9598 is mounted using flow soldering or wave soldering, the ground via(s) for the exposed pad should have a finished hole size of at least 14 mils to ensure adequate wicking of soldering onto the exposed pad. If the MAX9598 is mounted using solder mask technique, the via requirement does not apply. In either case, a good connection between the exposed pad and ground is required in order to minimize noise from coupling onto the outputs.

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Table 12. Register 06h: TV Video Input Control

DESCRIPTION	BIT								COMMENTS	
	7	6	5	4	3	2	1	0		
Input Sources for TV Video									**TV_Y/CVBS_OUT**	**TV_R/C_OUT**
						0	0	0	ENC_Y/CVBS_IN	ENC_R/C_IN
						0	0	1	ENC_Y_IN	ENC_C_IN
						0	1	0	VCR_Y/CVBS_IN	VCR_R/C_IN
						0	1	1	TV_Y/CVBS_IN	MUTE
						1	0	0	Not used	Not used
						1	0	1	Mute	Mute
						1	1	0	Mute	Mute
						1	1	1	Mute (power-on default)	Mute (power-on default)
Input Sources for TV_G_OUT and TV_B_OUT									**TV_G_OUT**	**TV_B_OUT**
				0	0				ENC_G_IN	ENC_B_IN
				0	1				VCR_G_IN	VCR_B_IN
				1	0				Mute	Mute
				1	1				Mute (power-on default)	Mute (power-on default)

Table 13. Register 07h: TV Video Output Control

DESCRIPTION	BIT								COMMENTS
	7	6	5	4	3	2	1	0	
Set TV Slow Switching							0	0	Low (< 2V). Internal source (power-on default).
							0	1	Medium (4.5V to 7V). External SCART source with 16:9 aspect ratio.
							1	0	High impedance
							1	1	High (> 9.5V). External SCART source with 4:3 aspect ratio.
Set TV Fast Switching				0	0				GNDVID (power-on default)
				0	1				Not used
				1	0				Same level as VCR_FB_IN
				1	1				VVID

Table 14. Register 08h: VCR Video Input Control

DESCRIPTION	BIT								COMMENTS	
	7	6	5	4	3	2	1	0		
Input Sources for VCR Video									VCR_Y/CVBS_OUT	VCR_R/C_OUT
						0	0	0	ENC_Y/CVBS_IN	ENC_R/C_IN
						0	0	1	ENC_Y_IN	ENC_C_IN
						0	1	0	VCR_Y/CVBS_IN	VCR_R/C_IN
						0	1	1	TV_Y/CVBS_IN	MUTE
						1	0	0	Not used	Not used
						1	0	1	Mute	Mute
						1	1	0	Mute	Mute
						1	1	1	Mute (power-on default)	Mute (power-on default)
ENC_R/C_IN Clamp/Bias					0				DC restore clamp active at input (power-on default)	
					1				Chrominance bias applied at input	
VCR_R/C_IN Clamp/Bias	0								DC restore clamp active at input (power-on default)	
	1								Chrominance bias applied at input	

Table 15. 09h: VCR Video Output Control

DESCRIPTION	BIT								COMMENTS
	7	6	5	4	3	2	1	0	
Set VCR Function Switching							0	0	Low (< 2V). Internal source (power-on default)
							0	1	Medium (4.5V to 7V). External SCART source with 16:9 aspect ratio.
							1	0	High impedance
							1	1	High (> 9.5V). External SCART source with 4:3 aspect ratio.
VCR_R/C_OUT Ground						0			Normal operation. Pulldown on TV_R/C_OUT is off (power-on default).
						1			Ground. Pulldown on TV_R/C_OUT is on, the output amplifier driving VCR_R/C_OUT turns off.

Low-Power Audio/Video Switch for Dual SCART Connectors

Table 16. Register 0Dh: Output Enable

DESCRIPTION	BIT								COMMENTS
	7	6	5	4	3	2	1	0	
TVOUT_FS Enable							0		Off (power-on default)
							1		On
TV_Y/CVBS_OUT Enable						0			Off (power-on default)
						1			On
TV_B_OUT Enable					0				Off (power-on default)
					1				On
TV_G_OUT Enable				0					Off (power-on default)
				1					On
TV_R/C_OUT Enable			0						Off (power-on default)
			1						On
VCR_R/C_OUT Enable		0							Off (power-on default)
		1							On
VCR_Y/CVBS_OUT Enable	0								Off (power-on default)
	1								On

Table 17. Register 10h: Operating Modes

DESCRIPTION	BIT								COMMENTS
	7	6	5	4	3	2	1	0	
Operating Mode	0	0							Shutdown.
	0	1							Low-power mode with slow switching, CVBS input video detection, and video load detection active only, audio circuitry is off.
	1	0							Full-power mode WITH input video detection and video load detection active.
	1	1							Full-power mode WITHOUT input video detection and video load detection active (power-on default).

Table 18. Register 0Eh: Status

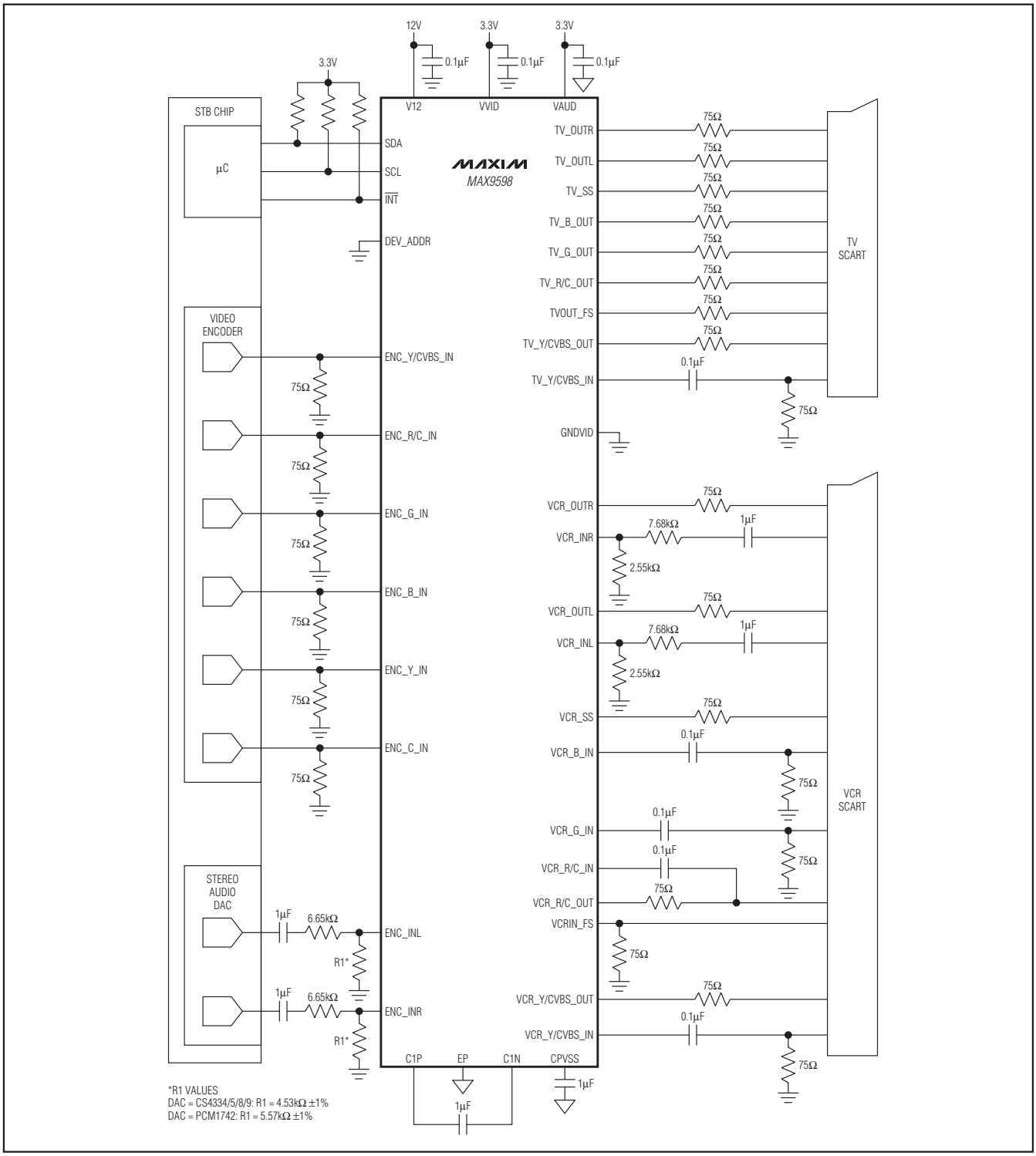
DESCRIPTION	BIT								COMMENTS
	7	6	5	4	3	2	1	0	
TV Slow-Switching Input Status							0	0	0 to 2V, internal source
							0	1	4.5V to 7V, external source with 16:9 aspect ratio
							1	0	Not used
							1	1	9.5V to 12.6V, external source with 4:3 aspect ratio
VCR Slow-Switching Input Status					0	0			0 to 2V, internal source
					0	1			4.5V to 7V, external source with 16:9 aspect ratio
					1	0			Not used
					1	1			9.5V to 12.6V, external source with 4:3 aspect ratio
Power-On Reset		0							V_DIG is too low for digital logic to operate
		1							V_DIG is high enough for digital logic to operate

Table 19. Register 0Fh: Video Activity Status

DESCRIPTION	BIT								COMMENTS
	7	6	5	4	3	2	1	0	
TV CVBS Input Video Detection								0	No video detected
								1	Video detected
TV CVBS Output Load							0		No load connected
							1		Load connected
VCR CVBS Input Video Detection						0			No video detected
						1			Video detected
VCR CVBS Output Load					0				No load connected
					1				Load connected
ENC_Y/CVBS_IN Input Video Detection				0					No video detected
				1					Video detected
ENC_Y_IN Input Video Detection			0						No video detected
			1						Video detected

Low-Power Audio/Video Switch for Dual SCART Connectors

Typical Application Circuit



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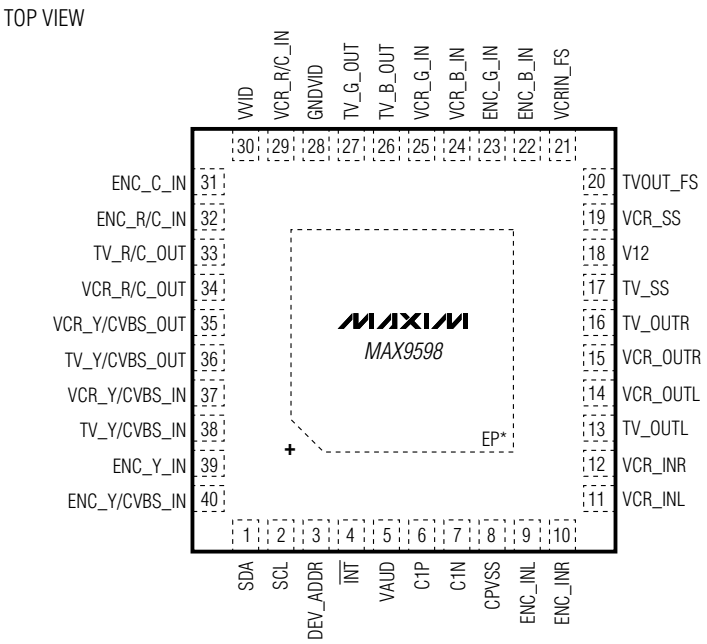
Pin Configuration



THIN QFN
(6mm x 6mm)

*EP = EXPOSED PAD

Chip Information

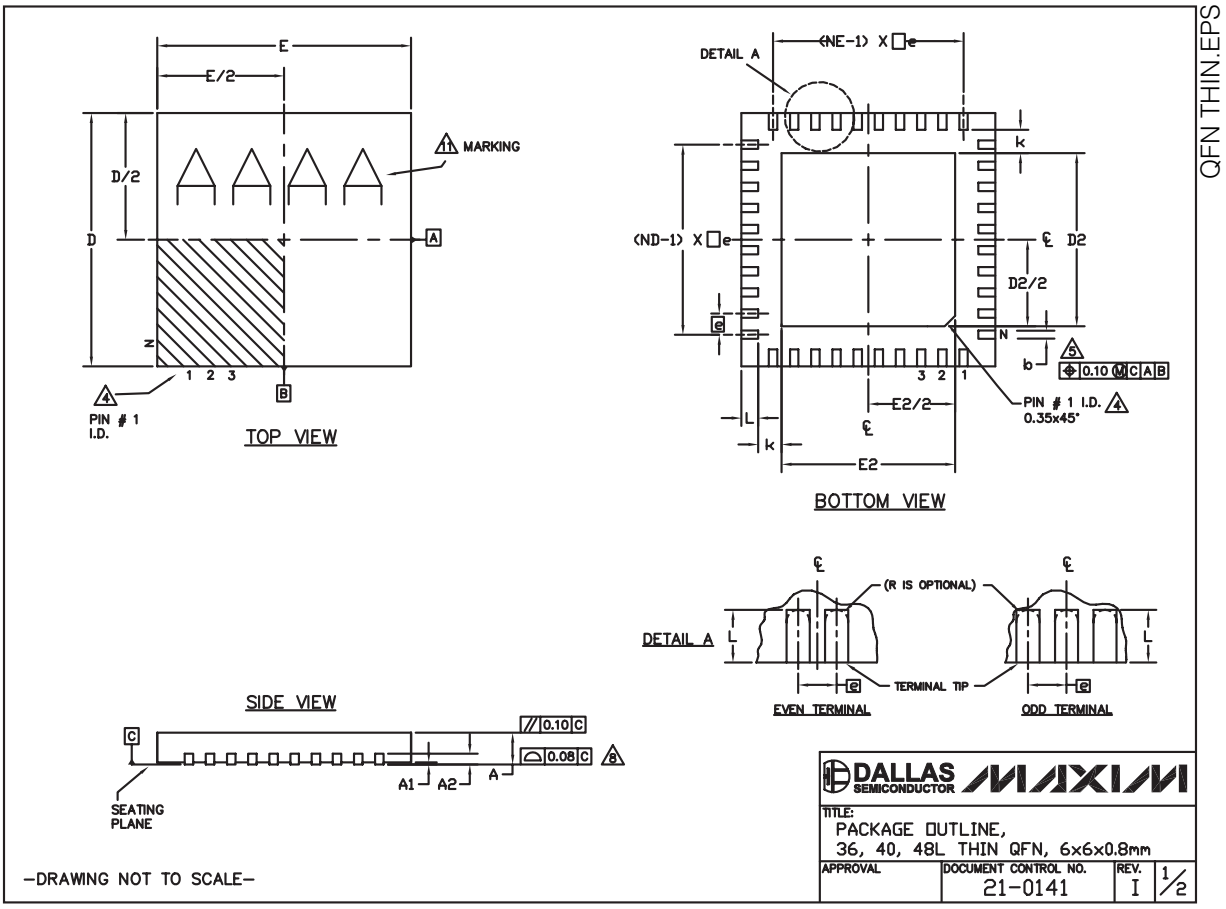
PROCESS: BiCMOS

Low-Power Audio/Video Switch for Dual SCART Connectors

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
40 TQFN-EP	T4066+3	21-0141



Package Information (continued)

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

COMMON DIMENSIONS									
PKG.	36L 6x6			40L 6x6			48L 6x6		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	–	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.		
b	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	5.90	6.00	6.10	5.90	6.00	6.10	5.90	6.00	6.10
E	5.90	6.00	6.10	5.90	6.00	6.10	5.90	6.00	6.10
e	0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	–	–	0.25	–	–	0.25	–	–
L	0.35	0.50	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	36			40			48		
ND	9			10			12		
NE	9			10			12		
JEDEC	WJJD-1			WJJD-2			–		

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T3666-2	3.60	3.70	3.80	3.60	3.70	3.80
T3666-3	3.60	3.70	3.80	3.60	3.70	3.80
T3666N-1	3.60	3.70	3.80	3.60	3.70	3.80
T3666MN-1	3.60	3.70	3.80	3.60	3.70	3.80
T4066-2	4.00	4.10	4.20	4.00	4.10	4.20
T4066-3	4.00	4.10	4.20	4.00	4.10	4.20
T4066-5	4.00	4.10	4.20	4.00	4.10	4.20
T4866-1	4.40	4.50	4.60	4.40	4.50	4.60
T4866N-1	4.40	4.50	4.60	4.40	4.50	4.60
T4866-2	4.40	4.50	4.60	4.40	4.50	4.60

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR 0.4mm LEAD PITCH PACKAGE T4866-1.
10. WARPAGE SHALL NOT EXCEED 0.10mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN FOR REFERENCE ONLY.
13. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 36, 40, 48L THIN QFN, 6x6x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0141	I	2/2

Low-Power Audio/Video Switch for Dual SCART Connectors

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	2/08	Initial release	—
1	2/09	Corrected various errors	4, 10, 16, 18, 21, 27, 31, 33

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