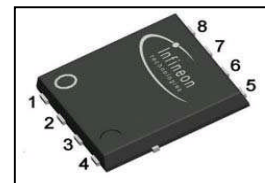


**OptiMOS™2 Power-Transistor**
**Features**

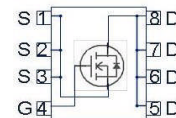
- For fast switching converters and sync. rectification
- Qualified according to JEDEC<sup>1)</sup> for target applications
- Super Logic level 2.5V rated; N-channel
- Excellent gate charge x  $R_{DS(on)}$  product (FOM)
- Very low on-resistance  $R_{DS(on)}$
- Superior thermal resistance
- Avalanche rated
- Pb-free plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

**Product Summary**

$V_{DS}$	20	V
$R_{DS(on),max}$	2.6	mΩ
$I_D$	100	A

**PG-TDSON-8**


Type	Package	Marking
BSC026N02KS G	PG-TDSON-8	026N02KS


**Maximum ratings, at  $T_j=25\text{ °C}$ , unless otherwise specified**

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	$I_D$	$V_{GS}=4.5\text{ V}, T_C=25\text{ °C}$	100	A
		$V_{GS}=4.5\text{ V}, T_C=100\text{ °C}$	85	
		$V_{GS}=2.5\text{ V}, T_C=25\text{ °C}$	100	
		$V_{GS}=2.5\text{ V}, T_C=100\text{ °C}$	65	
		$V_{GS}=4.5\text{ V}, T_A=25\text{ °C}, R_{thJA}=45\text{ K/W}^2$	25	
Pulsed drain current	$I_{D,pulse}$	$T_C=25\text{ °C}^3$	200	
Avalanche energy, single pulse	$E_{AS}$	$I_D=50\text{ A}, R_{GS}=25\text{ Ω}$	550	mJ
Reverse diode $dv/dt$	$dv/dt$	$I_D=50\text{ A}, V_{DS}=16\text{ V}, di/dt=200\text{ A/μs}, T_{j,max}=150\text{ °C}$	6	kV/μs
Gate source voltage	$V_{GS}$		±12	V

<sup>1)</sup> J-STD20 and JESD22

**Maximum ratings, at  $T_j=25\text{ °C}$ , unless otherwise specified**

Parameter	Symbol	Conditions	Value	Unit
Power dissipation	$P_{\text{tot}}$	$T_C=25\text{ °C}$	78	W
		$T_A=25\text{ °C}$ , $R_{\text{thJA}}=45\text{ K/W}^2)$	2.8	
Operating and storage temperature	$T_j, T_{\text{stg}}$		-55 ... 150	°C
IEC climatic category; DIN IEC 68-1			55/150/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Thermal characteristics**

Thermal resistance, junction - case	$R_{\text{thJC}}$	bottom	-	-	1.6	K/W
		top			18	
SMD version, device on PCB	$R_{\text{thJA}}$	minimal footprint	-	-	62	
		6 cm <sup>2</sup> cooling area <sup>2)</sup>	-	-	45	

**Electrical characteristics, at  $T_j=25\text{ °C}$ , unless otherwise specified**
**Static characteristics**

Drain-source breakdown voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}}=0\text{ V}, I_{\text{D}}=1\text{ mA}$	20	-	-	V
Gate threshold voltage	$V_{\text{GS(th)}}$	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=200\text{ }\mu\text{A}$	0.7	0.95	1.2	
Zero gate voltage drain current	$I_{\text{DSS}}$	$V_{\text{DS}}=20\text{ V}, V_{\text{GS}}=0\text{ V}, T_j=25\text{ °C}$	-	-	1	$\mu\text{A}$
		$V_{\text{DS}}=20\text{ V}, V_{\text{GS}}=0\text{ V}, T_j=125\text{ °C}$	-	-	100	
Gate-source leakage current	$I_{\text{GSS}}$	$V_{\text{GS}}=12\text{ V}, V_{\text{DS}}=0\text{ V}$	-	-	100	nA
Drain-source on-state resistance	$R_{\text{DS(on)}}$	$V_{\text{GS}}=2.5\text{ V}, I_{\text{D}}=50\text{ A}$	-	3.4	4.5	m $\Omega$
		$V_{\text{GS}}=4.5\text{ V}, I_{\text{D}}=50\text{ A}$	-	2.1	2.6	
Gate resistance	$R_{\text{G}}$		-	1.5	-	$\Omega$
Transconductance	$g_{\text{fs}}$	$ V_{\text{DS}} >2 I_{\text{D}} R_{\text{DS(on)max}}, I_{\text{D}}=50\text{ A}$	95	190	-	S

<sup>2)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70  $\mu\text{m}$  thick) copper area for drain connection. PCB is vertical in still air.

<sup>3)</sup> See figure 3

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Dynamic characteristics**

Input capacitance	$C_{iss}$	$V_{GS}=0\text{ V}, V_{DS}=10\text{ V},$ $f=1\text{ MHz}$	-	5900	7800	pF
Output capacitance	$C_{oss}$		-	1700	2300	
Reverse transfer capacitance	$C_{rss}$		-	250	380	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=10\text{ V}, V_{GS}=4.5\text{ V},$ $I_D=50\text{ A}, R_G=1.6\ \Omega$	-	21	-	ns
Rise time	$t_r$		-	115	-	
Turn-off delay time	$t_{d(off)}$		-	52	-	
Fall time	$t_f$		-	9	-	

**Gate Charge Characteristics<sup>4)</sup>**

Gate to source charge	$Q_{gs}$	$V_{DD}=10\text{ V}, I_D=30\text{ A},$ $V_{GS}=0\text{ to }4.5\text{ V}$	-	11.4	15.2	nC
Gate charge at threshold	$Q_{g(th)}$		-	6	7.4	
Gate to drain charge	$Q_{gd}$		-	7	10.8	
Switching charge	$Q_{sw}$		-	13	18.6	
Gate charge total	$Q_g$		-	40	52.7	
Gate plateau voltage	$V_{plateau}$		-	1.9	-	
Gate charge total, sync. FET	$Q_{g(sync)}$	$V_{DS}=0.1\text{ V},$ $V_{GS}=0\text{ to }4.5\text{ V}$	-	36	48.2	nC
Output charge	$Q_{oss}$	$V_{DD}=10\text{ V}, V_{GS}=0\text{ V}$	-	23	-	

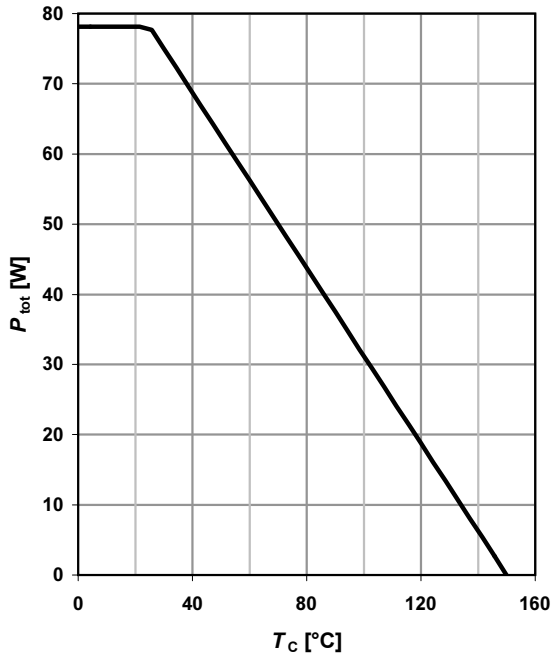
**Reverse Diode**

Diode continuous forward current	$I_S$	$T_C=25\text{ }^\circ\text{C}$	-	-	92	A
Diode pulse current	$I_{S,pulse}$		-	-	200	
Diode forward voltage	$V_{SD}$	$V_{GS}=0\text{ V}, I_F=50\text{ A},$ $T_j=25\text{ }^\circ\text{C}$	-	0.85	1.2	V
Reverse recovery charge	$Q_{rr}$	$V_R=10\text{ V}, I_F=I_S,$ $di_F/dt=100\text{ A}/\mu\text{s}$	-	28	-	nC

<sup>4)</sup> See figure 16 for gate charge parameter definition

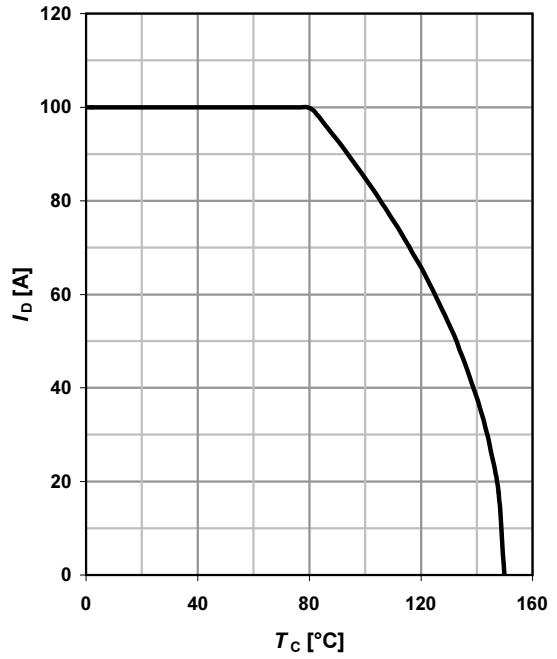
**1 Power dissipation**

$P_{tot}=f(T_C)$



**2 Drain current**

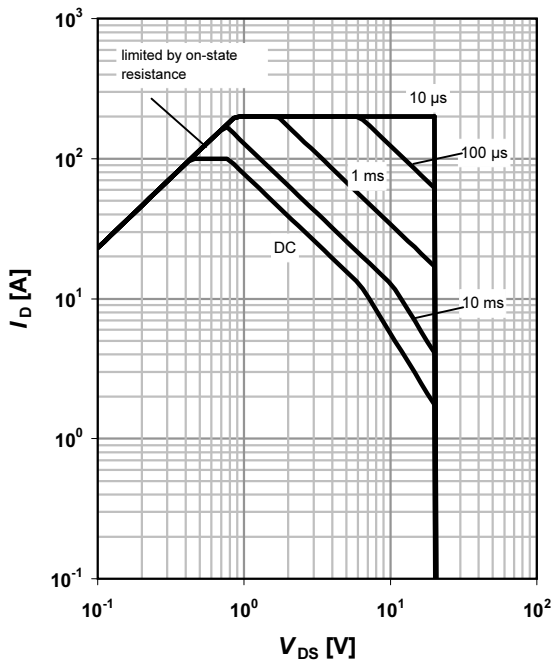
$I_D=f(T_C); V_{GS} \geq 4.5 V$



**3 Safe operating area**

$I_D=f(V_{DS}); T_C=25\text{ °C}; D=0$

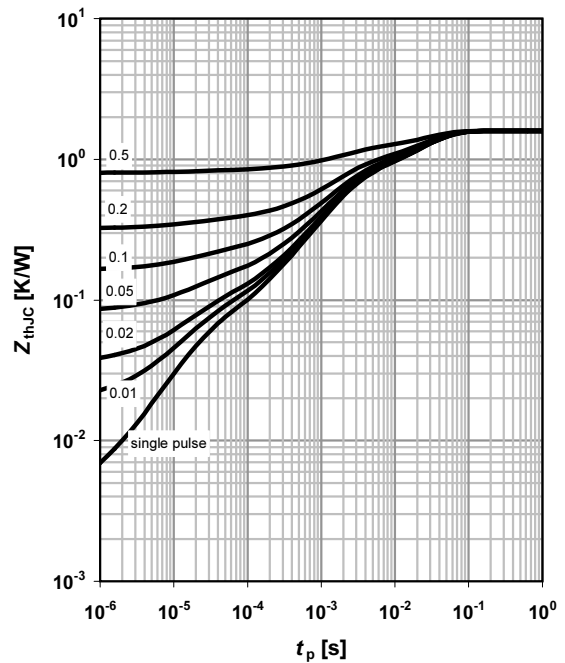
parameter:  $t_p$



**4 Max. transient thermal impedance**

$Z_{thJC}=f(t_p)$

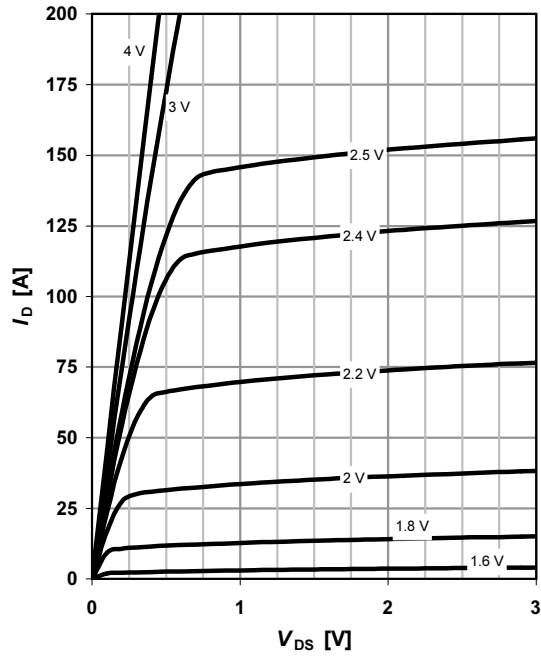
parameter:  $D=t_p/T$



**5 Typ. output characteristics**

$I_D = f(V_{DS}); T_j = 25\text{ }^\circ\text{C}$

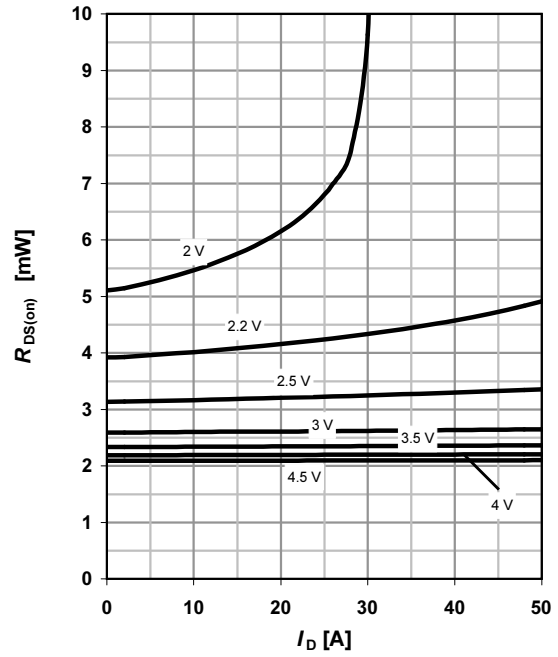
parameter:  $V_{GS}$



**6 Typ. drain-source on resistance**

$R_{DS(on)} = f(I_D); T_j = 25\text{ }^\circ\text{C}$

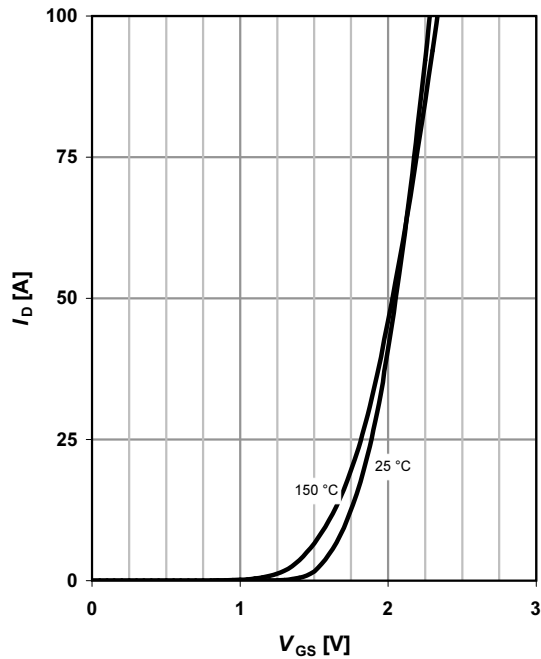
parameter:  $V_{GS}$



**7 Typ. transfer characteristics**

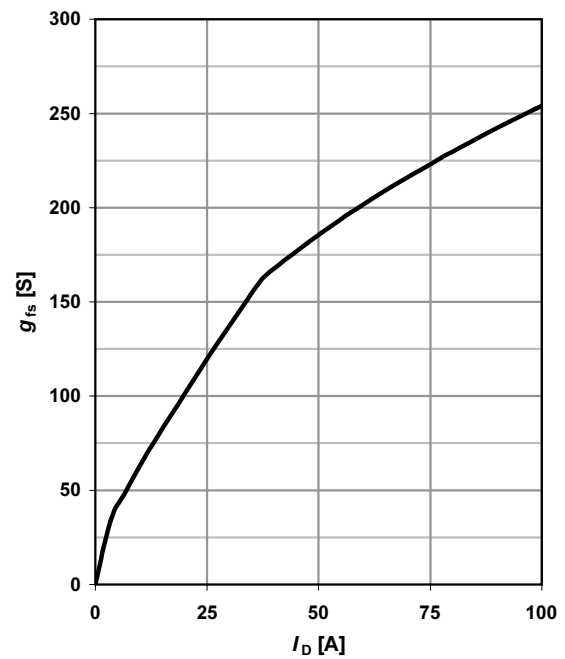
$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}$

parameter:  $T_j$



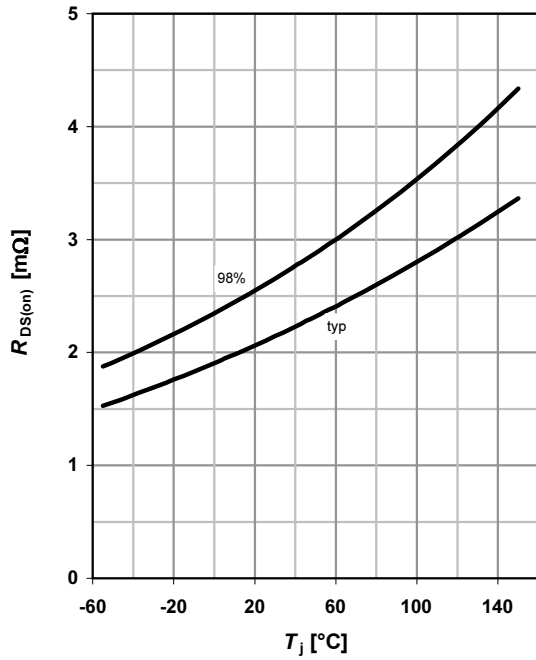
**8 Typ. forward transconductance**

$g_{fs} = f(I_D); T_j = 25\text{ }^\circ\text{C}$



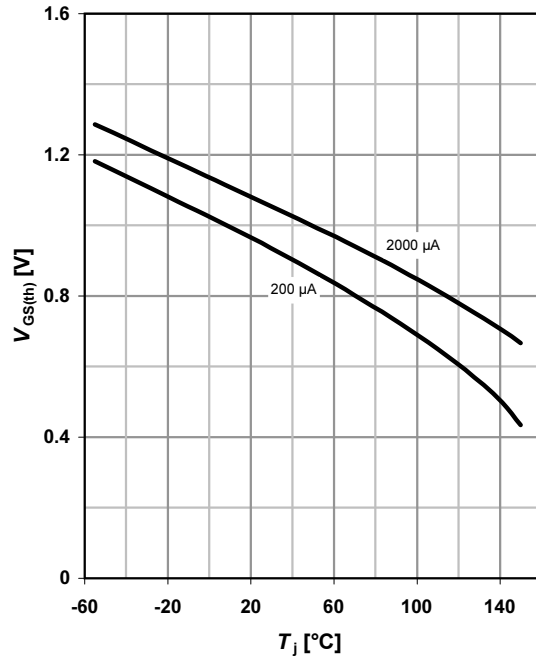
**9 Drain-source on-state resistance**

$R_{DS(on)} = f(T_j); I_D = 50 \text{ A}; V_{GS} = 4.5 \text{ V}$



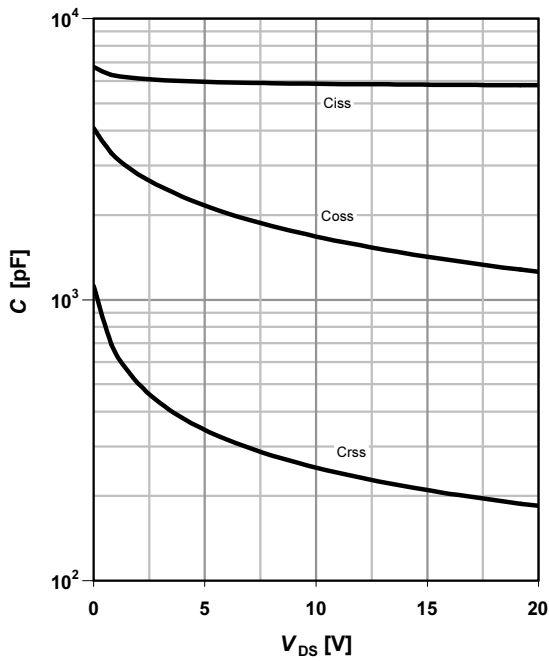
**10 Typ. gate threshold voltage**

$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$



**11 Typ. capacitances**

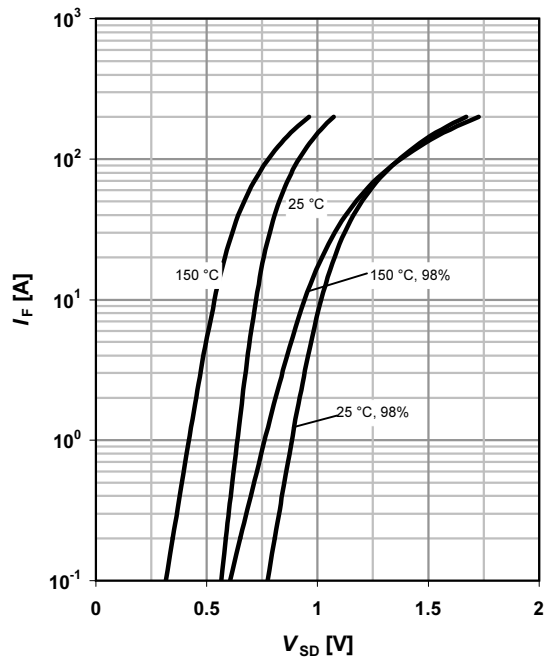
$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$



**12 Forward characteristics of reverse diode**

$I_F = f(V_{SD})$

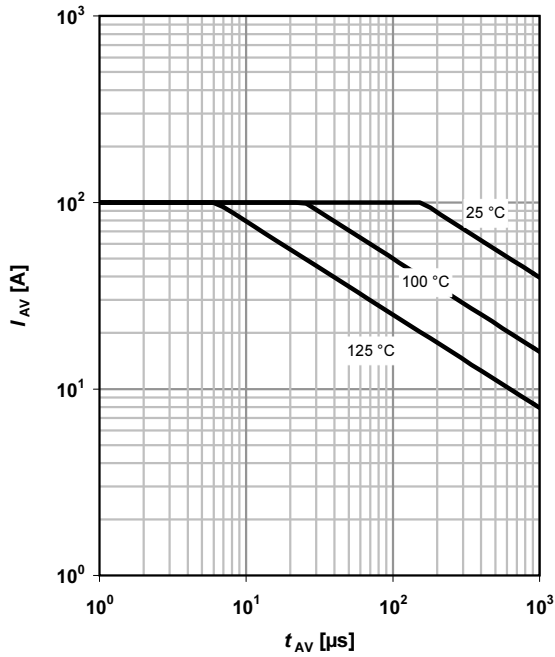
parameter:  $T_j$



**13 Avalanche characteristics**

$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$

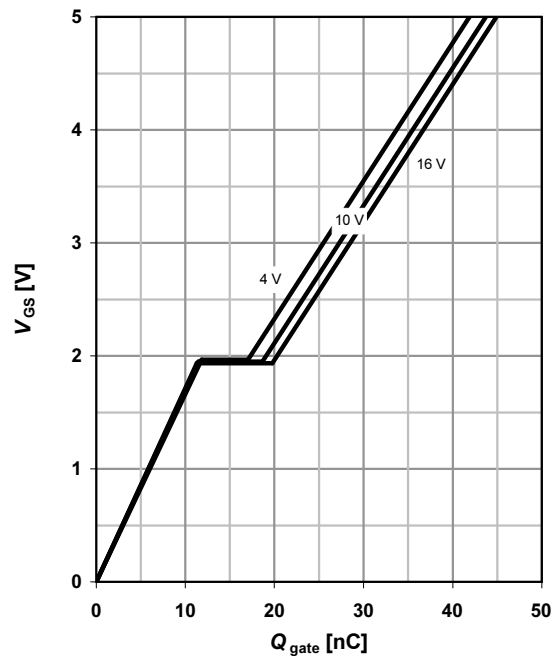
parameter:  $T_{j(start)}$



**14 Typ. gate charge**

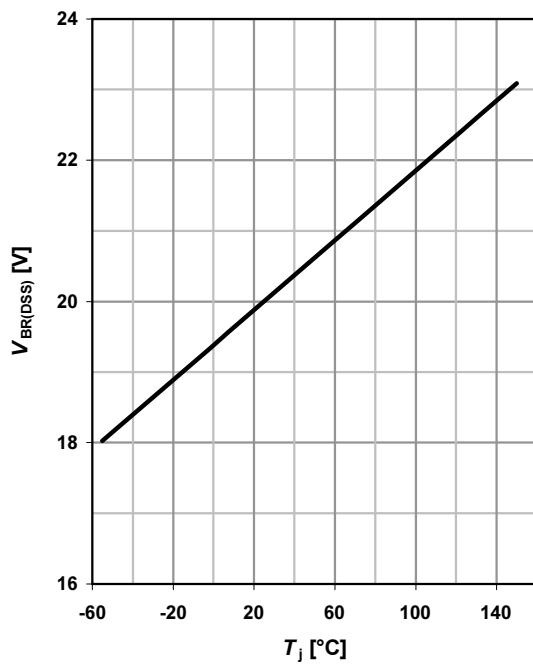
$V_{GS}=f(Q_{gate}); I_D=30 \text{ A pulsed}$

parameter:  $V_{DD}$

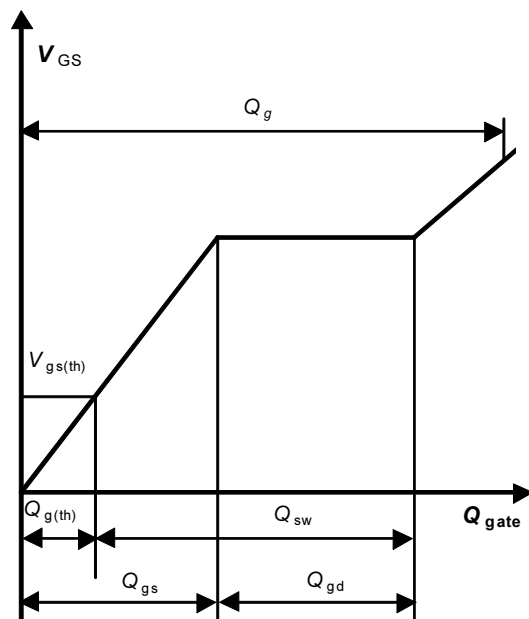


**15 Drain-source breakdown voltage**

$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$



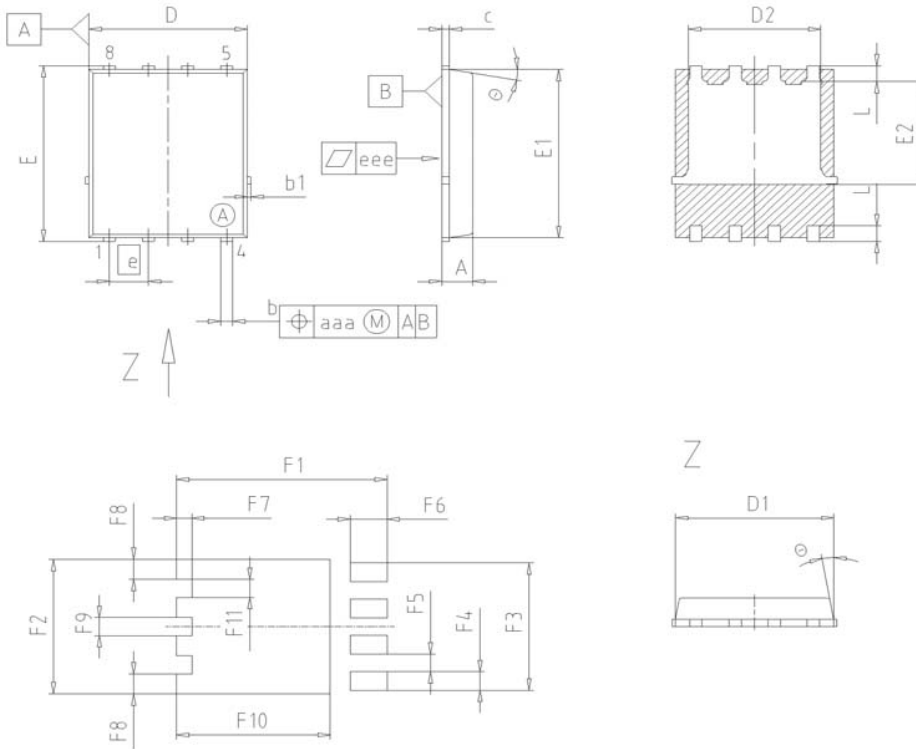
**16 Gate charge waveforms**



Package Outline

PG-TDSON-8

PG-TDSON-8: Outline



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.90	1.10	0.035	0.043
b	0.34	0.54	0.013	0.021
b1	0.02	0.22	0.001	0.008
c	0.15	0.35	0.006	0.014
D=D1	4.95	5.35	0.195	0.211
D2	4.20	4.40	0.165	0.173
E	5.95	6.35	0.234	0.250
E1	5.70	6.10	0.224	0.240
E2	3.40	3.80	0.134	0.150
e	1.27		0.050	
N	8		8	
L	0.45	0.65	0.018	0.026
□	8.5°	11.5°	8.5°	11.5°
aaa	0.25		0.010	
eee	0.05		0.002	
F1	6.75	6.95	0.266	0.274
F2	4.60	4.80	0.181	0.189
F3	4.36	4.56	0.172	0.180
F4	0.55	0.75	0.022	0.030
F5	0.52	0.72	0.020	0.028
F6	1.10	1.30	0.043	0.051
F7	0.40	0.60	0.016	0.024
F8	0.60	0.80	0.024	0.031
F9	0.53	0.73	0.021	0.029
F10	4.90	5.10	0.193	0.201
F11	0.53	0.73	0.021	0.029

**DOCUMENT NO.**  
Z8B00003332

**SCALE**

**EUROPEAN PROJECTION**

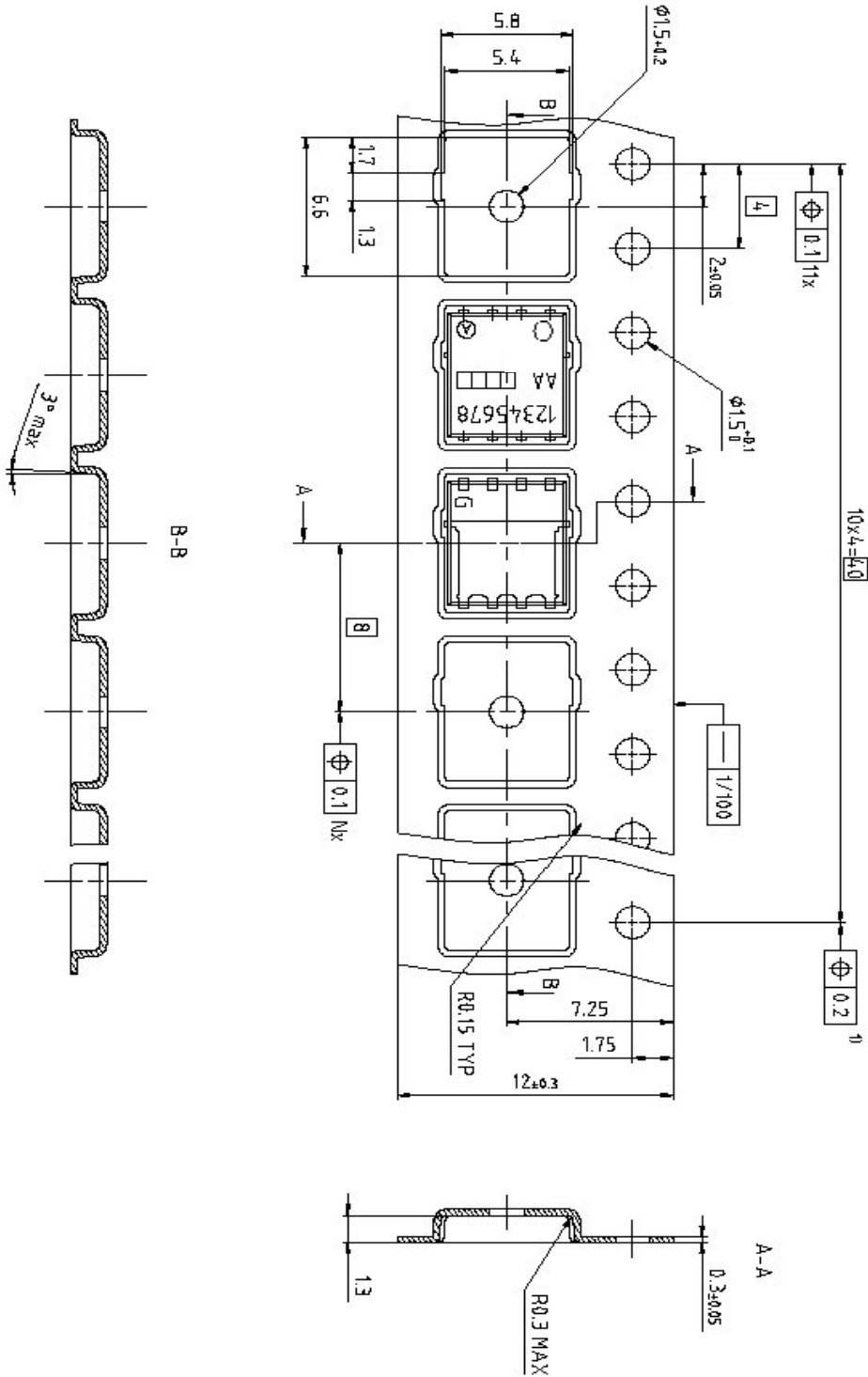
**ISSUE DATE**  
08-03-2007

**REVISION**  
03



Package Outline

PG-TDSON-8: Tape



Dimensions in mm

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