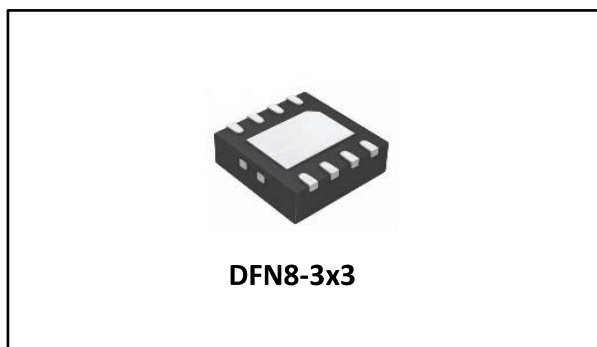


1 A ultra low-dropout regulator with reverse current protection

Datasheet - production data



Features

- Input voltage range: 2.2 V to 5.5 V
- Ultra low-dropout: 200 mV typ. at 1 A
- NMOS topology
- Very high PSRR: 78 dB @ 100 Hz, 70 dB @ 100 kHz
- Very fast response to load variation
- Stable with 1 μ F capacitor
- Thermal shutdown
- Current limit
- Adjustable from 1.2 V
- High output voltage accuracy:
 - 1 % typ. (3 % max.)

Applications

- Post-regulation generic POL
- Portable equipment
- Industrial applications
- Telecom infrastructure

Description

The LD59100 is a 1 A LDO regulator designed for use in various environments. Its N-MOS topology allows reduction of the R_{dson} of the pass-element, maintaining a very low-dropout voltage even with very low input power supply voltage.

The device features very high PSRR characteristics over a wide frequency band, rendering it suitable for use as a secondary regulator for noise-sensitive applications.

The enable function can be used to further decrease the overall current consumption in shutdown mode.

The LD59100 embeds protection features, such as current limit, thermal shutdown and reverse output current protection.

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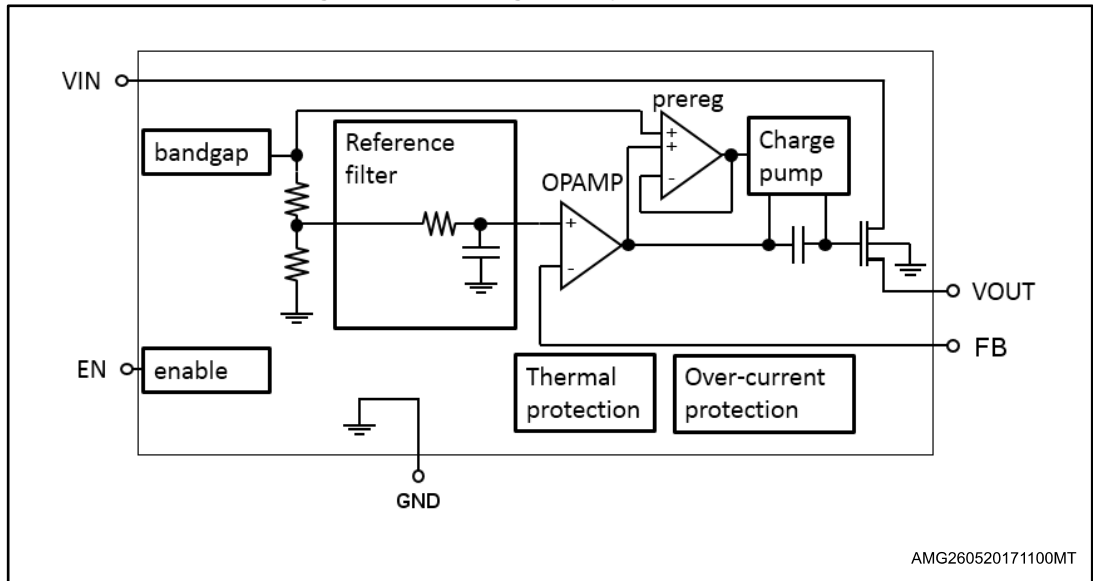
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1 Diagram

Figure 1: Block diagram, adjustable version



2 Pin configuration

Figure 2: Pin connection (top view)

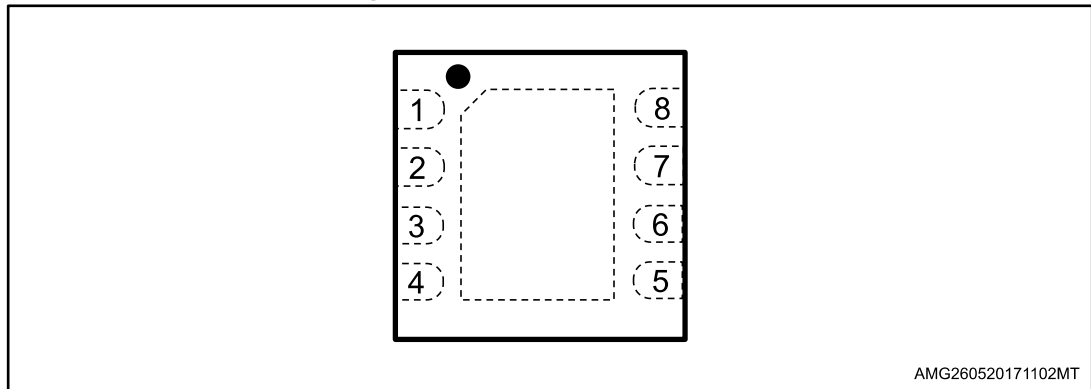
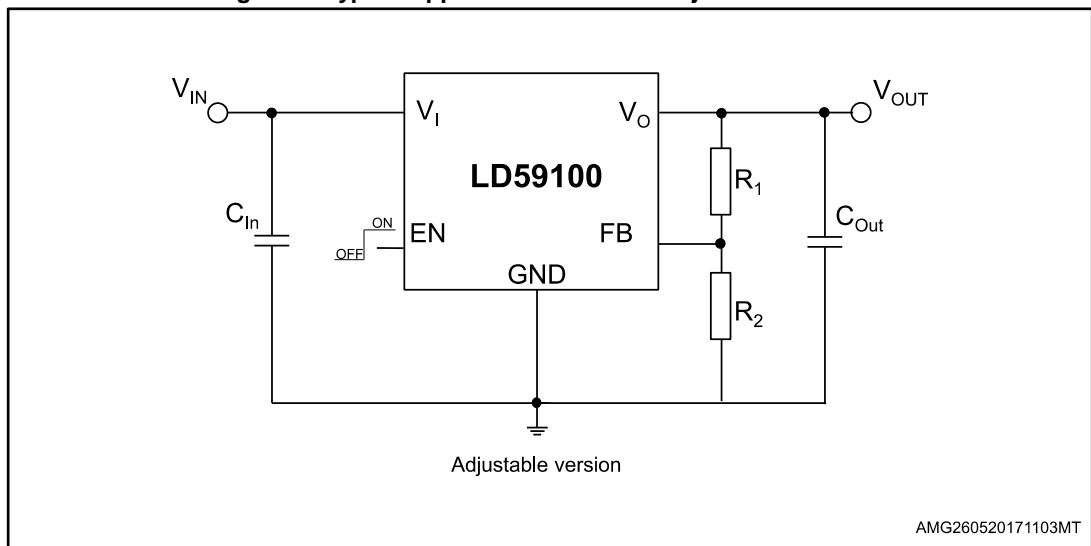


Table 1: Adjustable version: pin description

Pin	Symbol	Function
DFN8-3x3		
1	OUT	Regulated output voltage of the LDO
3	FB	Feedback to set the output voltage
4	GND	Ground
5	EN	Enable pin logic input: Low = shutdown, High = active
2, 6, 7	NC	Not connected
8	IN	Input pin
Tab	EXP	Exposed pad. Connect to GND on PCB.

3 Typical application

Figure 3: Typical application circuit for adjustable version



4 Maximum ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{IN}	DC input voltage	- 0.3 to 6	V
V _{OUT}	DC output voltage	- 0.3 to 5.5	V
V _{EN}	Enable input voltage	- 0.3 to 6	V
V _{FB}	Feedback pin voltage	- 0.3 to 6	V
I _{OUT}	Output current	Internally limited	mA
P _D	Power dissipation	Internally limited	mW
T _{ST}	Storage temperature range	- 65 to 150	°C
T _{OP}	Operating temperature range	- 40 to 125	°C



Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. All values are referred to GND.

Table 3: Thermal data

Symbol	Parameter	DFN8-3x3	Unit
R _{thJA}	Thermal resistance junction-ambient	55	°C/W
R _{thJC}	Thermal resistance junction-case	10	°C/W

Table 4: Electrostatic discharge

Symbol	Parameter	DFN8-3x3	Unit
HBM	Human body model	+/-2	kV
CDM	Charged device model	+/-500	V

5 Electrical characteristics

$T_A = T_J = -40\text{ °C}$ to $+125\text{ °C}$, typical values refer to $T_A = +25\text{ °C}$, $V_{EN} = 2.2\text{ V}$,
 $V_{IN} = V_{OUT} + 1\text{ V}$, $I_{OUT} = 10\text{ mA}$, $C_{IN} = C_{OUT} = 1\text{ }\mu\text{F}$, unless otherwise specified (see note 1).

Table 5: Electrical characteristics for LD59100 adjustable

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{IN}	Operating input voltage		2.2		5.5	V
I_{OUT}	Guaranteed output current		0		1	A
V_{OUT}	Output voltage range		V_{FB}		$5.5 - V_{DROP}$	
	V_{OUT} accuracy	Nominal	-1		1	%
		$V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$ to 5.5 V $I_{OUT} = 0\text{ mA}$ to 1 A	-3		3	%
V_{FB}	Internal reference		1.192	1.204	1.216	V
I_{FB}	Adjustable pin leakage current			0.1	0.6	μA
ΔV_{OUT}	Static line regulation	$V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$ to 5.5 V		0.005		%V
		$I_{OUT} = 10\text{ mA}$				
ΔV_{OUT}	Static load regulation	$I_{OUT} = 1\text{ mA}$ to 1 A		0.0001		%/mA
V_{DROP}	Dropout voltage	$I_{OUT} = 1\text{ A}$, $V_{OUT} > 2.4\text{ V}$		200	500	mV
		$V_{IN} = V_{OUT(NOM)} - 0.1\text{ V}$				
eN	Output noise voltage ⁽¹⁾	$f = 10\text{ Hz}$ to 100 kHz , $I_{OUT} = 10\text{ mA}$ $C_{OUT} = 10\text{ }\mu\text{F}$		$27 \times V_{OUT}$		μV_{RMS}
SVR	Supply voltage rejection ⁽²⁾	$V_{IN} = V_{OUT(NOM)} + 1\text{ V} \pm V_{RIPPLE}$ $V_{RIPPLE} = 0.5\text{ V}$, $I_{OUT} = 10\text{ mA}$ $f = 100\text{ Hz}$		78		dB
		$V_{IN} = V_{OUT(NOM)} + 1\text{ V} \pm V_{RIPPLE}$ $V_{RIPPLE} = 0.5\text{ V}$, $I_{OUT} = 10\text{ mA}$ $f = 10\text{ KHz}$		62		
		$V_{IN} = V_{OUT(NOM)} + 1\text{ V} \pm V_{RIPPLE}$ $V_{RIPPLE} = 0.5\text{ V}$, $I_{OUT} = 10\text{ mA}$ $f = 100\text{ kHz}$		70		
		$V_{IN} = V_{OUT(NOM)} + 1\text{ V} \pm V_{RIPPLE}$ $V_{RIPPLE} = 0.5\text{ V}$, $I_{OUT} = 1\text{ A}$ $f = 100\text{ Hz}$		58		

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
		$V_{IN} = V_{OUT(NOM)} + 1\text{ V} \pm V_{RIPPLE}$ $V_{RIPPLE} = 0.5\text{ V}$, $I_{OUT} = 1\text{ A}$ $f = 10\text{ KHz}$		37		
I_Q	Quiescent current	$I_{OUT} = 0\text{ mA}$		130		μA
		$I_{OUT} = 10\text{ mA}$		140		
		$I_{OUT} = 1\text{ A}$		280		
		V_{IN} Input current in OFF mode		0.02		
		$V_{EN} = \text{GND}$				
I_{CL}	Output current limit	$V_{OUT} = 0.9 \times V_{OUT(NOM)}$	1.05	1.6	2.2	A
I_{SC}	Short-circuit current	$R_L = 0$		450		mA
I_{REV}	Reverse leakage current	$V_{EN} < 0.5\text{ V}$, $0 < V_{IN} < V_{OUT}$		0.1		μA
V_{EN}	Enable input logic low				0.5	V
	Enable input logic high		1.7			
I_{EN}	Enable pin input current	$V_{EN} = V_{IN} = 5.5\text{ V}$		20		nA
T_{SHDN}	Thermal shutdown ⁽²⁾			160		$^{\circ}\text{C}$
	Hysteresis ⁽²⁾			20		
T_{STR}	Start-up time	$V_{OUT} = 3\text{ V}$, $R_L = 30\ \Omega$, $C_{OUT} = 1\ \mu\text{F}$		600		μs

Notes:

⁽¹⁾Values at below 0 °C are guaranteed by design and/or characterization tested at $T_A = \sim T_J$. Low duty cycle pulse techniques are used.

⁽²⁾Guaranteed by design, not tested in production.

6 Application information

6.1 Output voltage setting for adjustable version

In the adjustable version, the output voltage can be set from 1.204 V (V_{FB}) up to the input voltage minus the voltage drop across the pass transistor (dropout voltage), by connecting a resistor divider between the FB pin and the output, thereby implementing remote voltage sensing. With reference to the typical circuit shown in [Figure 4: "Line regulation vs temperature \(\$V_{IN} = 2.5\$ to \$5.5\$ V, \$V_{OUT} = V_{FB}\$, \$I_{OUT} = 10\$ mA\)"](#), the resistor divider can be designed by using the following equation:

Equation 2

$$V_{OUT} = V_{FB}(1 + R_1/R_2), \quad \text{with} \quad V_{FB} = 1.204 \text{ V} \quad \text{typ.}$$

It is recommended to use resistors with values in the range of 10 k Ω to 100 k Ω . Lower values can also be suitable, but will result in an increase in current consumption.

The following table shows an example of R_1 , R_2 choices, among standard 1% resistors, to obtain the most common output voltages.

Table 6: Resistor divider settings for common output voltages

V_{OUT}	R_1	R_2
1.204 (V_{FB})	Short	Open
1.5	23.2 k Ω	95.3 k Ω
1.8	28.0 k Ω	56.2 k Ω
2.5	39.2 k Ω	36.5 k Ω
2.8	44.2 k Ω	33.2 k Ω
3	46.4 k Ω	30.9 k Ω
3.3	52.3 k Ω	30.1 k Ω

6.2 Input and output capacitors

Input capacitor

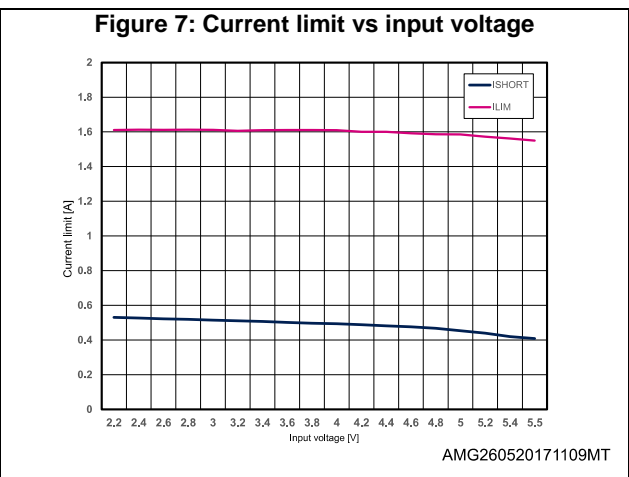
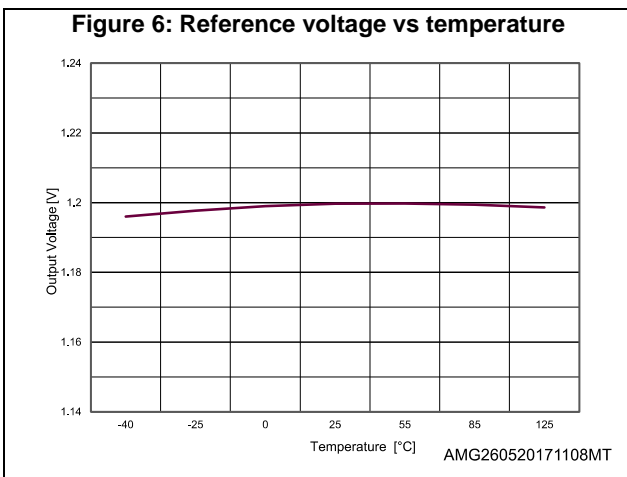
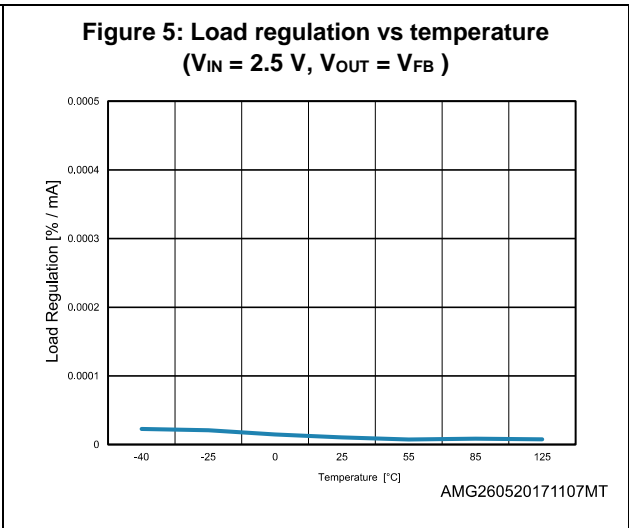
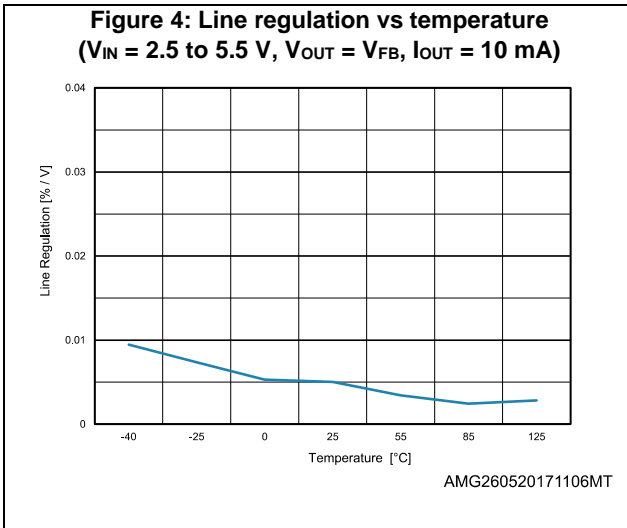
An input capacitor with a minimum value of 1 μF must be located as close as possible to the input pin of the device and returned to a clean analog ground. A good quality, low-ESR ceramic capacitor is recommended. This capacitor helps to ensure stability of the control loop, reduces the effects of inductive sources and improves ripple rejection. A capacitance value larger than 1 μF can be used in the case of fast load transients in the application.

Output capacitor

The LD59100 requires a capacitor connected to its output, to keep the control loop stable and reduce the risk of ringing and oscillations. The control loop is designed to be stable with any good quality ceramic capacitor (such as X5R/X7R types) with a minimum value of 1 μF and equivalent series resistance in the 5 m Ω to 1 Ω range. It is important to highlight that the output capacitor must maintain its capacitance and ESR in the stable region over the full operating temperature, load and input voltage ranges, to assure stability. Therefore, capacitance and ESR variations must be taken into account in the design phase to ensure the device works in the expected stability region. There is no maximum limit to the output capacitance, provided that the above conditions are respected.

7 Typical characteristics

$C_{IN} = C_{OUT} = 1 \mu F$, $V_{EN} = V_{IN} = 2.5 V$, $V_{OUT} = V_{FB}$, $T_J = 25 \text{ }^\circ\text{C}$, unless otherwise specified.



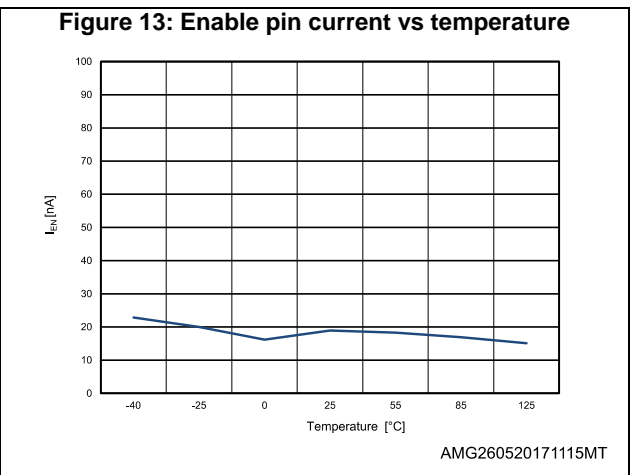
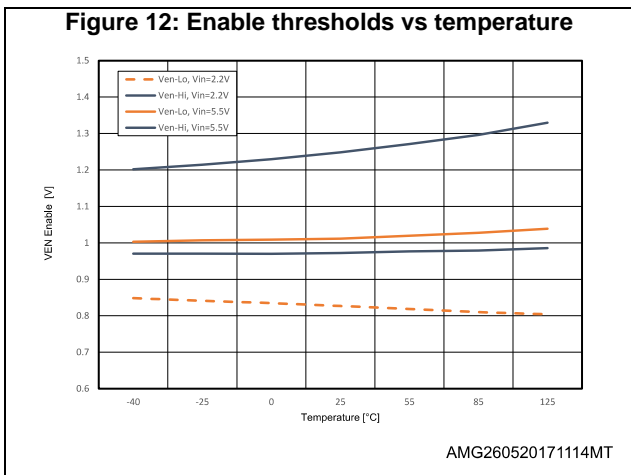
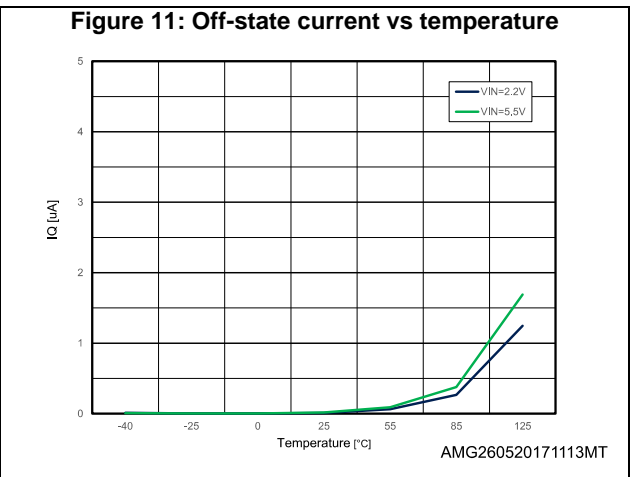
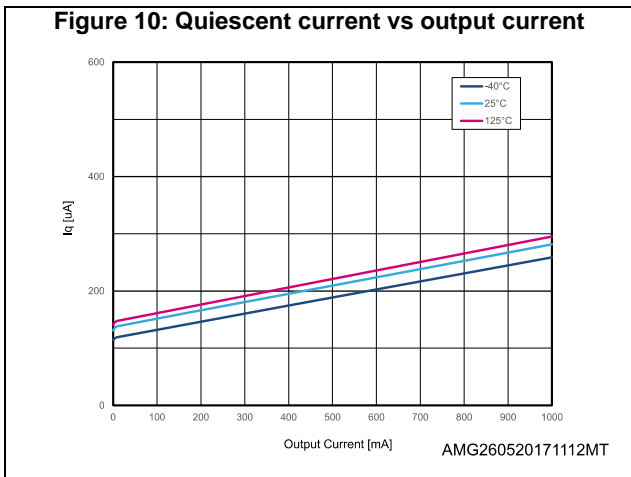
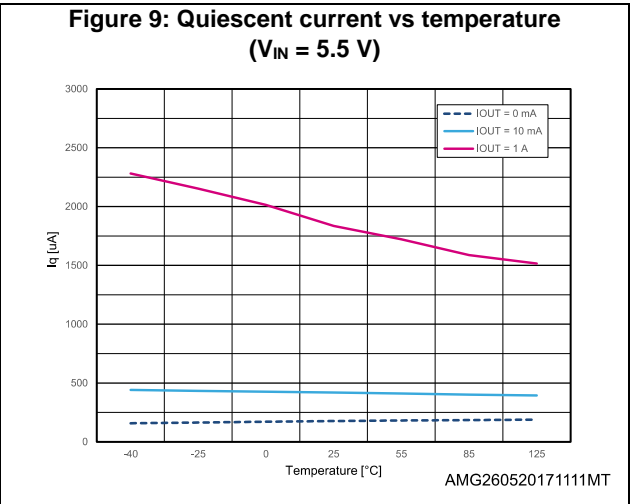
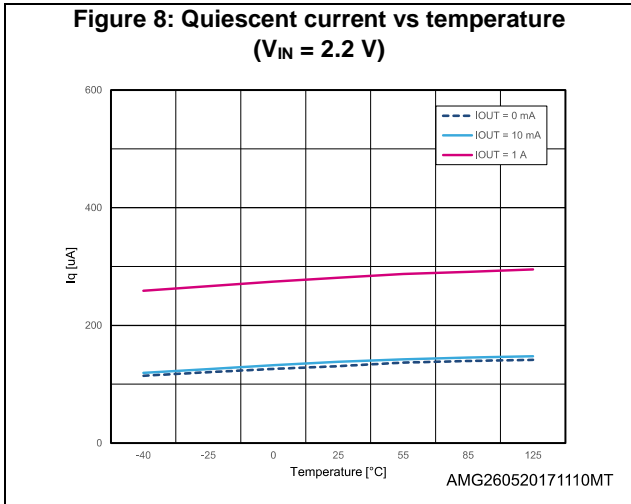


Figure 14: Feedback pin current vs temperature

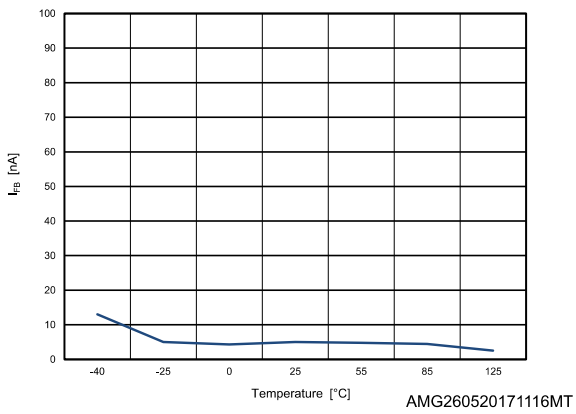


Figure 15: Reverse current vs temperature

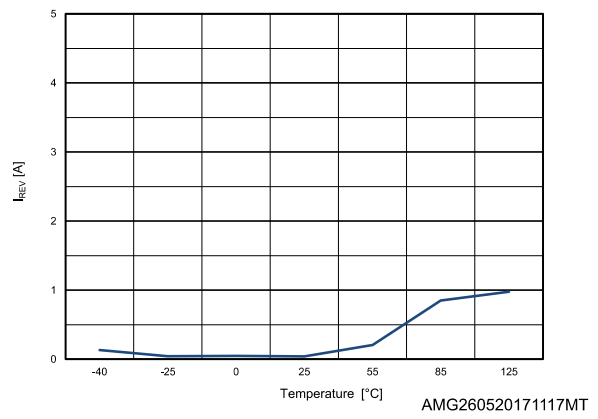


Figure 16: Dropout voltage vs temperature

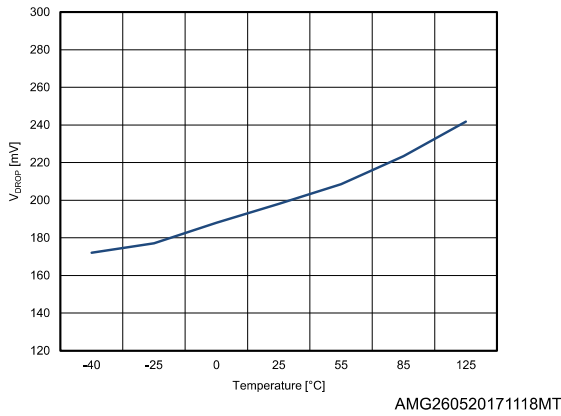


Figure 17: Dropout voltage vs output current

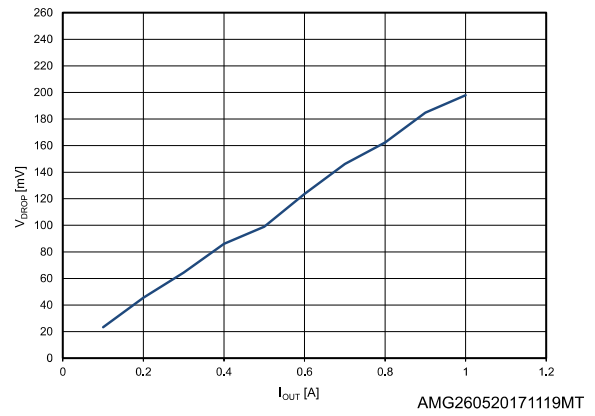


Figure 18: Dropout voltage vs input voltage

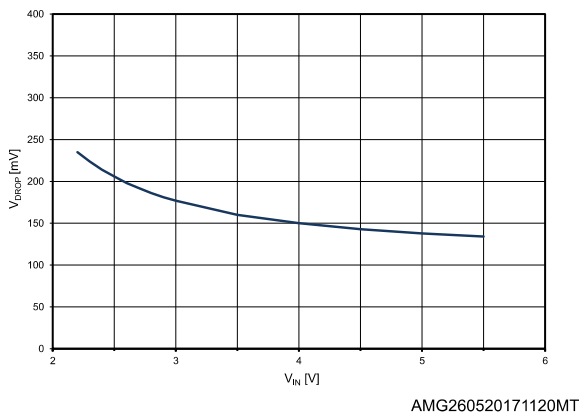
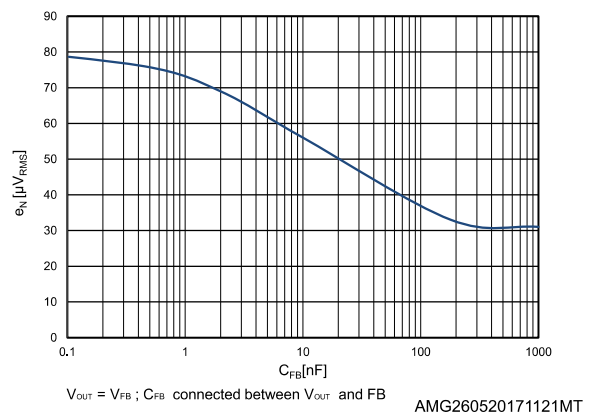
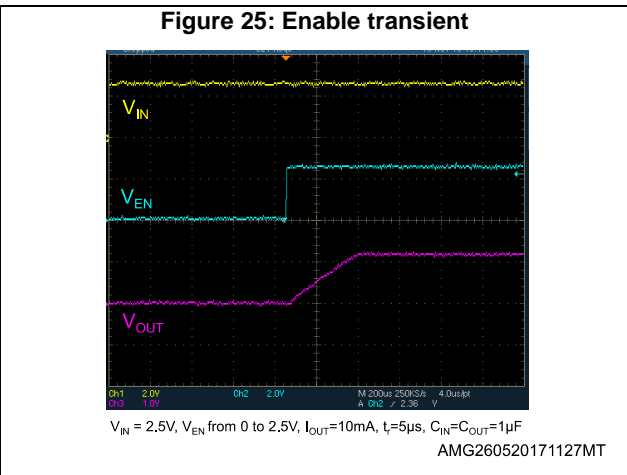
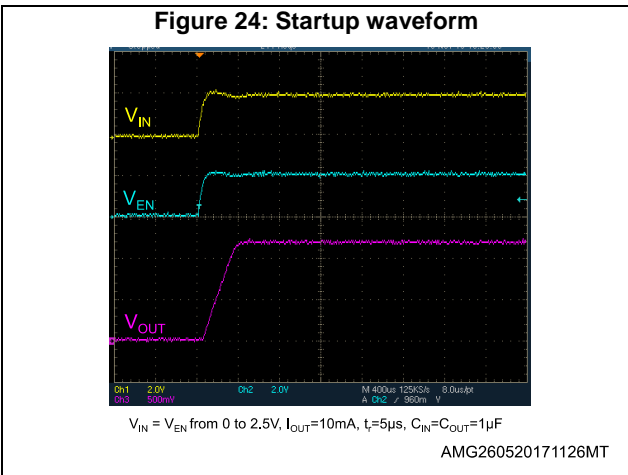
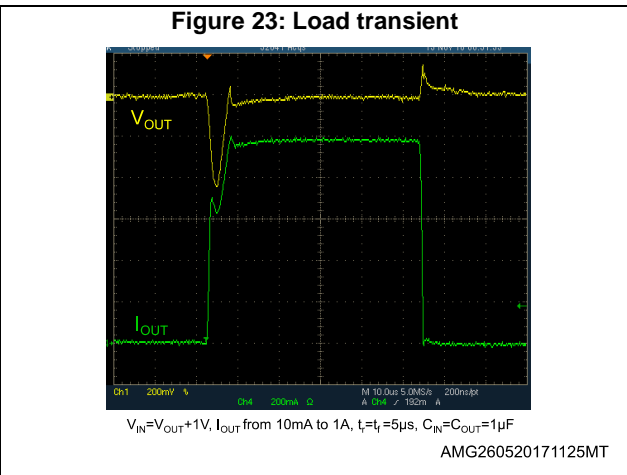
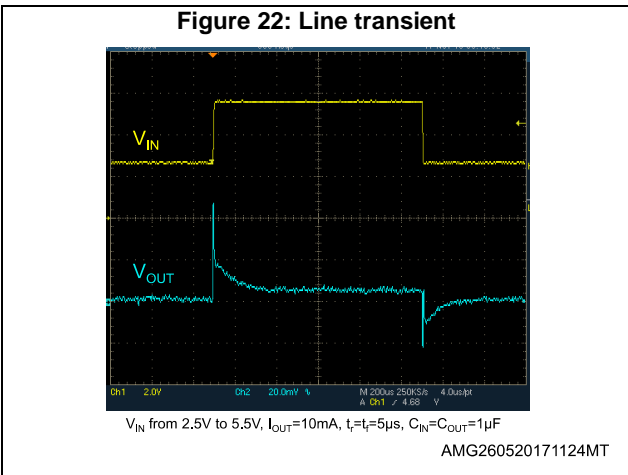
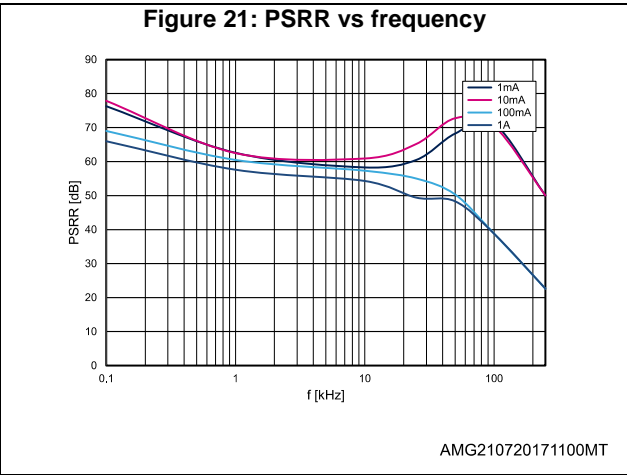
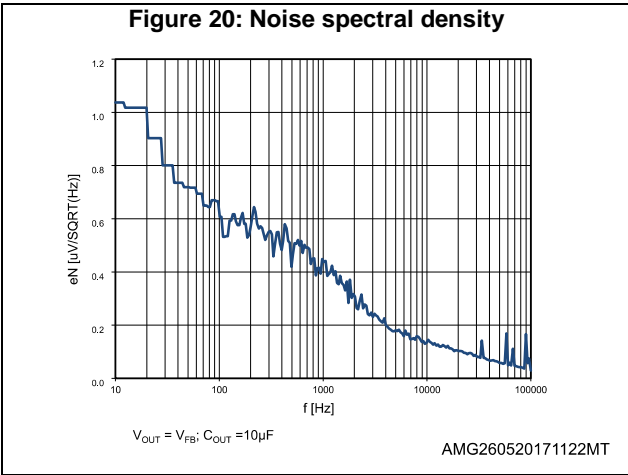


Figure 19: RMS noise vs CFB





8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

8.1 DFN8-3x3 package information

Figure 26: DFN8-3x3 package outline

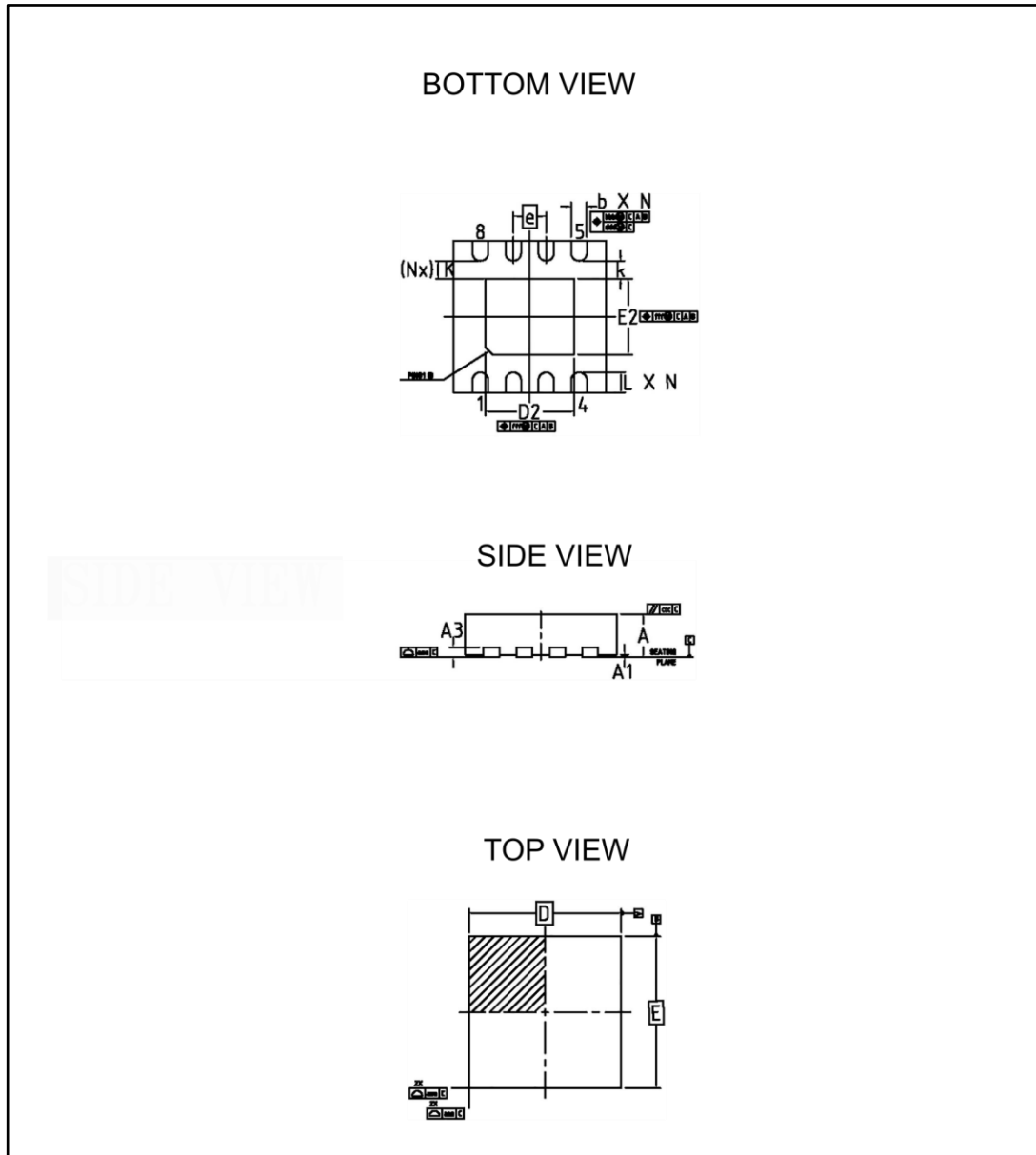
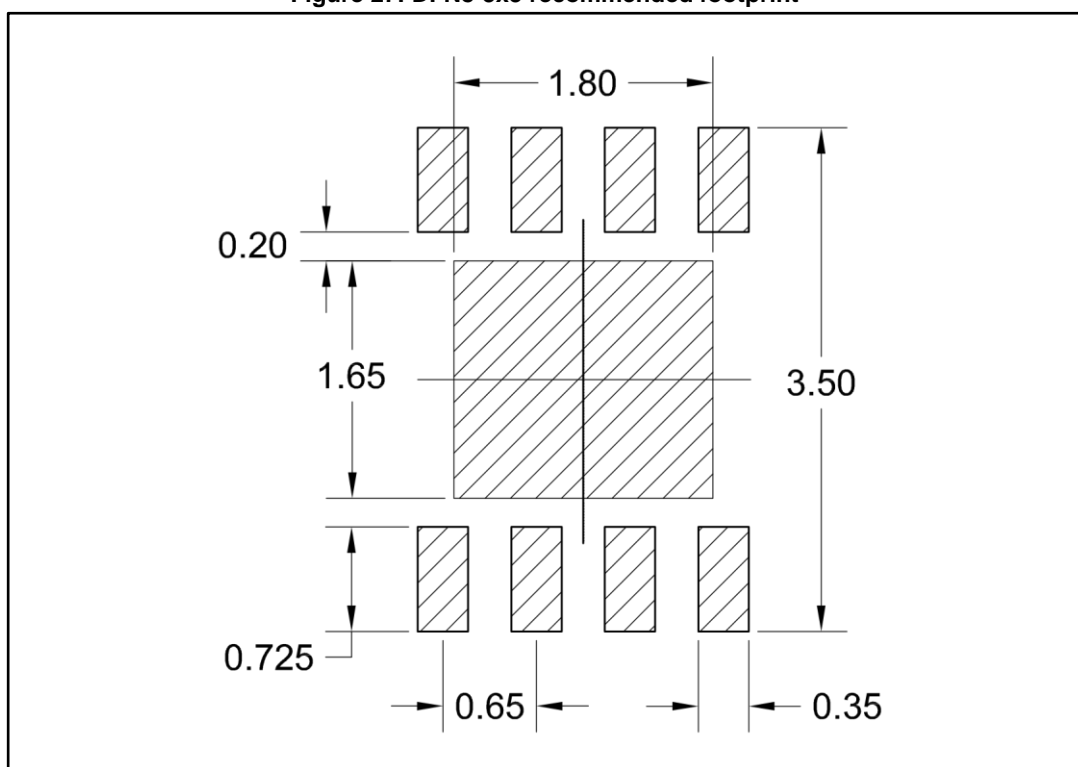


Table 7: DFN8-3x3 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1
A1	0.00	-	0.05
A3	0.20 REF.		
b	0.26	0.31	0.36
D	3.00 BSC		
D2	1.65	1.75	1.85
e	0.65 BSC		
E	3.00 BSC		
E2	1.40	1.50	1.60
L	0.30	0.40	0.50
k	0.20		
N	8		

Figure 27: DFN8-3x3 recommended footprint



8.2 DFN8-3x3 packing information

Figure 28: DFN8-3x3 tape outline

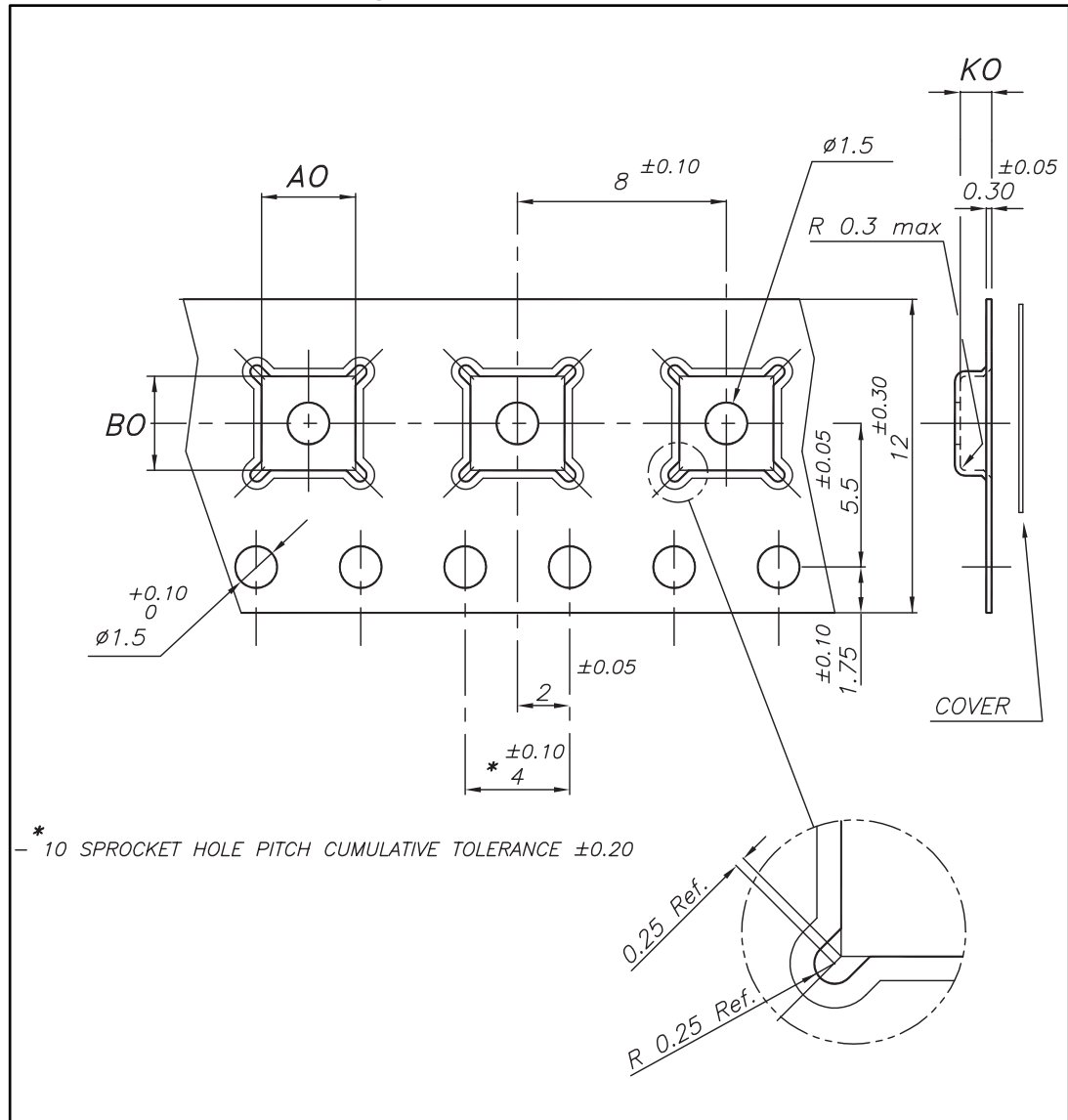
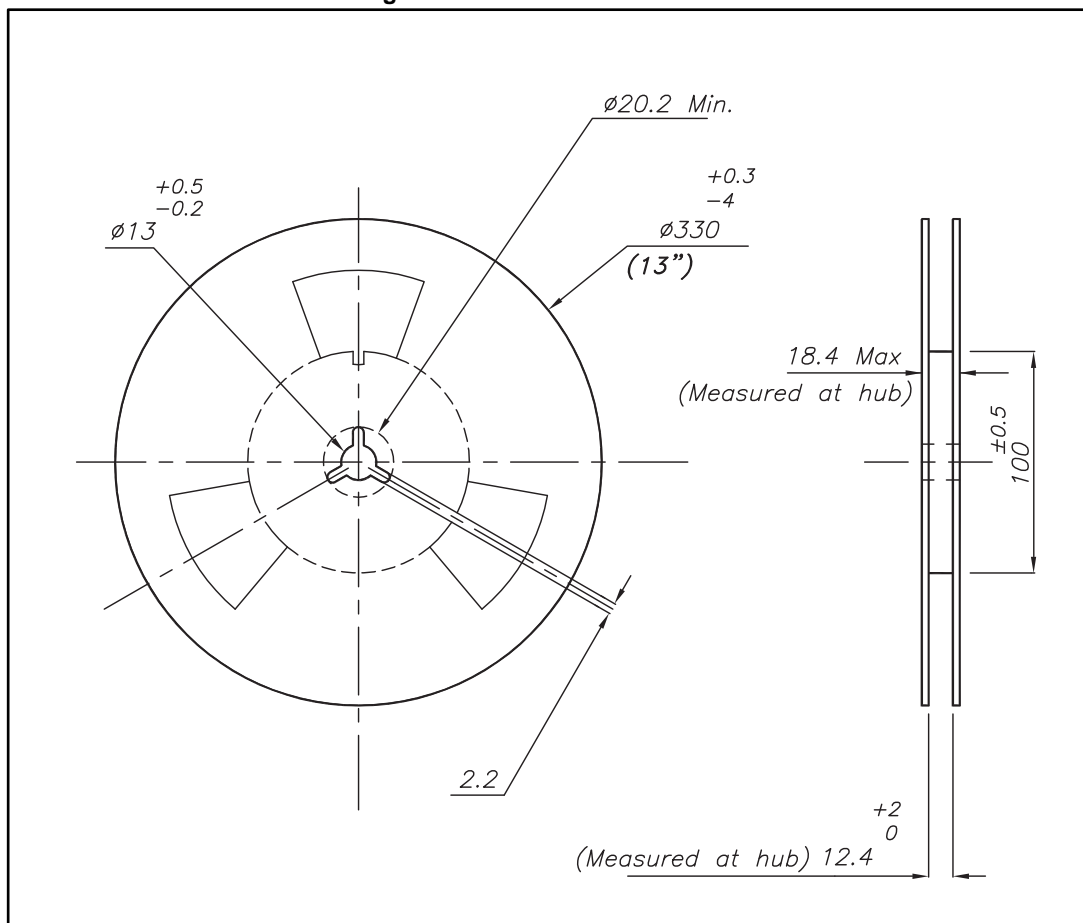


Table 8: DFN8-3x3 tape mechanical data

Dim.	mm
	Value
Ao	3.30 ± 0.10
Bo	3.30 ± 0.10
Ko	1.10 ± 0.10

Figure 29: DFN8-3x3 reel outline



9 Ordering information

Table 9: Order codes

DFN8-3x3		Output voltage
Order code	Marking	
LD59100PUR	5910	Adjustable

10 Revision history

Table 10: Document revision history

Date	Revision	Changes
06-Sep-2017	1	Initial release

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