Powering AMD Uni-Plane and Split-Plane Processors with the ISL6323

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Introduction

The ISL6323 supports hybrid power control of AMD processors which operate from either a 6-bit parallel VID interface (PVI) or a serial VID interface (SVI). The dual output ISL6323 features a multi-phase controller to support uniplane VDD core voltage and a single phase controller to power the Northbridge (VDDNB) in SVI mode. Only the multi-phase controller is active in PVI mode to support uniplane VDD only processors.

The ISL6323EVAL1Z evaluation board showcases the functionality of the ISL6323 in an easy to use platform that allows designers to fully evaluate all the features of the ISL6323 controller. The ISL6323EVAL1Z evaluation board is configurable for core regulation utilizing two to four channels in the multiphase Core regulator. A PC can be used to send PVI and SVI commands to the ISL6323. The response of the regulators, both the Core and the North Bridge, can be reviewed through the use of the on board load transient generators. The platform also allows for customization of the design in order to evaluate a solution that adheres to different regulator specifications.

The ISL6323 is packaged in an 48 Ld, 7mmx7mm QFN. The datasheet of the ISL6323 can be referred to for more detailed information[1].

Reference Design

The ISL6323EVAL1Z evaluation board regulates the Core voltage rail, V_{CORE}, when in Parallel VID Interface (PVI) Mode via a multiphase DC/DC regulator. In Serial VID Interface (SVI) mode, the ISL6323EVAL1Z evaluation board regulates the Core voltage rail, V_{CORE}, via the multiphase DC/DC regulator and the North Bridge voltage rail, V_{NB}, via a single phase DC/DC regulator. The Core and North Bridge regulators were designed to meet the following specifications:

TABLE 1. ELECTRICAL SPECIFICATIONS

	CORE	NB
I_{LOAD_MAX}	95A	20A
DC Tolerance	±50mV	±50mV
AC Tolerance	-140/+150mV	-140/+150mV
$I_{LOAD\_STEP\_MAX}$	70A	12A
$\left(\frac{dI_{LOAD}}{dt}\right)_{MAX}$	400A/µs	400A/µs
I_{OCP_TRIP}	130A	30A

In order to meet these specifications, the Core regulator was given a no load offset of 35mV. Droop was enabled and a load line of 0.75mΩ was applied to the Core regulator. This allowed for a reduction in output capacitance while still maintaining adherence to both the AC and DC specifications listed in Table 1.

The Schematic, Bill of Materials, and Board Layouts for the ISL6323EVAL1Z can be found on page 11 through page 16.

Quick Start Evaluation

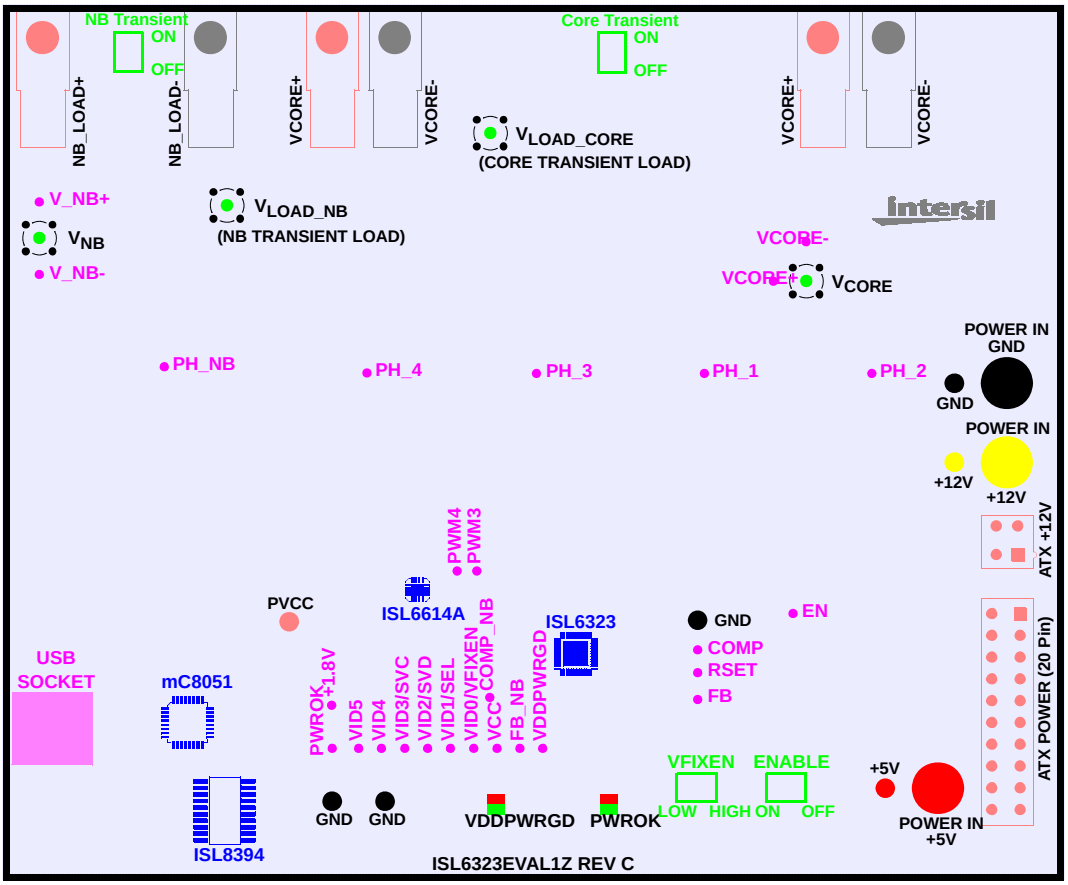
The ISL6323EVAL1Z board is shipped ‘ready to use’ right from the box. While there are ATX connectors available for supplying power to the board, it is recommended that laboratory power supplies be used. There are three labeled banana jacks available for connecting power supplies to the board. One is for +12V, one is for +5V and the third is the ground return for both. Both regulated outputs can be exercised through external loads or through the on-board transient load generators.

The ISL6323EVAL1Z evaluation board has four probe sockets available for monitoring of the Core and North Bridge outputs as well as the Core and North Bridge transient loads. There are also individually labeled probe points available for use. These probe points provide Kelvin connections to signals which may be of interest to the designer.

There are four switches on the board that have individual uses. There is a switch labeled EN, which when toggled to the ON position will allow regulation of the output rails. The VFIXEN switch is for use when the ISL6323 is in SVI mode (see datasheet for details). The last two switches are enable switches for the Core and North Bridge transient loads.

There are two LED indicators on the board. One shows the status of the VDDPWRGD signal. The other shows the status of the PWROK signal. For both LEDs, Red indicates a Low state while Green indicates a High state.

The Evaluation board also includes a USB port that allows for communication to a PC. This allows for a broader evaluation to be performed than could be done with the board on its own. Software and drivers specific for PC to board communication can be downloaded from the Intersil Website. See “Operation” on page 4 for more details.



KEY:

- = Scope Probe Socket
- = Test Point
- = Toggle Switch
- = Red/Green LED Indicator
- = Ground Post for Probe Return
- = Post for +5V Monitoring
- = Post for +12V Monitoring
- = Post to Monitor and/or Supply PVCC

FIGURE 1. LOCATIONS OF INPUTS,OUTPUTS, SWITCHES, PROBE AND MONITORING POINTS

Recommended Test Equipment

To test the full functionality of the ISL6323, the following equipment is recommended:

- A Laboratory Power supply capable of supplying +12V and at least 15A.
- A Laboratory Power supply capable of supplying +5V and at least 2A.
- One or more Electronic Loads (can be placed in parallel) capable of drawing up to 95A.
- 4-Channel oscilloscope with probes
- Precision digital multimeters
- A Personal Computer (PC) with ISL6323 control software and drivers. See “Operation” on page 4 for more details.

Circuit Set Up

Refer to Figure 1 for the locations of the switches, connectors, components and probe points.

SWITCH Settings

There are four switches on the board. The Switch labeled ENABLE is used to enable and disable regulation of the output rails. The switch labeled VFIXEN is used to emulate the presence of a processor. The two switches labeled CORE_TRANSIENT and NB_TRANSIENT are used to turn on/off the on board load transient generators. Table 2 shows the functions of each switch.

TABLE 2. SWITCH SETTINGS AND DESCRIPTIONS

SWITCH		FUNCTION
ENABLE	ON	With all POR conditions of the ISL6323 satisfied, this will allow regulation of the output rail(s)
	OFF*	Disables regulation of the output rails.
VFIXEN	Low*	Only applicable to SVI mode. Emulates a processor in place. Normal Metal VID and SVI codes are recognized.
	High	Only applicable in SVI mode. Emulates lack of a processor. SVI codes are not recognized.
CORE_TRANSIENT	ON	Transient Load Generator for Core Regulator Enabled
	OFF*	Transient Load Generator for Core Regulator Disabled
NB_TRANSIENT	ON	Transient Load Generator for North Bridge Regulator Enabled
	OFF*	Transient Load Generator for North Bridge Regulator Disabled

*Denotes default configuration

Connecting Loads

LOADING THE CORE REGULATOR

There are two sets of lugs at the top of the board that can be used to attach an external load to the Core Regulator. There are two load lugs (labeled VCORE+) and two load return lugs (labeled VCORE-). The Core Regulator is capable of supporting 95A of continuous current. This level of load can be realized by placing a number of loads in parallel and using short low gauge wire to connect the loads to the lugs. An attempt at an even distribution of the load current between the two sets of lugs should be sought.

LOADING THE NORTH BRIDGE REGULATOR

The North Bridge regulator has a single set of lugs (labeled NB_LOAD+ and NB_LOAD-) that are used to attach an external load. The North Bridge regulator was designed to support up to 30A of continuous current. A short connection between the external load and the lugs using low gauge wire is recommended.

Connecting Probes

Table 3 lists all the locations available for monitoring. The scope probe test points provide a low impedance ground connection and all GND posts can be utilized as a ground connection for probes.

TABLE 3. PROBE TYPES AND LOCATIONS

TYPE	VOLTAGE	REF DES
POST	+5V	TP7
	+12V	TP8
	PVCC	TP6
	GND	TP1, TP9, TP19, TP20
TEST POINT	VDDPWRGD	TP18
	PWROK	TP17
	VCC	TP2
	EN	TP3
	VID0/VFIXEN	TP11
	VID1/SEL	TP12
	VID2/SVD	TP13
	VID3/SVC	TP14
	VID4	TP15
	VID5	TP16
	+1.8V	TP10
	FB	TP100
	COMP	TP101
	RSET	TP102
	VCORE+	TP109
	VCORE-	TP110
	PH1	TP103
	PH2	TP104
	PH3	TP105
	PH4	TP106
	FB_NB	TP200
	COMP_NB	TP201
	V_NB+	P6
	V_NB-	P7
	PH_NB	TP202
SCOPE PROBE SOCKET	V_CORE	SP101
	CORE_LOAD	SP2
	V_NB	SP201
	NB_LOAD	SP1

NOTE: The ISL6323 utilizes remote sensing for accurate regulation of the Core and North Bridge output rails. It is important to note that the scope probe return contact of the Core regulator probe socket and the VCORE- probe point are tied to the remote ground return for the Core regulator. Also, the scope probe return contact of the North Bridge regulator probe socket and the V_NB- probe point are tied to the remote ground return for the North Bridge regulator.

These points are not tied to the ground plane and care should be taken to avoid creating a ground loop through an oscilloscope by connecting probe returns to the ground plane and any of the remote ground returns simultaneously. If probing the Core regulator, then all scope probe returns should either be tied to the ground plane through the GND posts or they should all be tied to the remote ground return for the core regulator. It is important that the probe return connections not be mixed. Similar care should also be taken when probing the North Bridge regulator output.

USB CONNECTION

Connect a USB cable to the evaluation board and then to the PC being used. Open the communication software. This step should be completed prior to applying power to the board.

NOTE: This section assumes that the Intersil PC/Eval Board USB software has already been installed on the computer being used. If it has not, refer to the section titled “PC to EVAL Board USB Communication” on page 21 for details on installing and using this software.

CONNECTING POWER

Prior to connecting the power supplies to the evaluation board, the power supplies should either be turned off or the outputs should be disabled. While an ATX power supply can be used to apply power to the board by utilizing both the 20 pin connector and the four pin 12V connector, laboratory power supplies are recommended as they allow for more flexibility and monitoring capabilities.

A +12V and +5V supply should be used to power the board. Three banana jacks are available for bringing power to the evaluation board. Connect the power supply return lines to the black banana jack labeled GND (reference designator P5). Connect the +12V power supply lead to the red banana jack labeled +12V (reference designator P4). Connect the +5V power supply lead to the red banana jack labeled +5V (reference designator P3).

Operation

This section presents the performance of the ISL6323EVAL1Z evaluation board while subjected to various conditions.

START-UP

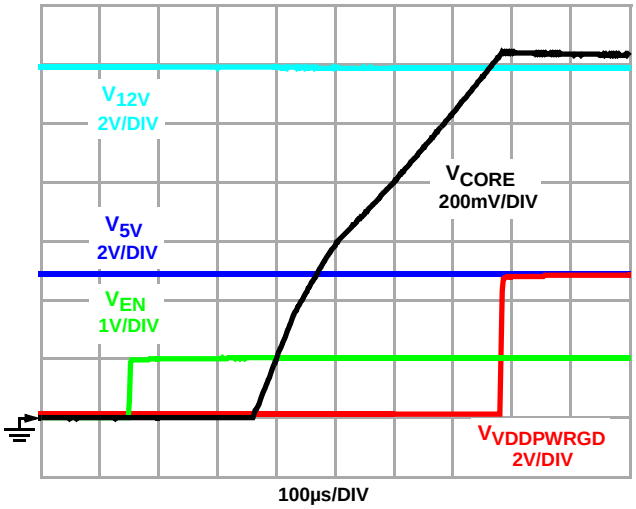


FIGURE 2. PVI MODE - START-UP VIA ENABLE

Figure 2 shows the start-up of the ISL6323 when in Parallel VID (PVI) mode. This shows the Core output ramping up to the prescribed VID code after all POR conditions have been met and the voltage on the ENABLE pin exceeds its rising threshold. Once the Core regulator is at the nominal VID level, the VDDPWRGD signal will go high.

In Serial VID (SVI) mode (see Figure 3), both the Core regulator and the North Bridge regulator will ramp-up to the same Metal VID level once all POR levels have been satisfied and the voltage on the ENABLE pin has exceeded the rising threshold. Once both the Core and North Bridge outputs are at the nominal Metal VID level, the VDDPWRGD signal will go high. The ISL6323 will only recognize SVI commands once the PWROK input has been set to high by the system.

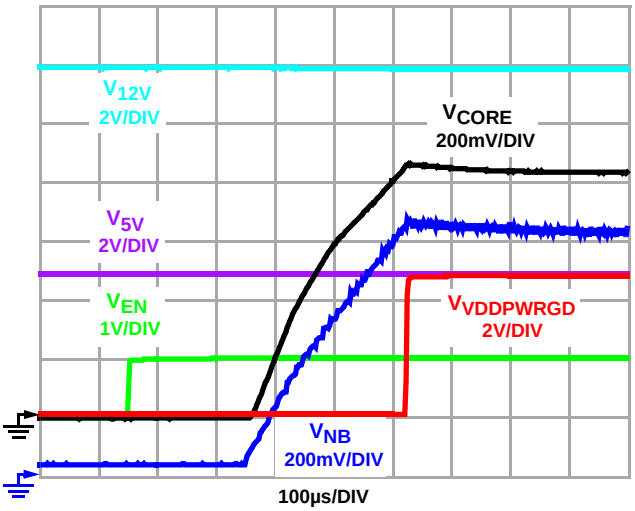


FIGURE 3. SVI MODE - START-UP VIA ENABLE - 0.800V METAL VID

STEADY STATE

Figure 4 shows the ripple on the output of the Core regulator. This also shows the phasing of the channels with all four of the channels being active. The ripple voltage is less than $10mV_{P-P}$.

Figure 5 shows the ripple voltage on the output of the North Bridge regulator. Here the ripple is somewhat larger than the core since the North Bridge regulator is a single phase regulator. The ripple voltage is approximately $20mV_{P-P}$.

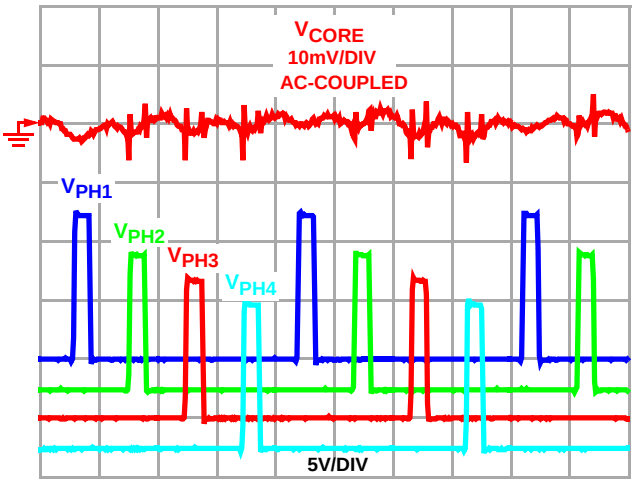


FIGURE 4. CORE REGULATOR - STEADY STATE

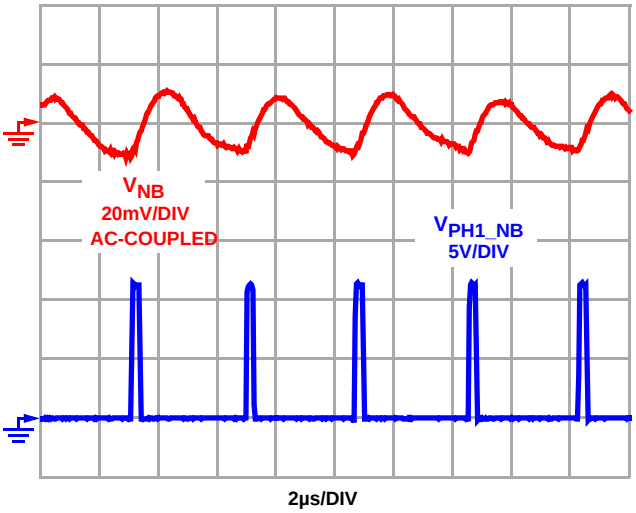


FIGURE 5. NORTH BRIDGE REGULATOR - STEADY STATE

SVI VID TRANSITIONS

Once the PWROK signal has gone high, the ISL6323 will accept and respond to SVI commands. The only SVI commands that the ISL6323 recognizes are VID change commands. When changing from one VID level to another, the ISL6323 maintains a nominal 3mV/µs slew rate on the rail that is being modified. Figure 6 shows the SVI commands that are received on the SVC and SVD pins and the corresponding VID transition on the Core rail from a VID level of 0.8V to 1.2V. Figure 7 shows the reverse SVI Core VID transition from 1.2V to 0.8V. The North Bridge regulator is controlled in the same manner as the Core regulator. Figure 8 shows the SVI commands and the corresponding VID voltage transition from 0.8V to 1.2V. Figure 9 shows the reverse SVI VID transition on the North Bridge regulator.

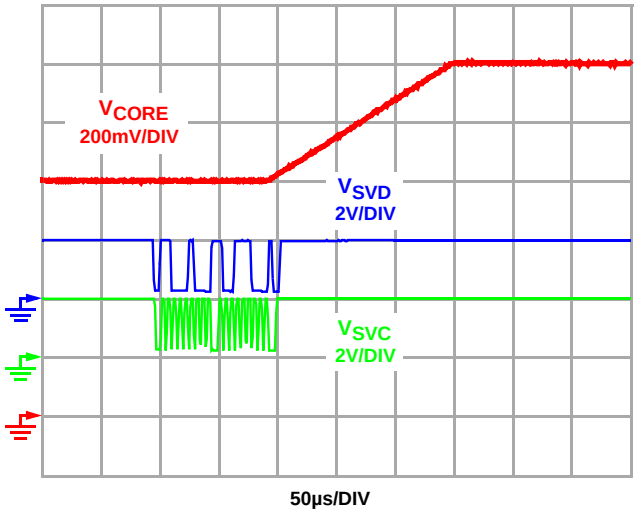


FIGURE 6. CORE SVID TRANSITION: 0.8V TO 1.2V

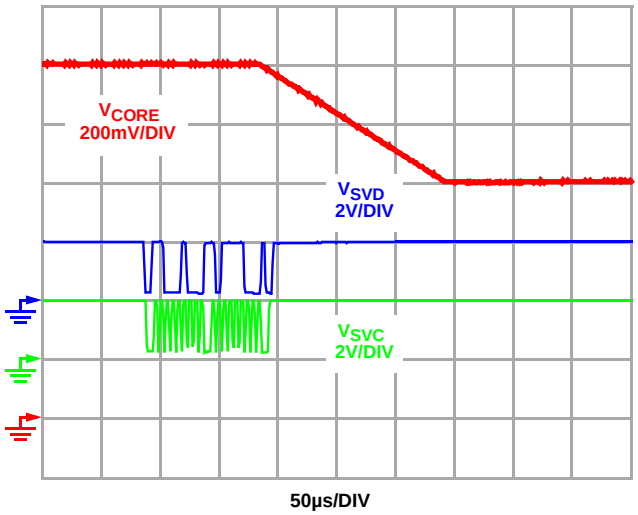


FIGURE 7. CORE SVID TRANSITION: 1.2V TO 0.8V

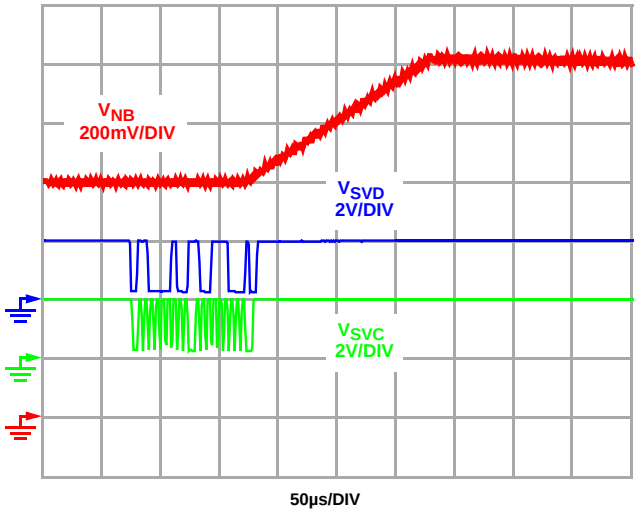


FIGURE 8. NORTH BRIDGE SVID TRANSITION: 0.8V to 1.2V

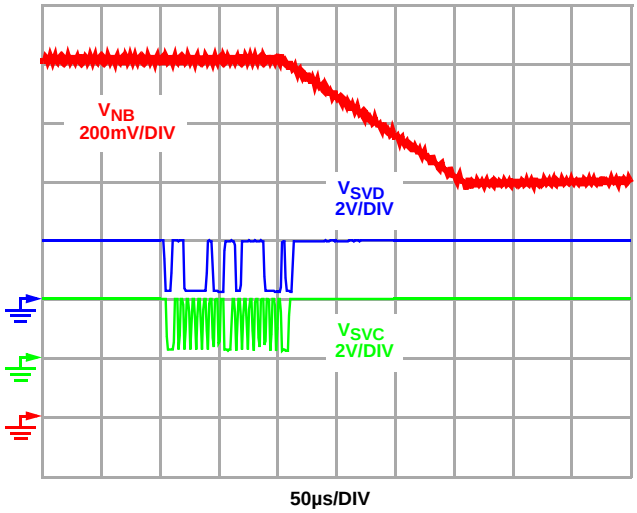


FIGURE 9. NORTH BRIDGE SVID TRANSITION: 1.2V TO 0.8V

RETURN TO METAL-VID IN SVI MODE

If the PWROK signal goes low, the ISL6323 will immediately ramp both the Core output level and the North Bridge output level to the Metal-VID level. If, at the onset of this transition, the VID level of either the Core regulator or the North Bridge regulator is at a level far enough away from the Metal-VID such that the output voltage is outside of the VDDPWRGD window, then the VDDPWRGD signal will go low until the output has ramped to within the VDDPWRGD window that is centered around the Metal-VID level. Figure 10 shows such a transition when the PWROK signal is forced low. At the time that the PWROK signal goes low, the VID has changed to the Metal-VID level of 1.1V. Since the 0.6V level, which the Core regulator was at, is well out of the VDDPWRGD window for a 1.1V level, the VDDPWRGD signal is forced low until the output has ramped to a level that allows the VDDPWRGD signal to transition high again.

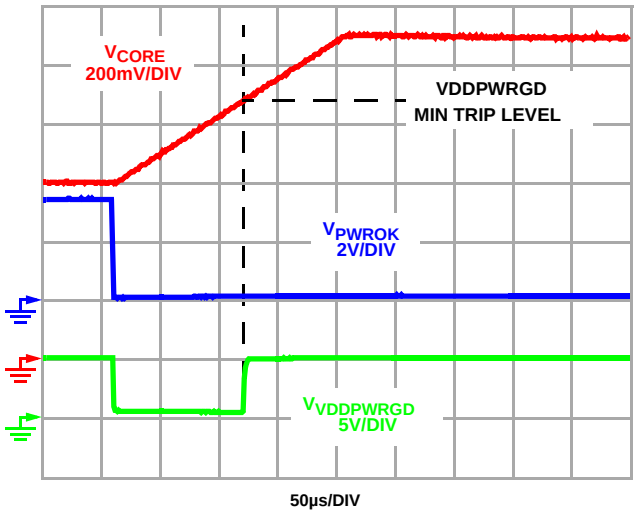


FIGURE 10. CORE VID @ 0.6V; METALVID @ 1.1V

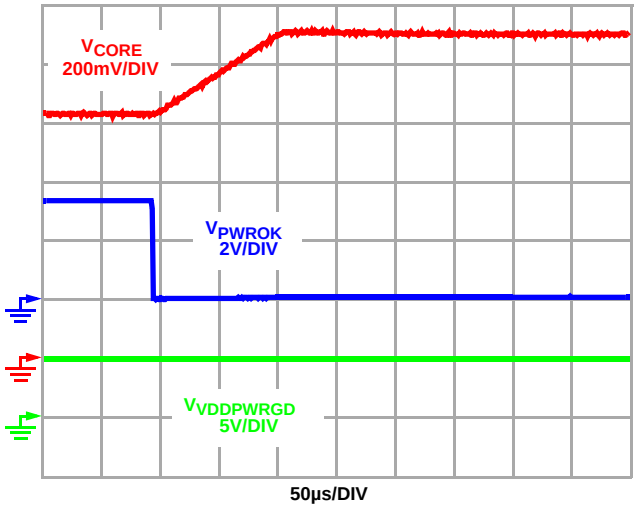


FIGURE 11. CORE VID @ 0.825V; METALVID @ 1.100V

Figure 11 illustrates a transition from a VID level to a Metal-VID level that does not force the VDDPWRGD signal low.

TRANSIENT RESPONSE

The Core and North Bridge regulators on the ISL6323EVAL1Z evaluation board were tuned to yield a quick and stable response to large load transients. Figures 12 and 13 show the response of the Core regulator to a 70A, 400µs load application and release, respectively, with the VID set to 1.2V. During the load application, the output voltage remains well within the -140mV AC limit while only being out of the -50mV DC limit for only a few microseconds.

During the load release, the Core output stays well within the +150mV maximum AC limit while only exceeding the +50mV DC limit for approximately 6µs.

The response of the North Bridge regulator to a load application and release is shown in Figures 14 and 15. The response to the load application is very quick, does not exceed the -140mV AC limit and only exceeds the -50mV

DC limit for a few microseconds. The load release response does not exceed the +150mV AC limit. The output remains above the +50mV DC limit for approximately 17µs. This response is a trade off between response time and number of output capacitors. A larger output capacitor bank on the North Bridge regulator would decrease the excursion above the +50mV window. More bulk capacitance, however, costs more and requires more board space to accommodate.

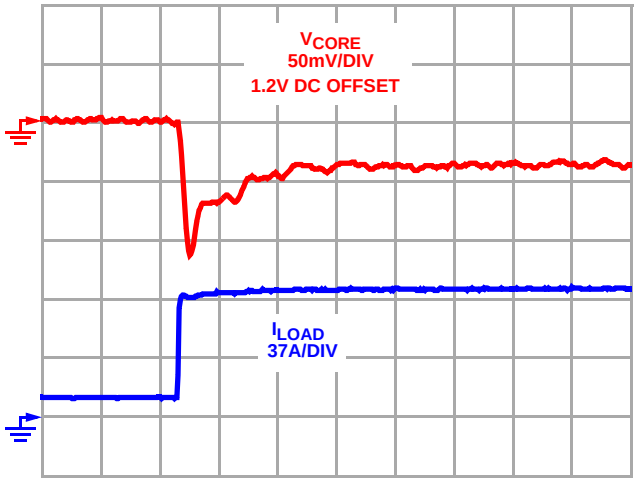


FIGURE 12. CORE LOAD TRANSIENT: 10A DC AND 70A LOAD APPLY (400A/µs)

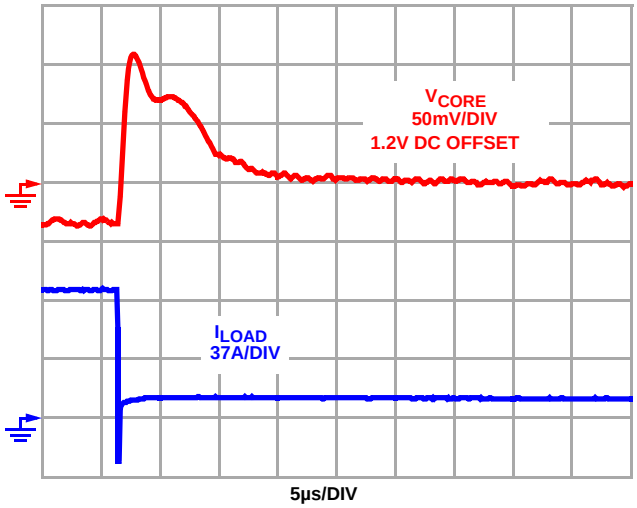


FIGURE 13. CORE LOAD TRANSIENT: 10A DC AND 70A LOAD RELEASE (400A/µs)

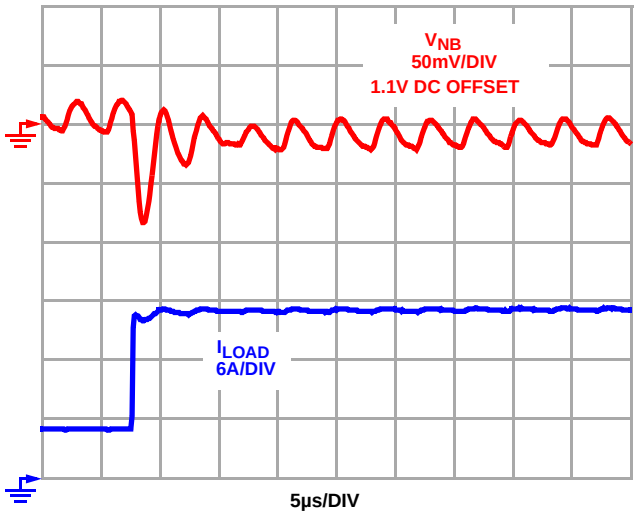


FIGURE 14. CORE LOAD TRANSIENT: 5A DC AND 12A LOAD APPLY (400A/µs)

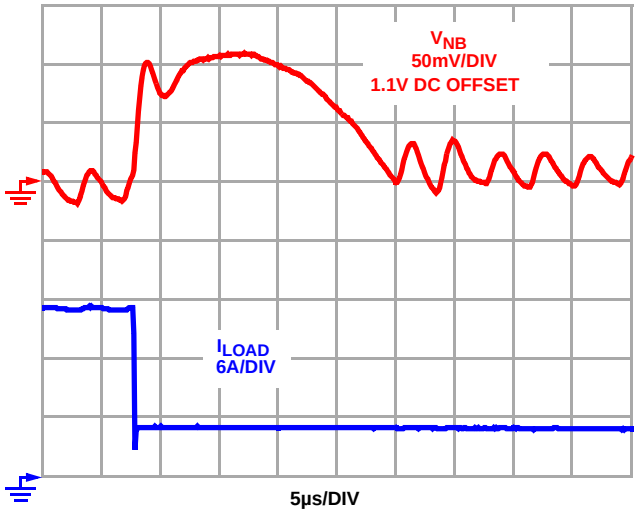


FIGURE 15. CORE LOAD TRANSIENT: 5A DC AND 12A LOAD RELEASE (400A/µs)

CONTROLLED SHUTDOWN

Figure 17 shows how the ISL6323 walks the output rails down when disabled via the ENABLE pin.

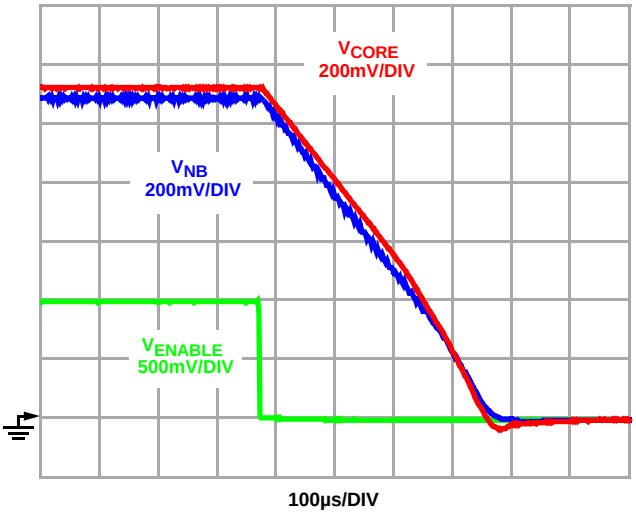


FIGURE 16. SHUTDOWN VIA ENABLE

EFFICIENCY

Figure 17 shows the efficiency of the 4-Channel Core regulator. Figure 18 shows the efficiency of the North Bridge regulator. Both sets of efficiencies were measured with the regulator at a “Cold” temperature (+25°C) and with the regulator at a “Hot” temperature. The “Hot” efficiency curve data was collected by allowing the regulator to sit at the recorded load level for five minutes prior to taking the efficiency data. The ambient temperature was at +25°C with no airflow.

The Core regulator remains well over 80% throughout the usable load range. The North Bridge regulator remains above 84% throughout the usable load range.

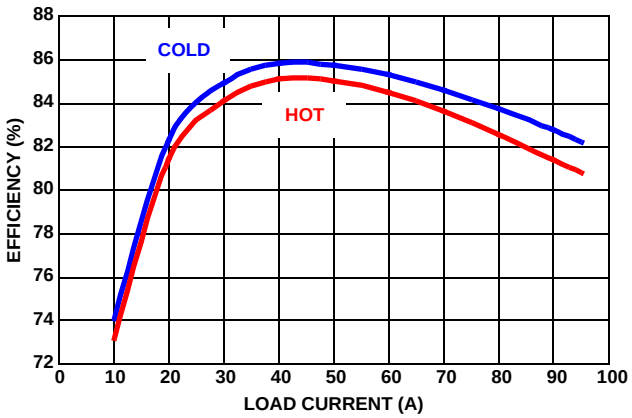


FIGURE 17. CORE REGULATOR EFFICIENCY

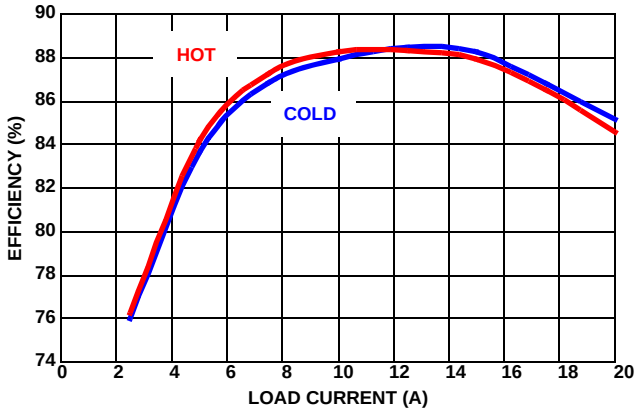


FIGURE 18. NORTH BRIDGE REGULATOR EFFICIENCY

Board Layout Considerations

The ISL6323EVAL1Z evaluation board was designed to demonstrate layout techniques and practices that are recommended by Intersil. These recommendations should provide a regulator that has robust performance and minimal noise injection.

The evaluation board uses four layers of 2oz copper. The top layer is used for placement of all components and for routing signal traces and some power traces and copper fills. The second layer is a dedicated ground plane. This allows for all component ground connections to use very short traces to ground plane connected vias which reduces parasitics. This also places a ground plane directly under the ISL6323 IC that shields the IC from radiated noise. The third layer consists of power only. Large areas of copper dedicated to input power, output power and phase nodes reduce impedances in these paths. The bottom layer is used for signal traces and some power traces and copper fills.

The ISL6323 IC is packaged in a 48 Ld QFN package that has a large pad in the center that must be tied to ground. The accepting foot print should have at least four to five ground connected vias dispersed evenly. The ISL6323EVAL1Z evaluation board uses nine vias on the ground pad.

All small signal components should be located as close as possible to the ISL6323 IC. This includes the RC filter components tied across the inductors for current sensing.

The high frequency decoupling capacitors on the input rail should be located as close to the drains of the upper MOSFETs as possible. The ground pads of these capacitors should tie to the ground plane through short traces tied to ground plane connected vias.

All MOSFET gate traces, for both the upper and lower MOSFETs, should have a minimum width of 0.020 inches (20 mils). Two vias should be used for all layer transitions. This will allow for large peak currents with low parasitics.

The traces that tie both sides of the inductor to the low pass RC filters for current sensing should be routed very carefully. These traces should be treated as kelvin sense traces. The trace widths can be thin, 0.004 (4 mils). There are a number of ways that these traces may be tied to the inductor pads.

The initial length of the traces may be placed on the top layer with the traces emanating from the center of the inductor pads and tracking toward one another to the geometric center of the inductor. From that point the traces should be routed directly next to each other until they reach the low pass filter components. If a layer change is required, then both traces must switch to the same layer and continue to track next to each other. An alternative method is to place a via in the geometric center of each inductor pad. These vias are tied only to the inductor pad and to the sense trace on a separate layer. Again, the sense traces should route toward the geometric center of the inductor and they should then track each other until they reach the low pass filter components. Care should be taken so that the traces are not routed so that they overlap any noisy nodes, such as the phase nodes. Refer to Figure 19 for a graphical representation.

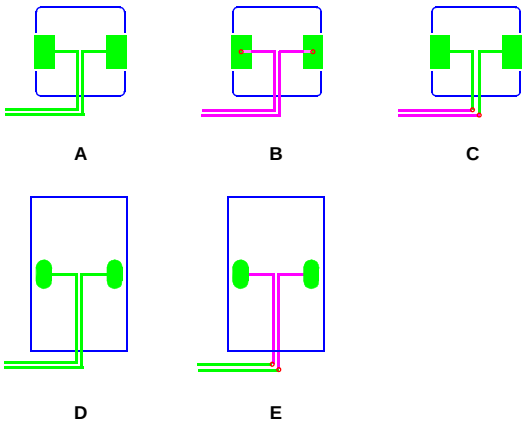


FIGURE 19. INDUCTOR CURRENT SENSING TRACES

The current sense traces shown in Example A in Figure 19 show how the traces emanate from the pads of a surface mount inductor to the geometric center of the inductor and then track each other until they reach the filter components. Example B shows how vias can be used to connect the inductor pads to the sense traces. It is important to note that the vias are electrically connected only to the inductor pads and to the sense traces. Example C illustrates how the sense traces must stay on the same layer. In Example C, the traces begin on the top layer, but then dive into a lower layer through vias. Examples D and E show how the sense traces can be tied to a through hole inductor. Example D shows a connection to the inductor pads on the top layer. Example E shows the connection to the inductor leads through a connection with the plated through hole on a lower layer.

ISL6323EVAL1Z Customizing

There are numerous ways in which a designer might modify the ISL6323EVAL1Z evaluation board for differing requirements. Some of the changes which are possible include:

- The output inductors: L101, L102, L103, L104 and/or L202. Changing the inductors will likely require the retuning of the RC filters for current sensing. Refer to the datasheet for complete details.
- The input and output capacitance for either of the regulators.
- The Overcurrent Trip point. Refer to the datasheet for details on modification of the OCP trip point.
- The number of active phases for the Core regulator. Installing a 0Ω jumper at R116 will disable Channel 4 for a 3-phase regulator. Installing 0Ω jumpers at R116 and R117 will disable both Channels 3 and 4 for a 2-phase regulator.
- The PVCC voltage (gate drive) can be 5V, 12V or any voltage in between. Refer to Table 4

TABLE 4. PVCC VOLTAGE

DESIRED PVCC	R15	R16	COMMENT
12V	0Ω	DNP	Gate drive derived from +12V
5V	DNP	0Ω	Gate drive derived from +5V
5V to 12V range	DNP	DNP	Connect external PVCC to TP6

- The number of upper and/or lower MOSFETs
- Switching frequency (R2/R2B set the switching frequency)
- Output Droop Enabling/Disabling and Load Line control
- Positive (R107) or Negative (R106) offset voltage.

Conclusion

The ISL6323EVAL1Z is a versatile platform that allows designers to gain a full understanding of the functionality of the ISL6323 when powering AMD uni-plane or split plane processors. The board is also flexible enough to allow the designer to modify the board for differing requirements.

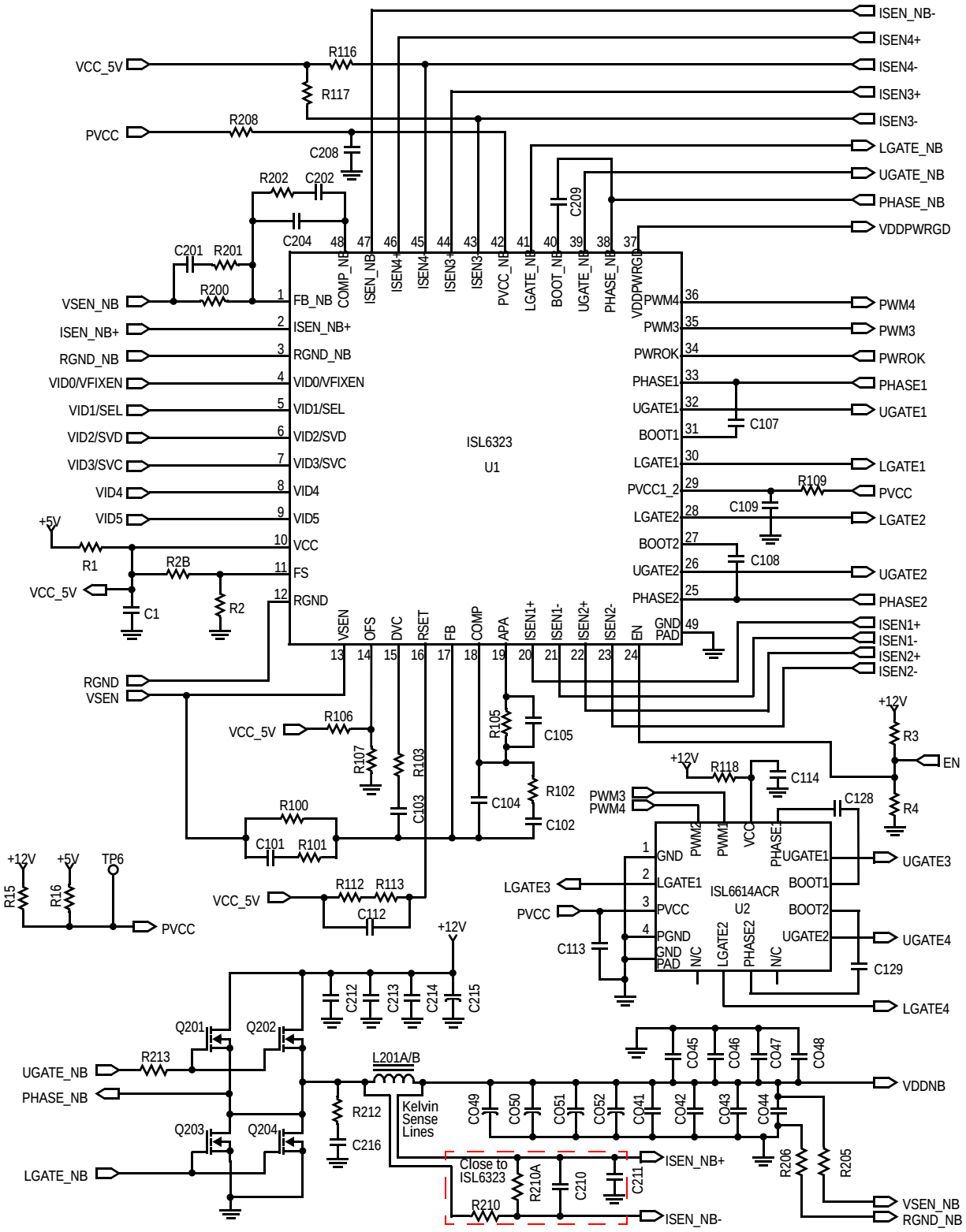
References

For Intersil documents available on the web, see http://www.intersil.com/

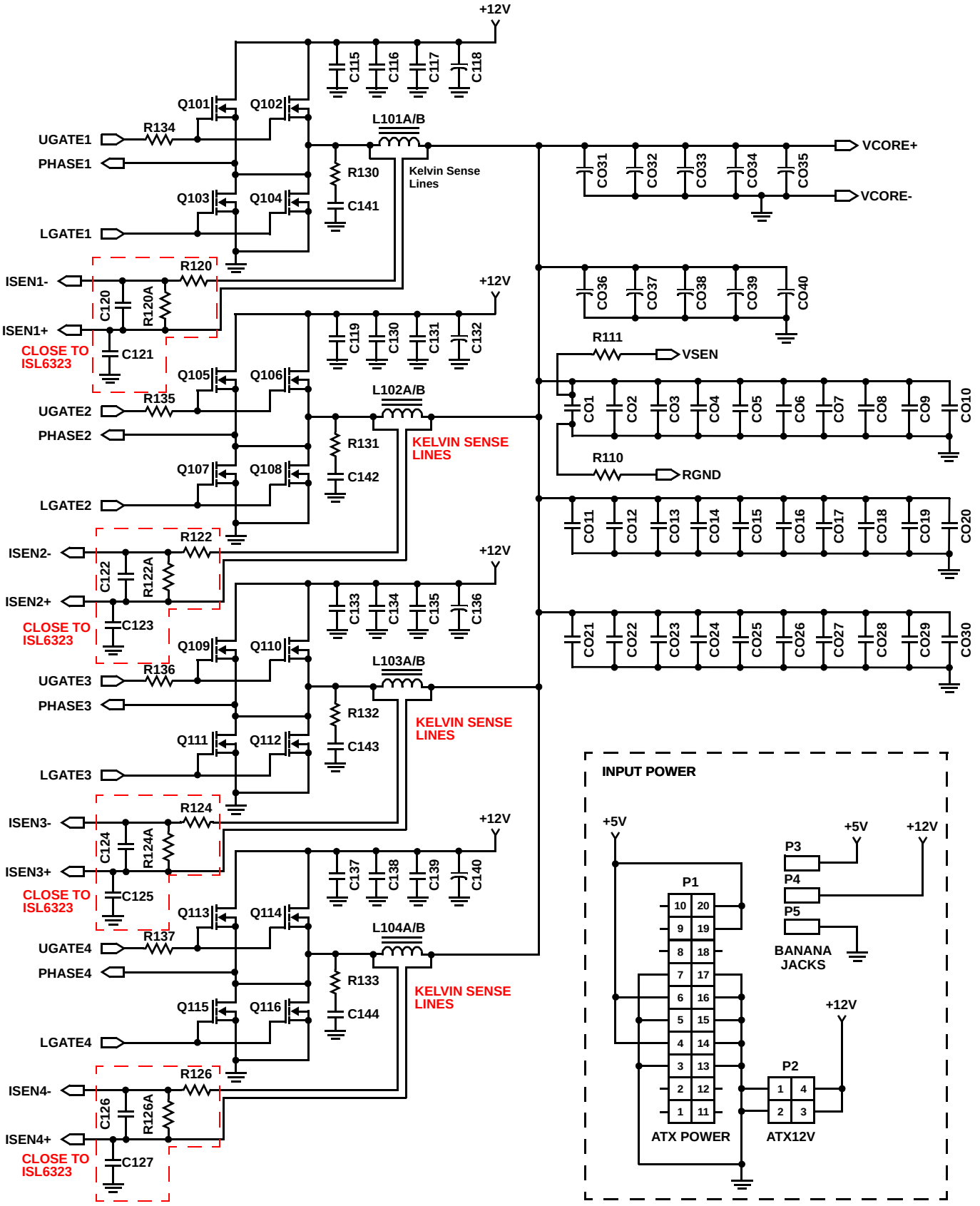
[1] *ISL6323 Data Sheet,* Intersil Corporation, File No. FN9278.

http://www.intersil.com/data/fn/fn9278.pdf

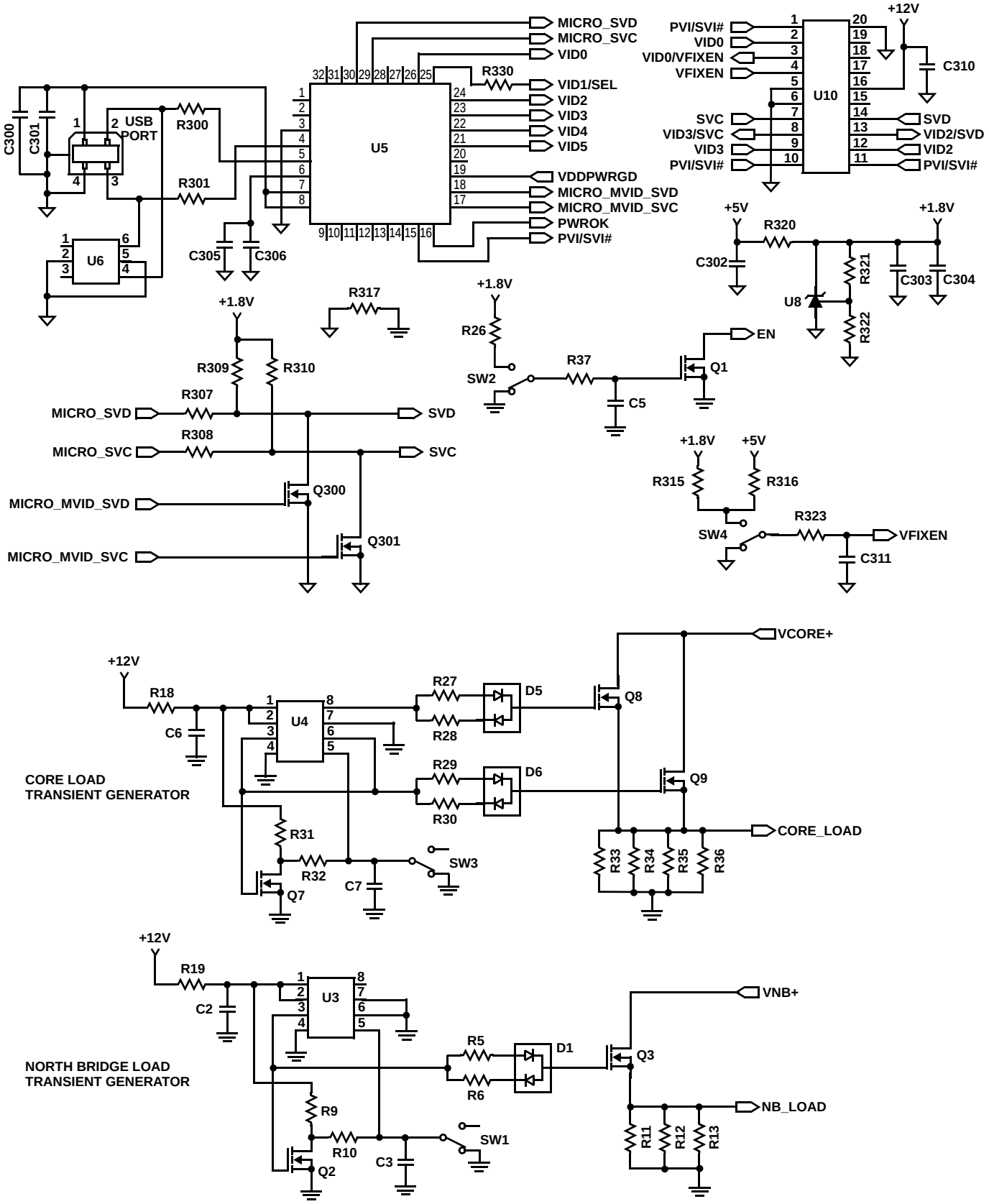
ISL6323EVAL1Z Schematic



ISL6323EVAL1Z Schematic (Continued)



ISL6323EVAL1Z Schematic (Continued)



ISL6323EVAL1Z Bill of Material

REF DES	DESCRIPTION	PKG	VENDOR	VENDOR P/N	QTY
C1, 109, 208	1µF, X7R Capacitor	0805	Various	-	3
C5	1000pF, X7R Capacitor	0603	Various	-	1
C101	100nF, X7R Capacitor	0603	Various	-	1
C102	33nF, X7R Capacitor	0603	Various	-	1
C103	27nF, X7R Capacitor	0603	Various	-	1
C104,204	100pF, X7R Capacitor	0603	Various	-	2
C105, 112, 120-127, 210, 211, 300, 306, 310	0.1µF, X7R Capacitor	0603	Various	-	15
C107, 108, 128, 129, 209	0.22µF, X7R Capacitor	0603	Various	-	5
C113, 114, 301, 305, 311	1µF, X7R Capacitor	0603	Various	-	5
C201, 202	47nF, X7R Capacitor	0603	Various	-	2
C302-304	Do Not Populate	0603	-	-	-
C2, 6	1µF, X7R Capacitor	1206	Various	-	2
C3, 7	22µF, X7R Capacitor	1206	Various	-	2
C115, 119, 133, 137, 212	0.1µF, X7R Capacitor	1206	Various	-	5
C116, 117, 130, 131, 134, 135, 138, 139, 213, 214	4.7µF, X5R Capacitor	1206	Various	-	10
CO1-CO30, CO41-CO48	10µF, X5R Capacitor	1206	Various	-	38
C141-144, 216	Do Not Populate	1206	-	-	-
C118, 132, 136, 140, 215	10µF Aluminum Electrolytic Capacitor, 16V	-	Rubycon	16MCZ1800M10x25	5
CO35-37, CO51	820µF Polymer Capacitor, 2.5V	-	Fujitsu	FP-2R5RE821M-L8	4
CO31-34, 38-40, 49, 50, 52	Do Not Populate	-	-	-	-
R1, 118	2.00Ω, 1% Resistor	0603	Various	-	2
R2	100kΩ, 1% Resistor	0603	Various	-	1
R3	10.7kΩ, 1% Resistor	0603	Various	-	1
R4, 302, 309, 310	1.00kΩ, 1% Resistor	0603	Various	-	4
R9, 31	46.4kΩ, 1% Resistor	0603	Various	-	2
R10, 32	402Ω, 1% Resistor	0603	Various	-	2
R37, 321, 323	10.0kΩ, 1% Resistor	0603	Various	-	3
R100	909Ω, 1% Resistor	0603	Various	-	1
R101	100Ω, 1% Resistor	0603	Various	-	1
R102, 103	499Ω, 1% Resistor	0603	Various	-	2
R105	4.99kΩ, 1% Resistor	0603	Various	-	1
R107	7.50kΩ, 1% Resistor	0603	Various	-	1
R112	30.1kΩ, 1% Resistor	0603	Various	-	1
R113	301Ω, 1% Resistor	0603	Various	-	1
R120, 122, 124, 126	10.0kΩ, 1% Resistor	0603	Various	-	4
R200	357Ω, 1% Resistor	0603	Various	-	1
R201	200Ω, 1% Resistor	0603	Various	-	1

ISL6323EVAL1Z Bill of Material (Continued)

REF DES	DESCRIPTION	PKG	VENDOR	VENDOR P/N	QTY
R202	3.74kΩ, 1% Resistor	0603	Various	-	1
R210	64.9kΩ, 1% Resistor	0603	Various	-	1
R210A	226kΩ, 1% Resistor	0603	Various	-	1
R320	267Ω, 1% Resistor	0603	Various	-	1
R322	4.53kΩ, 1% Resistor	0603	Various	-	1
R5, 6, 26, 27, 28, 29, 30, 109, 110, 111, 205, 206, 208, 300, 301, 307, 308, 315, 317, 330	0Ω Jumper	0603	Various	-	20
R2B, 106, 116, 117, 120A, 122A, 124A, 126A, 316	Do Not Populate	0603	-	-	-
R134-137	2.21Ω, 1% Resistor	0805	Various	-	4
R213	0Ω Jumper	0805	Various	-	1
R15,18,19	0Ω Jumper	1206	Various	-	3
R16, 130-133, 212	Do Not Populate	1206	-	-	-
R12	100mΩ Power Resistor	2512	Various	-	1
R13, 33, 34	500mΩ Power Resistor	2512	Various	-	3
R35	20mΩ Power Resistor	2512	Various	-	1
R36	50mΩ Power Resistor	2512	Various	-	1
R11	Do Not Populate	2512	-	-	-
D1,5,6	Dual Diode	SOT-23	Various	BAV99	3
Q102, 106, 110, 114, 202	Control MOSFET	TO-252AA	IR	IRL7821	5
Q103, 104, 107, 108, 111, 112, 115, 116, 203, 204	Synchronous MOSFET	TO-252AA	IR	IRL7833	10
Q101, 105, 109, 113, 201	Do Not Populate	TO-252AA	-	-	-
Q1, 2, 5-7, 300, 301	General Purpose MOSFET	SOT-23	Various	2N7002	7
Q3, 8, 9	MOSFET	TO-252AA	Vishay	SUD50N03-07	3
L101, 102, 103, 104	0.38µH, 0.85mΩ Inductor T68-8A/90 Core, 4 Turns Bifilar 16 AWG	-	Various	-	4
L201	0.90µH, 1.3mΩ Inductor T68-8A/90 Core, 6Turns Bifilar 16 AWG	-	Various	-	1
U1	Multiphase PWM Controller	48 Ld QFN	Intersil	ISL6323CR	1
U2	Two Channel MOSFET Driver	14 Ld SOIC	Intersil	ISL6614ACR	1
U3,4	Half Bridge Driver	8 Ld SOIC	Intersil	HIP2100CB	1
U10	Quad SPDT Analog Switch	20 Ld SOIC	Intersil	ISL8394IB	1
U5	Programmed 8051 Microcontroller w/USB	32 Ld LQFP	-	-	1
U6	USB Port Transient Suppressor	SOT23(DBV)	TI	SN65220DBV	1
U8	Shunt Regulator	SOT23	National	LM4041CIM3-ADJ	1

ISL6323EVAL1Z Layout

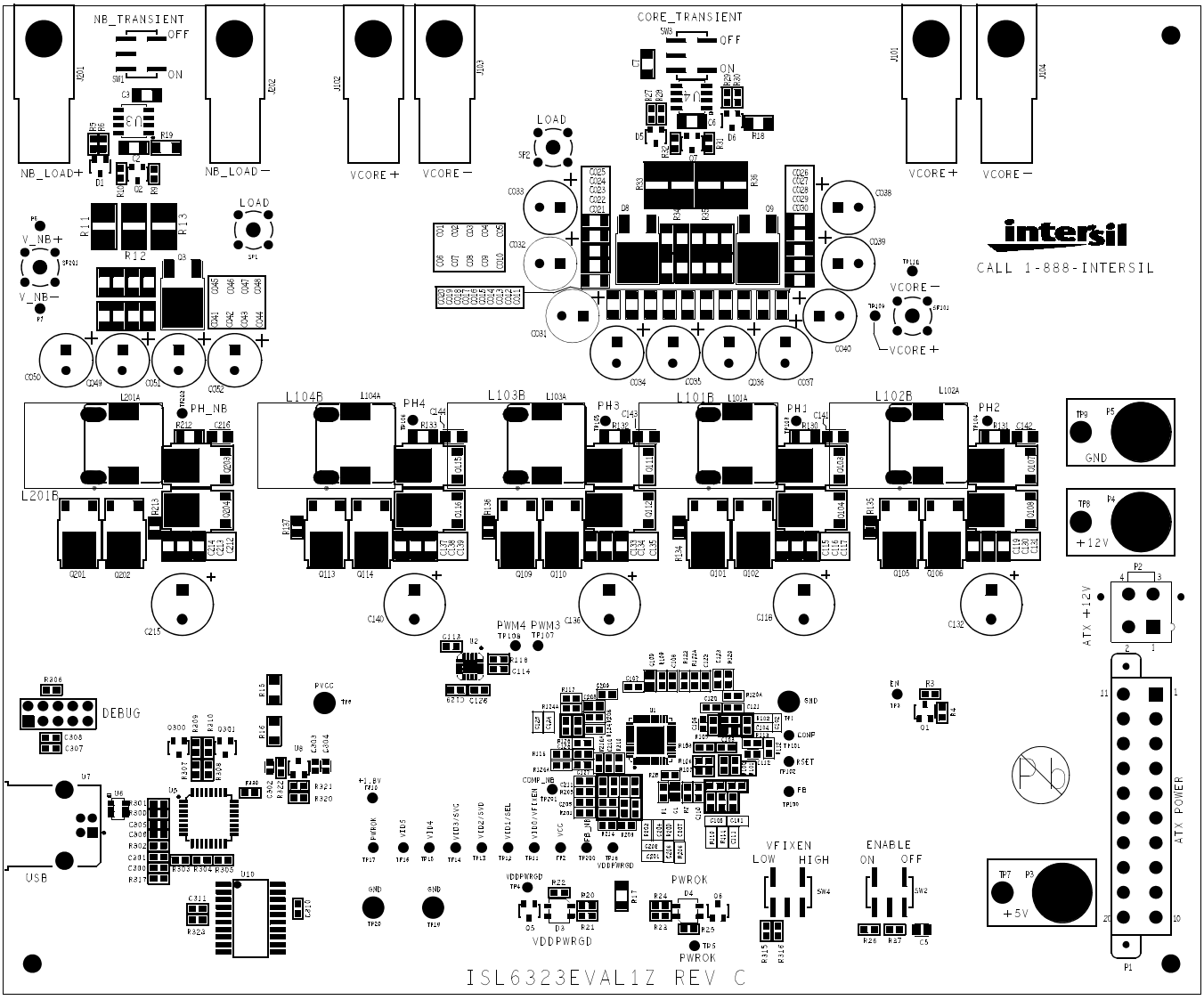


FIGURE 20. TOP SILK SCREEN AND SOLDERMASK

ISL6323EVAL1Z Layout (Continued)

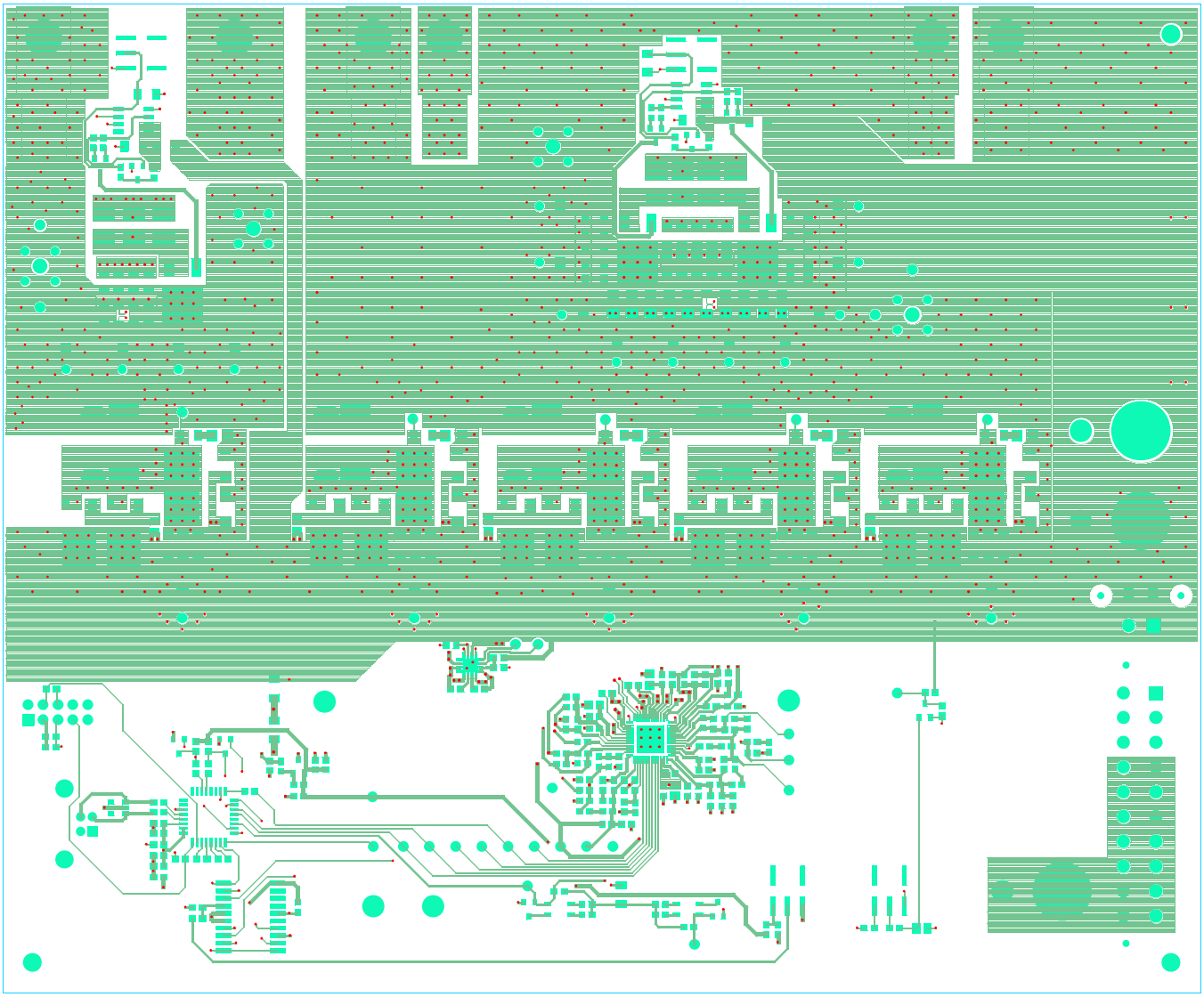


FIGURE 21. TOP

ISL6323EVAL1Z Layout (Continued)

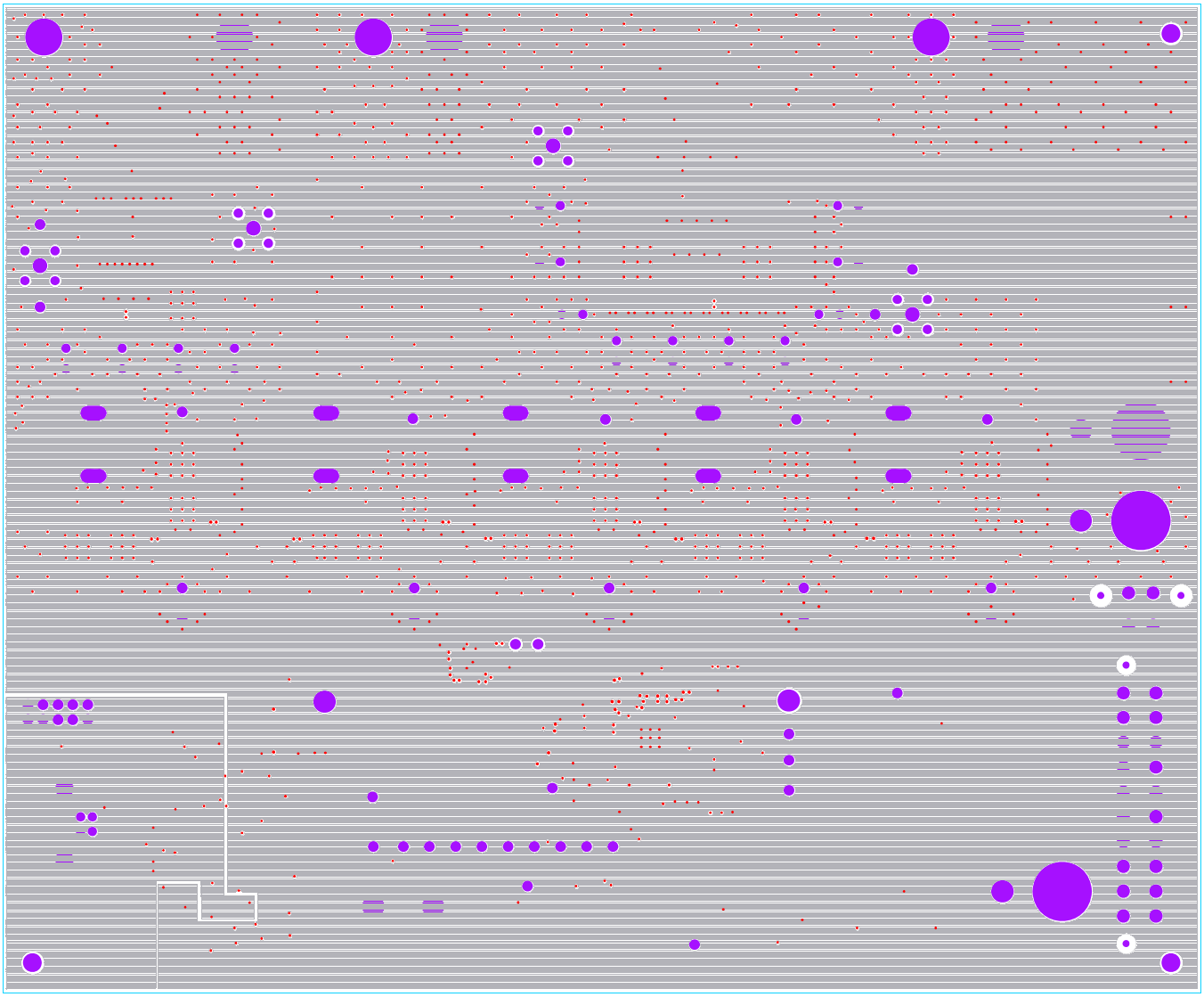


FIGURE 22. INTERNAL 1 GROUND

ISL6323EVAL1Z Layout (Continued)

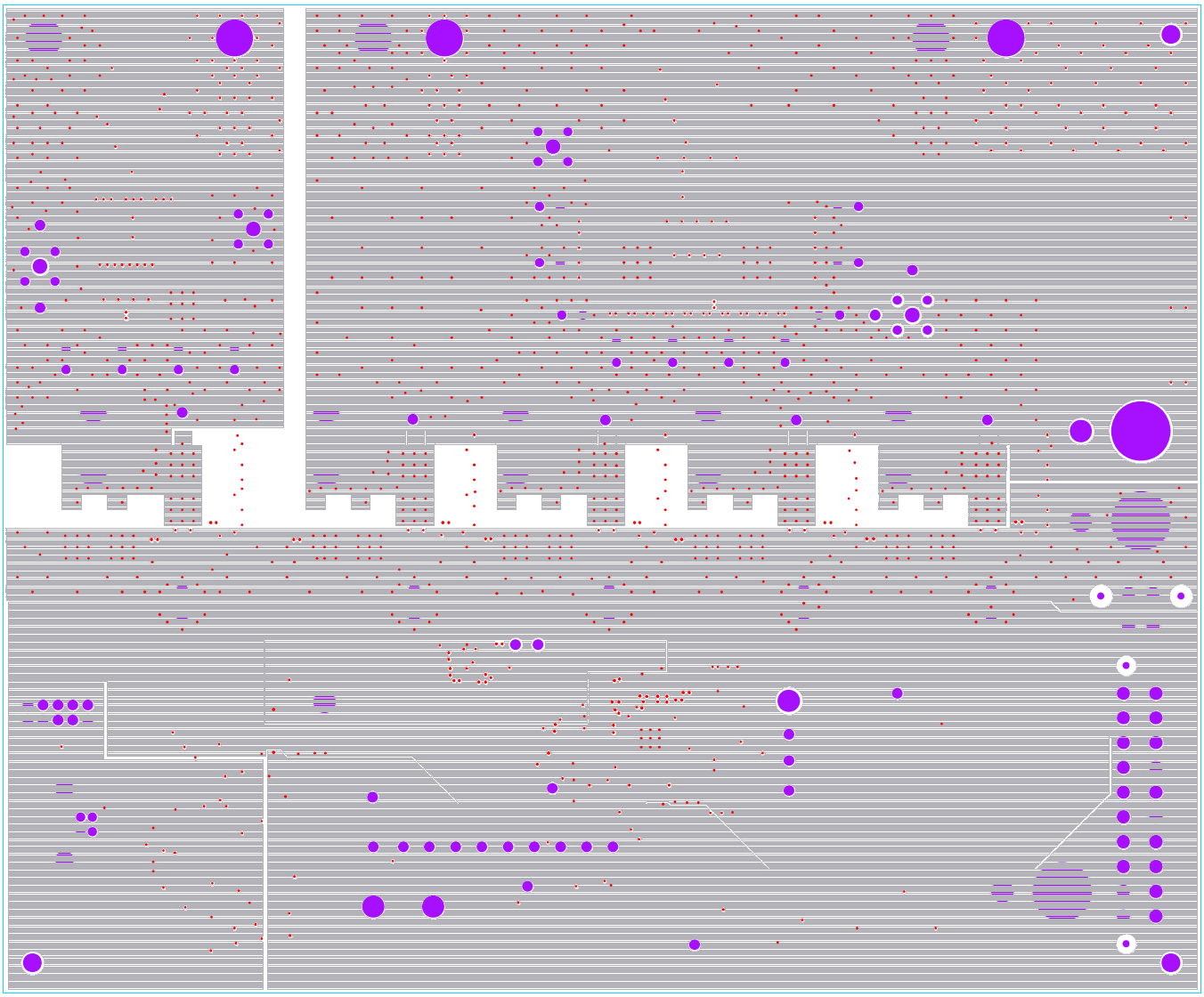


FIGURE 23. INTERNAL 2 POWER

ISL6323EVAL1Z Layout (Continued)

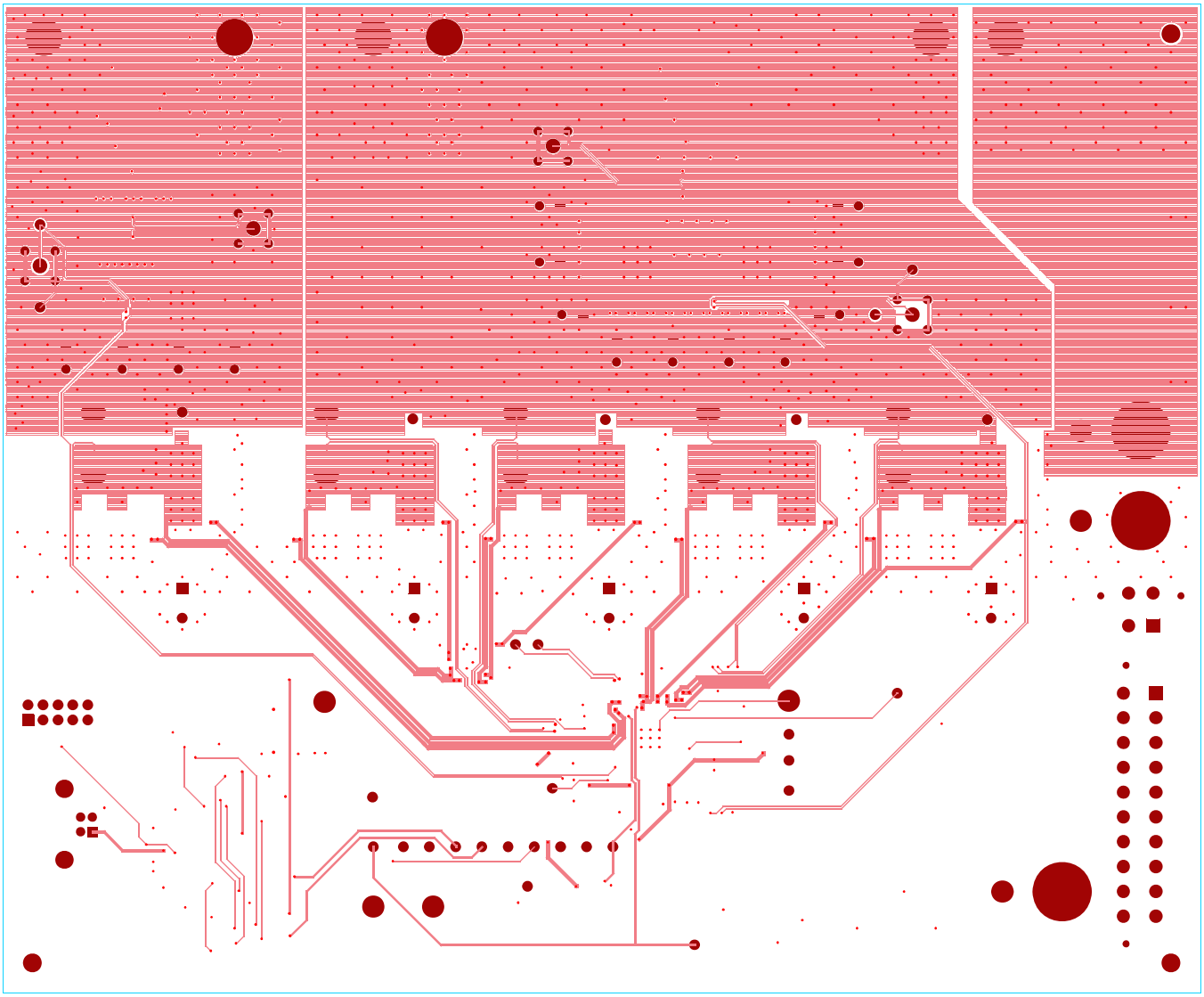


FIGURE 24. BOTTOM

PC to EVAL Board USB Communication

The ISL6323EVAL1Z evaluation board includes a microcontroller that is capable of communicating to a PC that has the ISL6323 Control Software and Drivers installed. This communication is performed via the Universal Serial Bus (USB) using National Instruments VISA runtime engine. The microcontroller is then used to send either SVI commands or PVI parallel VID codes to the ISL6323.

DOWNLOAD AND EXTRACT THE SOFTWARE

Download the self extracting archive file ISL6323_v2_installer.exe. The URL for the file is

http://www.intersil.com/data/ev/isl6323_v2_installer.exe

A dialog box will give you the opportunity to define the location of the folder that the extracted files will be saved to.

Make a note of the location of the ISL6323 Installer folder. You will need to direct the New Hardware Wizard to this folder for the driver.

SOFTWARE INSTALLATION

Both the ISL6323 control program and the National Instruments run time engine are installed from the “ISL6323 Installer” Folder. Navigate to the folder and double click the “Autoexec.exe” file. You should see the window in Figure 25.

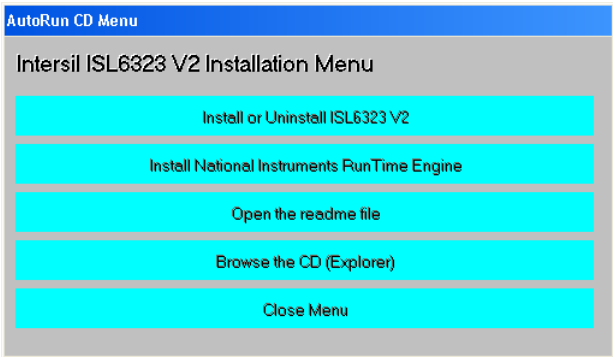


FIGURE 25. ISL6323 SOFTWARE INSTALLATION MENU

Click on the top button to run the Installation Wizard.

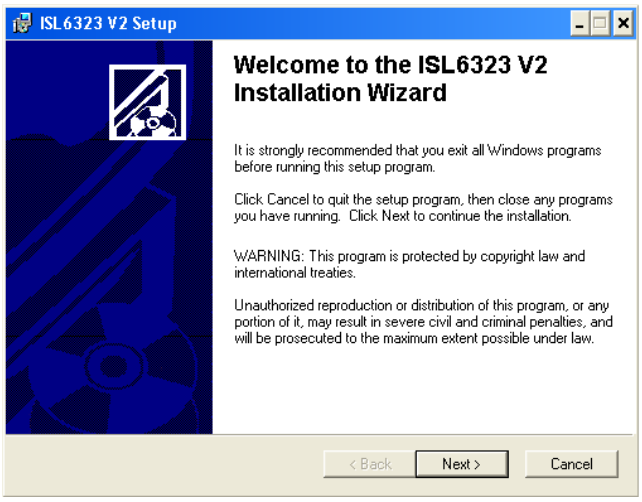


FIGURE 26. ISL6323 INSTALLATION WIZARD

In most PCs the National Instruments Runtime Engine will be installed automatically after the ISL6323 software. You should see the window in Figure 27.

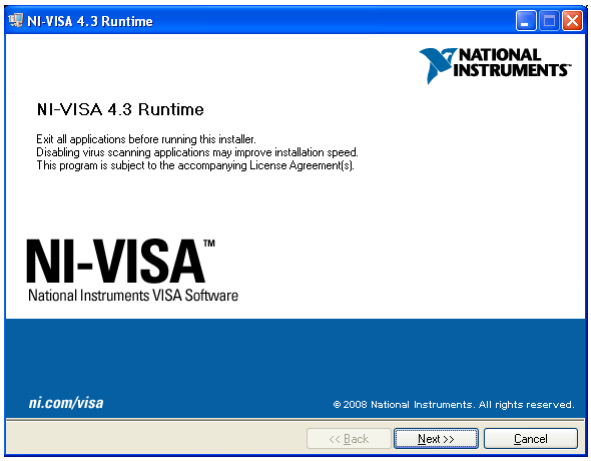


FIGURE 27. NATIONAL INSTRUMENTS RUNTIME ENGINE INSTALLATION WIZARD

Follow the instructions to install the Runtime Engine. If it does not run automatically, click on the second button on the ISL6323 Control Software Installation Menu (Figure 25 on page 21). After installation, click on the Close Menu button.

DRIVER INSTALLATION

Connect the ISL6323EVAL1Z to the USB port the PC.

Note: The USB interface is powered by the 5V from the USB port on the PC. It is not necessary to have other power supplies connected or enabled to establish communication between the microcontroller and the PC. It is necessary to have bias to the ISL6323 in order to send PVI or SVI commands to the ISL6323.

When WINDOWS detects new hardware, the new hardware wizard should appear. Direct it to look for the driver

information file in the “ISL6323 Installer” folder (extracted from the downloaded file). In some systems, it may be necessary to specify the driver information file (USB-I2C_WDM.inf).

RUNNING THE ISL6323 APPLICATION

This section assumes that software and the drivers have already been installed.

1. Connect the ISL6323EVAL1Z evaluation board to the USB port of the PC. The ISL6323 application will be available in START → ALL PROGRAMS. Run the application. Once the software has started, the window on the computer desktop should look like Figure 28.

Figure 28 shows a successful initiation of the communication software. Communication between the PC and the evaluation board is known to be active because there is an address in the “VISA resource name” box and the “WRITE ERROR” LED is dark. If the software was unsuccessful in establishing communications with the evaluation board, the “WRITE ERROR” LED would be lit red and the “VISA resource name” box may or may not be blank.

2. If testing the evaluation board in SVI mode is desired, make sure the SVI toggle switch is in the SVI position. If testing the evaluation board in PVI mode is desired, the toggle switch needs to be in the PVI position. Click on the switch to change its position. See Figure 29.
3. The desired VID code must now be set. If the software is set for PVI mode, then go to step 4. If the software is set for SVI mode, then the Metal VID level should be set to the desired level. This can be done by clicking on the UP or DOWN arrows for the Metal VID level. The display will change the Metal VID voltage and also show the 2-bit code that corresponds with that voltage (these voltages assume that the VFIXEN switch is toggled to LOW). See Figure 30.

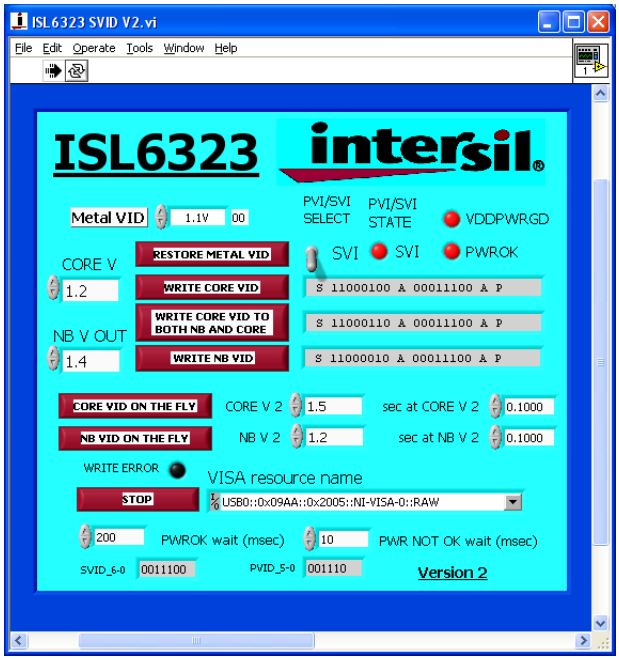


FIGURE 28. ISL6323 DESKTOP WINDOW

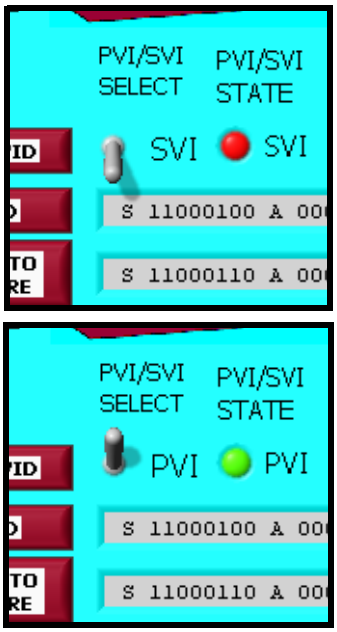


FIGURE 29. SVI/PVI TOGGLE SWITCH

4. To set the VID code in PVI mode, either toggle the UP or DOWN buttons for “CORE V” or type the desired output voltage level in the “CORE V” text box and then click on the “WRITE CORE VID” button. See Figure 30.

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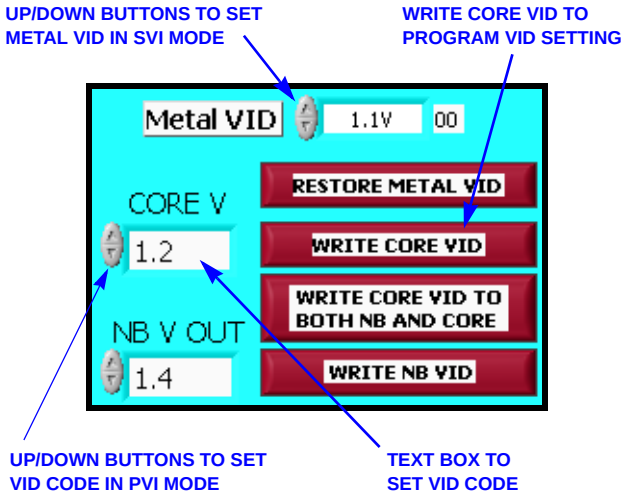

FIGURE 30. SETTING INITIAL VID CODES FOR POWER-UP

5. Changing VID codes. If the software is set for PVI mode, then go to STEP 6. If the software is set for SVI mode, then the ISL6323 is regulating the Core and North Bridge voltages to the same level which was set in Step 3 via the Metal VID code. While in SVI mode, the ISL6323 will not acknowledge SVI commands unless the PWROK signal is asserted High. This assertion can be confirmed visually either on the evaluation board or through the ISL6323 control software. On the evaluation board, the PWROK LED will be lit green. In the ISL6323 control software

window, the PWROK LED will also be lit green if PWROK is asserted High. In order to change the output voltage, toggle the UP or DOWN buttons for “CORE V” and/or “NB VOUT” until the text box shows the desired output voltage. An alternative method would be to click in the text box for “CORE V” and/or “NB V OUT” and then type the desired voltage in the text box. Once the desired voltage is shown in the text box through either the UP/DOWN buttons or typing in the level, the VIDs can be changed in one of three ways. If just the output level for the Core regulator is to be changed, then click on the “WRITE CORE VID” button. If just the output level for the North Bridge regulator is to be changed, then click on the “WRITE NB VID” button. If both the Core and the North Bridge are to be changed at the same time, then click on the “WRITE CORE VID TO BOTH NB AND CORE” button. Note that this option will set the regulation point of both the Core and the North Bridge regulators to the level shown for the Core regulator. The VID can only be changed if the PWROK signal is asserted High.

6. While PVI mode, the ISL6323 does not require a PWROK signal to change VID codes. To change the VID code in PVI mode, either toggle the UP/DOWN buttons for “CORE V” or use the mouse to select inside the “CORE V” text box and type in the desired output level. If toggling the UP/DOWN buttons, the VID code is sent immediately and the output will change every time the UP or DOWN buttons are toggled. If the desired level is typed in, the output will change when the “WRITE CORE VID” button is clicked.