



MCP9800/1/2/3

MCP9800/1/2/3 Rev. A Silicon/Data Sheet Errata

The MCP9800/1/2/3 parts you have received conform functionally to the MCP9800/1/2/3 Data Sheet (DS21909B), except for the anomalies described below.

All of the issues listed here will be addressed in future revisions of the MCP9800/1/2/3 silicon.

Contact Microchip for the latest Silicon fix.

Clarification/Corrections to the Data Sheet:

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS21909B):

None at this time.

1. Module: Device Internal Latch-up at Higher Temperatures

The MCP9800/1/2/3 devices may latch-up during I²C™ communication at high temperatures. This is caused by the internal I²C interface slew control circuit.

At temperatures >80°C (typically), High-to-Low transition <500 ns on the SDA or SCL lines causes the slew control circuit to latch-up.

Work around

Connect a capacitor across the SDA and SCL pull-up resistors so that the SDA and SCL fall time is >500 ns. For example, use 5 kΩ/0.01 μf.

Date Codes that pertain to this issue:

This issue concerns the devices produced on or before 718. This issue is fixed in devices with a date code of 721.

2. Module: POR Active During Oneshot Mode

At high temperatures the MCP9800/1/2/3 may reset while waking up from the Oneshot mode. All registers may be set at the power-up default states.

Work around

Shutdown and wake the device using the Shutdown bit in the Configuration register.

Date Codes that pertain to this issue:

This issue concerns the devices produced on or before 718. This issue is fixed in devices with a date code of 721.

MCP9800/1/2/3

APPENDIX A: REVISION HISTORY

Revision B (8/2011)

Specifies the device date codes that pertain to the issues described in this errata.

Revision A (7/2007)

- Device Internal latch-up at higher temperature.
- POR active during Oneshot mode.

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