PIC18C601/801

PIC18C601/801 Rev. C0 Silicon/Data Sheet Errata

The PIC18C601/801 parts you have received conform functionally to the Device Data Sheet (DS39541**A**), except for the anomalies described below.

All the problems listed here will be addressed in future revisions of the PIC18C601/801 silicon.

1. Module: WDT

When the device is configured for either EC or RC oscillator modes, with the Power-up Timer enabled, bit $\overline{TO}$ of the RCON register (RCON<3>) may default to '0', even though no WDT time-out has occurred.

The $\overline{TO}$ bit functions normally in all other configurations.

Work around

1. Use bit $\overline{TO}$ in conjunction with bit $\overline{POR}$ (RCON<1>) to determine if a RESET condition has occurred.
2. Use the latest silicon revision when it becomes available.

2. Module: I/O

The four Least Significant bits of the data direction registers TRISD, TRISE and TRISJ cannot be written to while the EBDIS bit of the MEMCOM register (MEMCOM<7>) is cleared. These bits remain set (TRISn<7:0> = '1111'), and the corresponding pins for their ports remain configured as inputs, until the EBDIS bit is set (= '1').

Work around

1. Write to the four Least Significant bits of TRISD, TRISE and TRISJ, only after setting the EBDIS bit.
2. Use the latest silicon revision when it becomes available.

3. Module: Interrupts

High priority interrupts may become improperly enabled, while low priority interrupts become improperly disabled at the same time. This may occur when low priority interrupts are in an enabled state and the following conditions occur simultaneously:

- High priority interrupts are being changed from an enabled to a disabled state; and
- One or more low priority interrupts occur.

Work around

1. Always disable low priority interrupts before disabling high priority interrupts. Re-enable the low priority interrupts afterwards, if necessary.
2. Use the latest silicon revision (C1 or higher) when it becomes available.

Date Codes that pertain to this issue:

ALL

Note:	When the manufacture date of a newer version of silicon is in production, the last date where this issue may occur will be specified.

4. Module: I/O (PORTB Interrupt-on-Change)

The RB Port Change Flag bit of the INTCON register (RBIF, INTCON<0>) may be inadvertently cleared, even when the PORTB<7:4> pins have not been read. This will occur only when the following two conditions occur simultaneously:

- The four Least Significant bits of the BSR register are equal to 0Fh (BSR<3:0> = '1111'), and
- Any instruction that contains 81h in its 8 Least Significant bits (i.e., register file addresses, literal data, address offsets, etc.) is executed.

Work around

All work arounds will involve setting the contents of BSR<3:0> to some value other than 0Fh. In addition to those proposed below, other solutions may exist.

1. When developing or modifying code, keep these guidelines in mind:
   - Assign 12-bit addresses to all variables. This allows the assembler to know when Access Banking can be used.
   - Do not set the BSR to point to Bank 15 (BSR = 0Fh).
   - Allow the assembler to manipulate the Access bit present in most instructions. Accessing the SFRs in Bank 15 will be done through the Access Bank. Continue to use the BSR to select Banks 1 through 5, and the upper half of Bank 0.
2. If accessing a part of Bank 15 is required and the use of Access Banking is not possible, consider using indirect addressing.
3. If pointing the BSR to Bank 15 is unavoidable, review the absolute file listing. Verify that no instructions contain 81h in the 8 Least Significant bits, while the BSR points to Bank 15 (BSR = 0Fh).

Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS39541**A**), the following clarifications and corrections should be noted.

1. Module: Core (DC Characteristics)

The specification for the device Supply Current (parameter D013, FOSC = 25 MHz, VDD = 5.5V) has changed. The new maximum value is 65 mA.

This new value applies to both standard and extended voltage range devices.

2. Module: Interrupts

The operation of the GIE/GIEH bit (INTCON<7>) is clarified as follows: when the bit is cleared, all interrupts are disabled. This is regardless of the state of the IPEN bit (RCON<7>), the priority of the interrupt, or whether or not the interrupt is unmasked. This varies from the original description, in which clearing the bit when IPEN = '1' would only disable high priority interrupts.

The seventh paragraph in Section 8.0 of the Device Data Sheet (beginning "When an interrupt is responded to....") is amended by adding the following sentence to the end:

"It is important to note, however, that clearing the GIE/GIEH bit, regardless of the state of the IPEN bit, will disable **all** interrupts."

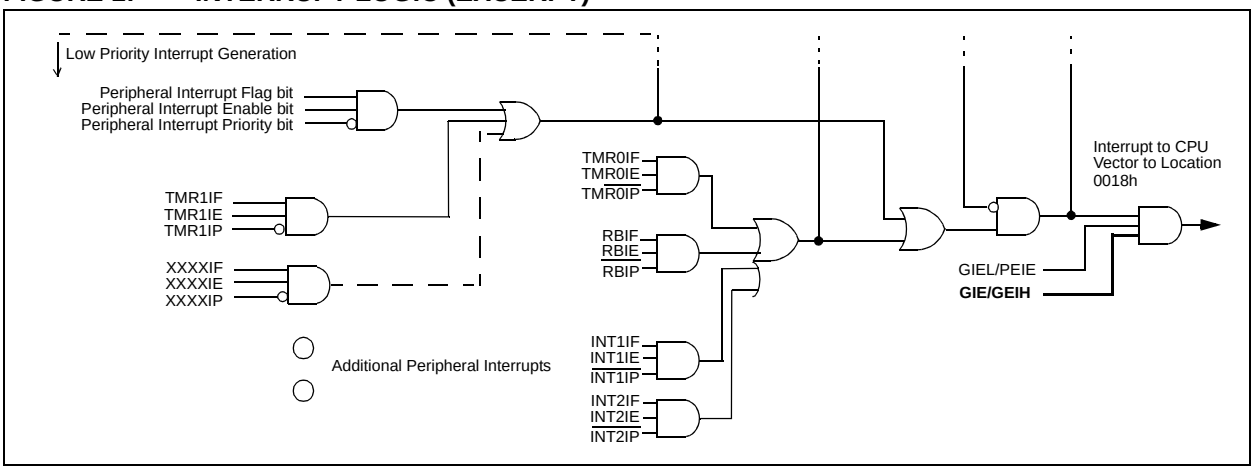
The changes to the bit descriptions in Register 8-1 in the Device Data Sheet are shown in the excerpt below (changes in **bold**).

Also, the interrupt logic funnel shown in Figure Figure 1 of the Device Data Sheet is amended with the addition of a GIE/GIEH control line, as shown in Figure 1 (new material in **bold line**).

REGISTER 8-1: INTCON REGISTER (EXCERPT)

bit 7	**GIE/GIEH:** Global Interrupt Enable bit When IPEN (RCON<7>) = 0: 1 = Enables all unmasked interrupts 0 = Disables all interrupts When IPEN (RCON<7>) = 1: 1 = Enables all high priority interrupts 0 = **Disables all interrupts**

FIGURE 1: INTERRUPT LOGIC (EXCERPT)



3. Module: Low Voltage Detect

The minimum and maximum values for specification D420 (LVD voltage) have changed. The new values for Table 22-1 of the Device Data Sheet (DS39541A) are shown in Table 1, below.

Typical values for specification D420 remain unchanged.

Also, the minimum and maximum values for specification D423 (bandgap voltage reference) have been added. These are shown in Table 2, below.

The typical value for specification D423 remains unchanged.

TABLE 1: MINIMUM AND MAXIMUM LOW VOLTAGE DETECT SPECIFICATIONS

Param No	Symbol	Characteristic		New Specification		Data Sheet Specification		Units
				Min	Max	Min	Max	
D420	VLVD	Low Voltage Detect	LVV<3:0> = 0100	2.34	2.78	2.5	2.66	V
			LVV<3:0> = 0101	2.54	3.02	2.7	2.86	V
			LVV<3:0> = 0110	2.64	3.14	2.8	2.98	V
			LVV<3:0> = 0111	2.84	3.36	3.0	3.2	V
			LVV<3:0> = 1000	3.12	3.70	3.3	3.52	V
			LVV<3:0> = 1001	3.30	3.92	3.5	3.72	V
			LVV<3:0> = 1010	3.40	4.04	3.6	3.84	V
			LVV<3:0> = 1011	3.59	4.25	3.8	4.04	V
			LVV<3:0> = 1100	3.78	4.48	4.0	4.26	V
			LVV<3:0> = 1101	3.96	4.70	4.2	4.46	V
			LVV<3:0> = 1110	4.25	5.03	4.5	4.78	V

TABLE 2: MINIMUM AND MAXIMUM BANDGAP VOLTAGE SPECIFICATIONS

Param No	Symbol	Characteristic	New Specification			Data Sheet Specification			Units
			Min	Typ	Max	Min	Typ	Max	
D423	VBG	Bandgap Reference Voltage Value	1.19	1.22	1.25	—	1.22	—	V

4. Module: Core

The minimum value for parameter specification number D001 (V_{DD}) for extended voltage range devices has changed from 2.0V. The new value is shown in Table 3.

All other values for specification D001 remain unchanged.

Because of this change, the voltage vs. frequency graph for extended voltage range devices has been modified. Figure 22-2 of the Device Data Sheet is replaced with Figure 2, below. This also clarifies that the graph refers to extended voltage range ("LC") devices.

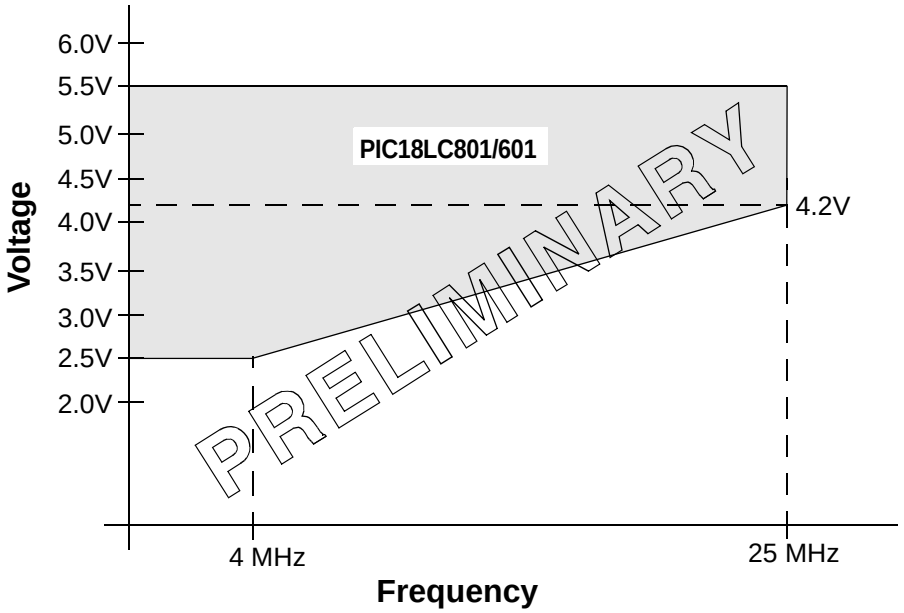
Also, the title for Figure 22-1 of the Device Data Sheet is amended to read:
"PIC18C601/801 Voltage-Frequency Graph (Industrial, Extended)".

This change also effects bits 3-0 in Register 18-1: LVDCON Register in the device data sheet.

TABLE 3: MINIMUM SUPPLY VOLTAGE SPECIFICATION (EXTENDED VOLTAGE RANGE)

Param No	Symbol	Characteristic		New Specification	Data Sheet Specification	Units
				Min	Min	
D001	V_{DD}	Supply Voltage	PIC18LC601/801	2.5	2.0	V

FIGURE 2: PIC18LC601/801 VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL)



F_{MAX} = (12.3 MHz/V) ($V_{DDAPPMIN}$ - 2.5V) + 4 MHz

Note: V_{DDAPP} is the minimum voltage of the PICmicro® device in the application.

REGISTER 18-1: LVDCON REGISTER

U-0	U-0	R-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-1
—	—	IRVST	LVDEN	LVDL3	LVDL2	LVDL1	LVDL0
bit 7							bit 0

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **IRVST:** Internal Reference Voltage Stable Flag bit

1 = Indicates that the Low Voltage Detect logic will generate the interrupt flag at the specified voltage range

0 = Indicates that the Low Voltage Detect logic will not generate the interrupt flag at the specified voltage range and the LVD interrupt should not be enabled

bit 4 **LVDEN:** Low Voltage Detect Power Enable bit

1 = Enables LVD, powers up LVD circuit
0 = Disables LVD, powers down LVD circuit

bit 3-0 **LVDL3:LVDL0:** Low Voltage Detection Limit bits

1111 = External analog input is used (input comes from the LVDIN pin)
1110 = 4.5V
1101 = 4.2V
1100 = 4.0V - Reserved on PIC18C601/801
1011 = 3.8V - Reserved on PIC18C601/801
1010 = 3.6V - Reserved on PIC18C601/801
1001 = 3.5V - Reserved on PIC18C601/801
1000 = 3.3V - Reserved on PIC18C601/801
0111 = 3.0V - Reserved on PIC18C601/801
0110 = 2.8V - Reserved on PIC18C601/801
0101 = 2.7V - Reserved on PIC18C601/801
0100 = 2.5V - Reserved on PIC18C601/801
0011 = Reserved on PIC18C601/801 and PIC18LC601/801
0010 = Reserved on PIC18C601/801 and PIC18LC601/801
0001 = Reserved on PIC18C601/801 and PIC18LC601/801
0000 = Reserved on PIC18C601/801 and PIC18LC801/601

LVDL3:LVDL0 modes which result in a trip point below the valid operating voltage of the device are not tested.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

5. Module: USART

The operation of the USART Transmit Interrupt flag bit TXIF (PIR1<4>) is clarified as follows:

TXIF is not cleared immediately upon loading data into the transmit buffer TXREG. The flag bit becomes valid in the second instruction cycle following the load instruction (see Example 1). Polling TXIF immediately following a load of TXREG will give invalid results (Example 2).

This clarification applies to **all** USART transmission modes (master or slave, synchronous or asynchronous, 8-bit or 9-bit).

EXAMPLE 1: CORRECTLY POLLING THE TXIF BIT

```
movwf   TXREG       ;load the register
nop                 :first instruction--
                    ;just a placeholder, it
                    ;could be any instruction
btfss   PIR1,TXIF   ;second instruction--
                    ;now TXIF is valid
```

EXAMPLE 2: POLLING THE TXIF BIT IMMEDIATELY AFTER LOADING THE TRANSMIT BUFFER

```
movwf   TXREG       ;load the register
btfss   PIR1,TXIF   ;first instruction--
                    ;reading TXIF now will
                    ;give invalid results
```

APPENDIX A: REVISION HISTORY

Rev A Document (6/2001)
First revision of this document.

Issues 1, 2 and 3 (WDT, I/O and Interrupt modules).

Under Clarifications/Corrections to the Data Sheet, added Core (DC Characteristics) issue (page 2, item 1).

Rev B Document (10/2001)
Added Issue 4 (I/O module - PORTB Interrupt-on-Change).

Rev C Document (2/2002)
Under Clarifications/Corrections to the Data Sheet, added Interrupts, LVD, Core and USART issues (pages 3 through 6, items 2, 3, 4 and 5).

Note the following details of the code protection feature on PICmicro® MCUs.

- The PICmicro family meets the specifications contained in the Microchip Data Sheet.
- Microchip believes that its family of PICmicro microcontrollers is one of the most secure products of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the PICmicro microcontroller in a manner outside the operating specifications contained in the data sheet. The person doing so may be engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable”.
- Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our product.

If you have any further questions about this matter, please contact the local sales office nearest to you.

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