

LTC4417

Prioritized PowerPath™ Controller

DESCRIPTION

Demonstration circuit DC1717A uses the LTC®4417 to arbitrate between three input supply rails, selecting the highest priority, valid supply to power the load. The rail's priority is defined by the input connection (V1-V3). Each rail has overvoltage and undervoltage thresholds set by external resistors. If the highest priority rail voltage falls out of the defined window (overvoltage or undervoltage), the rail with the next highest priority, which is valid, is

enabled and powers the load. Two or more LTC4417s can be cascaded to provide switchover between more than three rails.

Design files for this circuit board are available at <http://www.linear.com/demo/DC1717A>

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PERFORMANCE SUMMARY

Specifications are at $T_A = 25^\circ\text{C}$

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V1-V3, V _{OUT}	V1 to V3, V _{OUT} Operating Supply Range		2.5		36	V
ΔV_G	Open (VS-VG) Clamp Voltage	V _{OUT} = 11V, G1 to G3 = Open	5.4	6.2	6.7	V
$\Delta V_{G(\text{SOURCE})}$	Sourcing (VS-VG) Clamp Voltage	V _{OUT} = 11V, I = -10 μ A	5.8	6.6	7	V
$\Delta V_{G(\text{SINK})}$	Sinking (VS-VG) Clamp Voltage	V _{OUT} = 11V, I = 10 μ A	4.5	5.2	6	V
$\Delta V_{G(\text{OFF})}$	G1 to G3 Off (VS-VG) Threshold	V1 = V2 = V3 = 2.8V, V _{OUT} = 2.6V, G1 to G3 Rising Edge	0.12	0.35	0.6	V
$\Delta V_{G(\text{SLEW,ON})}$	G1 to G3 Pull-Down Slew Rate	V _{OUT} = 11V, C _{GATE} = 10nF	4	9	20	V/ μ s
$\Delta V_{G(\text{SLEW,OFF})}$	G1 to G3 Pull-Up Slew Rate	V _{OUT} = 11V, C _{GATE} = 10nF	7.5	13	22	V/ μ s
I _{GATE(LOW)}	G1 to G3 Low Pull-Down Current	V _{OUT} = 2.6V, V1 to V3 = 2.8V, (G1 to G3) = $\Delta V_G + 300\text{mV}$	0.8	2	7	μ A
V _{REV}	Reverse Voltage Threshold	Measure (V1 to V3) - V _{OUT} , V _{OUT} Falling	30	120	200	mV
t _{G(SWITCHOVER)}	Break-Before-Make Time	V _{OUT} = 11V, C _{GATE} = 10nF	0.7	2	3	μ s
V _{VALID(OL)}	$\overline{\text{VALID}}_1$ to $\overline{\text{VALID}}_3$ Output Low Voltage	I = 1mA, (V1 to V3) = 2.5V, V _{OUT} = 0V		0.2	0.55	V
t _{PVALID(OFF)}	$\overline{\text{VALID}}_1$ to $\overline{\text{VALID}}_3$ Delay OFF from OV/UV Fault		5	8	13	μ s
V _{SHDN(THR)}	SHDN Threshold Voltage	SHDN Rising	0.4	0.8	1.2	V
V _{SHDN_EN(HYS)}	SHDN, EN Threshold Hysteresis			100		mV
I _{SHDN_EN}	SHDN, EN Pull-Up Current	SHDN = EN = 0V	-0.5	-2	-5	μ A
V _{OV_UV(THR)}	OV1 to O3, UV1 to UV3 Comparator Threshold	V _{OUT} = 11V, OV1 to OV3 Rising, UV1 to UV3 Falling	0.985	1	1.015	V
V _{OV_UV(HYS)}	OV1 to O3, UV1 to UV3 Comparator Hysteresis	V _{OUT} = 11V	15	30	45	mV
t _{VALID}	V1 to V3 Validation Time		100	256	412	ms
V1	Operating Voltage of Channel V1		9.6	12	14.4	V
V2	Operating Voltage of Channel V2		4	5	6	V
V3	Operating voltage of Channel V3		6.4	8	9.6	V
I _{LOAD}	Load Current			2		A
AVI	Auxiliary Voltage Input		6		24	V

OVERVIEW

The LTC4417 controls three sets of external back-to-back P-channel MOSFETs to connect the proper rail to the load. Precision comparators are used to monitor each of the three input rails for both UV and OV conditions. The highest priority input supply whose voltage is within its respective OV/UV window for at least 256ms is considered valid and connected to the load. Low signals on the $\overline{\text{VALID1}}$, $\overline{\text{VALID2}}$, and $\overline{\text{VALID3}}$ pins indicate validation of the V1, V2, and V3 voltages.

DC1717A is designed to operate from inputs of 12V, 5V, and 8V, applied to V1, V2 and V3 respectively. The valid range of each supply is $\pm 20\%$, as set by OV and UV comparators and their associated resistive dividers. V1

has the highest priority, V3 has the lowest. The highest priority input that is also within its valid range is selected to power the output. V1, V2 and V3 inputs are protected against input glitches of up to $\pm 42\text{V}$. Maximum load current is 2A, limited by MOSFET capability.

Logic and LEDs are included to provide visual information about the operating status. These circuits are powered from a 6V to 24V auxiliary voltage input (AVI) which is regulated by an LT3060 (U4) to 5V. This auxiliary 5V rail also powers 100k Ω pull-ups for $\overline{\text{VALID}}$ pins. AVI must be present in order for the board to operate. See the Modification section for a means of eliminating AVI.

OPERATING PRINCIPLES

To eliminate back-and-forth switching during rail switchover, the LTC4417 provides a 30mV hysteresis in the OV and UV comparators, and an externally adjustable current mode hysteresis using the OV/UV resistive dividers. DC1717A's input reference hysteresis is 6%, and can be changed to 3% by moving the JP1 jumper to the 30mV position.

The controller's "break-before-make" switching method prevents cross conduction between input channels and reverse current from the output capacitor into the selected input supply.

Each channel's control circuit of the LTC4417 has a REV comparator, which monitors the connecting input supply and output load voltage. The REV comparator delays the connection until the output voltage droops 120mV below the input voltage. This prevents reverse current.

The LTC4417 has two common control pins: EN and $\overline{\text{SHDN}}$.

Pulling the EN pin below 1V turns off all external back-to-back P-channel MOSFETs. When this pin is driven above 1V, the highest priority valid channel is connected to the load. All these actions are provided without resetting the 256ms OV/UV timers.

Pulling the $\overline{\text{SHDN}}$ pin below 0.8V turns off all external back-to-back P-channel MOSFETs, placing the controller

in a low current state and resetting the 256ms timers used to validate input rail voltages. It requires at least 256ms to validate each rail voltage after the $\overline{\text{SHDN}}$ pin signal goes high.

The LTC4417 features two different driving modes for the P-channel MOSFET gates.

One mode is provided by the internal soft-start circuitry, which limits output voltage slew rate to no more than 5V/ms. As the highest output voltage slew rate, usually, can impose the highest requirements for circuit components, 5V/ms should be taken into account as a worst case for component selection.

The soft-start circuitry is enabled each time under the following conditions:

- If the LTC4417 is first powered on, or
- If $\overline{\text{SHDN}}$ is forced low, or
- If V_{OUT} falls below $\sim 0.7\text{V}$

Soft-start is disabled when:

- any channel turns off, including the channel that is soft starting.
- 32ms validation delay time has elapsed during the soft-start interval.

OPERATING PRINCIPLES

The other driving mode of the P-channel MOSFETs is used in the voltage switching operation, when the higher priority rail replaces the rail losing validity. The gate driver operates with a fixed current, which is defined by the external component parameters R_S and C_S shown in Figure 1.

The LTC4417 circuit designer should select the value of R_S and C_S based on the MOSFET parameters, power rail source characteristics, acceptable output voltage droop during transient, and the value of load capacitance.

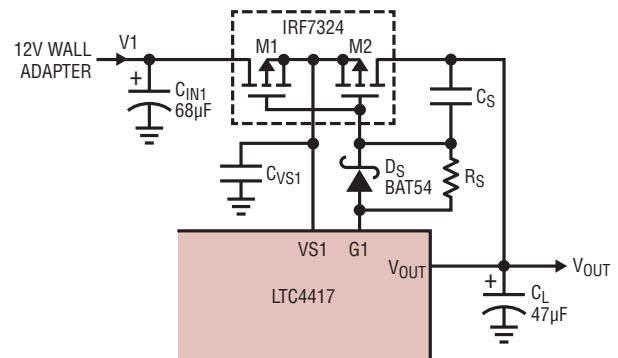


Figure 1

DESIGN PROCEDURE FOR MODIFICATION OF DC1717A

The valid input range for any supply is controlled by the OV and UV comparators with resistive dividers (R4-R13). See the LTC4417 data sheet for design equations to select resistors to match a particular requirement.

Dual MOSFETs, Q1-Q3, may be replaced with single devices Q4-Q9 by simply removing Q1-Q3. Pads for Q4-Q9 are located on the bottom side of the board.

The requirement for AVI may be eliminated by removing jumpers JP2 and JP3, and removing resistor R19. This modification leaves the LEDs unpowered and the inputs of U2 and U3 clamp the $\overline{\text{VALID}}$ pins at 0.7V, but otherwise leaves the LTC4417 operating autonomously.

The following design considerations and equations demonstrate the interrelation of the main component values and transient parameters in the rail transitions, when the output voltage exceeds 0.7V. The variables C_S and R_S used in the design equations correspond to the following board components:

- C20, R23 for V1 (+12V channel)
- C21, R26 for V2 (+5.0V channel)
- C22, R28 for V3 (+8.0V channel)

To have dominant influence on the transient time C_S should be at least ten times larger than the P-channel MOSFET's reverse transfer capacitance (Miller). In this design, for all rails, C_S (C20, C21, and C22) equals 47nF.

The slew rate of the output voltage can be expressed as a function of C_S :

$$\frac{dV_{OUT}}{dt} = \frac{dV_{CS}}{dt} = \frac{V_{SINK} - |V_{THRES}|}{R_S \cdot C_S} \quad (1)$$

where:

- V_{SINK} is the LTC4417 parameter rated in the data sheet as $\Delta V_{G(SINK)} = 4.5V-6V$.
- V_{THRES} is the P-channel gate threshold voltage, which is between $-1.5V$ and $-3.5V$ for the Si7905DN installed on the board.
- $R_S = 249\Omega$ and $C_S = 47nF$.

Given that dV_{OUT}/dt is based on the transient time requirement, it is possible to define R_S from equation 1.

The output voltage slew rate, dV_{OUT}/dt , range for the circuit with the listed parameters is between 85V/ms and 385V/ms.

During the transition of rails, the load can be disconnected from any rail for a time:

$$T_{DISCON} = t_{G(SWITCHOVER)} + t_{pVALID(OFF)} + t_{GATE_THRES}$$

Two first summands of the T_{DISCON} are rated in the LTC4417 data sheet as:

$$t_{G(SWITCHOVER)} = (0.3 \text{ to } 3)\mu s$$

$$t_{pVALID(OFF)} = (5 \text{ to } 13)\mu s$$

DESIGN PROCEDURE FOR MODIFICATION OF DC1717A

The second summand, $t_{pVALID(OFF)}$, should be taken into account if the associated LTC4417 input does not have any bypass capacitor and the rail can be disconnected from the input instantly.

The third one must be calculated as:

$$t_{GATE_THRES} = R_S \cdot C_S \left[-\ln \left(1 - \frac{V_{THRES}}{V_{SINK}} \right) \right] \quad (2)$$

It is possible to determine the minimum capacitive load required to hold the output up during switchover as a:

$$C_{LOAD(MIN)} \geq \frac{I_{LOAD(MAX)} \cdot T_{DISCON}}{V_{OUT(DROOPMAX)}} \quad (3)$$

where:

- $I_{LOAD(MAX)}$ is the maximum load current, A
- $V_{OUT(DROOPMAX)}$ is the maximum acceptable voltage droop, V

As shown in the equation (3), the use of external slew rate control will add additional delay to the total switchover time. Unfortunately, the actual components cannot be chosen until the load capacitance is known. This circular issue can only be resolved through an iterative process.

The process starts by calculating the $C_{LOAD(MIN)}$, assuming that $t_{GATE_THRES} = 10\mu s$. For clarity this value will be labeled $C_{LOAD(INIT)}$. Using the calculated $C_{LOAD(INIT)}$, calculate R_S from the expression of the T_{DISCON} . To ensure the newly calculated R_S based on $C_{LOAD(INIT)}$ is sufficient, calculate C_{LOAD} with the calculated R_S .

If $C_{LOAD(INIT)}$ (the initial calculated C_{LOAD}) is higher than the newly calculated C_{LOAD} then the process is completed. If the $C_{LOAD(INIT)}$ is lower than the newly calculated C_{LOAD} , calculate R_S using the higher value and repeat this process.

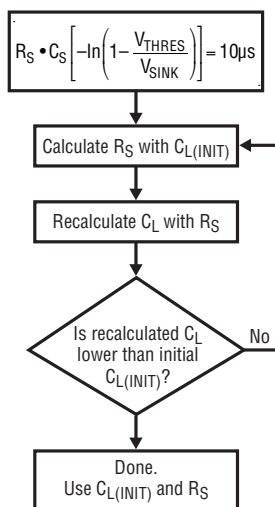


Figure 2

TURRETS

V1: 12V supply input; do not exceed $\pm 42V$.

V2: 5V supply input; do not exceed $\pm 42V$.

V3: 8V supply input; do not exceed $\pm 42V$.

GND: Adjacent ground connection for input supplies.

VOUT: Output for up to 2A load.

GND: Adjacent ground connection for load.

AVI: Auxiliary Voltage Input. 6V to 24V input regulated by U4 to 5V for LEDs, logic and pull ups on various pins.

GND: Adjacent ground connection for auxiliary supply.

5V: 5V regulated output provided by U4, for powering logic, LEDs and pull ups. Use this turret to verify that 5V is present.

Each of the following turrets is a direct connection to the like-name LTC4417 pin:

$\overline{VALID1}$: pulled up with 100kOhm to auxiliary 5V supply.

$\overline{VALID2}$: pulled up with 100kOhm to auxiliary 5V supply.

$\overline{VALID3}$: pulled up with 100kOhm to auxiliary 5V supply.

EN: pulled up by 2 μA internal to the LTC4417. Optional R33 may be added as a pull-up to the auxiliary 5V power supply.

\overline{SHDN} : pulled up by 2 μA internal to the LTC4417. Optional R36 may be added as a pull-up to the auxiliary 5V power supply.

CAS: used to cascade a second DC1717A. Connect the CAS turret of the high priority DC1717A to the EN turret of the lower priority DC1717A.

Grounds must be connected in common.

JUMPERS

JP1, HYS: Add 30mV fixed hysteresis to the OV and UV comparators, or 3% referred to actual supply input. In the RHYS position input-referred hysteresis is set to 6.4%, as controlled by R11. Default stuffing position is for 30mV.

JP2, EN: Directly controls EN pin. Default stuffing position is ON, pulled up by internal 2 μA current source.

LEDS

No more than one of D8, D9 and D10 will be illuminated at any given moment:

D8: indicates power is being taken from V1.

D9: indicates power is being taken from V2.

D10: indicates power is being taken from V3.

D11, D16 and D17 indicate the presence of a valid input on any of the three supplies:

D17: V1 is 12V $\pm 20\%$.

D11: V2 is 5V $\pm 20\%$.

D16: V3 is 8V $\pm 20\%$.

QUICK START PROCEDURE

Refer to the Figure 3 for proper measurement equipment setup and follow the procedure below:

Initially, the LTC4417 should be disabled by:

- placing the jumper **JP2** (EN) header in the OFF position, and
- placing the jumper **JP3** ($\overline{\text{SHDN}}$) header in the OFF position

Connecting the auxiliary power source (6V to 24V) to the DC1717A (AVI and GND turrets) lights the green LED (LDO-D12) indicating the presence of auxiliary +5V supply for powering logic.

With power off, connect three power supplies with output voltages of 12V, 5V, and 8V to corresponding DC1717A turrets or banana jacks V1(+12V), V2(+5V), V3(+8V), and GND.

Connect 6Ω load resistor (30W) to the DC1717A output turret or banana jack (VOUT). Do not use an electronic load in constant current mode.

Turn on three power supplies. No additional LEDs should light.

Change the jumper **JP3** ($\overline{\text{SHDN}}$) header position from OFF to ON. Three LEDs (VALID1, VALID2, and VALID3) validating the input rail voltages should light.

Placing the jumper **JP2** (EN) in the ON position turns on the LTC4417 powering the load with 12V (2.0A). In an initial power up the LTC4417 uses a fixed slew rate for the output voltage, which should be not larger than 5V/ms.

The prioritizing function is demonstrated by simply turning off one or two of the V1, V2 and V3 supplies. The output will be powered from the remaining supply of the highest priority. V1, V2 and V3 may be adjusted up and down beyond ±20% to invalidate a given input.

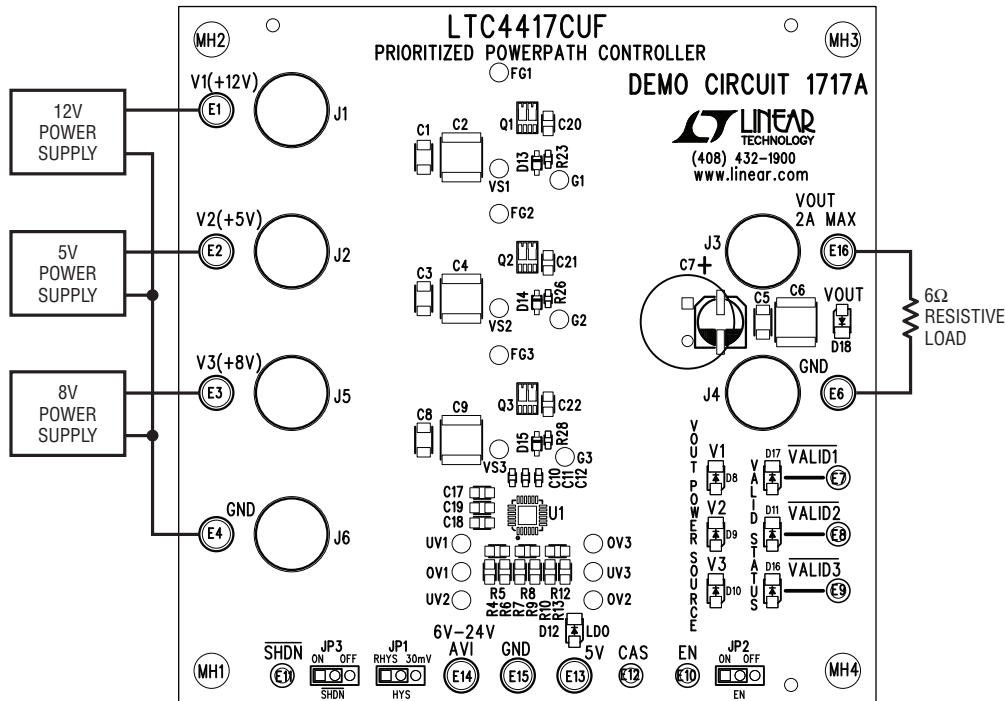


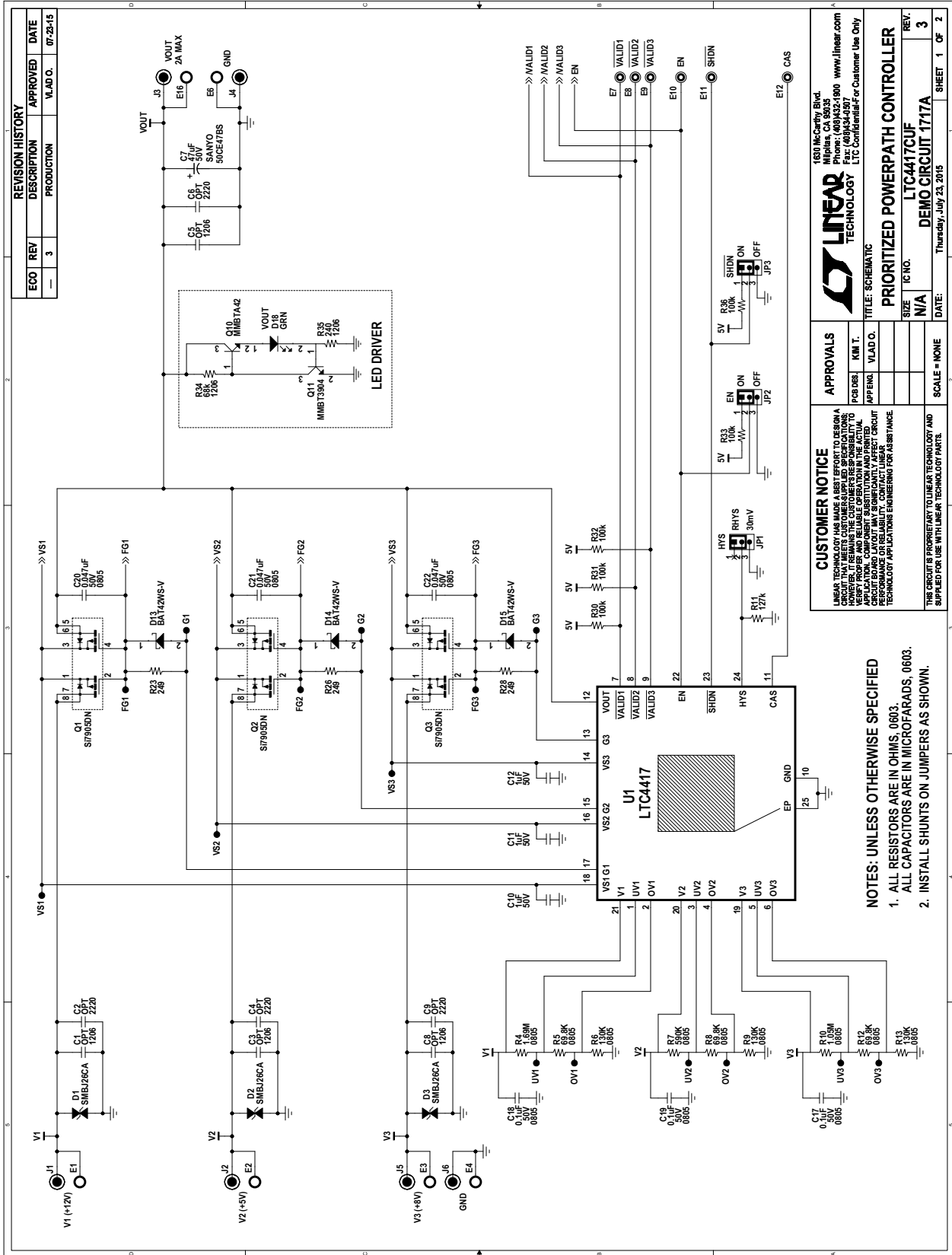
Figure 3

PARTS LIST

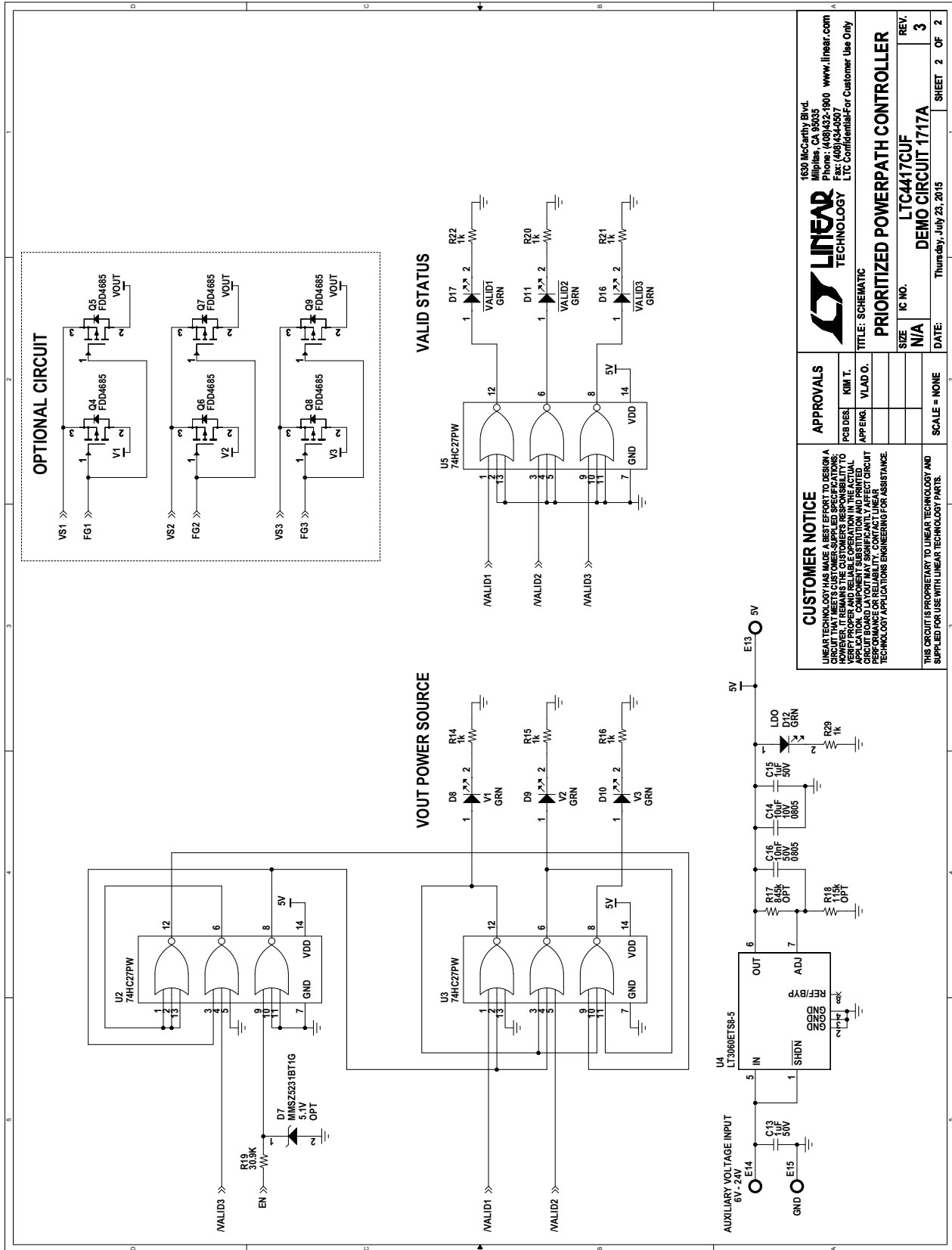
ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
1	0	C1, C3, C5, C8	CAP., 1206	OPT
2	0	C2, C4, C6, C9	CAP., 2220	OPT
3	1	C7	CAP., ALUM., 47µF 50V 20% SMT	SUN ELECT., 50CE47BS
4	5	C10, C11, C12, C13, C15	CAP., X5R, 1µF 50V, 10%, 0603	MURATA, GRM188R61H105KAALD
5	1	C14	CAP., X5R 10µF 10V 20% 0805	TAIYO YUDEN LMK212ABJ106MG -T
6	1	C16	CAP., NPO 10nF 50V 5% 0805	NIC, NMC0805NPO103J50TRPF
7	3	C17, C18, C19	CAP., X5R 0.1µF 50V 10% 0805	TAIYO YUDEN UMK212BJ104KG-T
8	3	C20, C21, C22	CAP., X7R 0.047µF 50V, 10%, 0805	MURATA, GRM21BR71H473KA01L
9	3	D1, D2, D3	DIODE, TVS BI-DIRECTIONAL, 26V, 600W	DIODES/ZETEX SMBJ26CA-13-F
10	0	D7	ZENER DIODE, 5.1V SOD-123	OPT
11	8	D8-D12, D16, D17, D18	LED, GREEN, LED-ROHM-SML-01	ROHM, SML-012P8TT86
12	3	D13, D14, D15	DIODE, SCHOTTKY, SOD323	VISHAY SEMI., BAT42WS-E3-08
13	9	E1-E4, E6, E13-E16	TURRET, 0.094"	MILL-MAX 2501-2-00-80-00-00-07-0
14	6	E7, E8, E9, E10, E11, E12	TURRET, 0.063"	MILL-MAX 2308-2-00-80-00-00-07-0
15	3	JP1, JP2, JP3	HEADERS, SGL. ROW 3 PINS 2mm CTRS.	SAMTEC TMM-103-02-L-S
16	3	SHUNTS ON JP1-JP3 (1&2)	SHUNT, 2mm CTRS.	SAMTEC 2SN-BK-G
17	6	J1, J2, J3, J4, J5, J6	JACK, BANANA	KEYSTONE 575-4
18	3	Q1, Q2, Q3	DUAL P-CHAN., 40V POWERPAK1212-8-DUAL	VISHAY Si7905DN-T1-GE3
19	0	Q4, Q5, Q6, Q7, Q8, Q9	MOSFET P-CHAN., 40V, FDD4685, DPAK	OPT
20	1	Q10	XTOR N-CHAN., SOT23	DIODE INC., MMBTA42-7-F
21	1	Q11	XTOR N-CHAN., SOT23	DIODE INC., MMBT3904-7-F
22	1	R4	RES., CHIP 1.69M 0.125W 1% 0805	VISHAY, CRCW08051M69FKEA
23	3	R5, R8, R12	RES., CHIP 69.8k 0.125W 1% 0805	VISHAY, CRCW080569K8FKEA
24	3	R6, R9, R13	RES., CHIP 130k 0.125W 1% 0805	NIC, NRC10F1303TRF
25	1	R7	RES., CHIP 590k 0.125W 1% 0805	VISHAY, CRCW0805590KFKEA
26	1	R10	RES., CHIP 1.05M 0.125W 1% 0805	VISHAY, CRCW08051M05FKEA
27	1	R11	RES., CHIP 127k 0.1W 1% 0603	VISHAY, CRCW0603127KFKEA
28	7	R14-R16, R20-R22, R29	RES., CHIP 1k 0.1W 5% 0603	VISHAY, CRCW06031K00JNEA
29	0	R17	RES., CHIP 845k 0.1W 1% 0603	OPT
30	0	R18	RES., CHIP 115k 0.06W 1% 0603	OPT
31	1	R19	RES., CHIP 30.9k 0.1W 1% 0603	VISHAY, CRCW060330K9FKEA
32	3	R23, R26, R28	RES., CHIP 249 0.1W 1% 0603	VISHAY, CRCW060249RFKEA
33	5	R30, R31, R32, R33, R36	RES., CHIP 100k 0.1W 5% 0603	NIC, NRC06J104TRF
34	1	R34	RES., CHIP 68k 0.25W 5% 1206	NIC, NRC12J683TRF
35	1	R35	RES., CHIP 240Ω 0.25W 1% 1206	VISHAY, CRCW1206240RFKEA
36	1	U1	I.C., POWERPATH CONTROLLER, QFN24UF-4x4	LINEAR TECH CORP. LTC4417CUF
37	3	U2,U3,U5	I.C., TRIPPLE 3-INPUT NOR GATE TSSOP14	NXP/PHILIPS SEMI. 74HC27PW
38	1	U4	I.C., LOW DROPOUT REG. TSOT23-8	LINEAR TECH CORP. LT3060ETS8-5
39	4	MH1-MH4	STANDOFF, NYLON, 0.50, 1/2"	KEYSTONE, 8833 (SNAP ON)

DEMO MANUAL DC1717A

SCHEMATIC DIAGRAM



SCHEMATIC DIAGRAM



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TITLE: SCHEMATIC
PRIORITIZED POWERPATH CONTROLLER

REV: 3
 DEMO CIRCUIT 1717A
 Thursday, July 23, 2015
 SHEET 2 OF 2

APPROVALS

POB DESG.	KIM T.
APP ENGR.	VLAD O.
SCALE	NONE

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DEMO MANUAL DC1717A

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