4.0 Gbps Dual Driver

ADATE209

FEATURES

>4.0 Gbps (2 V swings)
120 ps rise time/fall time (2 V swings)
<1.0 W for dual driver (<500 mW/channel)
−1 V to +3.5 V range
Fast termination mode (VTx)
Cable loss compensation

APPLICATIONS

Automatic test equipment
Semiconductor test systems
Board test systems
Instrumentation and characterization equipment
High speed memory testing (DDR2/DDR3/DDR4)
HDMI testing

FUNCTIONAL BLOCK DIAGRAM

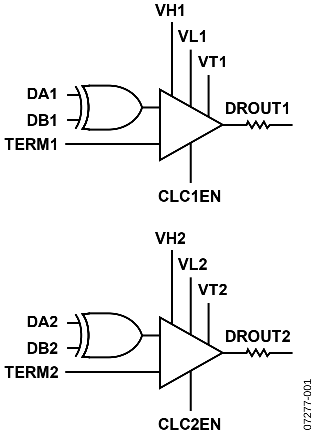

Figure 1.

GENERAL DESCRIPTION

The ADATE209 is a dual pin driver designed for testing DDR2, DDR3, and DDR4. It can also be used for high speed SoC applications, such as testing PCI Express 1.0 and HDMI™. The device is a three-level driver capable of high fidelity swings from 200 mV to 4 V over a −1 V to +3.5 V range. It has rise/fall times (20% to 80%) under 120 ps for a 2 V programmed swing and 150 ps for a 3 V programmed swing and is capable of supporting data rates of 4.4 Gbps and 3.2 Gbps, respectively.

The device is capable of high speed transitions into and out of termination mode. It also contains peaking/pre-emphasis circuitry.

The ADATE209 is available in an 8 mm × 8 mm, 49-ball CSP_BGA.

Rev. A

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REVISION HISTORY

2/10—Rev. 0 to Rev. A

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5/08—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

V_{CC} = 7.0 V, V_{EE} = −4.5 V, GND = 0.0 V; all test conditions are as defined in Table 8, unless otherwise specified. All specified values are at T_J = 70°C, where T_J corresponds to the internal temperature sensor, unless otherwise noted. Temperature coefficients are measured at T_J = 70°C ± 20°C, unless otherwise noted. Typical values are based on design, simulation analyses, and/or limited bench evaluations. Typical values are not tested or guaranteed.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Level[1]	Test Conditions/Comments
TOTAL FUNCTION						
DROUTx Pin Range	−1.0		+3.5	V	I	
POWER SUPPLIES						
Positive Supply, V_{CC}	6.65	7.0	7.35	V	I	Defines PSRR conditions
Negative Supply, V_{EE}	−4.73	−4.5	−4.28	V	I	Defines PSRR conditions
Data and Termination, V_{DAx}, V_{DBx}, V_{TERMx}	−1	+1.3	+3.3	V	I	
Data and Termination, I_{DAx}, I_{DBx}, I_{TERMx}		40		mA	I	Exceeding 40 mA through any input termination resistor may cause damage to the device or cause long-term reliability concerns
Positive Supply Current, I_{CC}	50	76	100	mA	II	
Negative Supply Current, I_{EE}	60	80	110	mA	II	
Total Power Dissipation	0.5	0.87	1.3	W	II	Quiescent; excludes current draw through data input termination resistors
		0.97		W	III	VLx = 0.0 V, VHx = 2.0 V; driver toggling into open circuit; excludes current draw through data input termination resistors
TEMPERATURE MONITORS						
Temperature Sensor Gain		−4.7		mV/°C	III	
Temperature Sensor Offset		3.1		V	III	Voltage reading at 30°C
DRIVER DC SPECIFICATIONS						
High Speed Differential Logic Input Characteristics (DAx, DBx, TERMx)						
Input Termination Resistance	45	48	55	Ω	II	9 mA pushed into DAxB/DBxB/TERMxB signal, 0.6 V forced on DAx/DBx/TERMx signal; DAxT, DBxT, TERMxT open; measure voltage from DAx/DBx/ TERMx signal to DAxB/DBxB/TERMxB signal, calculate resistance (ΔV/ΔI)
Input Voltage Differential	0.25		0.8	V	IV	
Common-Mode Voltage	−1.0		+3.3	V	IV	
Input Bias Current	−10	+1.2	+10	µA	II	Each pin tested at −1.0 V and +3.3 V, while other high speed pins (DAxB, DBx, DBxB, TERMx, TERMxB) are left open, termination pins (DAxT, DBxT, TERMxT) open
Pin Output Characteristics						
Output High Range, VHx	−0.9		+3.5	V	I	
Output Low Range, VLx	−1.0		+3.4	V	I	
Output Termination Range, VTx	−1.0		+3.5	V	I	
Output High Range, VHx	−0.9		+4.0	V	I	V_{CC} = 7.5 V, this range is not production tested
Output Low Range, VLx	−1.0		+3.9	V	I	V_{CC} = 7.5 V, this range is not production tested
Output Termination Range, VTx	−1.0		+4.0	V	I	V_{CC} = 7.5 V, this range is not production tested
Functional Amplitude (VHx − VLx)	0.2		4.5	V	I	Amplitude can be programmed to VHx = VLx, accuracy specifications apply when VHx − VLx ≥ 200 mV
DC Output Current-Limit Source	50	60	70	mA	II	Driver high, VHx = 3.5 V, short DROUTx pin to −1.0 V, then measure current

Parameter	Min	Typ	Max	Unit	Test Level[1]	Test Conditions/Comments
DC Output Current-Limit Sink	−70	−60	−50	mA	II	Driver high, VHx = −1.0 V, short DROUTx pin to 3.5 V, then measure current
Output Resistance, ±30 mA	46.5	48.5	50.5	Ω	II	Source: driver high, VHx = 3.0 V, I_{DUT} = 1 mA and 9 mA; sink: driver low, VLx = 0.0 V, I_{DUT} = −1 mA and −9 mA; $\Delta V_{DROUTx}/\Delta I_{DROUTx}$
Absolute Accuracy						VHx tests conducted with VLx = −1.0 V and VTx = −1.0 V; VLx tests conducted with VHx = 3.5 V and VTx = 3.5 V; VTx tests conducted with VLx = −1.0 V and VHx = +3.5 V
VHx, VLx, VTx Offset	−150	+20	+150	mV	II	Measured at 0.0 V, target: improve offset
VHx, VLx, VTx Offset Temperature Coefficient		270		μV/°C	III	Measured at calibration points, 0.0 V and 2.0 V
VHx, VLx, VTx Gain	0.97	1.02	1.03	%FSR	II	Relative to straight line from 0.0 V to 2.0 V
VHx, VLx, VTx Linearity	−15	±2.4	+15	mV	II	After two-point gain/offset calibration, relative to straight line from 0.0 V to 2.0 V
VLx, VHx, VTx Interaction		0.3		mV	III	VLx = −1.0 V, VHx swept from −0.9 V to +3.5 V, VTx swept from −1.0 V to +3.5 V, VHx = 3.5 V, VLx swept from −1.0 V to +3.4 V, VTx swept from −0.8 V to +3.5 V, VTx = 1.5 V, VLx swept from −1.0 V to +3.5 V, VHx swept from −1.0 V to +3.5 V
VHx, VLx, VTx DC PSRR	−36	+24	+36	mV/V	II	Change in output voltage as power supplies are moved by ±5%; measured at calibration points, 0.0 V and 2.0 V
VHx, VLx, VTx Input Bias Current	−10	+1	+10	μA	II	
DRIVER AC SPECIFICATIONS						
Rise/Fall Times						Toggle DAx inputs
0.2 V Programmed Swing		115		ps	V	VHx = 0.2 V, VLx = 0.0 V, terminated, 20% to 80%
0.5 V Programmed Swing		90		ps	V	VHx = 0.5 V, VLx = 0.0 V, terminated, 20% to 80%
1.0 V Programmed Swing		90		ps	V	VHx = 1.0 V, VLx = 0.0 V, terminated, 20% to 80%
2.0 V Programmed Swing	90	110	130	ps	II/V	VHx = 2.0 V, VLx = 0.0 V, terminated, 20% to 80%
3.0 V Programmed Swing		150		ps	V	VHx = 3.0 V, VLx = 0.0 V, terminated, 20% to 80%
4.0 V Programmed Swing		190		ps	V	VHx = 3.5 V, VLx = −0.5 V, terminated, 20% to 80%
Rise-to-Fall Matching		10		ps	V	VHx = 1.0 V, VLx = 0.0 V, terminated; rise to fall within one channel
Minimum Pulse Width						Toggle both DAx and DBx inputs
0.2 V Programmed Swing		200		ps	V	VHx = 0.2 V, VLx = 0.0 V, terminated, timing error less than ±25 ps
0.5 V Programmed Swing		180		ps	V	VHx = 0.5 V, VLx = 0.0 V, terminated, timing error less than ±25 ps
1.0 V Programmed Swing		180		ps	V	VHx = 1.0 V, VLx = 0.0 V, terminated, timing error less than ±25 ps
2.0 V Programmed Swing		200		ps	V	VHx = 2.0 V, VLx = 0.0 V, terminated, timing error less than ±25 ps
3.0 V Programmed Swing		300		ps	V	VHx = 3.0 V, VLx = 0.0 V, terminated, timing error less than ±25 ps
Maximum Toggle Rate		2.5		GHz	V	VHx = 1.0 V, VLx = 0.0 V, terminated, 10% amplitude degradation
		2.2		GHz	V	VHx = 2.0 V, VLx = 0.0 V, terminated, 10% amplitude degradation
		1.8		GHz	V	VHx = 3.0 V, VLx = 0.0 V, terminated, 10% amplitude degradation

Parameter	Min	Typ	Max	Unit	Test Level[1]	Test Conditions/Comments
Dynamic Performance, Drive (VHx to VLx)						Toggle DAx inputs
Propagation Delay Time	300	660	1400	ps	II/V	VHx = 2.0 V, VLx = 0.0 V, terminated
Propagation Delay Temperature Coefficient		0.7		ps/°C	III	VHx = 2.0 V, VLx = 0.0 V, terminated
Delay Matching, Edge to Edge		±15		ps	V	VHx = 2.0 V, VLx = 0.0 V, terminated, rising vs. falling
Delay Matching Channel to Channel	−70	±50	+70	ps	II/V	VHx = 2.0 V, VLx = 0.0 V, terminated
Delay Change vs. Duty Cycle		±10		ps	V	VHx = 2.0 V, VLx = 0.0 V, terminated, 5% to 95% duty cycle
Preshoot and Undershoot		10		mV	V	VHx = 2.0 V, VLx = 0.0 V, terminated
Settling Time (VHx to VLx)						Toggle DAx Inputs
To Within 3% of Final Value		0.4		ns	V	VHx = 2.0 V, VLx = 0.0 V, terminated
To Within 1% of Final Value		2		ns	V	VHx = 2.0 V, VLx = 0.0 V, terminated
Rise/Fall Times (VTx to/from VHx/VLx)						Toggle DAx inputs
1.0 V Programmed Swing		110		ps	V	VHx = 1.0 V, VTx = 0.5V, VLx = 0.0 V, terminated, 20% to 80%
2.0 V Programmed Swing		170		ps	V	VHx = 2.0 V, VTx = 1.0 V, VLx = 0.0 V, terminated, 20% to 80%
Dynamic Performance, V_{TERM} (VHx or VLx to/from VTx)						Toggle TERMx inputs
Propagation Delay Time		720		ps	V	VHx = 3.0 V, VTx = 1.5 V, VLx = 0.0 V, terminated
Cable Loss Compensation						
Logic Control Inputs, CLCxEN	0		3.3	V	I	
Logic High	0.9		3.3	V	IV	
Logic Low	0		0.7	V	IV	
I_{CLCxEN}	−10	±1.2	+10	µA	II	V_{IN} = 0.0 V and 3.3 V
Compensation Constants						
Boost Time Constant		275		ps	V	CLCxEN = 3.3 V, VHx = 1.0 V, VLx = 0.0 V, terminated
Boost Peaking Amplifier		18		%	V	CLCxEN = 3.3 V, VHx = 1.0 V, VLx = 0.0 V, terminated

[1] See the Explanation of Test Levels section.

V_{CC} = 7.5 V, V_{EE} = −4.5 V, GND = 0.0 V; all test conditions are as defined in Table 8, unless otherwise specified. All specified values are at T_J = 70°C, where T_J corresponds to the internal temperature sensor, unless otherwise noted. Temperature coefficients are measured at T_J = 70°C ± 20°C, unless otherwise noted. Typical values are based on design, simulation analyses, and/or limited bench evaluations. Typical values are not tested or guaranteed.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Level[1]	Test Conditions/Comments
TOTAL FUNCTION						
DROUTx Pin Range	−1.0		+4	V	I	
POWER SUPPLIES						
Positive Supply, V_{CC}	7.125	7.5	7.875	V		
Negative Supply, V_{EE}	−4.73	−4.5	−4.28	V		
DRIVER DC SPECIFICATIONS						
Pin Output Characteristics						
Output High Range, VHx	−0.9		+4.0	V	I	This range is not production tested
Output Low Range, VLx	−1.0		+3.9	V	I	This range is not production tested
Output Termination Range, VTx	−1.0		+4.0	V	I	This range is not production tested
Functional Amplitude (VHx − VLx)	+0.2		+5	V	I	Amplitude can be programmed to VHx = VLx, accuracy specifications apply when VHx − VLx ≥ 200 mV, this is not production tested

[1] See the Explanation of Test Levels section.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltages	
Positive Supply Voltage (V_{CC} to GND)	−0.5 V to +8.0 V
Negative Supply Voltage (V_{EE} to GND)	−5.0 V to +0.5 V
Supply Voltage Difference (V_{CC} to V_{EE})	−1.0 V to +13 V
Reference Ground (DUTGND to GND)	−0.5 V to +0.5 V
Input Voltages	
Input Common-Mode Voltage	V_{EE} to V_{CC}
Short-Circuit Voltage (R_L = 0 Ω, V_{DUT} Continuous Short-Circuit Condition)	−1.5 V to +4.0 V
High Speed Input Voltage (Data and Termination Inputs, DAx, DBx, and TERMx)	−1.5 V to +3.9 V
High Speed Differential Input Voltage (DAx, DBx, TERMx to Termination Pin DAxT, DBxT, TERMxT)	2 V
VHx, VLx, VTx	−2 V to +4.5 V
CLCxEN	−1 V to +3.5 V
DROUTx I/O Pin Current	
DCL Maximum Short-Circuit Current (R_L = 0 Ω, V_{DUT} = −1.5 V to +4 V; DCL Current Limit)	±100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the following conditions: JEDEC 4L PCB, 50°C, and 100 LFM forced convection. θ_{JC} is specified for a 50°C cold plate and 50°C ambient temperature.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
49-Ball CSP_BGA	48.4	3.9	°C/W

EXPLANATION OF TEST LEVELS

I. Definition.

II. 100% Production Tested.

III. Characterized on Tester.

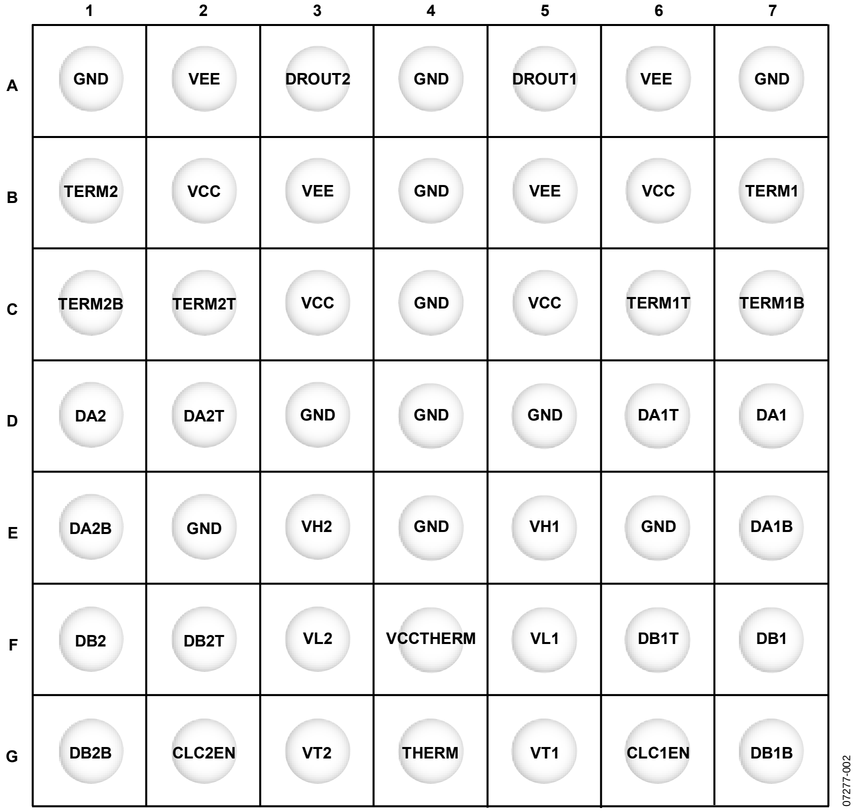
IV. Functionally Checked During Production Test.

V. Characterized on Bench.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



	1	2	3	4	5	6	7
A	GND	VEE	DROUT2	GND	DROUT1	VEE	GND
B	TERM2	VCC	VEE	GND	VEE	VCC	TERM1
C	TERM2B	TERM2T	VCC	GND	VCC	TERM1T	TERM1B
D	DA2	DA2T	GND	GND	GND	DA1T	DA1
E	DA2B	GND	VH2	GND	VH1	GND	DA1B
F	DB2	DB2T	VL2	VCCTHERM	VL1	DB1T	DB1
G	DB2B	CLC2EN	VT2	THERM	VT1	CLC1EN	DB1B

Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
A1	GND	Ground.
A2	VEE	Negative Power Supply, −4.5 V.
A3	DROUT2	Driver Output, Channel 2.
A4	GND	Ground.
A5	DROUT1	Driver Output, Channel 1.
A6	VEE	Negative Power Supply, −4.5 V.
A7	GND	Ground.
B1	TERM2	Termination Mode Data Input. Noninverting input for Channel 2.
B2	VCC	Positive Power Supply, 7.0 V.
B3	VEE	Negative Power Supply, −4.5 V.
B4	GND	Ground.
B5	VEE	Negative Power Supply, −4.5 V.
B6	VCC	Positive Power Supply, 7.0 V.
B7	TERM1	Termination Mode Data Input. Noninverting input for Channel 1.
C1	TERM2B	Termination Mode Data Input. Inverting input for Channel 2.
C2	TERM2T	Termination Pin for Termination Mode Data Input, Channel 2.
C3	VCC	Positive Power Supply, 7.0 V.
C4	GND	Ground.
C5	VCC	Positive Power Supply, 7.0 V.
C6	TERM1T	Termination Pin for Termination Mode Data Input, Channel 1.
C7	TERM1B	Termination Mode Data Input. Inverting input for Channel 1.
D1	DA2	Data Input A. Noninverting input for Channel 2.
D2	DA2T	Termination for Data Input A, Channel 2.
D3	GND	Ground.

Pin No.	Mnemonic	Description
D4	GND	Ground.
D5	GND	Ground.
D6	DA1T	Termination for Data Input A, Channel 1.
D7	DA1	Data Input A. Noninverting input for Channel 1.
E1	DA2B	Data Input A. Inverting input for Channel 2.
E2	GND	Ground.
E3	VH2	VH Input, Channel 2.
E4	GND	Ground.
E5	VH1	VH Input, Channel 1.
E6	GND	Ground.
E7	DA1B	Data Input A. Inverting input for Channel 1.
F1	DB2	Data Input B. Noninverting input for Channel 2.
F2	DB2T	Termination for Data Input B, Channel 2.
F3	VL2	VL Input, Channel 2.
F4	VCCTHERM	Positive Power Supply for Thermal Diode String, 7.0 V.
F5	VL1	VL Input, Channel 1.
F6	DB1T	Termination for Data Input B, Channel 1.
F7	DB1	Data Input B. Noninverting input for Channel 1.
G1	DB2B	Data Input B. Inverting input for Channel 2.
G2	CLC2EN	Cable-Loss Compensation Control Pin, Channel 2.
G3	VT2	VT Input, Channel 2.
G4	THERM	Thermal Diode Connection.
G5	VT1	VT Input, Channel 1.
G6	CLC1EN	Cable-Loss Compensation Control Pin, Channel 1.
G7	DB1B	Data Input B. Inverting input for Channel 1.

TYPICAL PERFORMANCE CHARACTERISTICS

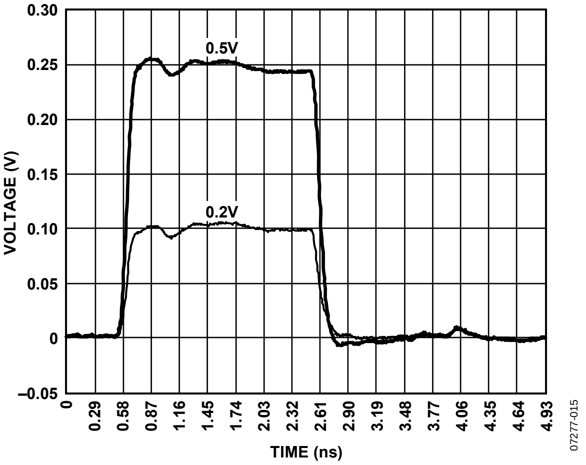


Figure 3. Small Signal Response, VHx = 500 mV, 200 mV, VLx = 0.0 V

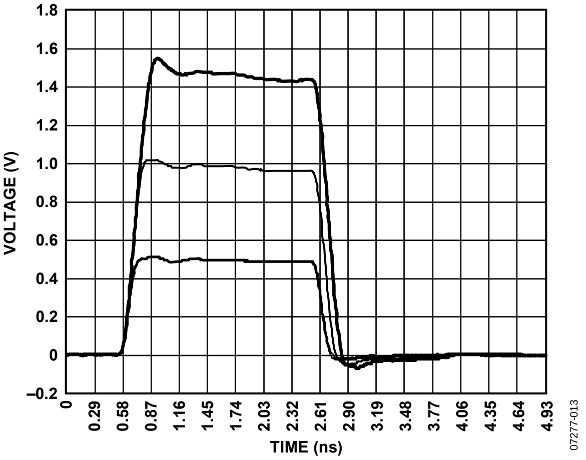


Figure 4. Large Signal Response, VHx = 3.0 V, 2.0 V, 1.0 V, VLx = 0.0 V

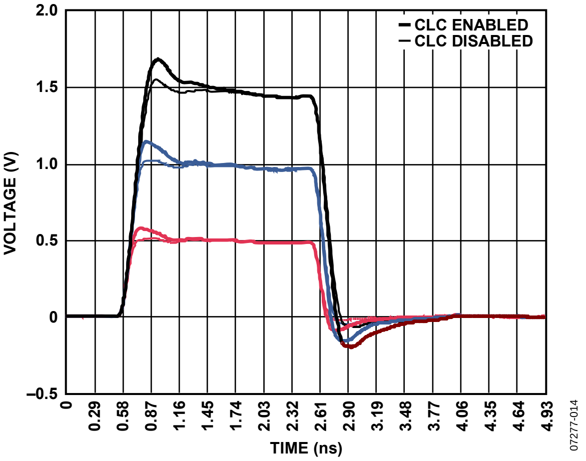


Figure 5. Large Signal Response, VHx = 3.0 V, 2.0 V, 1.0 V, VLx = 0.0 V, CLC Disabled and Enabled

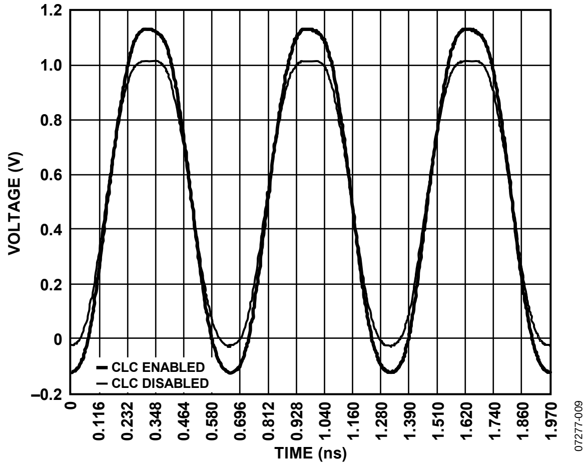


Figure 6. VHx = 2.0 V, VLx = 0.0 V, 1.5 GHz Waveform, CLC Disabled and Enabled

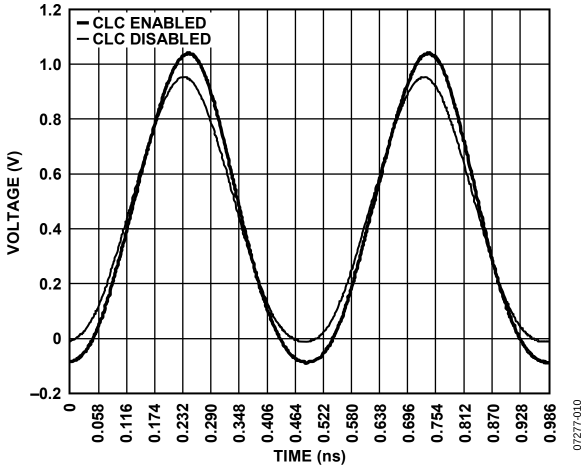


Figure 7. VHx = 2.0 V, VLx = 0.0 V, 2.0 GHz Waveform, CLC Disabled and Enabled

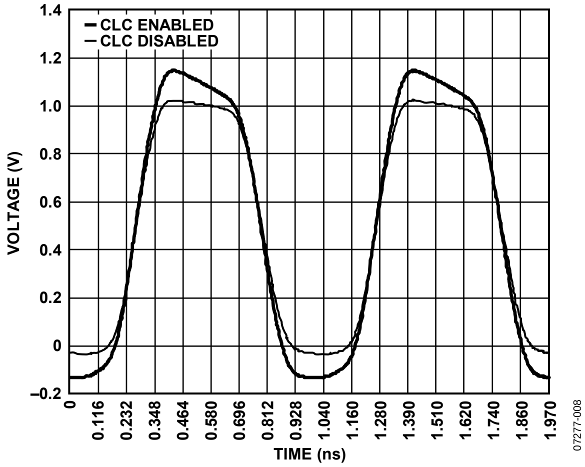


Figure 8. VHx = 2.0 V, VLx = 0.0 V, 1.0 GHz Waveform, CLC Disabled and Enabled

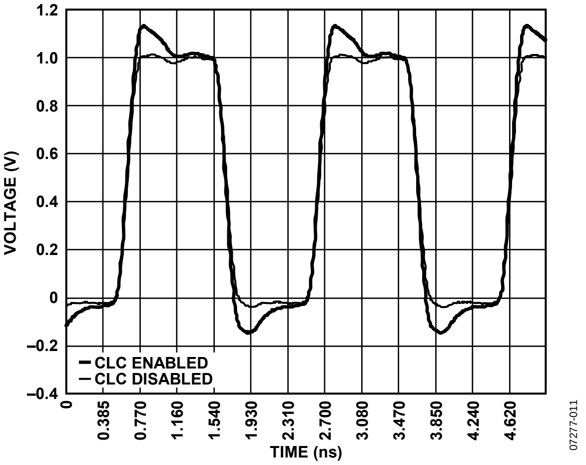


Figure 9. VHx = 2.0 V, VLx = 0.0 V, 500 MHz Waveform, CLC Disabled and Enabled

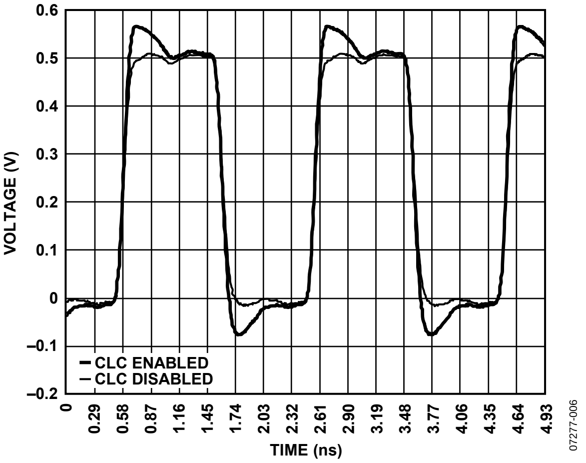


Figure 10. VHx = 1.0 V, VLx = 0.0 V, 500 MHz Waveform, CLC Disabled and Enabled

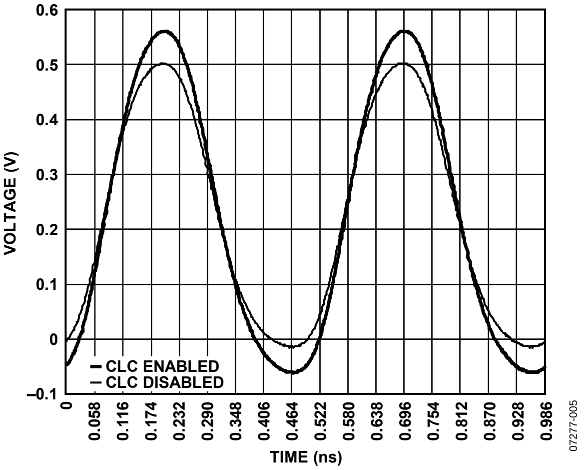


Figure 11. VHx = 1.0 V, VLx = 0.0 V, 2.0 GHz Waveform, CLC Disabled and Enabled

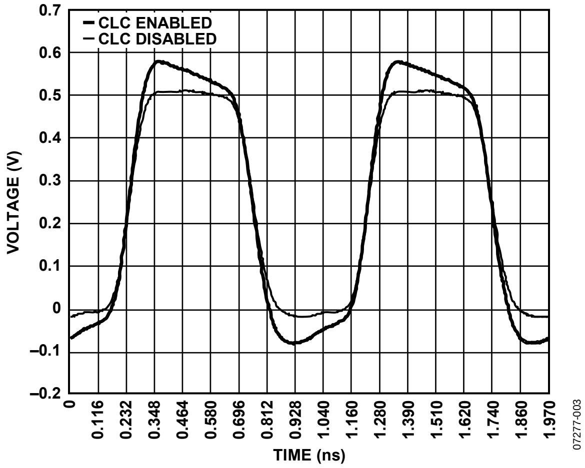


Figure 12. VHx = 1.0 V, VLx = 0.0 V, 1.0 GHz Waveform, CLC Disabled and Enabled

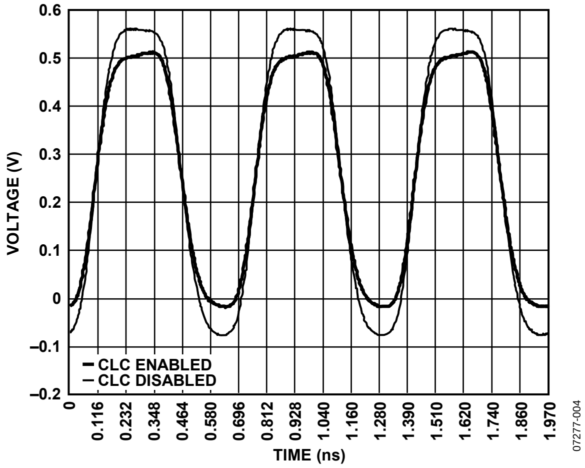


Figure 13. VHx = 1.0 V, VLx = 0.0 V, 1.5 GHz Waveform, CLC Disabled and Enabled

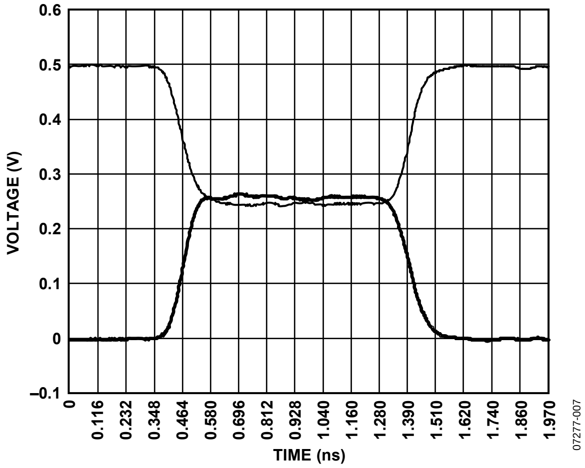


Figure 14. VHx = 1.0 V, VTx = 0.5 V, VLx = 0.0 V, Transitions Between VHx/VLx and VTx

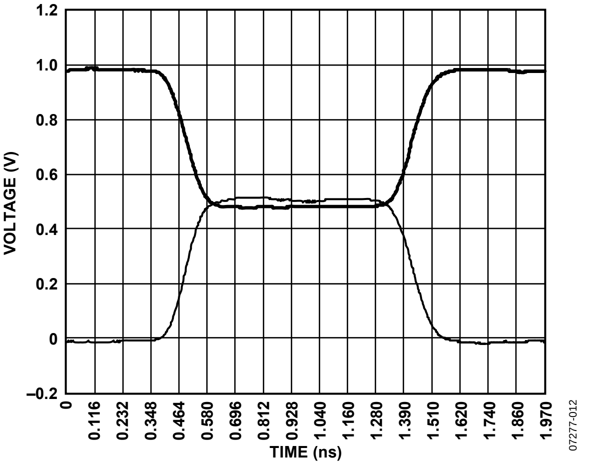


Figure 15. VHx = 2.0 V, VTx = 1.0 V, VLx = 0.0 V, Transitions Between VHx/VLx and VTx

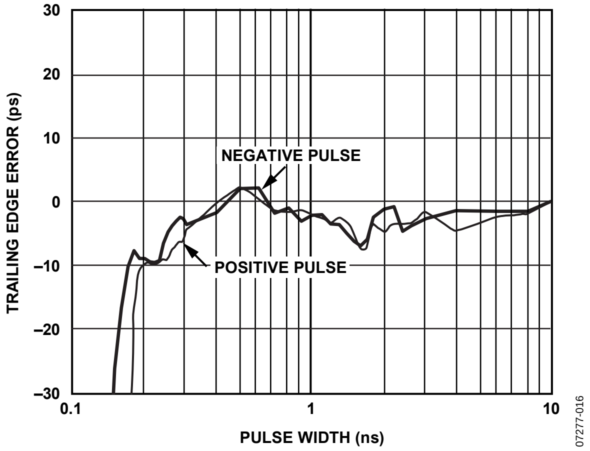


Figure 16. 1 V Minimum Pulse Width (VHx = 1.0 V, VLx = 0.0 V), CLC Disabled

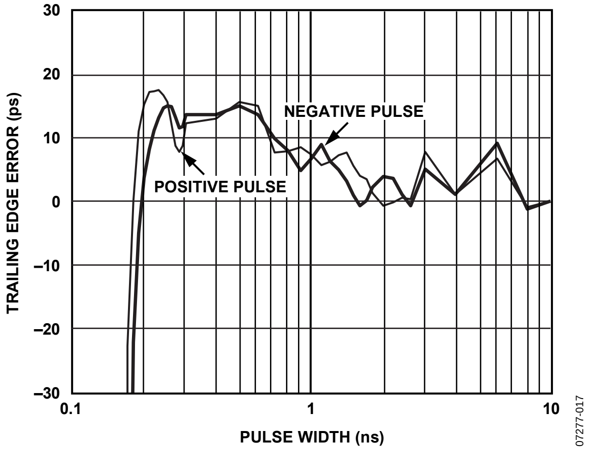


Figure 17. 2 V Minimum Pulse Width (VHx = 2.0 V, VLx = 0.0 V), CLC Disabled

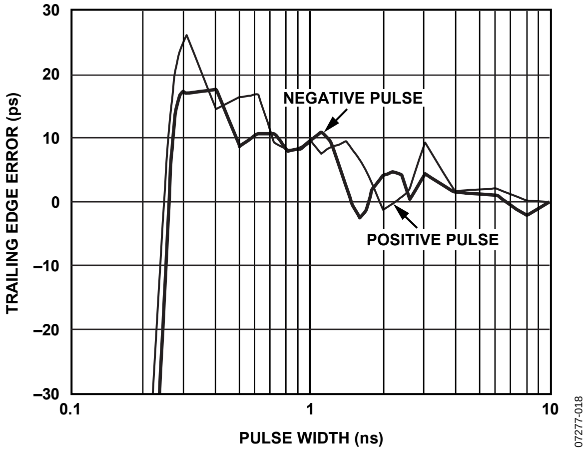


Figure 18. 3 V Minimum Pulse Width (VHx = 3.0 V, VLx = 0.0 V), CLC Disabled

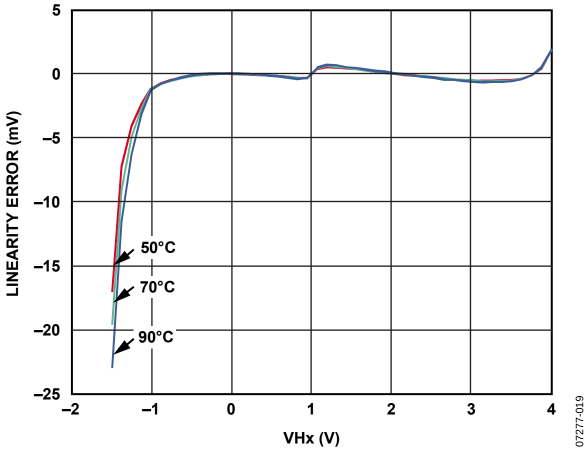


Figure 19. Driver Linearity (VHx), VLx = –1.1 V, VTx = 1.0 V

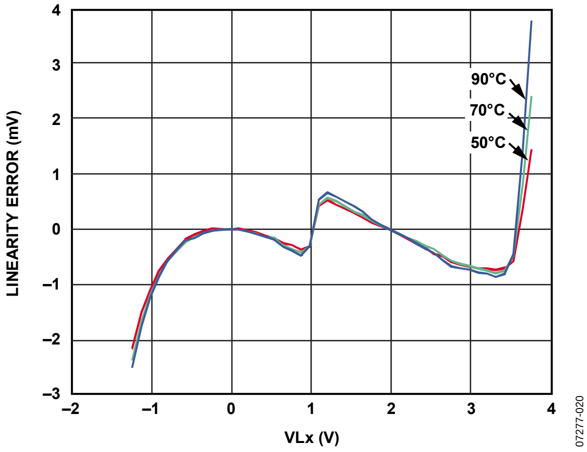


Figure 20. Driver Linearity (VLx), VHx = 3.6 V, VTx = 1.0 V

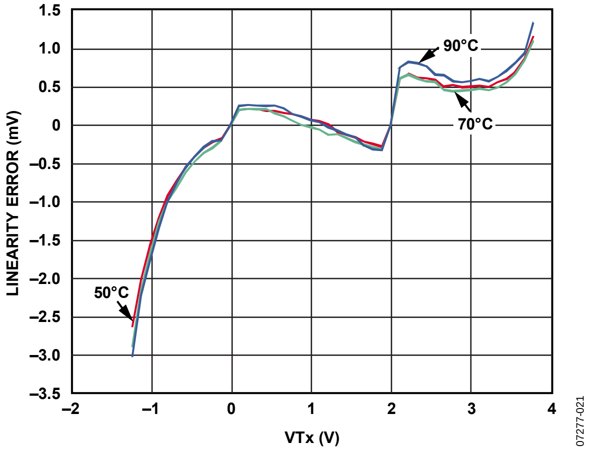


Figure 21. Driver Linearity (VTx), VHx = 2.0 V, VLx = 0.0 V

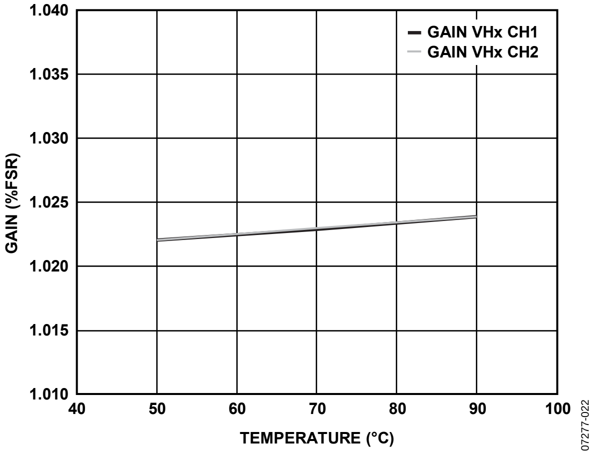


Figure 22. Gain of VHx

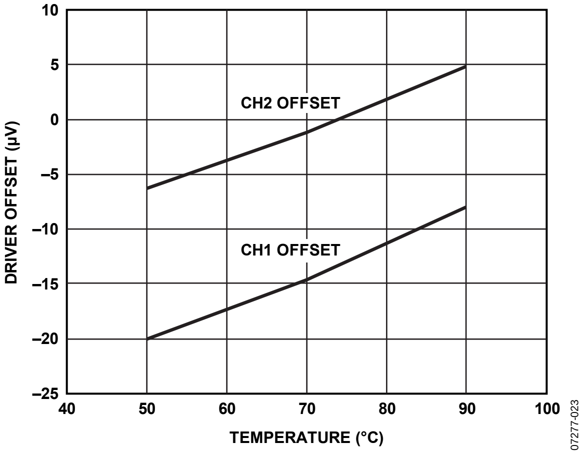


Figure 23. Driver Offset vs. Temperature

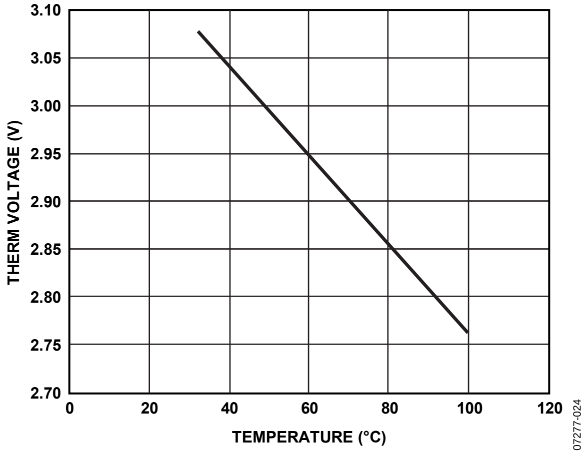


Figure 24. Temperature Sensor Output Voltage vs. Temperature

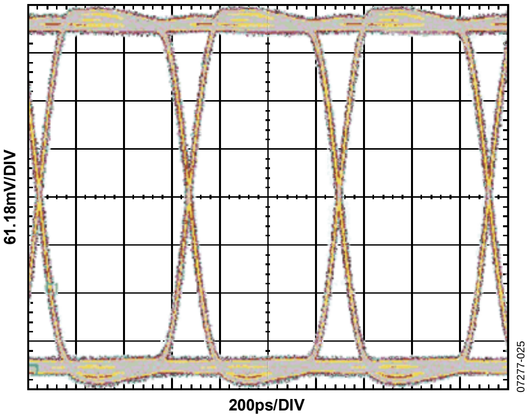


Figure 25. VHx = 1.8 V, VLx = 0.0 V, PRBS31, 1.6 Gbps, CLC Disabled

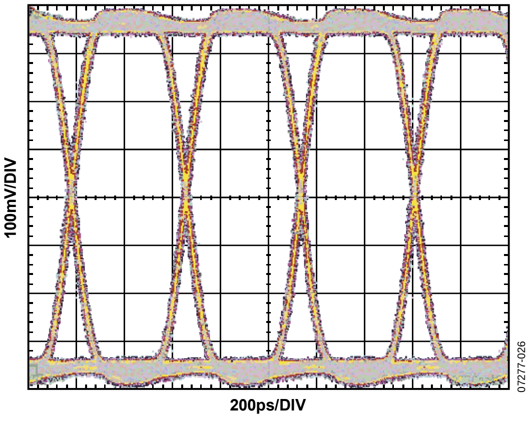


Figure 26. VHx = 1.8 V, VLx = 0.0 V, PRBS31, 2.1 Gbps, CLC Disabled

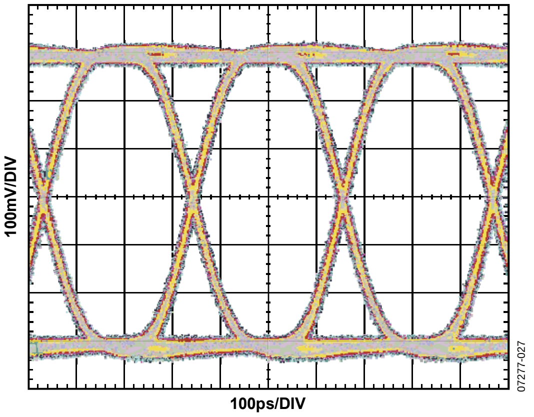


Figure 27. VHx = 1.5 V, VLx = 0.0 V, PRBS31, 3.2 Gbps, CLC Disabled

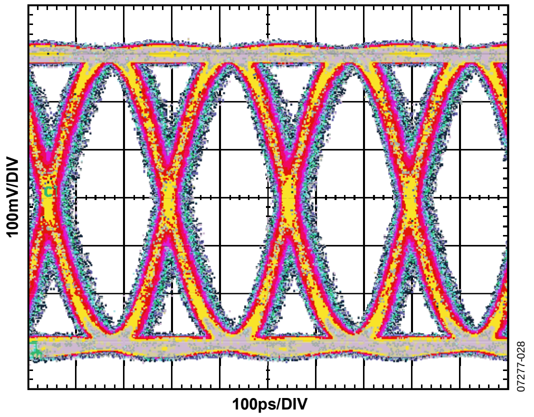


Figure 28. VHx = 1.5 V, VLx = 0.0 V, PRBS31, 4.0 Gbps, CLC Disabled

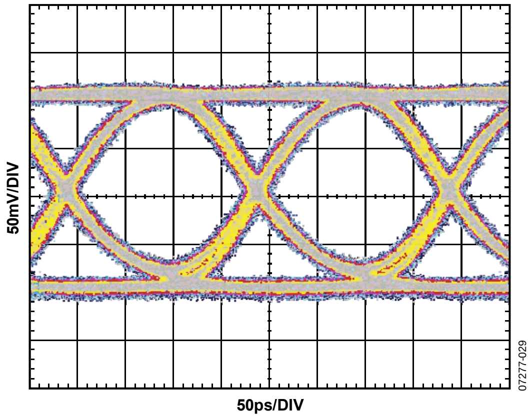


Figure 29. VHx = 0.5 V, VLx = 0.0 V, PRBS31, 5.0 Gbps, CLC Disabled

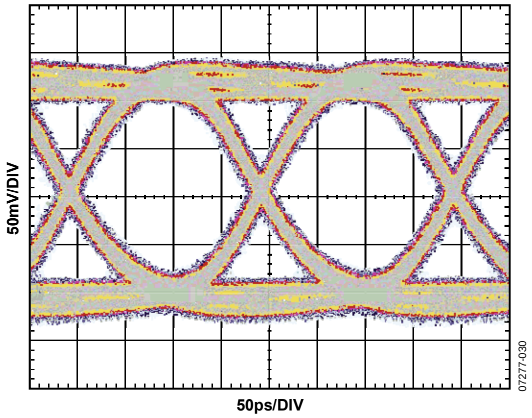


Figure 30. VHx = 0.5 V, VLx = 0.0 V, PRBS31, 5.0 Gbps, CLC Enabled

APPLICATIONS INFORMATION

DATA INPUTS

The ADATE209 contains three high speed differential inputs for each channel. Two of the inputs, combined in an on-chip exclusive-OR gate, control the VHx/VLx transitions. The exclusive-OR gate can be used as a data mux or for data inversion. The third input is used to control the transitions to the VTx level.

Table 6. Logic Truth Table

DAx	DBx	TERMx	DROUTx
Low	Low	Low	V_L
High	Low	Low	V_H
Low	High	Low	V_H
High	High	Low	V_L
X[1]	X[1]	High	V_T

[1] X = don't care.

The ADATE209 driver does not have a high impedance mode. The high speed inputs are designed to be compatible with most types of differential inputs. Each side of the differential inputs is terminated through 50 Ω to a common point. For connection to PECL inputs, connect the DAxT/DBxT/TERMxT input termination to V_{CC} – 2.0 V (V_{CC} of the input signal, not of the ADATE209) or to an appropriate resistor to ground. For connection to LVDS, do not connect DAxT/DBxT/TERMxT. For connection to CML signals, either leave DAxT/DBxT/TERMxT open or connect DAxT/DBxT/TERMxT to the appropriate V_{CC}/V_{DD} level.

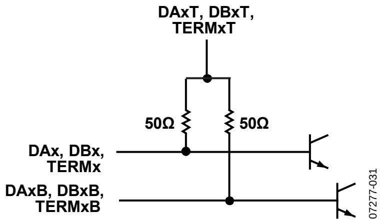


Figure 31. Input Termination Schematic Diagram

THERMAL DIODE STRING

Figure 32 shows a simplified schematic of the thermal diode string. To use the diode string, connect VCCTHERM to 7.0 V and measure the voltage at THERM. The nominal gain of the thermal diode string is −4.7 mV/°C.

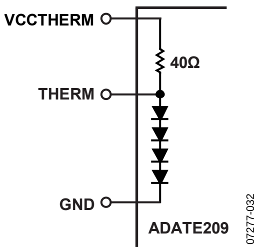


Figure 32. Thermal Diode String Schematic

CABLE LOSS COMPENSATION/PEAKING CIRCUITRY

The ADATE209 has two different CLC/peaking modes: nominal and boost. In nominal mode, a small amount of high frequency energy is injected in the driver output signal to compensate for high frequency losses in the test interface. In boost mode, a much larger percentage of high frequency energy is injected in the driver output signal. The two modes are controlled through the CLCxEN signal.

Table 7.

CLCxEN	CLC/Peaking Mode
Logic low	Nominal
Logic high	Boost

For applications using very short path lengths, very high fidelity cables and connectors, and/or lower data rates, nominal mode should be used. For applications using lower fidelity cables and connectors (and often lower cost) and/or at higher data rates, use boost mode.

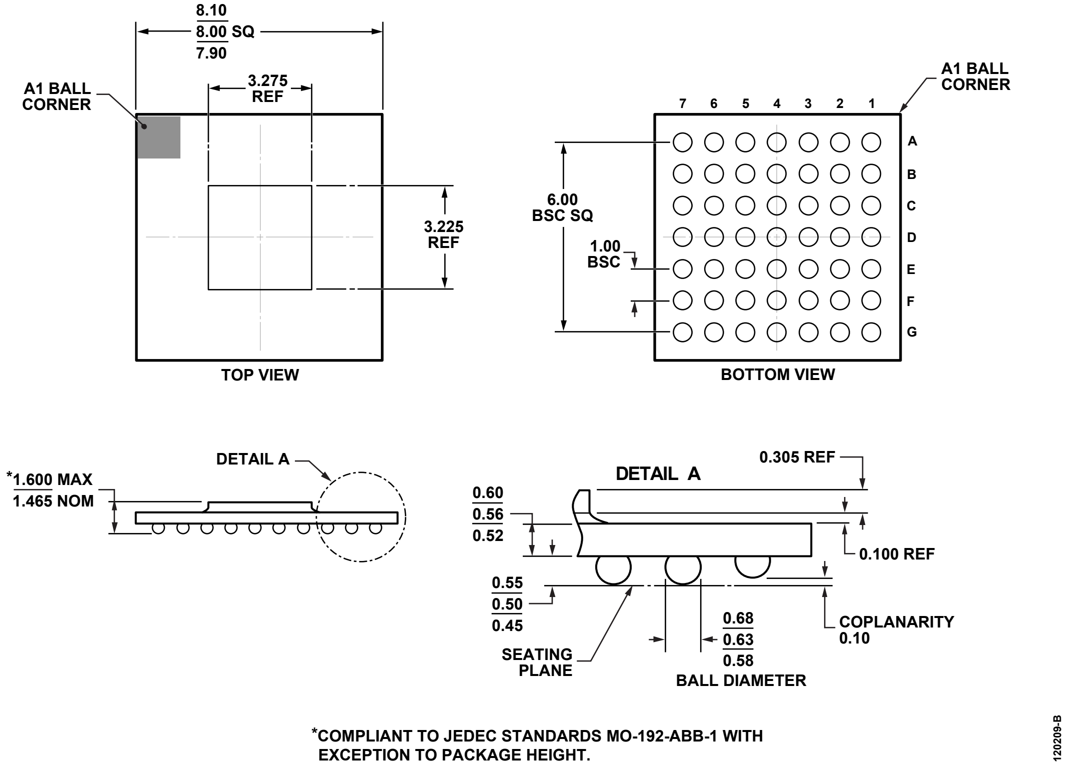
DEFAULT TEST CONDITIONS

Table 8 lists the default test conditions.

Table 8.

Name	Default Test Condition
DB1/DB1B	Logic high
DB2/DB2B	Logic high
DA1T/DA2T/DB1T/DB2T	1.3 V
VHx	2.0 V
VLx	0.0 V
VTx	1.0 V

OUTLINE DIMENSIONS



*COMPLIANT TO JEDEC STANDARDS MO-192-ABB-1 WITH EXCEPTION TO PACKAGE HEIGHT.

Figure 33. 49-Ball Chip Scale Package Ball Grid Array [CSP_BGA] (BC-49-4) Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADATE209BBCZ	−40°C to +85°C	49-Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-49-4
EVAL-ADATE209BBCZ		Evaluation Board	

[1] Z = RoHS Compliant Part.