“Ultra-Low Jitter Oscillators”
ASG-ULJ Series

ABRACON® LLC
The Power of Linking Together

Ideal for **High Data Rate Applications**

Test & Measurement

- Spectrum analyzers
- Oscilloscopes
- ATE

High Speed Networking

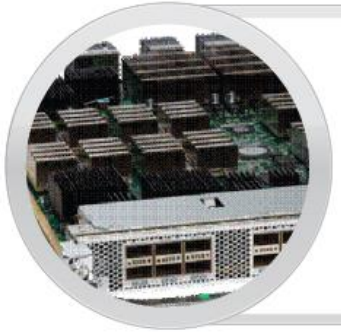
- 10/40/100/400 Gigabit Ethernet
- High port count switches

Wireless Infrastructure

- High speed back haul
- Base stations (BTS)
- RF Data converters

Medical Imaging

- High resolution endoscopy
- MRI



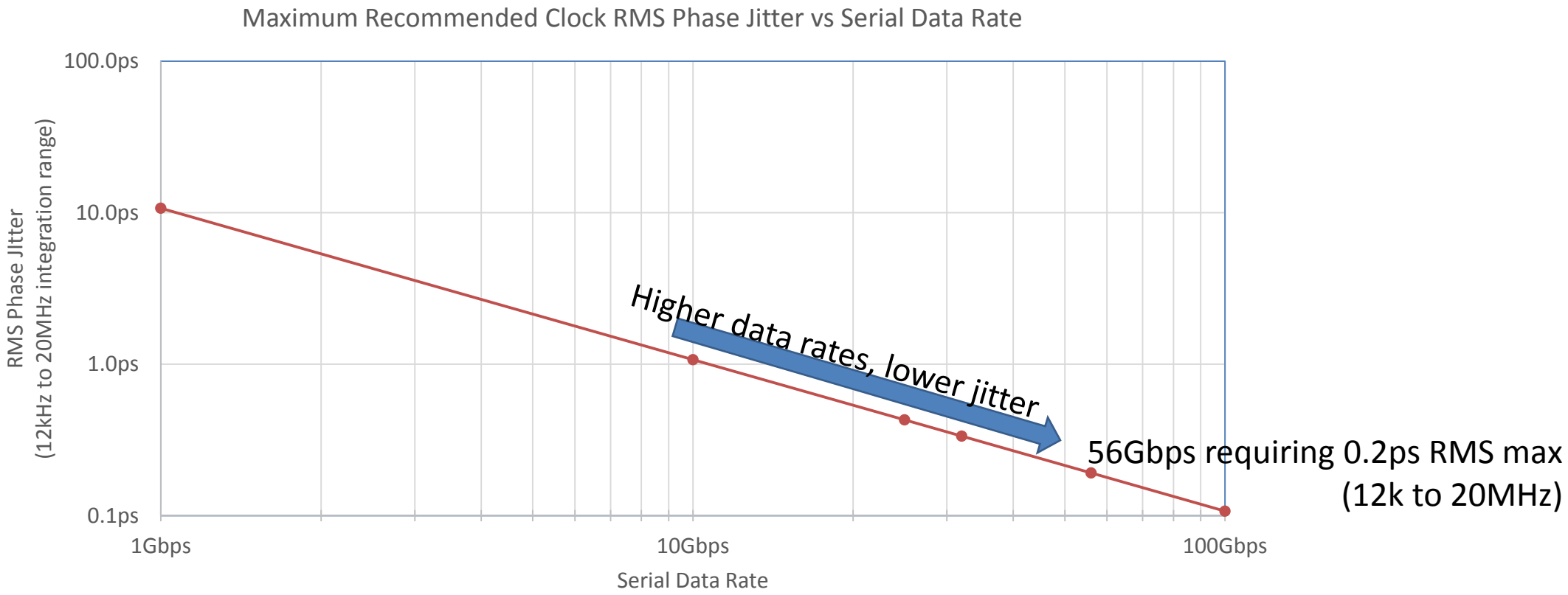
Storage

- Storage Area Networks
- 32Gbps Fibre Channel
- Network Attached Storage

Server

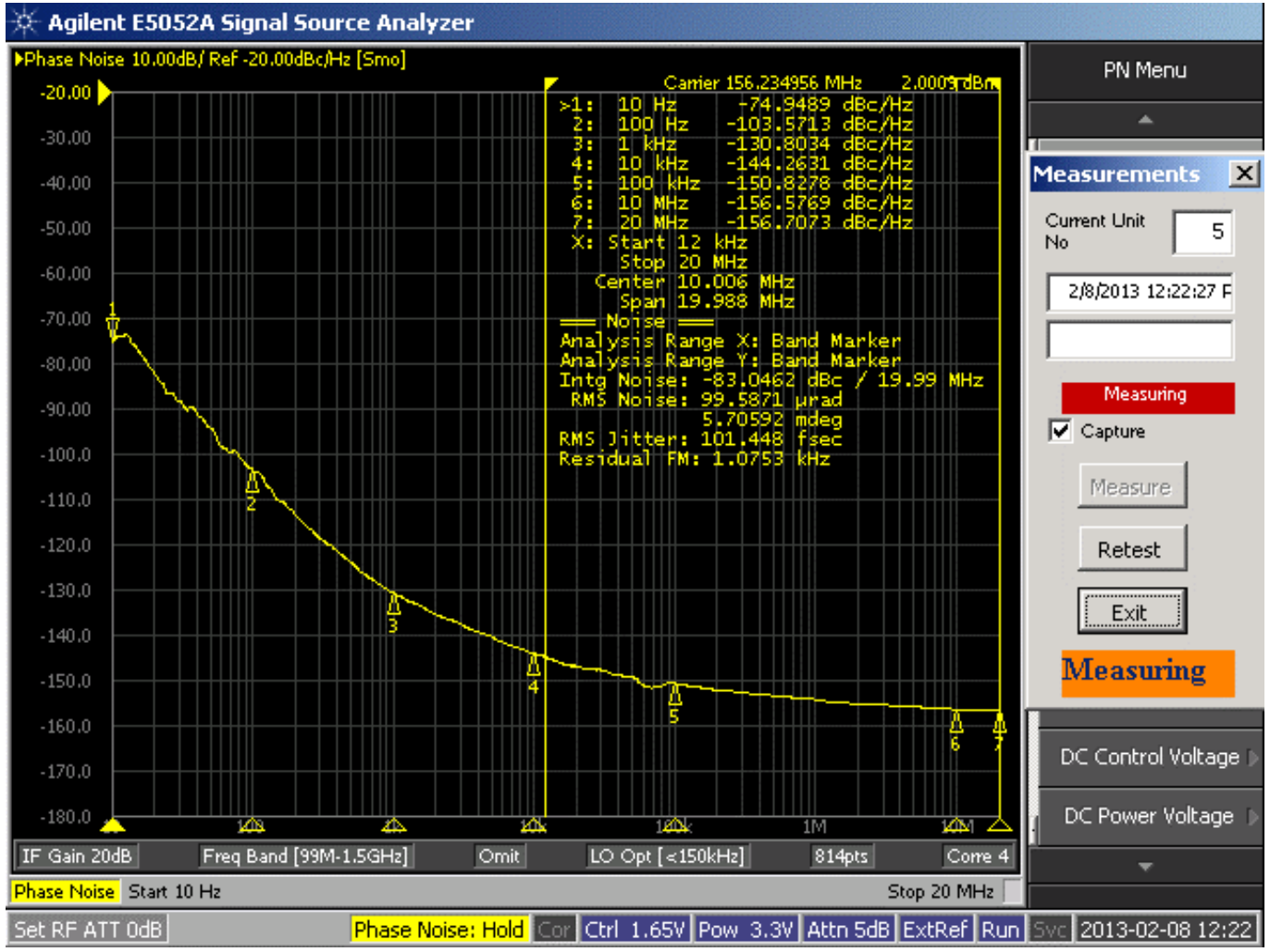
- High speed interconnect
- FPGA accelerator add-on cards

Challenge: Maintain low BER while bit rates double or quadruple



- Higher data rates demand lower clock jitter to **maintain low bit error rate (BER)**
- Excessive or undeterminable clock jitter **induces failures** and usually **increases design and debug time**

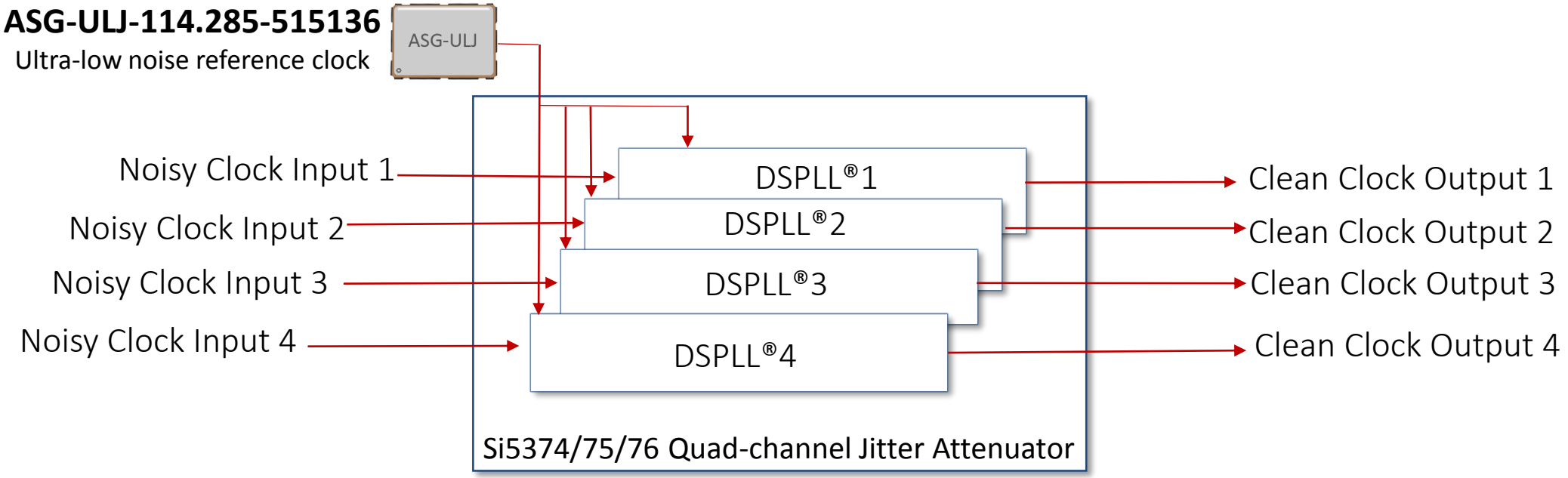
Solution: **0.15ps Guaranteed Jitter ASG-ULJ minimizes BER**



- Delivering a max output jitter specification takes the guesswork out of the design providing **guaranteed guard banding** that ensures **reliable system margin**
- **150fsec MAX** RMS phase jitter, typically 102fsec at 156.25MHz (12kHz to 20MHz integration bandwidth)
- **Improve system performance** and **readily migrate to next data rate** without extensive clock design challenges
- **Small 5 x 7mm footprint** saves PCB space compared to other ultra performance oscillators

Application: Reference Clock for Precision Jitter Attenuators

ASG-ULJ-114.285-515136
Ultra-low noise reference clock



- Ideal companion **ultra-low noise reference clock** required by multi-channel precision jitter attenuators
- Jitter attenuator **relies on ultra-low jitter clock source to remove noise** from incoming clock signals
- **Small 5 x 7mm** footprint saves space

ASG-ULJ Guaranteed Ultra-Low Jitter XOs

- Guaranteed phase jitter delivers predictable performance
  - 150fs MAX at 156.25MHz (12kHz to 20MHz)
  - 100fs MAX at 705.8MHz (12kHz to 20MHz)
- 1MHz to 705.8MHz output frequency range
- LVDS/LVPECL options supported
- LVCMOS output supports up to 200MHz
- Space saving 5x7mm footprint
- Low 40mA MAX IDD when using CMOS output, 190MHz
- 2.5V or 3.3V operation
- +/-50PPM total, +/-35PPM temperature stability
- -40C to 85C operating temperature range

5 x 7mm

ASG - ULJ - [ ] MHz - [ ] - [ ]

Frequency	Configuration Code	Packaging
See Table below for available frequencies	See Table below for available configurations	Blank = Bulk T = Tape & Reel(2k/reel) T2 = Tape & Reel(250/reel)

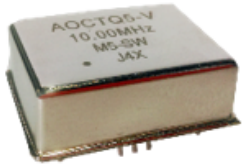
Available Configurations - Contact Abracon for Additional Options

Abracon P/N	Frequency (MHz)	Overall Freq. Stability max (1) (ppm)	Operating Temperature (°C)	Aging (years)	RMS Jitter max (2) (ps)	Supply Voltage (V)	Supply Current max. (mA)	Output Type
ASG-ULJ-156.250MHz-514613	156.250	±50	-40 to +85	10	0.15	3.3	75	LVPECL
ASG-ULJ-190.000MHz-514594	190.000	±50	-40 to +85	10	0.15 (12kHz to 5MHz BW)	3.3	40	LVCMOS
ASG-ULJ-156.250MHz-514644	156.250	±50	-40 to +85	10	0.15	2.5	75	LVPECL
ASG-ULJ-705.800MHz-514676	705.800	±50	-40 to +85	10	0.10	3.3	85	LVPECL
ASG-ULJ-100.000MHz-514895	100.000	±50	-40 to +85	10	0.15	2.5	75	LVPECL
ASG-ULJ-114.285MHz-515136	114.285	±25	-40 to +85	5	0.10 (12kHz to 5MHz BW)	3.3	30	LVCMOS
ASG-ULJ-156.250MHz-514804	156.250	±35	-40 to +85	10	0.15	3.3	75	LVPECL
ASG-ULJ-125.000MHz-514807	125.000	±35	-40 to +85	10	0.20	3.3	75	LVPECL

Note:

- Inclusive of initial tolerance at 25ºC±3ºC, operating temperature range, input voltage variation, load variation & aging at 25ºC.
- RMS Jitter Max is defined over 12kHz to 20MHz BW from the carrier at 25ºC, unless otherwise specified
- Please contact Abracon for the availability of other configurations
- 125MHz output frequency typically supports less 0.15ps MAX RMS jitter

XO- Ultra-Low Jitter for High Bandwidth Applications

Product Series	 ASG-ULJ	 ABLNO	 AOCTQ5
Size	7.0 x 5.0 x 1.5 mm	14.3 x 8.7 x 5.5mm	36.1 x 27.1 x 12.1 mm
Feature	Guaranteed 0.15fs RMS jitter	Lowest jitter—70fs typ	0.5ppb/day aging -145dBc/Hz at 1kHz offset
Benefit	Predictable, simplified design	Minimizes BER and SNR	– Enables extended holdover – Optimizes RF spectrum use
Applications	– Ref clock for jitter attenuators – Serdes or D/A, A/D reference	-RF and basestations	– Low noise holdover reference – RF local oscillator reference
Carrier frequency		100MHz	
		52fs	

THANK YOU!

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