SY100S834/SY100S834L

(÷1, ÷2, ÷4) or (÷2, ÷4, ÷8) Clock Generation Chip

Precision Edge®

General Description

The SY100S834/L is low skew (÷1, ÷2, ÷4) or (÷2, ÷4, ÷8) clock generation chip designed explicitly for low skew clock generation applications. The internal dividers are synchronous to each other, therefore, the common output edges are all precisely aligned. The devices can be driven by either a differential or single-ended ECL or, if positive power supplies are used, PECL input signal. In addition, by using the VBB output, a sinusoidal source can be AC-coupled into the device. If a single-ended input is to be used, the VBB output should be connected to the CLK input and bypassed to ground via a 0.01µF capacitor. The VBB output is designed to act as the switching reference for the input of the SY100S834/L under single-ended input conditions. As a result, this pin can only source/sink up to 0.5mA of current.

The Function Select (FSEL) input is used to determine what clock generation chip function is. When FSEL input is LOW, SY100S834/L functions as a divide by 2, by 4 and by 8 clock generation chip. However, if FSEL input is HIGH, it functions as a divide by 1, by 2 and by 4 clock generation chip. This latter feature will increase the clock frequency by two folds.

The common enable (EN) is synchronous so that the internal dividers will only be enabled/disabled when the internal clock is already in the LOW state. This avoids any chance of generating a runt clock pulse on the internal clock when the device is enabled/disabled as can happen with an asynchronous control. An internal runt pulse could lead to losing synchronization between the internal divider stages. The internal enable flip-flop is clocked on the falling edge of the input clock, therefore, all associated specification limits are referenced to the negative edge of the clock input.

Upon start-up, the internal flip-flops will attain a random state; the master reset (MR) input allows for the synchronization of the internal dividers, as well as for multiple SY100S834/Ls in a system.

Data sheets and support documentation can be found on Micrel's web site at www.micrel.com.

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Features

- 3.3V (SY100S834L) and 5V (SY100S834) power supply options
- 50ps output-to-output skew
- Synchronous enable/disable
- Master reset for synchronization
- Internal 75KΩ input pulldown resistors
- Available in 16-pin SOIC package

Truth Table

CLK	$\overline{EN}$	MR	Function
Z	L	L	Divide
ZZ	H	L	Hold Q_{0-2}
X	X	H	Reset Q_{0-2}

Notes:

Z = LOW-to-HIGH transition.

ZZ = HIGH-to-LOW transition.

F_{SEL}	Q_0 Outputs	Q_1 Outputs	Q_2 Outputs
L	Divide by 2	Divide by 4	Divide by 8
H	Divide by 1	Divide by 2	Divide by 4

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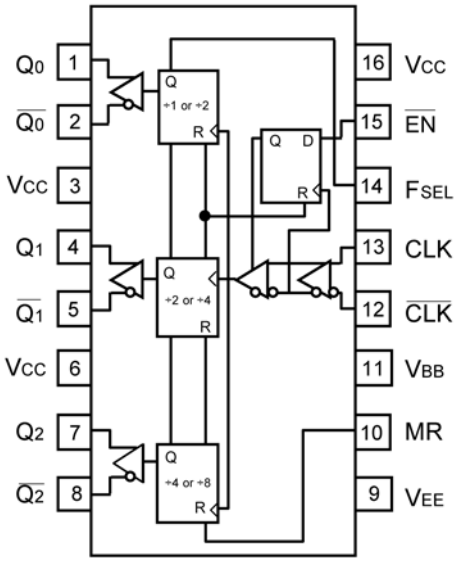
Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY100S834ZC	Z16-2	Commercial	SY100S834ZC	Sn-Pb
SY100S834ZCTR[1]	Z16-2	Commercial	SY100S834ZC	Sn-Pb
SY100S834LZC	Z16-2	Commercial	SY100S834LZC	Sn-Pb
SY100S834LZCTR[1]	Z16-2	Commercial	SY100S834LZC	Sn-Pb
SY100834ZI	Z16-2	Industrial	SY100S834ZI	Sn-Pb
SY100834ZITR[1]	Z16-2	Industrial	SY100S834ZI	Sn-Pb
SY100834LZI	Z16-2	Industrial	SY100S834LZI	Sn-Pb
SY100834LZITR[1]	Z16-2	Industrial	SY100S834LZI	Sn-Pb
SY100834ZG[2]	Z16-2	Industrial	SY100S834ZG with Pb-Free bar-line indicator	NiPdAu Pb-Free
SY100834ZGTR[1, 2]	Z16-2	Industrial	SY100S834ZG with Pb-Free bar-line indicator	NiPdAu Pb-Free
SY100834LZG[2]	Z16-2	Industrial	SY100S834LZG with Pb-Free bar-line indicator	NiPdAu Pb-Free
SY100834LZGTR[1, 2]	Z16-2	Industrial	SY100S834LZG with Pb-Free bar-line indicator	NiPdAu Pb-Free

Notes:

1. Tape and reel.
2. Pb-Free package is recommended for new designs.

Pin Configuration



16-Pin SOIC (Z16-2)

Pin Description

Pin Name	Pin Function
CLK	Differential clock inputs.
F_{SEL}	Function select, single-sided ECL logic.
$\overline{EN}$	Synchronous enable, single-sided ECL logic.
MR	Master reset, single-sided ECL logic.
V_{BB}	Reference output.
Q0	Differential ÷1 or ÷2 outputs.
Q1	Differential ÷2 or ÷4 outputs.
Q2	Differential ÷4 or ÷8 outputs.

3.3V PECL Output DC Electrical Characteristics[1]

V_{CC} = 3.3V ±10%; R_L = 50Ω to V_{CC} –2V; V_{EE} = GND.

Symbol	Parameter	T_A = –40°C			T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{EE}	Power Supply Current	–	–	49	–	–	49	–	–	49	–	–	54	mA
V_{CH}	Output HIGH Voltage	2.215	2.295	2.42	2.275	2.235	2.42	2.275	2.345	2.42	2.275	2.345	2.42	V
V_{OL}	Output LOW Voltage	1.47	1.605	1.745	1.49	1.595	1.68	1.49	1.595	1.68	1.49	1.595	1.68	V
V_{IH}	Input HIGH Voltage	2.135	–	2.42	2.135	–	2.42	2.135	–	2.42	2.135	–	2.42	V
V_{IL}	Input LOW Voltage	1.49	–	1.825	1.49	–	1.825	1.49	–	1.825	1.49	–	1.825	V
V_{BB}	Output Reference Voltage	1.92	–	2.04	1.92	–	2.04	1.92	–	2.04	1.92	–	2.04	V
V_{CMR}	Common Mode Range[2]	2	–	2.9	1.9	–	2.9	1.9	–	2.9	1.9	–	2.9	V
I_{IH}	Input HIGH Current	–	–	150	–	–	150	–	–	150	–	–	150	µA
I_{IL}	Input LOW Current	0.5	–	–	0.5	–	–	0.5	–	–	0.5	–	–	µA

Notes:

1. These values are for V_{CC} = 3.3V. Level specifications will vary 1:1 with V_{CC}.
2. The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP} (min.) and 1V. The lower end of the CMR range varies 1:1 with V_{EE}. Note for PECL operation that the V_{CMR} (min.) will be fixed at 3.3V – IV_{CMR} (min.)I.

5V PECL Output DC Electrical Characteristics[2]

V_{CC} = 3.3V ±10%; R_L = 50Ω to V_{CC} –2V; V_{EE} = GND.

Symbol	Parameter	T_A = –40°C			T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{EE}	Power Supply Current	–	–	49	–	–	49	–	–	49	–	–	54	mA
V_{CH}	Output HIGH Voltage	3.915	3.995	4.12	3.975	4.045	4.12	3.975	4.045	4.12	3.975	4.045	4.12	V
V_{OL}	Output LOW Voltage	3.17	3.305	3.445	3.19	3.295	3.38	3.19	3.295	3.38	3.19	3.295	3.38	V
V_{IH}	Input HIGH Voltage	3.835	–	4.12	3.835	–	4.12	3.835	–	4.12	3.835	–	4.12	V
V_{IL}	Input LOW Voltage	3.19	–	3.525	3.19	–	3.525	3.19	–	3.525	3.19	–	3.525	V
V_{BB}	Output Reference Voltage	3.62	–	3.74	3.62	–	3.74	3.62	–	3.74	3.62	–	3.74	V
V_{CMR}	Common Mode Range[2]	2	–	4.6	1.9	–	4.6	1.9	–	4.6	1.9	–	4.6	V
I_{IH}	Input HIGH Current	–	–	150	–	–	150	–	–	150	–	–	150	µA
I_{IL}	Input LOW Current	0.5	–	–	0.5	–	–	0.5	–	–	0.5	–	–	µA

Notes:

1. These values are for V_{CC} = 5V. Level specifications will vary 1:1 with V_{CC}.
2. The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP} (min.) and 1V. The lower end of the CMR range varies 1:1 with V_{EE}. Note for PECL operation that the V_{CMR} (min.) will be fixed at 3.3V – IV_{CMR} (min.)I.

NECL Output DC Electrical Characteristics

V_{CC} = GND; R_L = 50Ω to V_{CC} –2V; V_{EE} = –3.0V to –5.5V.

Symbol	Parameter	T_A = –40°C			T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{EE}	Power Supply Current	–	–	49	–	–	49	–	–	49	–	–	54	mA
V_{CH}	Output HIGH Voltage	–1085	–1005	–880	–1025	–955	–880	–1025	–955	–880	–1025	–955	–880	V
V_{OL}	Output LOW Voltage	–1830	–1695	–1555	–1830	–1705	–1620	–1810	–1705	–1620	–1810	–1705	–1620	V
V_{IH}	Input HIGH Voltage	–1165	–	–880	–1165	–	–880	–1165	–	–880	–1165	–	–880	V
V_{IL}	Input LOW Voltage	–1810	–	–1475	–1810	–	–1475	–1810	–	–1475	–1810	–	–1475	V
V_{BB}	Output Reference Voltage	–1.38	–	–1.26	–1.38	–	–1.26	–1.38	–	–1.26	–1.38	–	–1.26	V
V_{CMR}	Common Mode Range[1]	–1.3	–	–0.4	–1.4	–	–0.4	–1.4	–	–0.4	–1.4	–	–0.4	V
I_{IH}	Input HIGH Current	–	–	150	–	–	150	–	–	150	–	–	150	µA
I_{IL}	Input LOW Current	0.5	–	–	0.5	–	–	0.5	–	–	0.5	–	–	µA

Note:

1. The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP} (min.) and 1V. The lower end of the CMR range varies 1:1 with V_{EE}. The numbers in the spec table assume a nominal V_{EE} = –3.3V. Note for PECL operation, the V_{CMR} (min.) will be fixed at 3.3V – IV_{CMR} (min.)I.

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AC Electrical Characteristics[1]

V_{EE} = V_{EE} (min.) to V_{EE} (max.); V_{CC} = GND.

Symbol	Parameter	T_A = –40°C			T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{PLH}	Propagation Delay to Output CLK	960	1100	1200	960	1100	1200	960	1100	1200	960	1100	1200	ps
t_{PHL}	MR	650	800	1010	650	800	1010	650	800	1010	650	800	1010	ps
t_{SKEW}	Within-Device Skew[2]	–	–	50	–	–	50	–	–	50	–	–	50	ps
t_S	Set-Up Time $\overline{EN}$	400	–	–	400	–	–	400	–	–	400	–	–	ps
t_H	Hold Time $\overline{EN}$	200	–	–	200	–	–	200	–	–	200	–	–	ps
V_{PP}	Minimum Input Swing	250	–	–	250	–	–	250	–	–	250	–	–	mV
tr tf	Output Rise/Fall Times Q (20% – 80%)	275	400	525	275	400	525	275	400	525	275	400	525	ps

Notes:

1. Parametric values specified at:
   - 5V power supply range, 100S834 series: –4.2V to –5.5V
   - 3V power supply range, 100S834L series: –3.0V to –3.8V
2. Within-Device Skew is specified for identical transition.

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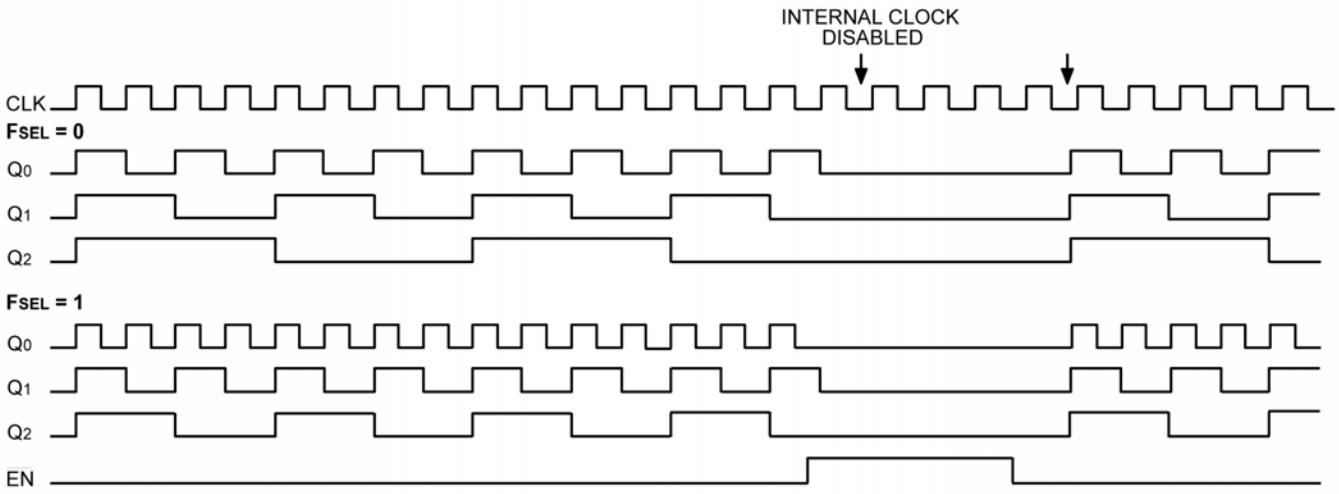
Timing Diagram



The $\overline{EN}$ signal will freeze the internal clocks to the flip-flops on the first falling edge of CLK after its assertion. The internal dividers will maintain their state during the internal clock freeze and will return to clocking once the internal clocks are unfrozen. The outputs will transition to their next states in the same manner, time, and relationship as they would have had the $\overline{EN}$ signal not been asserted.

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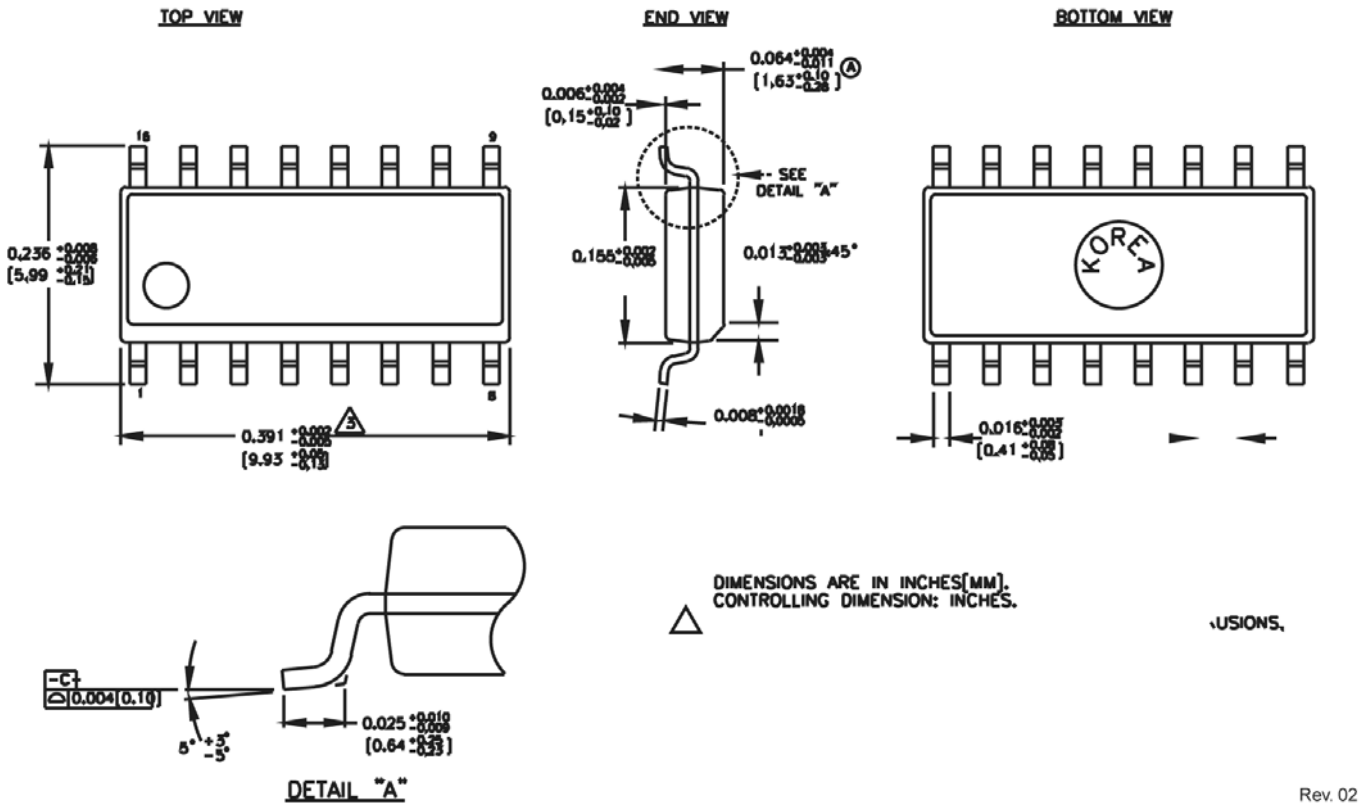
Package Information



xx-Pin Package Type (code)

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