



# STB160N75F3 STP160N75F3 - STW160N75F3

N-channel 75V - 3.5mΩ - 120A - TO-220 - TO-247 - D<sup>2</sup>PAK  
STripFET™ Power MOSFET

## Features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub> (max.)	I <sub>D</sub>
STB160N75F3	75V	3.7 mΩ	120 A <sup>(1)</sup>
STP160N75F3	75V	4 mΩ	120 A <sup>(1)</sup>
STW160N75F3	75V	4 mΩ	120 A <sup>(1)</sup>

1. Current limited by package

- Ultra low on-resistance
- 100% Avalanche tested

## Application

- Switching applications

## Description

This N-channel enhancement mode Power MOSFET is the latest refinement of ST's STripFET™ process. The resulting transistor shows extremely high packing density for low on resistance, rugged avalanche characteristics and low gate charge.

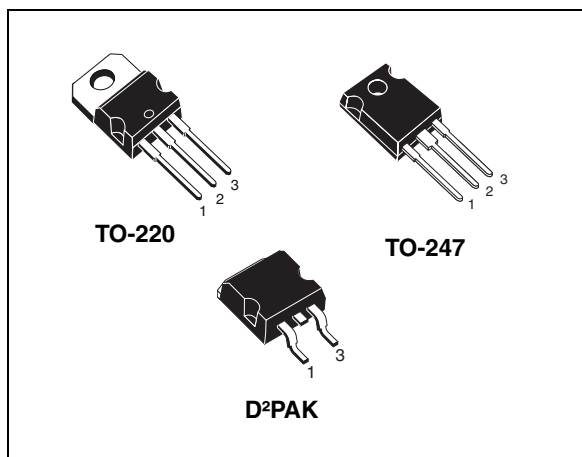


Figure 1. Internal schematic diagram

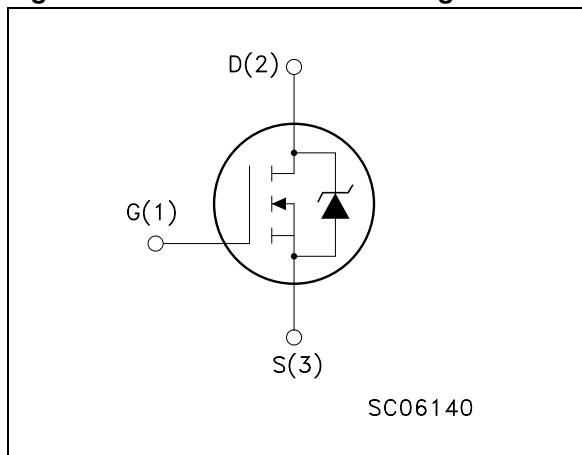


Table 1. Device summary

Order codes	Marking	Package	Packaging
STB160N75F3	160N75F3	D <sup>2</sup> PAK	Tape & reel
STP160N75F3	160N75F3	TO-220	Tube
STW160N75F3	160N75F3	TO-247	Tube

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	75	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	120	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	120	A
$I_{DM}^{(2)}$	Drain current (pulsed)	480	A
$P_{TOT}$	Total dissipation at $T_C = 25^\circ\text{C}$	330	W
	Derating factor	2.2	W/ $^\circ\text{C}$
$dv/dt^{(3)}$	Peak diode recovery voltage slope	20	V/ns
$E_{AS}^{(4)}$	Single pulse avalanche energy	600	mJ
$T_j$ $T_{stg}$	Operating junction temperature Storage temperature	-55 to 175	$^\circ\text{C}$

1. Current limited by package
2. Pulse width limited by safe operating area
3.  $I_{SD} \leq 120\text{A}$ ,  $di/dt \leq 1100\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq 60\text{V}$ ,  $T_J \leq T_{JMAX}$
4. Starting  $T_J = 25^\circ\text{C}$ ,  $I_D = 60\text{A}$ ,  $V_{DD} = 25\text{V}$

**Table 3. Thermal resistance**

Symbol	Parameter	Value			Unit
		TO-220	TO-247	D <sup>2</sup> PAK	
$R_{thj-case}$	Thermal resistance junction-case max	0.45			$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.5	50	--	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	--	--	50	$^\circ\text{C}/\text{W}$
$T_l$	Maximum lead temperature for soldering purpose	300			$^\circ\text{C}$

1. When mounted on 1 inch<sup>2</sup> FR4 2 oz Cu

## 2 Electrical characteristics

( $T_{CASE}=25^{\circ}C$  unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\mu A, V_{GS} = 0$	75			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max rating},$ $V_{DS} = \text{Max rating}, @ 125^{\circ}C$			10 100	$\mu A$ $\mu A$
$I_{GSS}$	Gate body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20V$			$\pm 200$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	2		4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10V, I_D = 60A$		3.5 3.2	4 3.7	$m\Omega$ $m\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 25V, f = 1 \text{ MHz}, V_{GS} = 0$		6750		pF
$C_{oss}$	Output capacitance			1080		pF
$C_{rss}$	Reverse transfer capacitance			40		pF
$Q_g$	Total gate charge	$V_{DD} = 37.5V, I_D = 120A$		85		nC
$Q_{gs}$	Gate-source charge	$V_{GS} = 10V$		27		nC
$Q_{gd}$	Gate-drain charge	(see Figure 16)		26		nC

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD}=37.5\text{ V}$ , $I_D=60\text{ A}$ , $R_G=4.7\Omega$ , $V_{GS}=10\text{ V}$ , (see Figure 18)		22		ns
$t_r$	Rise time			65		ns
$t_{d(off)}$	Turn-off delay time			100		ns
$t_f$	Fall time			15		ns

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current				120	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				480	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=120\text{ A}$ , $V_{GS}=0$			1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD}=120\text{ A}$ , $V_{DD}=20\text{ V}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $T_j=25^\circ\text{C}$ (see Figure 17)		70		ns
$Q_{rr}$	Reverse recovery charge			150		nC
$I_{RRM}$	Reverse recovery current			4.2		A

1. Pulse with limited by safe operating area
2. Pulsed: pulse duration = 300 $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220 / TO-247

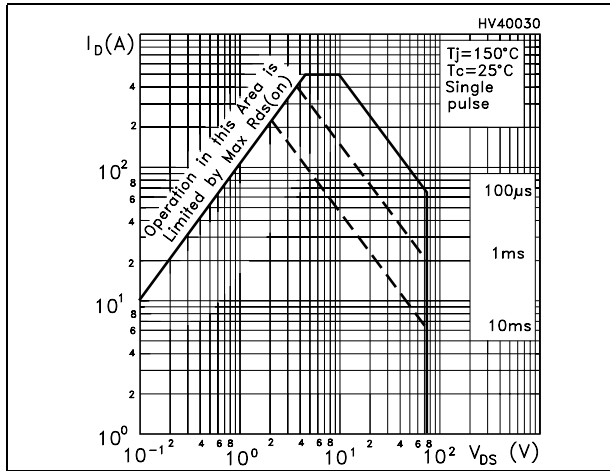


Figure 3. Thermal impedance for TO-220 / TO-247

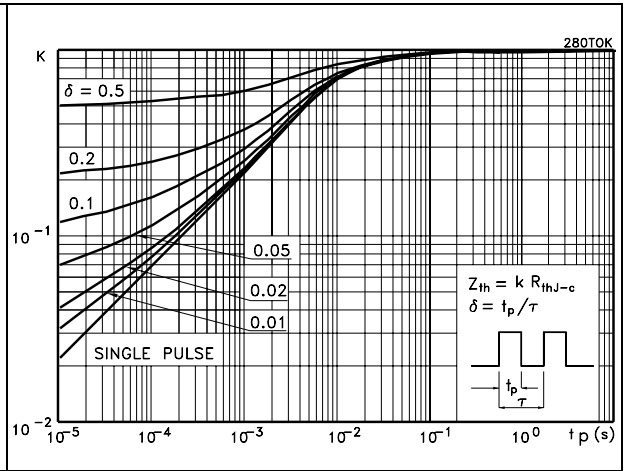


Figure 4. Safe operating area for D<sup>2</sup>PAK

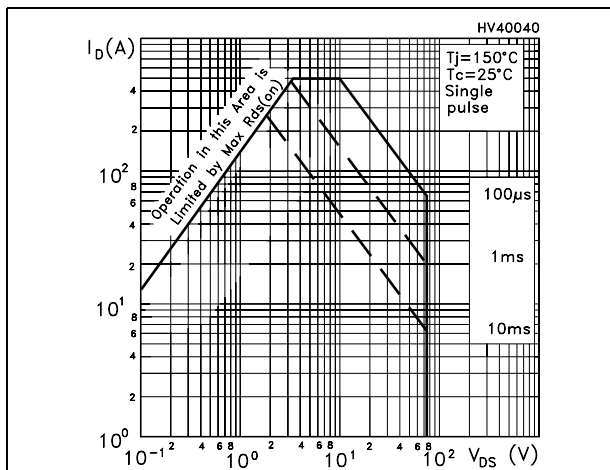


Figure 5. Thermal impedance for D<sup>2</sup>PAK

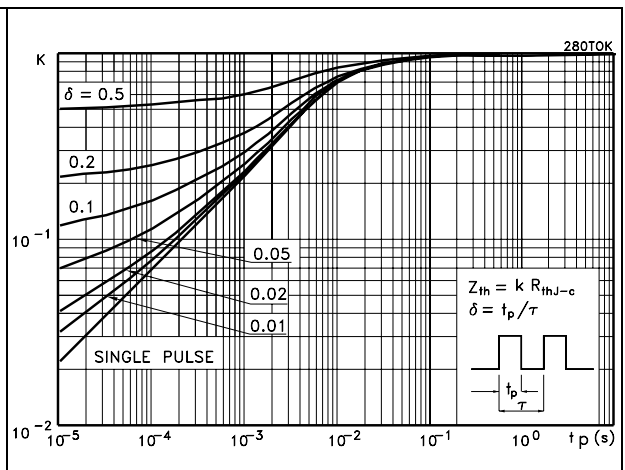


Figure 6. Output characteristics

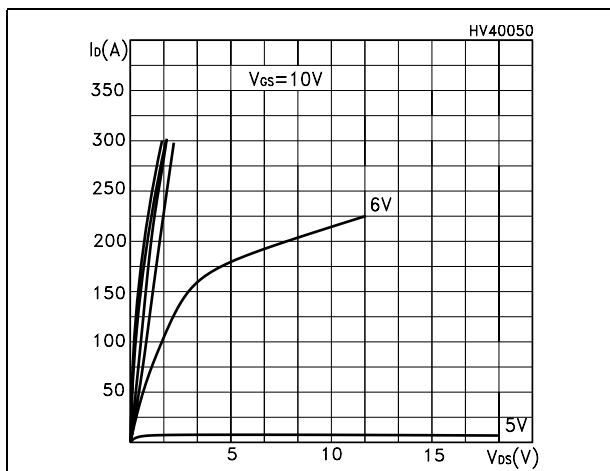


Figure 7. Transfer characteristics

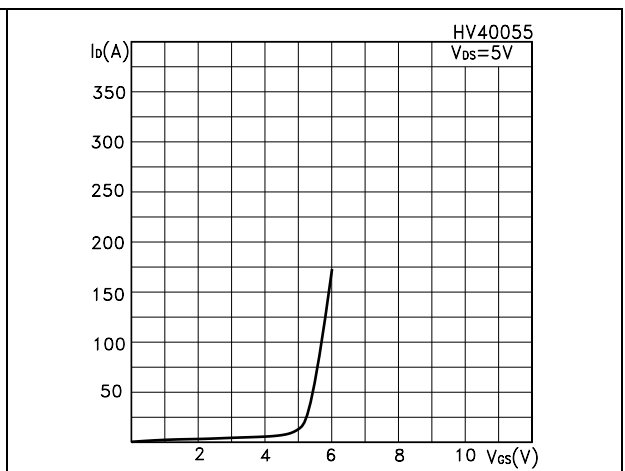


Figure 8. Normalized  $BV_{DSS}$  vs temperature      Figure 9. Static drain-source on resistance

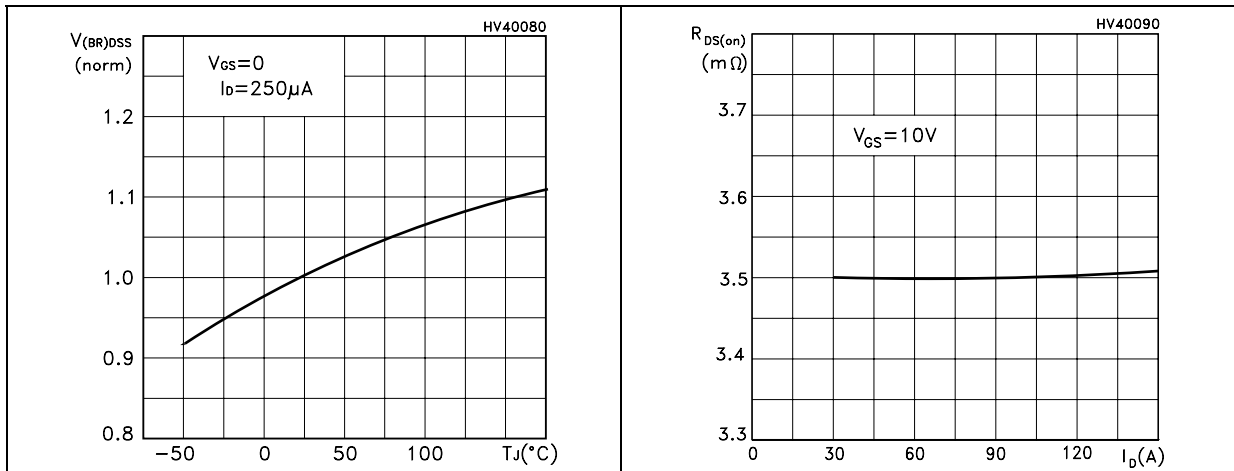


Figure 10. Gate charge vs gate-source voltage      Figure 11. Capacitance variations

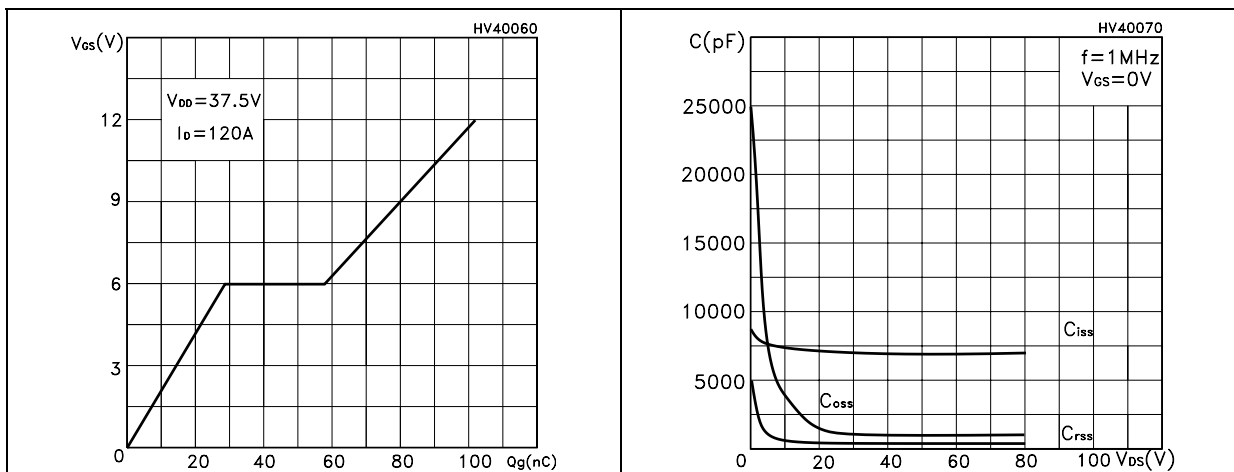


Figure 12. Normalized gate threshold voltage vs temperature      Figure 13. Normalized on resistance vs temperature

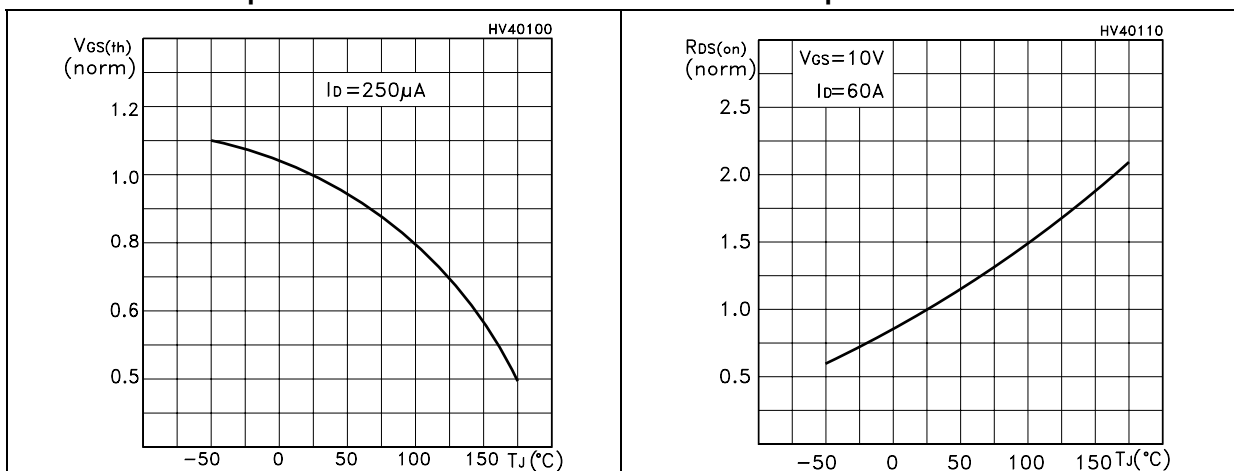
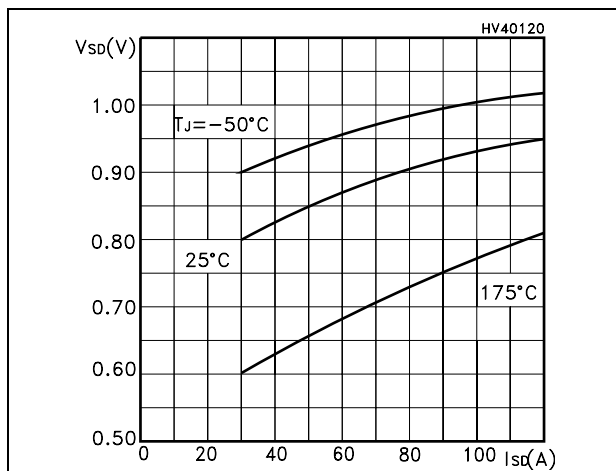


Figure 14. Source-drain diode forward characteristics





### 3 Test circuit

Figure 15. Switching times test circuit for resistive load

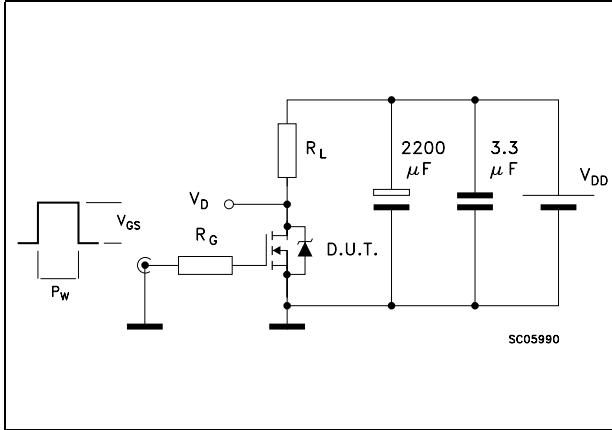


Figure 16. Gate charge test circuit

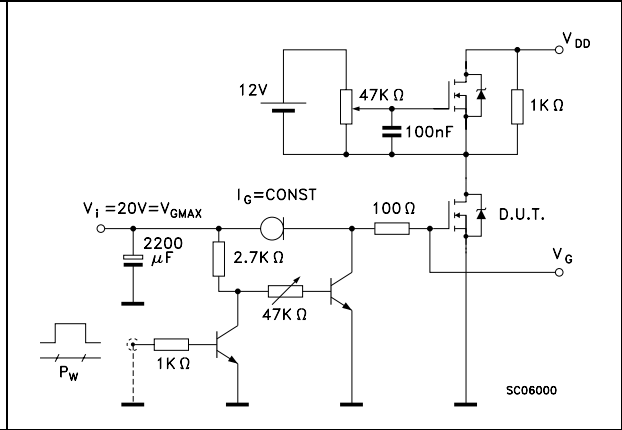


Figure 17. Test circuit for inductive load switching and diode recovery times

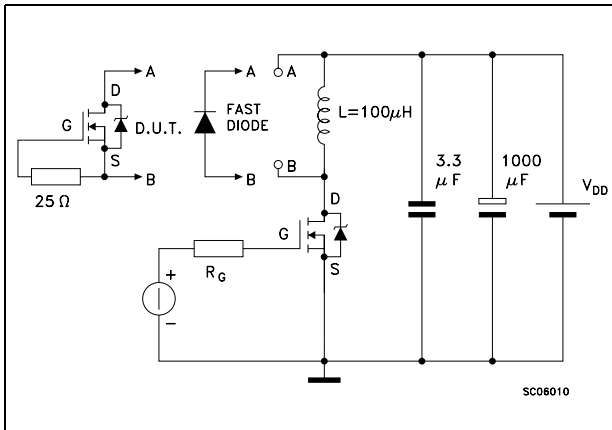


Figure 18. Unclamped inductive load test circuit

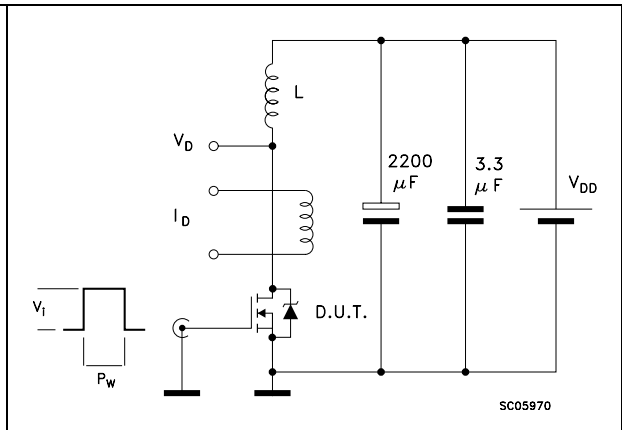


Figure 19. Unclamped inductive waveform

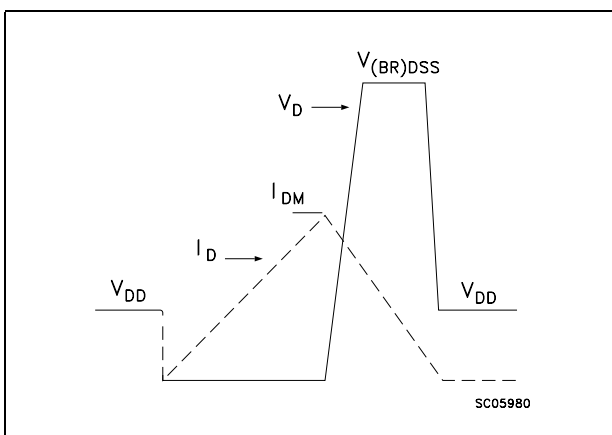
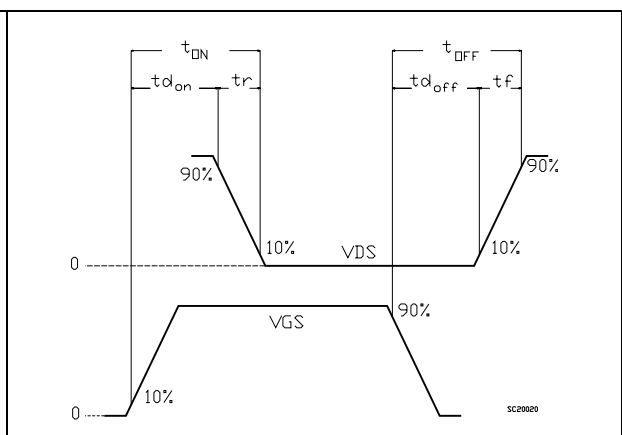


Figure 20. Switching time waveform

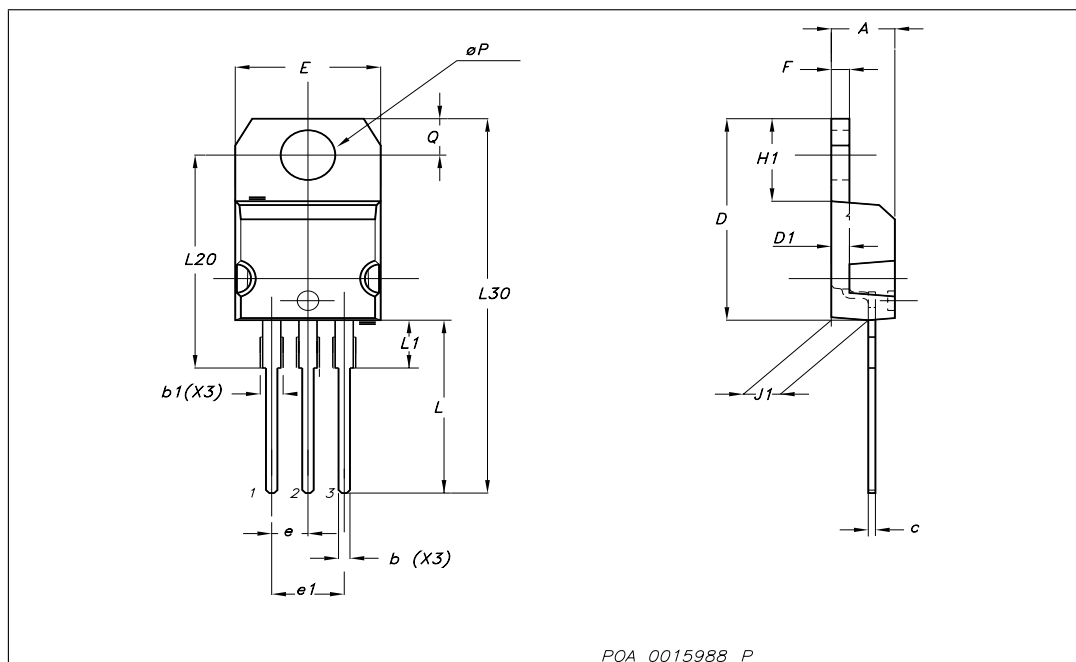


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

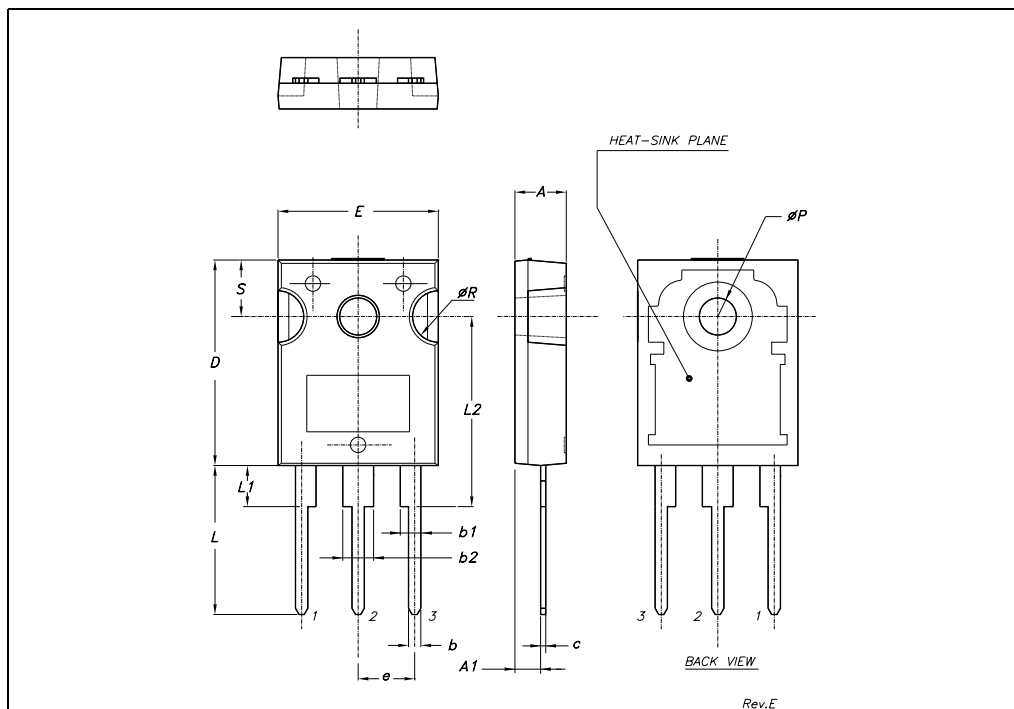
## TO-220 mechanical data

Dim	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.14		1.70	0.044		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.6		0.62
D1		1.27			0.050	
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.051
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
∅P	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



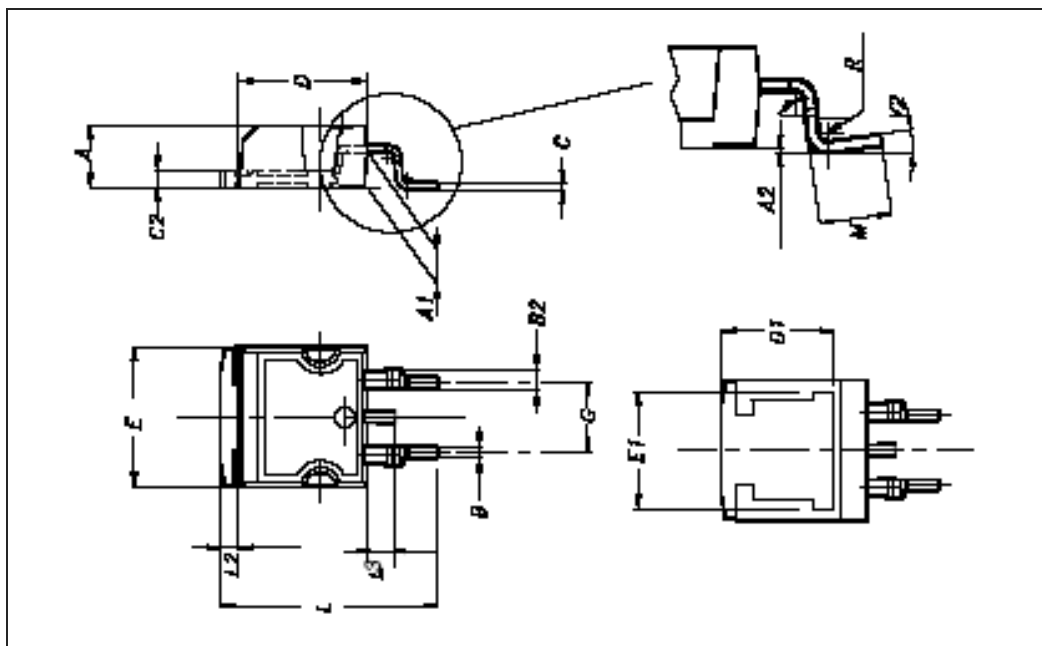
**TO-247 MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.85		5.15	0.19		0.20
A1	2.20		2.60	0.086		0.102
b	1.0		1.40	0.039		0.055
b1	2.0		2.40	0.079		0.094
b2	3.0		3.40	0.118		0.134
c	0.40		0.80	0.015		0.03
D	19.85		20.15	0.781		0.793
E	15.45		15.75	0.608		0.620
e		5.45			0.214	
L	14.20		14.80	0.560		0.582
L1	3.70		4.30	0.14		0.17
L2		18.50			0.728	
øP	3.55		3.65	0.140		0.143
øR	4.50		5.50	0.177		0.216
S		5.50			0.216	



D<sup>2</sup>PAK mechanical data

Dim	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		0.409
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.50		0.55
L3	1.4		1.75	0.055		0.68
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		4°			



# 5 Packaging mechanical data

## D<sup>2</sup>PAK FOOTPRINT



## TAPE AND REEL SHIPMENT

**TAPE MECHANICAL DATA**

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	10.5	10.7	0.413	0.421
B0	15.7	15.9	0.618	0.626
D	1.5	1.6	0.059	0.063
D1	1.59	1.61	0.062	0.063
E	1.65	1.85	0.065	0.073
F	11.4	11.6	0.449	0.456
K0	4.8	5.0	0.189	0.197
P0	3.9	4.1	0.153	0.161
P1	11.9	12.1	0.468	0.476
P2	1.9	2.1	0.075	0.082
R	50		1.574	
T	0.25	0.35	0.0098	0.0137
W	23.7	24.3	0.933	0.956

**REEL MECHANICAL DATA**

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	24.4	26.4	0.960	1.039
N	100		3.937	
T		30.4		1.197

BASE QTY	BULK QTY
1000	1000

10 pitches cumulative tolerance on tape +/- 0.2 mm

Center line of cavity

User Direction of Feed

FEED DIRECTION

Bending radius R min.

\* on sales type

## 6 Revision history

Table 8. Document revision history

Date	Revision	Changes
07-Feb-2007	1	First release
02-Oct-2007	2	New section has been added: <a href="#">Electrical characteristics (curves)</a>

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