19-4745; Rev 2; 1/10

EVALUATION KIT AVAILABLE

USB Host Charger Identification Analog Switch

General Description

The MAX14550E is a USB Hi-Speed analog switch with a USB host charger (dedicated charger) identification circuit. The MAX14550E supports both the USB Battery Charging Specification Revision 1.0 and a set resistor bias for Apple®-compliant devices.

The MAX14550E features a high-performance Hi-Speed USB switch with low 4pF (typ) on-capacitance and low 4Ω (typ) on-resistance. In addition, the MAX14550E features two digital inputs (CB0 and CB1) to switch between pass-through and charger modes. The USB host charger identification circuit allows a host USB port to support USB chargers with shorted D+/D- detection and to provide support for Apple-compliant devices using a resistor bias. When an Apple-compliant device is attached to the port, the MAX14550E provides the voltage from the resistor-divider. The MAX14550E uses the internal or external resistor based on the voltage at RDP. If a USB Revision 1.0-compliant device is attached, the MAX14550E connects a short across DP and DM to allow correct charger detection. The MAX14550E auto-detection circuit can be disabled and either a DP/DM short or resistor network is chosen as the default.

The MAX14550E has enhanced high electrostatic discharge (ESD) protection on the DP and DM inputs up to ±15kV Human Body Model (HBM).

The MAX14550E is available in a 10-pin (3mm x 3mm) TDFN package and is specified over the -40°C to +85°C extended temperature range.

Typical Operating Circuit appears at end of data sheet.

Features

- **USB 2.0 Hi-Speed Switching**
- **Low 4.0pF On-Capacitance**
- **Low 4.0Ω On-Resistance**
- **Ultra-Low 0.1Ω On-Resistance Flatness**
- **+2.8V to +5.5V Supply Range**
- **Ultra-Low 7µA Supply Current**
- **Automatic USB Charger Identification Circuit**
- **Optional External Resistor-Divider with Auto Selection**
- **±15kV High ESD HBM Protection on DP/DM**
- **3mm x 3mm, 10-Pin TDFN Package**

Applications

Laptops

Netbooks

Cell Phones

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX14550EETB+	-40°C to +85°C	10 TDFN-EP*	AWG

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Apple is a registered trademark of Apple, Inc.

USB Host Charger Identification Analog Switch

ABSOLUTE MAXIMUM RATINGS

V_{CC}, DP, DM, TDP, TDM, RDP, RDM, CB_ to GND ..... -0.3V to +6V
Continuous Current Into Any Terminal ..... ±30mA
Continuous Power Dissipation (T_A = +70°C)
10-Pin TDFN (derate 24.4mW/°C above +70°C) 1951mW
Thermal Resistance (Note 1)
Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 41°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ..... 9°C/W

Operating Temperature Range ..... -40°C to +85°C
Maximum Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Soldering Temperature (Reflow) ..... 260°C

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.8V to +5.5V, T_A = T_J = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Power-Supply Voltage	V_{CC}			2.8		5.5	V
Supply Current	I_{CC}	V_{CC} = 3.3V	V_{CB0} = V_{CB} = V_{CC}		0.7	2	µA
			V_{CB0} = 0V, V_{CB} = V_{CC}		6.5	10	
			External resistors used, V_{CB0} = V_{CB} = 0V or V_{CB0} = V_{CC}, V_{CB} = 0V		7	12	
			Internal resistors used, V_{CB0} = V_{CB} = 0V or V_{CB0} = V_{CC}, V_{CB} = 0V		76	120	
		V_{CC} = 5.5V	V_{CB0} = V_{CB} = V_{CC}		2.5	7	
			V_{CB0} = 0V, V_{CB} = V_{CC}		8.5	15	
			External resistors used, V_{CB0} = V_{CB} = 0V or V_{CB0} = V_{CC}, V_{CB} = 0V		9	16	
			Internal resistors used, V_{CB0} = V_{CB} = 0V or V_{CB0} = V_{CC}, V_{CB} = 0V		125	180	
Supply Current Increase	ΔI_{CC}	0V ≤ $V_{CB\_}$ ≤ V_{IL} or V_{IH} ≤ $V_{CB\_}$ ≤ V_{CC}				2	µA
Analog Signal Range	V_{DP}, V_{DM}			0		V_{CC}	V
ANALOG SWITCH							
On-Resistance TDP/TDM Switch	R_{ONT}	0V ≤ $V_{DP/DM}$ ≤ V_{CC}, I_{DP} or I_{DM} = 10mA			4	6.5	Ω
On-Resistance Match Between Channels TDP/TDM Switch	ΔR_{ONT}	V_{DP} = V_{DM} = 400mV, I_{DP} or I_{DM} = 10mA			0.1		Ω

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +2.8V to +5.5V, T_A = T_J = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
On-Resistance Flatness TDP/TDM Switch	R_{FLATT}	V_{DP} = V_{DM}, 0V ≤ V_{DP} ≤ V_{CC}, I_{DP} = I_{DM} = 10mA		0.1		Ω
On-Resistance RDP/RDM Switch	R_{ONR}	0.4V ≤ $V_{RDP/RDM}$ ≤ V_{CC}, I_{RDP} = I_{RDM} = 10mA		4	7.5	Ω
On-Resistance Flatness RDP/RDM Switch	R_{FLATR}	V_{RDP} = V_{RDM}, 0.4V ≤ V_{RDP} ≤ V_{CC}, I_{RDP} = I_{RDM} = 10mA		0.1		Ω
On-Resistance of DP/DM Short	R_{SHORT}	V_{CB0} = 0V, V_{CB} = V_{CC}, V_{DP} = V_{DM}, 0V ≤ V_{DP} ≤ V_{CC}, I_{DP} = I_{DM} = 1mA		50	70	Ω
TDP/TDM Off-Leakage Current	I_{TDPOFF}, I_{TDMOFF}	V_{CC} = 5.5V, V_{CB0} = V_{CC}, V_{CB} = 0V, V_{DP} = V_{DM} = 5.5V to 0V, V_{TDP} = V_{TDM} = 0V to 5.5V	-250		+250	nA
DP/DM On-Leakage Current	I_{DPON}, I_{DMON}	V_{CC} = 5.5V, V_{CB0} = V_{CB} = V_{CC}, V_{DP} = V_{DM} = 5.5V to 0V	-250		+250	nA
DYNAMIC PERFORMANCE						
Turn-On Time	t_{ON}	V_{TDP} or V_{TDM} = 1.5V, R_L = 300Ω, C_L = 35pF, V_{IH} = V_{CC}, V_{IL} = 0V, Figure 1		20	100	µs
Turn-Off Time	t_{OFF}	V_{TDP} or V_{TDM} = 1.5V, R_L = 300Ω, C_L = 35pF, V_{IH} = V_{CC}, V_{IL} = 0V, Figure 1		2.5	5	µs
TDP/TDM Switch Propagation Delay	t_{PLH}, t_{PHL}	R_L = R_S = 50Ω		60		ps
Output Skew Between Switches	$t_{SK(O)}$	Skew between DP and DM when connected to TDP and TDM, R_L = R_S = 50Ω, Figure 2		40		ps
TDP/TDM Off-Capacitance	C_{OFF}	f = 1MHz, V_{BIAS} = 0V, V_{SIGNAL} = 500mV_{P-P} (Note 3)		2.0		pF
DP/DM On-Capacitance (Connected to TD_)	C_{ON}	f = 240MHz, V_{BIAS} = 0V, V_{SIGNAL} = 500mV_{P-P}		4.0	5.5	pF
-3dB Bandwidth	BW	R_L = R_S = 50Ω		1000		MHz
Off-Isolation	V_{ISO}	V_{TDP}, V_{DP} = 0dBm, R_L = R_S = 50Ω, f = 250MHz, Figure 3		-20		dB
Crosstalk	V_{CT}	V_{TDP}, V_{DP} = 0dBm, R_L = R_S = 50Ω, f = 250MHz, Figure 3		-25		dB
INTERNAL RESISTORS						
DP/DM Short Pulldown	R_{PD}		350	500	700	kΩ
RP1/RP2 Ratio	RT_{RP}		1.485	1.5	1.515	Ratio
RP1 + RP2 Resistance	R_{RP}		93.75	125	156.25	kΩ
RM1/RM2 Ratio	RT_{RM}		0.854	0.863	0.872	Ratio
RM1 + RM2 Resistance	R_{RM}		69.75	93	116.25	kΩ

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +2.8V to +5.5V, T_A = T_J = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
COMPARATORS						
DM Comparator Threshold	V_{DMF}	V_{RDP} > 0.4V, DM falling	1.9	2.1	2.3	V
		V_{RDP} < 0.3V, DM falling	44	45	46	%V_{CC}
DP and RDP Comparator Threshold	V_{DPR}	DP or RDP falling	0.3	0.35	0.4	V
DM Comparator Hysteresis				1		%V_{DMF}
DP and RDP Comparator Hysteresis				1		%V_{DPR}
DM Comparator Debounce Time	t_{DM}	V_{DM} from 2.8V to 1.5V	30	100	200	µs
DP Comparator Debounce Time	t_{DP}	V_{DP} from 0.7V to 0V	30	100	200	µs
DIGITAL I/O (CB0, CB1)						
Input Logic Voltage High	V_{IH}		1.4			V
Input Logic Voltage Low	V_{IL}				0.4	V
Input Logic Hysteresis	V_{HYST}			100		mV
Input Leakage Current	I_{IN}	V_{CC} = 5.5V, 0V ≤ $V_{CB\_}$ ≤ V_{IL} or V_{IH} ≤ $V_{CB\_}$ ≤ V_{CC}	-250		+250	nA
ESD PROTECTION						
All Pins		Human Body Model		±2		kV
ESD Protection Level (DP and DM Only)		Human Body Model		±15		kV

Note 2: All devices are 100% production tested at T_A = +25°C. Specifications over temperature are guaranteed by design.
Note 3: Guaranteed by design.

Test Circuits/Timing Diagrams

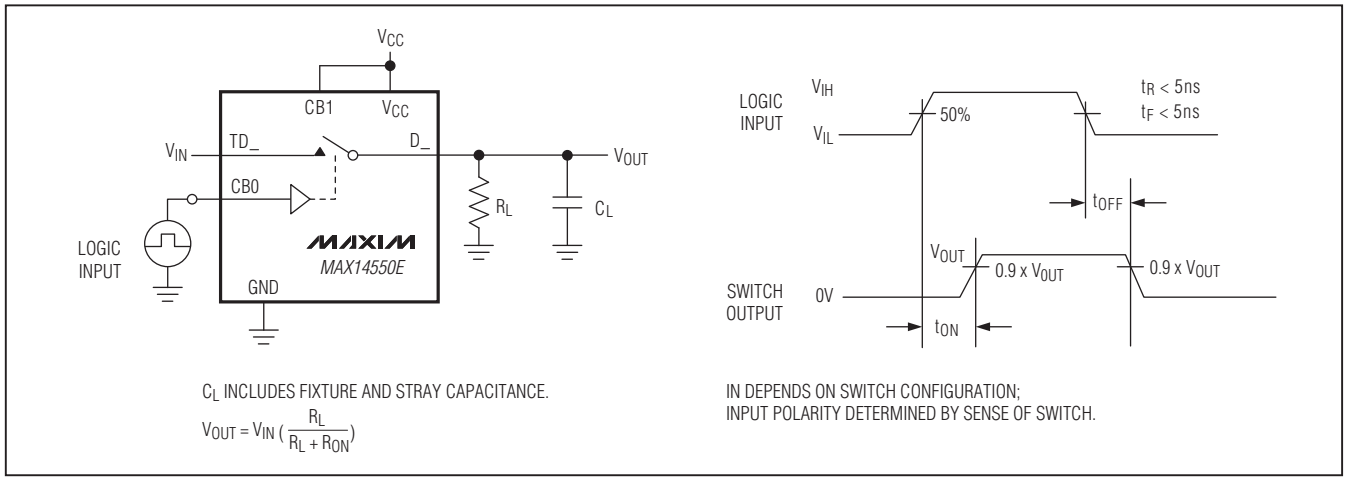


Figure 1. Switching Time

Test Circuits/Timing Diagrams (continued)

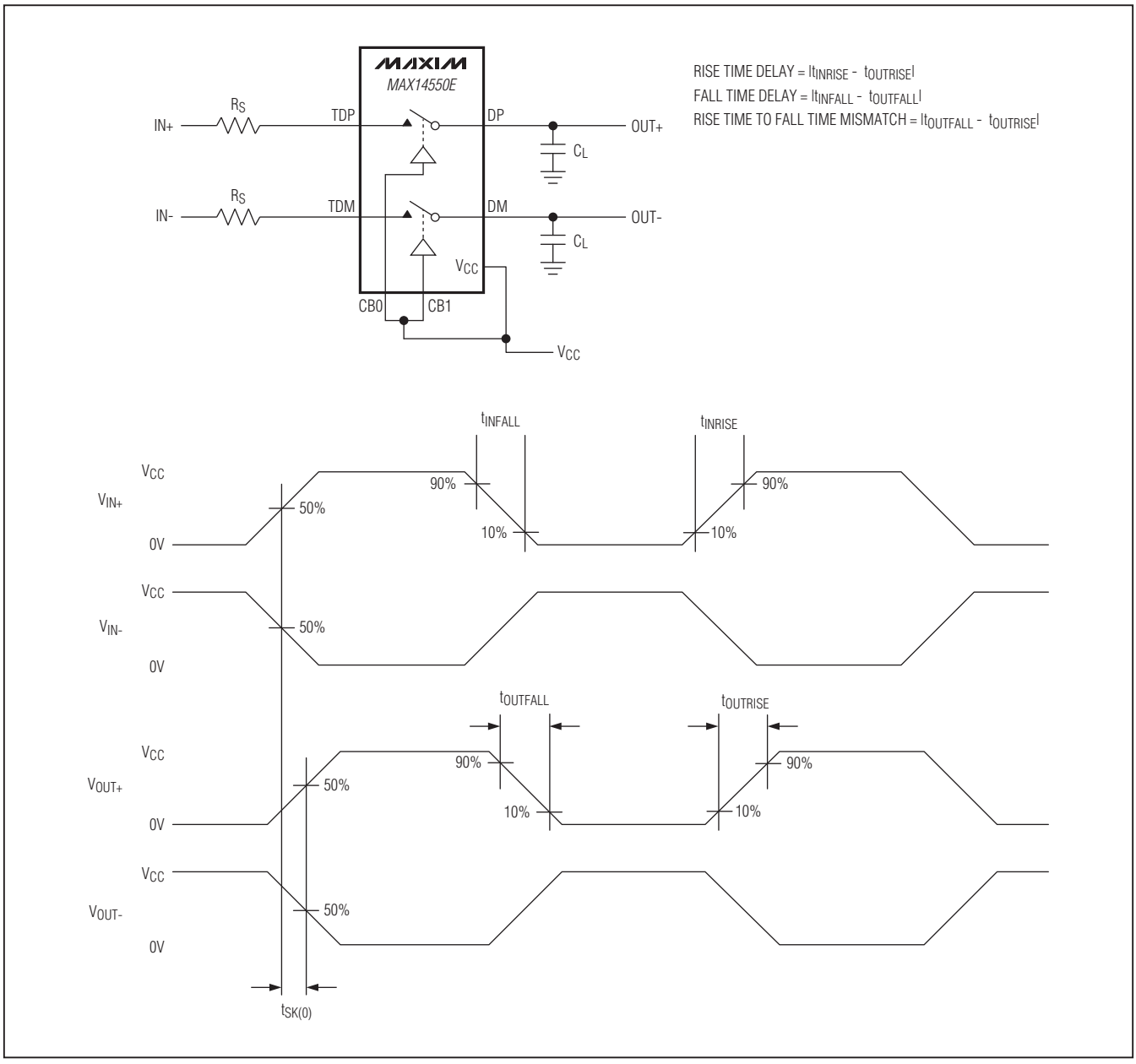


Figure 2. Output Signal Skew

USB Host Charger Identification Analog Switch

Test Circuits/Timing Diagrams (continued)

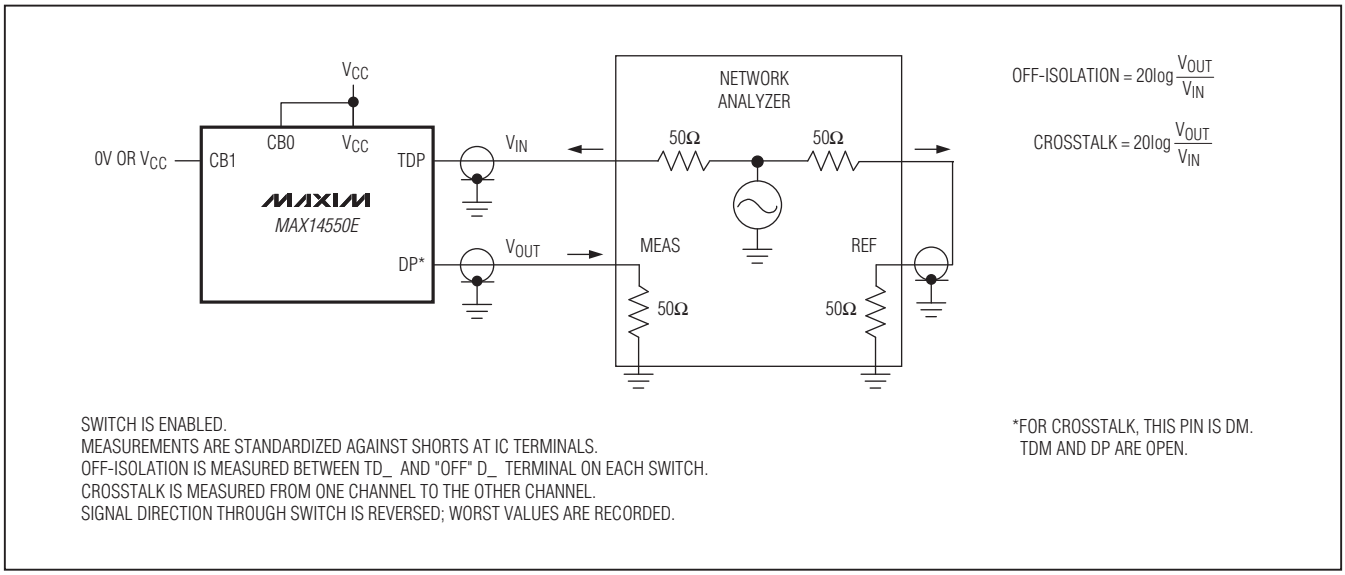
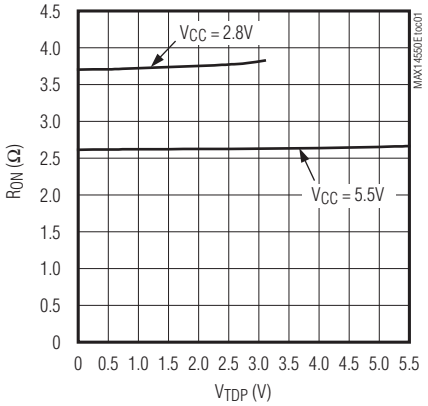


Figure 3. Off-Isolation and Crosstalk

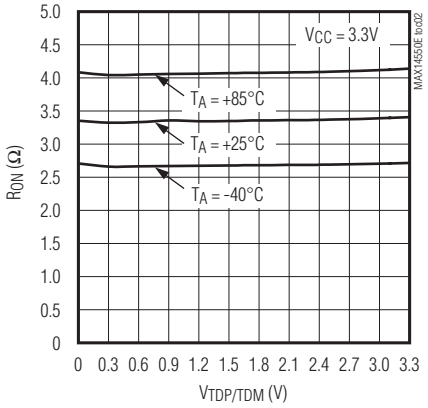
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

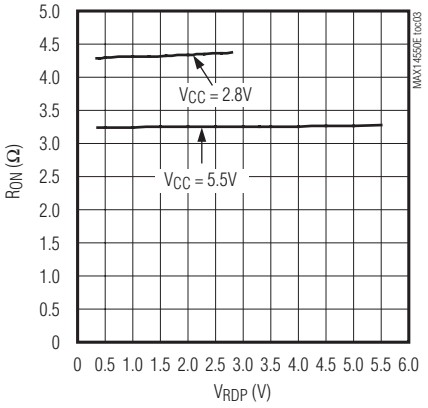
TDP/TDM ON-RESISTANCE vs. SUPPLY VOLTAGE



TDP/TDM ON-RESISTANCE vs. $V_{TDP/TDM}$



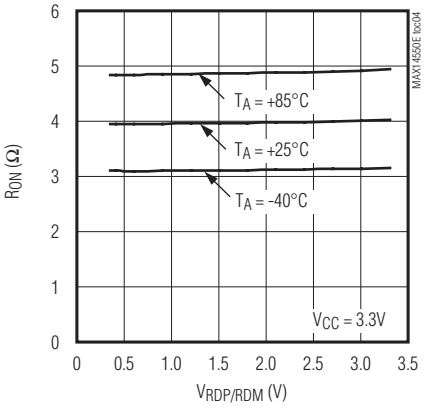
RDP/RDM ON-RESISTANCE vs. SUPPLY VOLTAGE



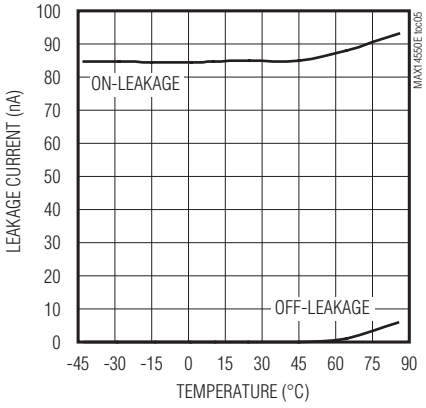
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

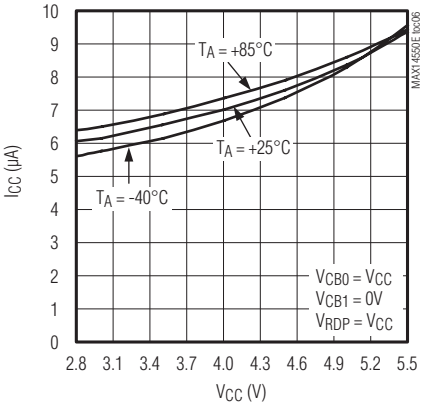
RDP/RDM ON-RESISTANCE vs. $V_{RDP/RDM}$



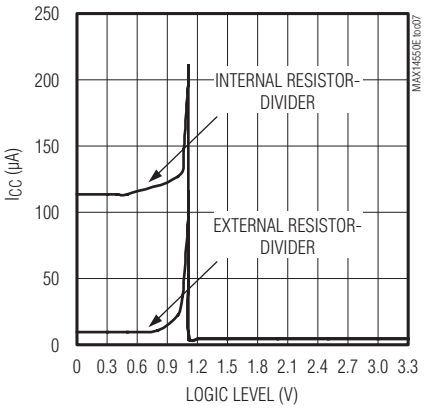
TDP/DP LEAKAGE CURRENT vs. TEMPERATURE



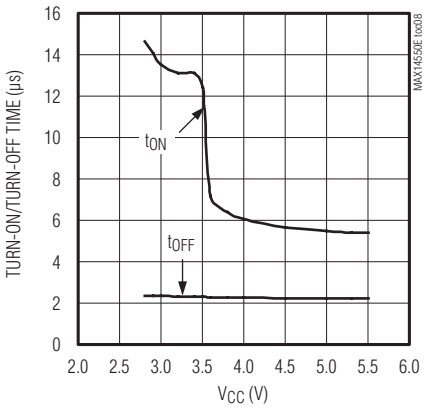
SUPPLY CURRENT vs. SUPPLY VOLTAGE



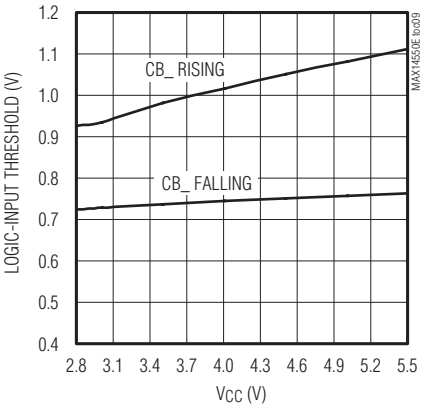
SUPPLY CURRENT vs. LOGIC LEVEL



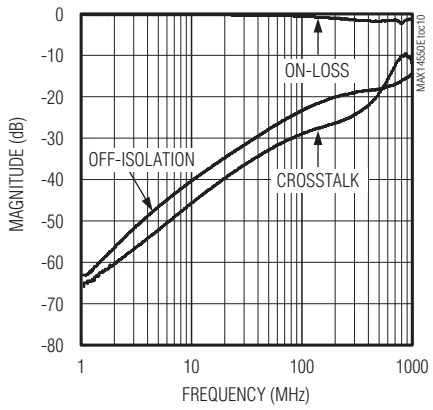
TURN-ON/TURN-OFF TIME vs. SUPPLY VOLTAGE



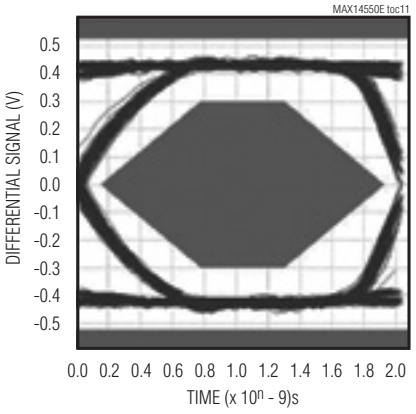
LOGIC-INPUT THRESHOLD vs. SUPPLY VOLTAGE



FREQUENCY RESPONSE



EYE DIAGRAM

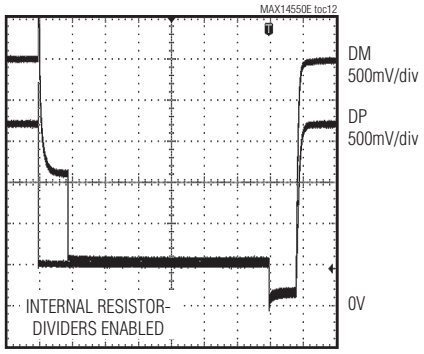


USB Host Charger Identification Analog Switch

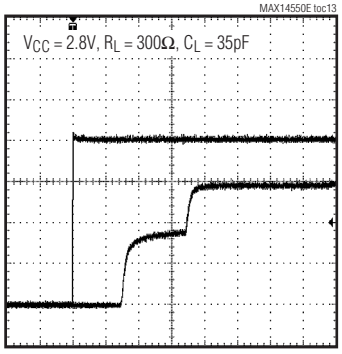
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

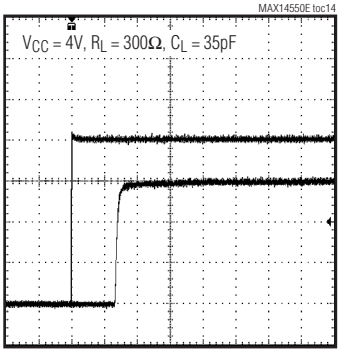
AUTODETECTION MODE



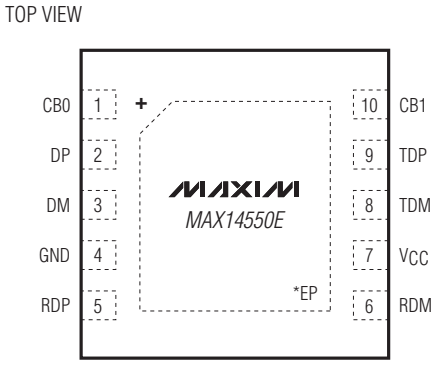
DP RISING



DP RISING



Pin Configuration



TDFN
(3mm × 3mm)

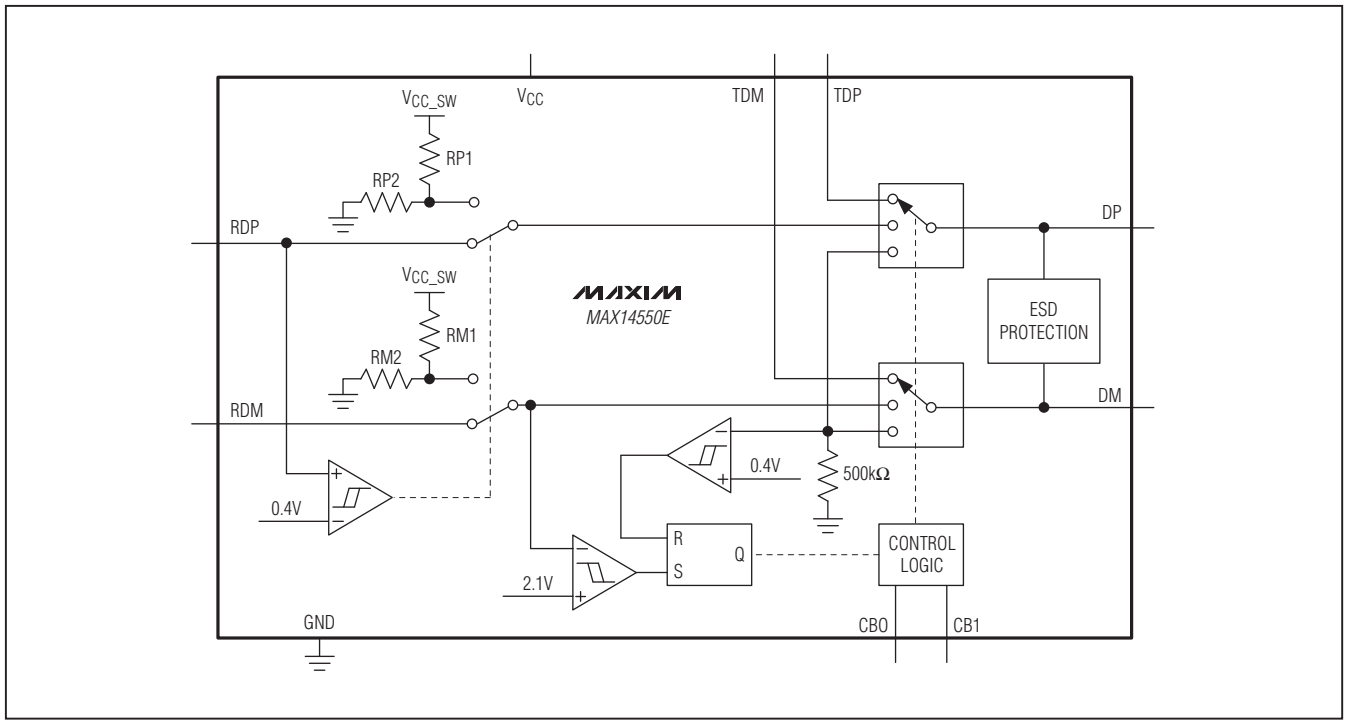
*CONNECT EP TO GND.

Pin Description

PIN	NAME	FUNCTION
1	CB0	Switch Control Bit 0. See the *Switch Control* section.
2	DP	USB Connector D+ Connection
3	DM	USB Connector D- Connection
4	GND	Ground
5	RDP	External Resistor Bias Input for D+ and Selection for External Resistors in RDP and RDM
6	RDM	External Resistor Bias Input for D-
7	V_{CC}	Power Supply. Bypass V_{CC} to GND through a 0.1µF capacitor. Place the capacitor as close as possible to the device.
8	TDM	USB Transceiver D- Connection
9	TDP	USB Transceiver D+ Connection
10	CB1	Switch Control Bit 1. See the *Switch Control* section.
—	EP	Exposed Pad. Connect EP to GND. Do not use EP as the main ground connection.

USB Host Charger Identification Analog Switch

Functional Diagram



Detailed Description

The MAX14550E is a combination of a Hi-Speed USB analog switch and a charger host identification detection analog switch, which allows USB hosts to identify the USB port as a charger port when the USB host is in a low-power mode and cannot enumerate USB devices. The MAX14550E features a high-performance, Hi-Speed USB switch with low 4pF on-capacitance and low 4Ω on-resistance. DP and DM can survive signals between 0V and 6V with any supply voltage.

Resistor-Dividers

The MAX14550E features an internal resistor-divider for biasing or can operate with external resistors. Connect RDP to ground to use the internal resistor-divider (see the *Typical Operating Circuit*). The user must provide 5V supply voltage to V_{CC} when the internal resistor-divider is used. When the MAX14550E is not operated with the internal resistor-dividers, the device disconnects the internal resistor-dividers' pullup voltage (V_{CC_SW}) to minimize supply current requirements.

Connect RDP to a voltage above 0.4V (max) to use external resistors (Figure 4). Internal resistor-dividers are always disconnected from the supply voltage when external resistor-dividers are detected at RDP (V_{RDP} > 0.4V).

Switch Control

The MAX14550E features two digital inputs, CB0 and CB1, for mode selection (Table 1). Connect CB0 and CB1 to a logic-level low voltage for autodetection mode (see the *Autodetection* section).

Connect CB0 and CB1 to a logic-level high voltage for normal Hi-Speed USB bypass functionality.

Connect CB0 to a logic-level low and CB1 to a logic-level high voltage to select charger mode. Optionally, CB0 and CB1 can be forced to set the detection to a particular state. The USB Implementers Forum (USB-IF) has defined that dedicated chargers have D+ and D- shorted together. In USB charger mode, DP and DM are shorted together for dedicated charging functionality. Connect CB0 to a logic-level high and CB1 to a logic-level low voltage to force the resistor network to be connected to DP and DM.

USB Host Charger Identification Analog Switch

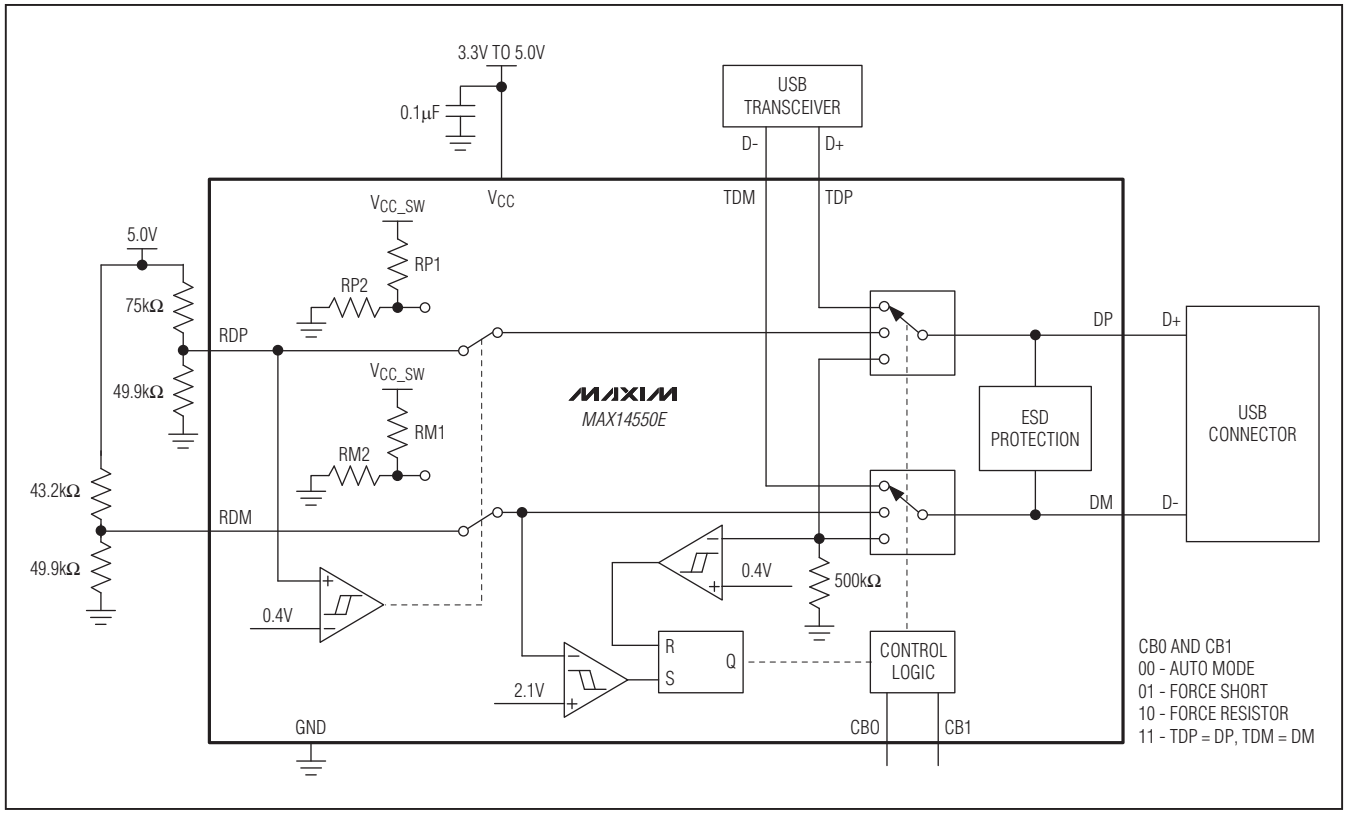


Figure 4. Operation with External Resistors

Autodetection

The MAX14550E features autodetection mode for dedicated chargers and USB masters. CB0 and CB1 must both be set low to activate autodetection mode.

In autodetection mode, the MAX14550E initially connects the resistor network to DP and DM. The MAX14550E monitors the voltage at DM to determine the type of device attached. If the voltage at DM is 2.1V (typ) or higher, the voltage stays as is.

If the voltage at DM is below the 2.1V (typ) threshold, the internal switch disconnects DP from the resistor network and DM. DP and DM are shorted together. The MAX14550E then monitors the voltage at DM to determine when to reconnect the resistor network. If the voltage at DM > 0.35V (typ), the short remains connected. If the voltage at DM drops below 0.35V (typ), the short is removed and the resistor network is reconnected to DP and DM.

DP and DM feature a 100µs (typ) debounce time to reject transients.

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

The Air-Gap test involves approaching the device with a charged probe. The Contact-Discharge method connects the probe to the device before the probe is energized.

Table 1. Digital Input States

V_{CC} (V)	RDP < 0.4V = INTERNAL RESISTOR > 0.4V = EXTERNAL RESISTOR	CB0	CB1	DP/DM POSITION	INTERNAL OR EXTERNAL RESISTOR CONNECTED TO DP/DM	COMMENT
3.3	RDP < 0.4V	X	X	—	—	Not recommended
3.3	RDP > 0.4V	0	0	Autodetection circuit active	External resistor	Auto mode
		0	1	Shorted	Not connected	Auto mode disabled
		1	0	Connected to resistor-divider	External resistor	Auto mode disabled
		1	1	Connected to TDP/TDM	Not connected	USB traffic active
5.0	RDP < 0.4V	0	0	Autodetection circuit active	Internal resistor	Auto mode
		0	1	Shorted	Not connected	Auto mode disabled
		1	0	Connected to resistor-divider	Internal resistor	Auto mode disabled
		1	1	Connected to TDP/TDM	Not connected	USB traffic active
	RDP > 0.4V	0	0	Autodetection circuit active	External resistor	Auto mode
		0	1	Shorted	Not connected	Auto mode disabled
		1	0	Connected to resistor-divider	External resistor	Auto mode disabled
		1	1	Connected to TDP/TDM	Not connected	USB traffic active

USB Host Charger Identification Analog Switch

Extended ESD Protection (Human Body Model)

ESD-protection structures are incorporated on all pins to protect against electrostatic discharges up to ±2kV (Human Body Model) encountered during handling and assembly. DP and DM are further protected against ESD up to ±15kV (Human Body Model) without damage. The ESD structures withstand high ESD both in normal operation and when the device is powered down. After an ESD event, the device continues to function without latchup (Figures 5a and 5b).

Table 2. Tested Portable Device

MANUFACTURER/ SPECIFICATION	DEVICE	IDENTIFICATION	DETECTION METHOD/COMMENTS	MAX14550E SUPPORT
Apple	iPod® and some iPhones®	None	Immediately draws 500mA when 5V is attached to V_{BUS}	iPhone 2G, 3G, and 3GS; iPod classic®; iPod video; iPod touch (1st and 2nd generations); iPod nano® (3rd, 4th, 5th generation); and iPod mini
	iPod touch® and iPhone 3G	Resistor-divider on D+ and D-	USB FS/HS configuration: draws < 500mA D+/D- voltage detection: <1A	
Motorola	All phones with mini-USB	Resistor to GND on ID line	USB FS/HS configuration: draws < 500mA. Follows CEA-936-A specification, which is the only known company to use this specification.	Depends on model
RIM	BlackBerry®	Some models look for shorted D+/D-	USB FS/HS configuration: draws < 500mA. Some models look for shorted D+/D- with a pullup to 2.7V for dedicated charger.	Depends on model
HTC	QUALCOMM®-based phones	None	Immediately draws 500mA when 5V is attached to V_{BUS}	Full support
USB-IF Standard	—	Shorted D+/D-	Device uses a specific method (voltages and timing well defined)	2009 and newer LG and Samsung models with micro-USB connector
China Standard	—	Shorted D+/D-	Method not defined	Depends on model

iPod, iPhone, iPod touch, iPod classic, and iPod nano are registered trademarks of Apple, Inc.

BlackBerry is a registered trademark/servicemark of Research In Motion Limited.

QUALCOMM is a registered trademark of QUALCOMM Incorporated.

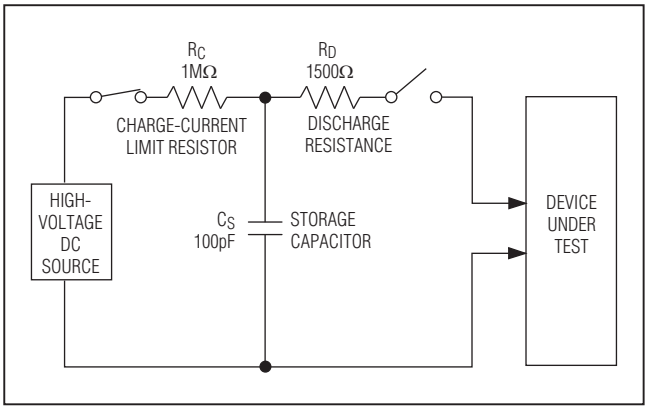


Figure 5a. Human Body ESD Test Model

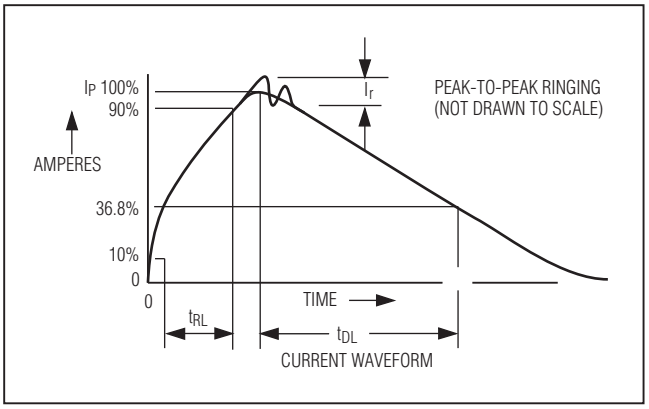
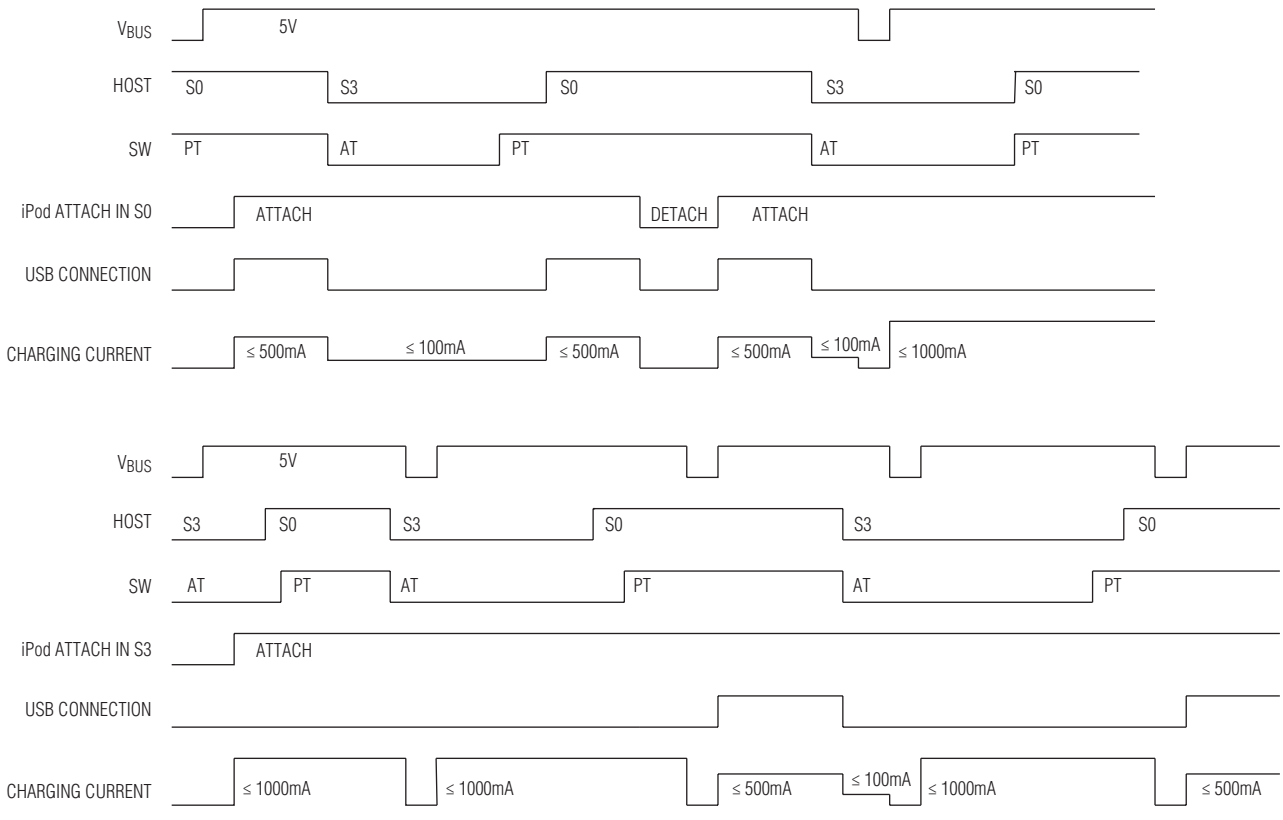


Figure 5b. Human Body Current Waveform

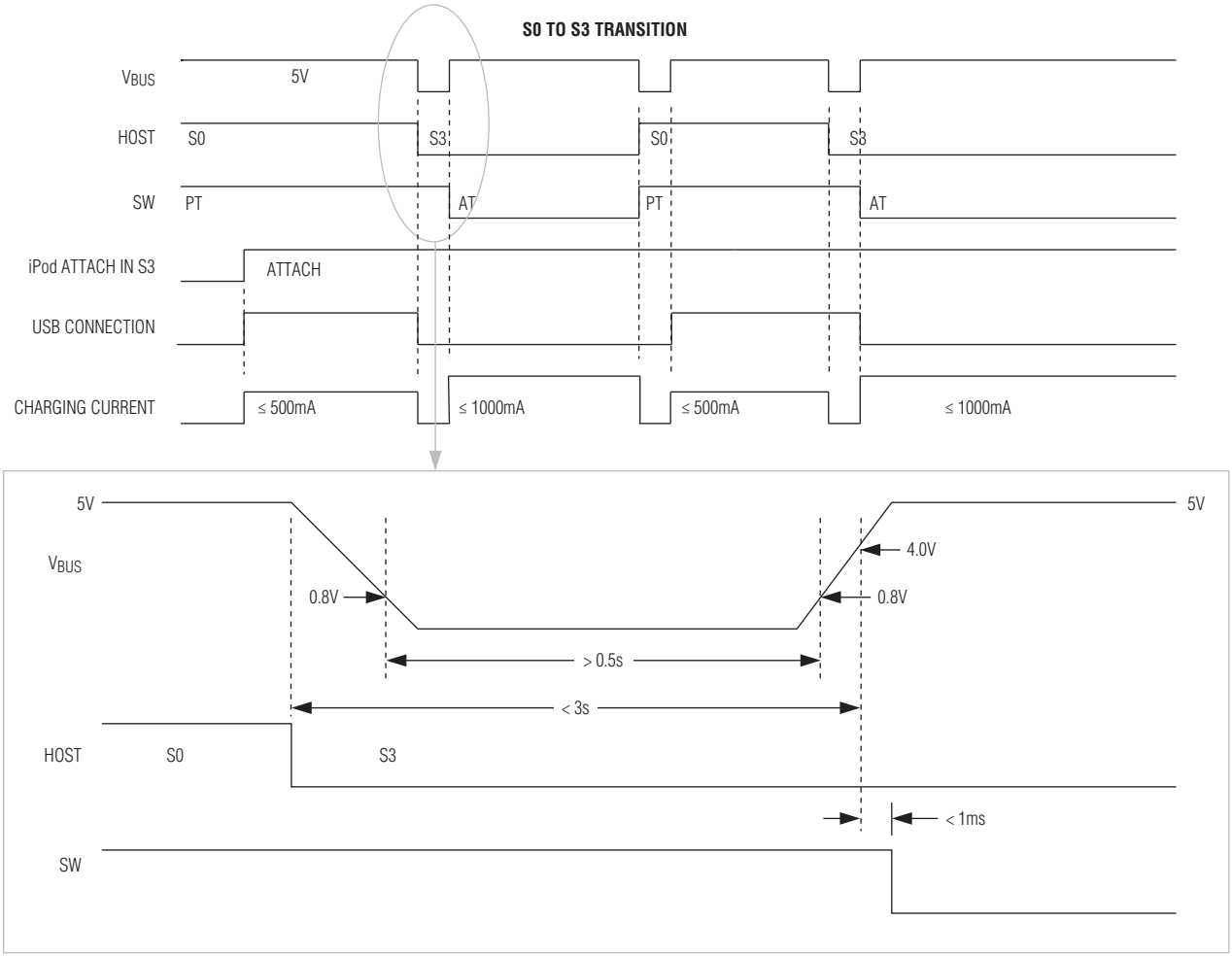
Timing Charts



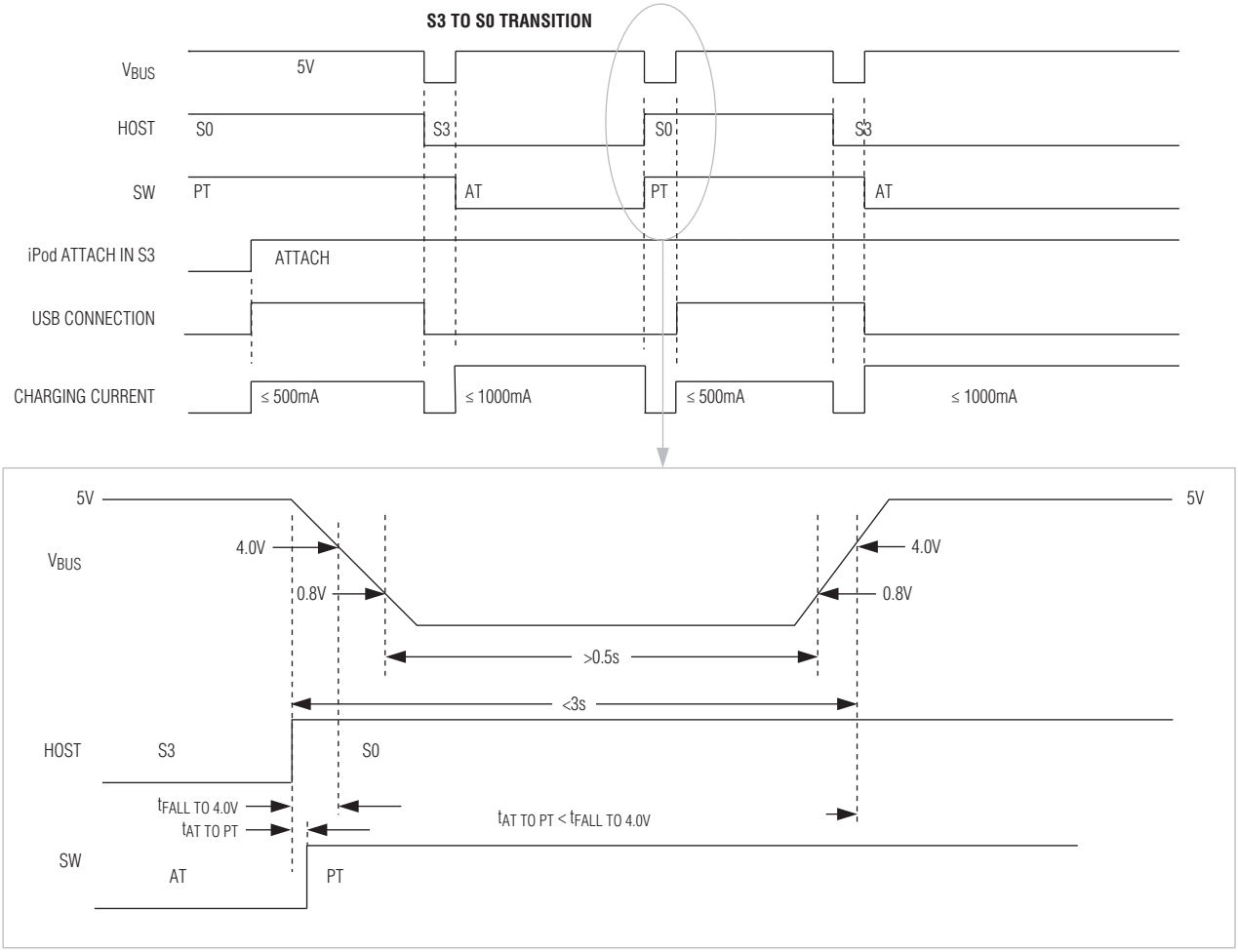
NOTE: WHEN USING THIS TIMING, IT IS RECOMMENDED TO SUPPLY V_{CC} WITH V_{BUS}, AND V_{BUS} SHOULD BE IMMEDIATELY DISCHARGED WHEN V_{BUS} IS TURNED OFF.

USB Host Charger Identification Analog Switch

Timing Charts (continued)



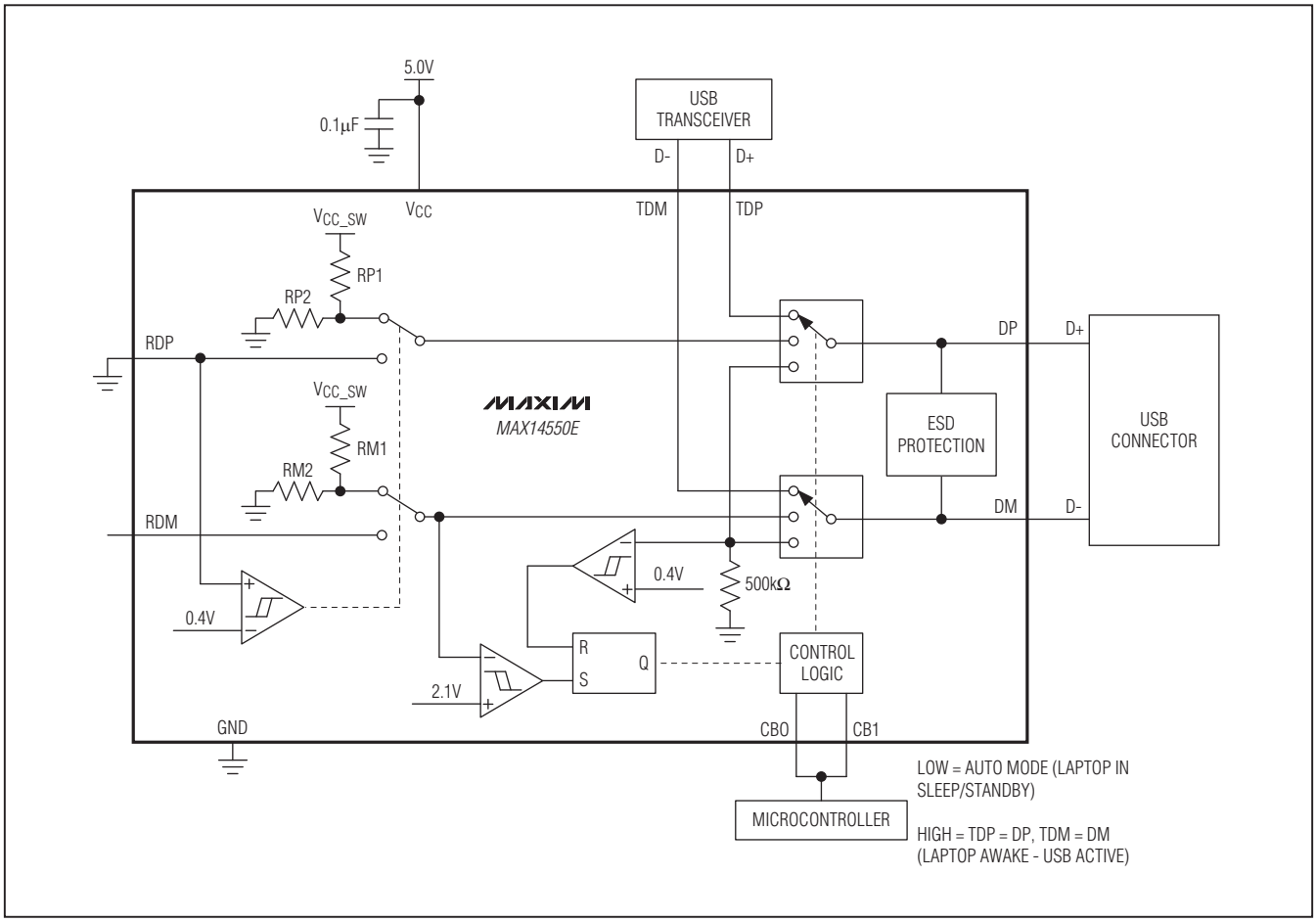
Timing Charts (continued)



NOTE: THIS TIMING IS TO AVOID THE VOLTAGE FROM THE RESISTOR-DIVIDER FROM APPEARING ON DP/DM WHILE V_{BUS} IS OFF BY SWITCHING DP/DM TO TDP/TDM, WHICH IS GROUNDED BY 15kΩ.

USB Host Charger Identification Analog Switch

Typical Operating Circuit



Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
10 TDFN-EP	T1033+1	21-0137

USB Host Charger Identification Analog Switch

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/09	Initial release.	—
1	11/09	• Replaced the Lead Temperature with Soldering Temperature in the *Absolute Maximum Ratings* section. • Changed the “DP/DM On-Capacitance” specification in the *Electrical Characteristics* table conditions from f = 1MHz to f = 240MHz and 6.0pF (max) to 5.5pF (max). • Replaced TOC11 (Eye Diagram) in the *Typical Operating Characteristics* section. • Replaced Table 1 and added Table 2. • Added the *Timing Chart*.	2, 3, 7, 11, 12, 13
2	1/10	Replaced the timing diagrams in *Timing Charts*.	13, 14,15