CLOCK SYNCHRONIZER AND MULTIPLIER IDT9170B

Description

The IDT9170B generates an output clock which is synchronized to a given continuous input clock with zero delay (±1ns at 5 V VDD). Using IDT's proprietary phase-locked loop (PLL) analog CMOS technology, the IDT9170B is useful for regenerating clocks in high speed systems where skew is a major concern. By the use of the two select pins, multiples or divisions of the input clock can be generated with zero delay (see Tables 2 and 3). The standard versions produce two outputs, where CLK2 is always a divide by two version of CLK1.

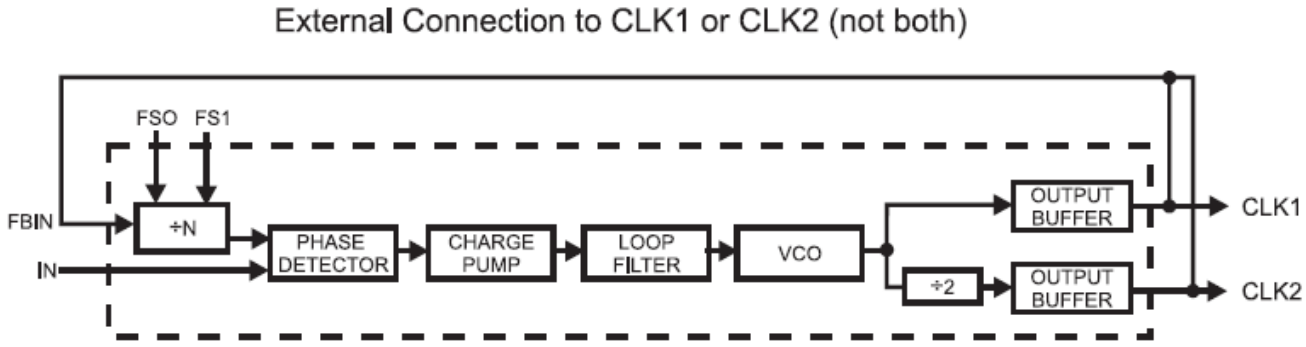
The IDT9170B is also useful to recover poor duty cycle clocks. A 50 MHz signal with a 20/80% duty cycle, for example, can be regenerated to the 48/52% typical of the part.

The IDT9170B allows the user to control the PLL feedback, making it possible, with an additional 74F240 octal buffer (or other such device that offers controlled skew outputs), to synchronize up to 8 output clocks with zero delay compared to the input (see Figure 1). Application notes for the IDT9170B are available. Please consult IDT.

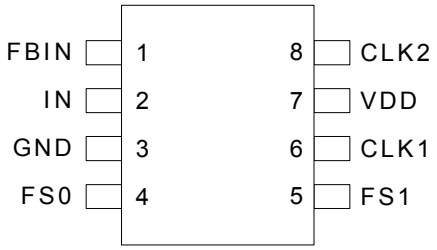
Features

- On-chip Phase-Locked Loop for clocks synchronization.
- Synchronizes frequencies up to 107 MHz (output) @ 5.0 V
- ±1ns skew (max) between input & output clocks @ 5.0 V
- Can recover poor duty cycle clocks
- CLK1 to CLK2 skew controlled to within ±1ns @ 5.0 V
- 3.0 - 5.5 V supply range
- Low power CMOS technology
- Small 8-pin DIP or SOIC package
- On chip loop filter
- **IDT9170B-01** for output clocks 20-107 MHz @ 5.0 V, 20 - 66.7 MHz @ 3.3 V
- **IDT9170B-02** for output clocks 5-26.75 MHz @ 5.0 V, 5 - 16.7 MHz @ 3.3 V

Block Diagram



Pin Assignment



Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	FBIN	Input	Feedback input.
2	IN	Input	Input for reference clock.
3	GND	Power	Connect to ground.
4	FS0	Input	Frequency select 0.
5	FS1	Input	Frequency select 1.
6	CLK1	Output	Clock output 1. See tables 1, 2 for values.
7	VDD	Power	Power supply.
8	CLK2	Output	Clock output 2. See tables 1, 2 for values.

Using the IDT9170B

The IDT9170B has the following characteristics:

1. Rising edges at IN and FBIN are lined up. Falling edges are not synchronized.

2. The relationship between the frequencies at FBIN and IN with CLK1 feedback is shown in Table 1 below.

Functionality (Table 1)

FS1	FS0	f_{FBIN} (-01, -02)
0	0	$2 * f_{IN}$
0	1	$4 * f_{IN}$
1	0	f_{IN}
1	1	$8 * f_{IN}$

3. The frequency of CLK2 is half the CLK1 frequency.

4. The CLK1 frequency ranges are:

		VDD=5 V	VDD=3.3 V
IDT9170B-01	$20 < f_{CLK1}$	<107 MHz	<66.7
IDT9170B-02	$5 < f_{CLK1}$	<26.75 MHz	<16.7

Eliminate High Speed Clock Routing Problems

The IDT9170B makes it possible to route lower speed clocks over long distances on the PC board and to place an IDT9170B next to the device requiring a higher speed clock. The multiplied output can then be used to produce a phase locked, higher speed output clock.

Compensate for Propagation Delays

Including an IDT9170B in a timing loop allows the use of PALs, gate arrays, etc., with loose timing specifications. The IDT9170B compensates for the delay through the PAL and synchronizes the output to the input reference clock.

Operating Frequency Range

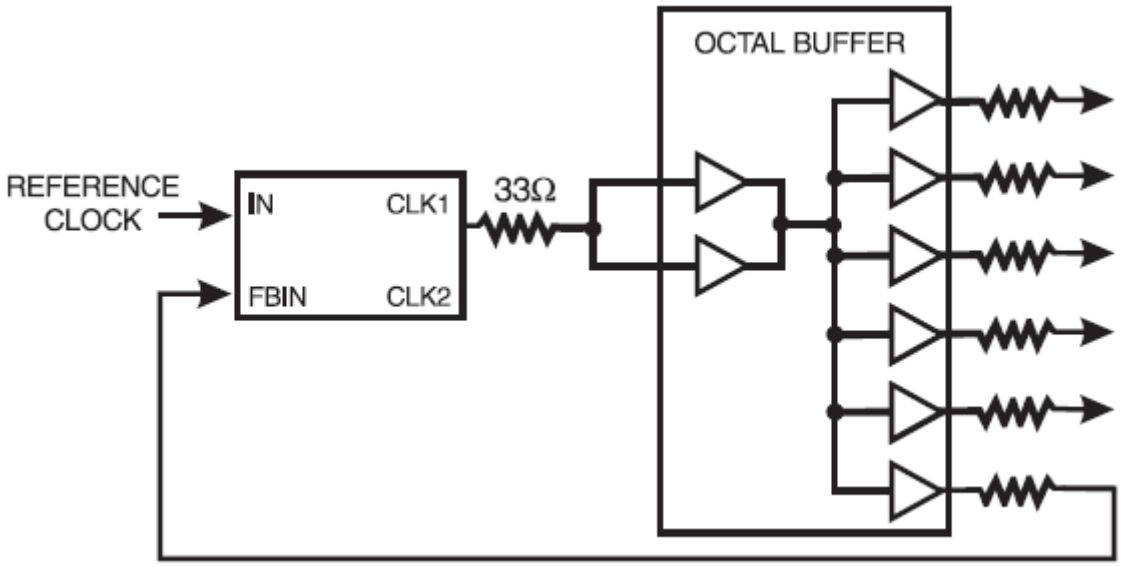
The IDT9170B is offered in versions optimized for operation in two frequency ranges. The -01 covers high frequencies, 20 to 100 MHz.* The -02 operates from 5 to 25 MHz.* The IDT9170B can be supplied with custom multiplication factors and operating ranges. Consult IDT for details.

3.3 V VDD Operation

The IDT9170B does operate at both 5.0 V and 3.3 V system conditions. Please note the Electrical Characteristic specifications at 3.3 V include a limited output frequency (66.6 MHz max.) and a wider skew of FBIN to CLK1. For 3.3 V±5% (3.15 V min.), this skew is -5.0 to 0 ns. At 3.3 V±10% (3.0 V min.), the skew is widened to -8 ns to 0 ns and should be accounted for in system design.

*At 3.3 V, the maximum CLK1 frequency is 66.7 MHz for - 01 4 and 16.7 MHz for -02.

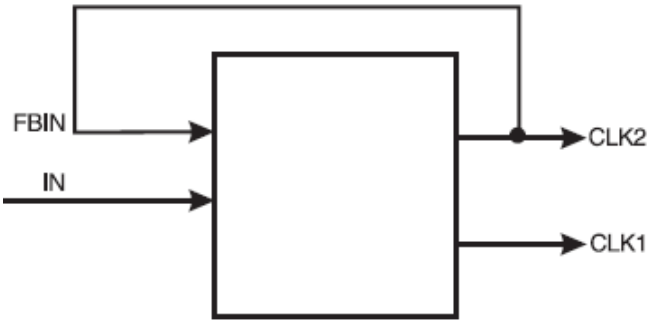
Figure 1: Application of Multiple Outputs



Using CLK2 Feedback

Connecting CLK2 to FBIN as shown in Figure 2 will cause all of the rising edges to be aligned (Figure 4).

Figure 2



For CLK2 frequencies 10 - 53.5 MHz* (-01)
For CLK2 frequencies 2.5 - 13.37 MHz (-02)
*Maximum 33.3 MHz@3.3 V (-01), 8.33 MHz@3.3 V (-02)

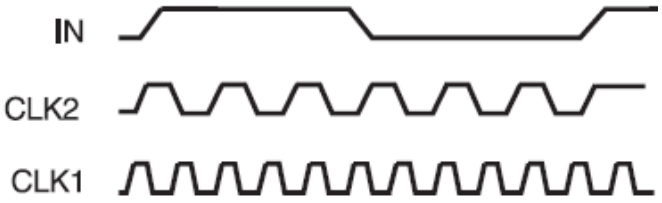
Table 2

Functionality Table for IDT9170B-01, -02 with CLK2 Feedback

FS1	FS0	CLK1	CLK2
0	0	INx4	INx2
0	1	INx8	INx4
1	0	INx2	IN
1	1	INx16	INx8

Figure 4

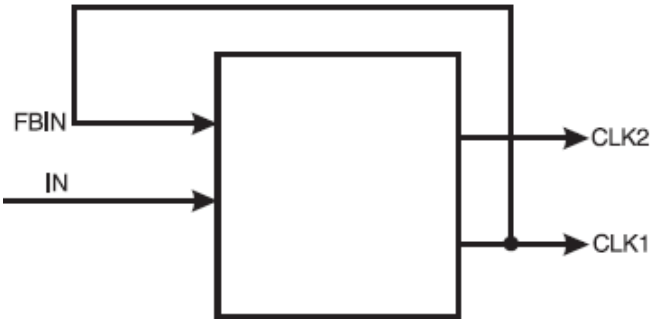
Input and Output Clock Waveforms with CLK2 Connected to FBIN



Using CLK1 Feedback

With CLK1 connected to FBIN as shown in Figure 3, the input and CLK1 output will be aligned on the rising edge, but CLK2 can be either rising or falling (Figure 5). Consult IDT if the CLK1 frequency is desired to be higher than 107 MHz.

Figure 3



For CLK1 frequencies 20 - 107 MHz†(-01)
For CLK1 frequencies 5 - 26.75 MHz (-02)
†Maximum 66.7 MHz@3.3 V (-01), 16.7 MHz@3.3 V (-02)

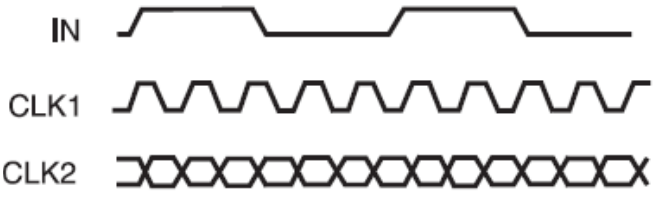
Table 3

Functionality Table for IDT9170B-01, -02 with CLK2 Feedback

FS1	FS0	CLK1	CLK2
0	0	INx2	IN
0	1	INx4	INx2
1	0	IN	IN/2
1	1	INx8	INx4

Figure 5

Input and Output Clock Waveforms with CLK1 Connected to FBIN



Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the IDT9170B. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Parameter	Condition	Min.	Typ.	Max.	Units
Supply Voltage, VDD	referenced to GND			7	V
Ambient Operating Temperature	under bias	0		+70	°C
Voltage I/O Pins	referenced to GND	-0.5		VDD+0.5	V
Storage Temperature		-65		150	°C
Soldering Temperature				260	°C
Power Dissipation				0.5	W

DC Electrical Characteristics at 5 V

Unless stated otherwise, **VDD = 5 V ±5%**, Ambient Temperature 0 to +70°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Supply Current	IDD1	No load, 107 MHz (-01)		30	50	mA
Operating Supply Current	IDD2	No load, 26.5 MHz (-02)		13	20	mA
Input High Voltage	V_{IH}	VDD=5 V	2.0			V
Input Low Voltage	V_{IL}	VDD=5 V			0.8	V
Input High Current	I_{IH}	VIN=VDD			5	µA
Input Low Current	I_{IL}	VIN=0 V	-1.5	-5		µA
Output High Voltage*	V_{OH1}	I_{OH} = -1 mA	VDD-0.4			V
	V_{OH2}	I_{OH} = -4 mA	VDD-0.8			V
	V_{OH3}	I_{OH} = -8 mA	2.4			V
Output Low Voltage*	V_{OL}	I_{OL} = 8 mA			0.4	V

*Parameter guaranteed by design and characterization. Not 100% tested in production.

AC Electrical Characteristics at 5 V

Unless stated otherwise, **VDD = 5 V ±5%**, Ambient Temperature 0 to +70° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency	f_{I1}	Note 1, IDT9170B-01	2.5		107	MHz
	f_{I2}	IDT9170B-02	2		26.75	MHz
Output Frequency, CLK1	f_{O1}	IDT9170B-01	20		107	MHz
	f_{O2}	IDT9170B-02	5		26.75	MHz
Input Clock Rise Time	ICLKr				10	ns
Input Clock Fall Time	ICLKf				10	ns
Output Rise Time	t_{R1}	0.8 to 2.0 V, 15 pF load		0.6	2	ns
Rise Time	t_{R2}	20% to 80% VDD, 15 pF load		1.2	3	ns
Output Fall Time	t_{F1}	2.0 to 0.8 V, 15 pF load		0.4	2	ns
Fall Time	t_{F2}	80% to 20% VDD, 15 pF load		0.9	2	ns
Output Duty Cycle, IDT9170B-01	d_{T1}	15 pF load, Note 2, 3	40	48-52	60	%
Output Duty Cycle, IDT9170B-02	d_{T2}	15 pF load, Note 2, 3	45	49-51	55	%
One Sigma Jitter				125	300	ps
Absolute Jitter	t_{abs1}	CLK1>20 MHz (-01)	-500		500	ps
		CLK1>5 MHz (-02)				
FBIN to IN Skew	T_{skew1}	15 pF load, input rise time <5 ns, Note 2, 4	-1	-0.3	1	ns
	T_{skew2}	15 pF load, input rise time <10 ns, Note 2, 4	-2	-0.3	2	ns
CLK1 to CLK2 Skew	T_{skew3}	Note 2, 4	-1	0.4	1	ns

Parameters guaranteed by design and characterization. Not 100% tested in production.

Note 1: It may be possible to operate the IDT9170B outside of these ranges. Consult IDT for your specific application.

Note 2: All AC specifications are measured with a 50Ω transmission line, load teminated with 50Ω to 1.4 V.

Note 3: Duty cycle measured at 1.4 V.

Note 4: Skew measured at 1.4 V on rising edges. Positive sign indicates the first signal precedes the second signal.

DC Electrical Characteristics at 3.3 V

Unless stated otherwise, **VDD = 3.3 V ±5%**, Ambient Temperature 0 to +70°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Supply Current	IDD1	No load, 66.7 MHz (-01)		17	30	mA
Operating Supply Current	IDD2	No load, 16.7 MHz (-02)		7	15	mA
Input High Voltage	V_{IH}	VDD=3.3 V	0.7VDD			V
Input Low Voltage	V_{IL}	VDD=3.3 V			0.2VDD	V
Input High Current	I_{IH}	VIN=VDD			5	µA
Input Low Current	I_{IL}	VIN=0 V	-7	-4		µA
Output High Voltage*	V_{OH1}	I_{OH} = -1 mA	VDD-0.4			V
	V_{OH2}	I_{OH} = -3 mA	VDD-0.8			V
	V_{OH3}	I_{OH} = -6 mA	2.4			V
Output Low Voltage*	V_{OL}	I_{OL} = 6 mA			0.4	V

Parameters guaranteed by design and characterization. Not 100% tested in production.

AC Electrical Characteristics at 3.3 V

Unless stated otherwise, **VDD = 3.3 V ±5%**, Ambient Temperature 0 to +70° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency	f_{I1}	IDT9170B-01	7		66.7	MHz
	f_{I2}	IDT9170B-02	2		16.7	MHz
Output Frequency, CLK1	f_{O1}	IDT9170B-01	20		66.7	MHz
	f_{O2}	IDT9170B-02	5		16.7	MHz
Input Clock Rise Time	ICLKr				10	ns
Input Clock Fall Time	ICLKf				10	ns
Output Rise Time	t_{R1}	0.8 to 2.0 V, 15 pF load		1.1	2	ns
Rise Time	t_{R2}	20% to 80% VDD, 15 pF load		1.8	4	ns
Output Fall Time	t_{F1}	2.0 to 0.8 V, 15 pF load		0.8	2	ns
Fall Time	t_{F2}	80% to 20% VDD, 15 pF load		1.2	3	ns
Output Duty Cycle, IDT9170B-01	d_{T1}	15 pF load, Note 2, 3	40	52	60	%
Output Duty Cycle, IDT9170B-02	d_{T2}	15 pF load, Note 2, 3	45	51	55	%
One Sigma Jitter				150	300	ps
Absolute Jitter	t_{abs1}	CLK1>10 MHz (-01)	-500		500	ps
		CLK1>2.5 MHz (-02)				
	t_{abs2}	CLK1<10 MHz (-01)	-2		2	%
		CLK1<2.5 MHz (-02)				
FBIN to IN Skew	T_{skew1}	15 pF load 3.0≤VDD≤ 3.7, Note 2, 4	-4.0	-1.0	1.5	ns
	T_{skew2}	15 pF load 3.0≤VDD≤ 3.7, Note 2, 4	-3.0	-1.0	1.5	ns
CLK1 to CLK2 Skew	T_{skew3}	Note 2, 4, 15 pF load	-2.0	-0.9	0	ns

Parameters guaranteed by design and characterization. Not 100% tested in production.

Note 1: It may be possible to operate the IDT9170B outside of these ranges. Consult IDT for your specific application.

Note 2: All AC specifications are measured with a 50Ω transmission line, load teminated with 50Ω to 1.4 V.

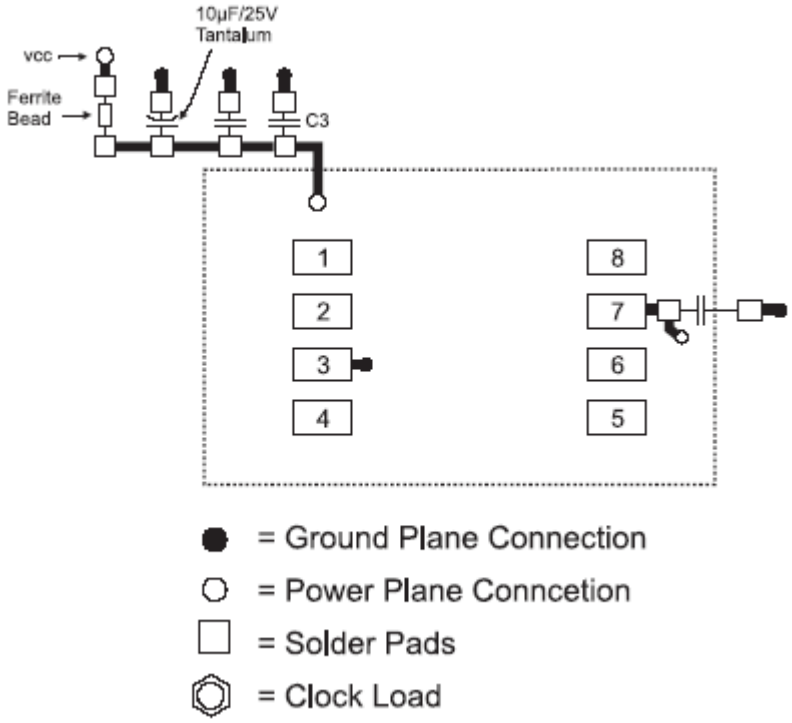
Note 3: Duty cycle measured at 1.4 V.

Note 4: Skew measured at 1.4 V on rising edges. Positive sign indicates the first signal precedes the second signal.

General Layout Precautions

1) Use a ground plane on the top layer of the PCB in all areas not used by traces.

2) Make all power traces and vias as wide as possible to lower inductance.



Note: All clock outputs should have series terminating resistor. Not shown in all places to improve readibility of diagram.

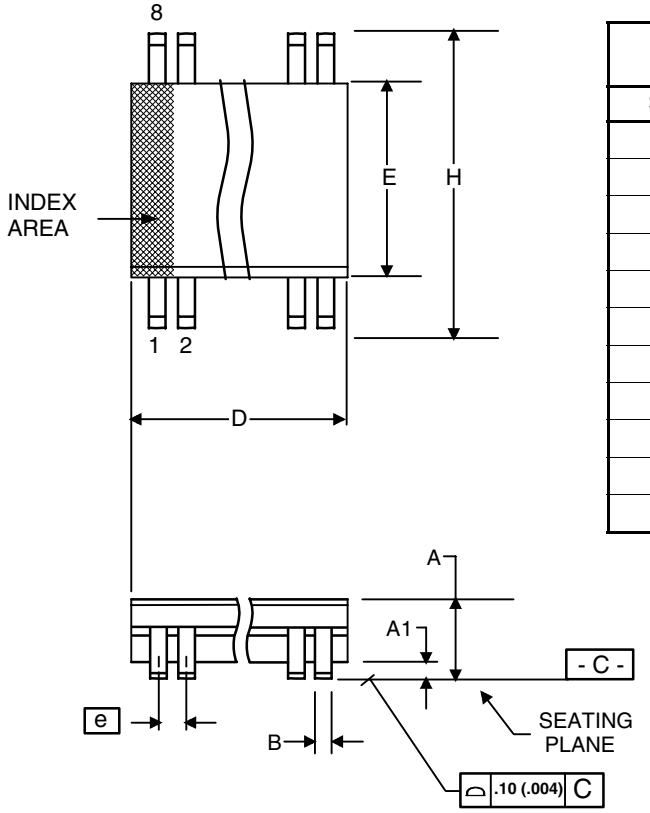
Connections to VDD

Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		150		°C/W
	θ_{JA}	1 m/s air flow		140		°C/W
	θ_{JA}	3 m/s air flow		120		°C/W
Thermal Resistance Junction to Case	θ_{JC}			40		°C/W
Thermal Resistance Junction to Top of Case	Ψ_{JT}	Still air		20		°C/W

Package Outline and Package Dimensions (8-pin SOIC, 150 Mil. Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches	
Symbol	**Min**	**Max**	**Min**	**Max**
A	1.35	1.75	.0532	.0688
A1	0.10	0.25	.0040	.0098
B	0.33	0.51	.013	.020
C	0.19	0.25	.0075	.0098
D	4.80	5.00	.1890	.1968
E	3.80	4.00	.1497	.1574
e	1.27 BASIC		0.050 BASIC	
H	5.80	6.20	.2284	.2440
h	0.25	0.50	.010	.020
L	0.40	1.27	.016	.050
α	0°	8°	0°	8°

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
9170B-01CS08LF	TBD	Tubes	8-pin SOIC	0 to +70° C
9170B-01CS08LFT		Tape and Reel	8-pin SOIC	0 to +70° C
9170B-02CS08LF		Tubes	8-pin SOIC	0 to +70° C
9170B-02CS08LFT		Tape and Reel	8-pin SOIC	0 to +70° C

Parts ordered with a "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History

Rev.	Originator	Date	Description of Change
A	R.Willner	09/23/08	New datasheet.
B	R. Willner	05/26/09	Datasheet release.

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