



Frequency Timing Generator for Pentium II Systems

General Description

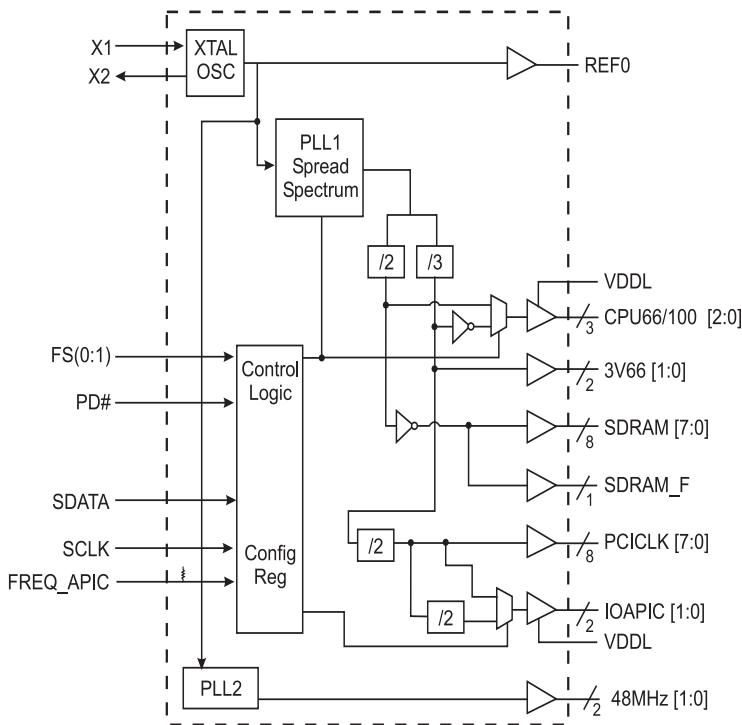
The ICS9250-10 is a single chip clock for Intel Pentium II. It provides all necessary clock signals for such a system.

Spread spectrum may be enabled through I²C programming. Spread spectrum typically reduces EMI by 8dB to 10 dB. This simplifies EMI qualification without resorting to board design iterations or costly shielding. The ICS9250-10 employs a proprietary closed loop design, which tightly controls the percentage of spreading over process and temperature variations.

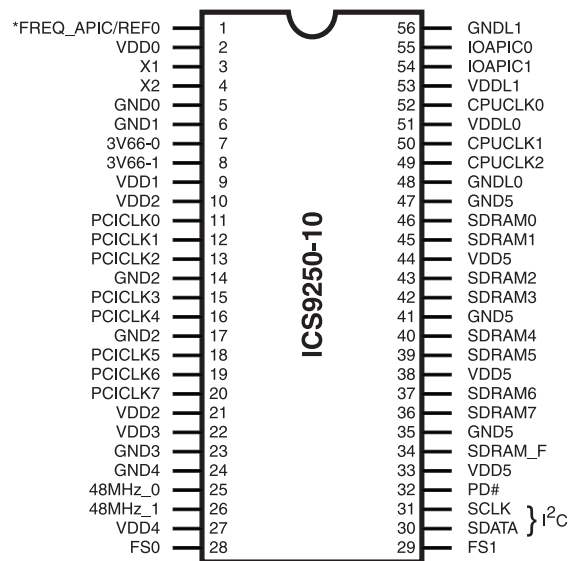
Features

- Generates the following system clocks:
 - 3 CPU (2.5V) 66.6/100 MHz (up to 133MHz through I²C selection)
 - 9 SDRAM (3.3V) up to 133MHz
 - 8 PCI (3.3 V) @33.3MHz
 - 2 IOAPIC (2.5V) @16.67 or 33.3MHz
 - 2 Hublink clocks (3.3 V) @ 66.6 MHz
 - 2 USB (3.3V) @ 48 MHz (Non spread spectrum)
 - 1 REF (3.3V) @14.318 MHz
- Supports spread spectrum modulation , down spread 0 to -0.5%
- I²C support for power management
- Efficient power management scheme through PD#
- Uses external 14.138 MHz crystal

Block Diagram



Pin Configuration



56-Pin 300 mil SSOP

*60K ohm pull-up to VDD on indicated inputs.

Power Groups

- VDD0, GND0 = REF & Crystal
- VDD1, GND1 = 3V66 [1:0]
- VDD2, GND2 = PCICLK [7:0]
- VDD3, GND3 = PLL core
- VDD4, GND4 = 48MHz [1:0]
- VDD5, GND5 = SDRAM_F, SDRAM [7:0]
- VDDL0, GNDL0 = CPUCLK [2:0]
- VDDL1, GNDL1 = IOAPIC [1:0]



Pin Descriptions

| PIN NUMBER | PIN NAME | TYPE | DESCRIPTION |
|----------------------------------|--------------|------|---|
| 1 | FREQ_APIC | IN | Latched input at Power On. this determines the IOAPIC frequency. When a "0" is latched, IOAPIC Freq=16.67MHz When "1" is latched, IOAPIC Freq=33.3MHz This pin has a 60K internal pull-up. |
| | REF0 | OUT | 3.3V, 14.318MHz reference clock output. |
| 3 | X1 | IN | Crystal input, has internal load cap (33pF) and feedback resistor from X2 |
| 4 | X2 | OUT | Crystal output, nominally 14.318MHz. Has internal load cap (33pF) |
| 5, 6, 14, 17, 23, 24, 35, 41, 47 | GND (0:5) | PWR | Ground pins for 3.3V supply |
| 8, 7 | 3V66 [1:0] | OUT | 3.3V Fixed 66MHz clock outputs for HUB |
| 2, 9, 10, 21, 22, 27, 33, 38, 44 | VDD (0:5) | PWR | 3.3V power supply |
| 20,19,18,16, 15,13,12,11 | PCICLK[7:0] | OUT | 3.3V PCI clock outputs, with Synchronous CPUCLKS |
| 25, 26 | 48MHz (0:1) | OUT | 3.3V Fixed 48MHz clock outputs for USB |
| 28, 29 | FS (0:1) | IN | Function Select pins. Determines CPU frequency, all output functionality. Please refer to Functionality table on page 3. |
| 30 | SDATA | IN | Data input for I ² C serial input. |
| 31 | SCLK | IN | Clock input of I ² C input |
| 32 | PD# | IN | Asynchronous active low input pin used to power down the device into a low power state. The internal clocks are disabled and the VCO and the crystal are stopped. The latency of the power down will not be greater than 3ms. |
| 36, 37, 39, 40, 42, 43, 45, 46 | SDRAM [7:0] | OUT | 3.3V output running 100MHz. All SDRAM outputs can be turned off through I ² C |
| 34 | SDRAM_F | OUT | 3.3V free running 100MHz SDRAM not affected by I ² C |
| 56,48 | GNDL [1:0] | PWR | Ground for 2.5V power supply for CPU & APIC |
| 49,50,52 | CPUCLK [2:0] | OUT | 2.5V Host bus clock output. 66MHz or 100MHz depending on FS (0:1) pins Refer page 3. |
| 51, 53 | VDDL (0:1) | PWR | 2.5V power supply for CPU & IOAPIC |
| 54, 55 | IOAPIC [1:0] | OUT | 2.5V clock outputs running at 16.67MHz or 33.3MHz. |



Functionality Table

| FS1 | FS0 | CPU | SDRAM | 3V66 | PCICLK | 48MHz | REF0 | IOAPIC | Notes |
|-----|-----|---------|---------|--------|--------|--------|-----------|----------|-----------|
| 0 | 0 | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Tristate |
| 0 | 1 | TCLK/2 | TCLK/4 | TCLK/4 | TCLK/8 | TCLK/2 | TCLK | TCLK/16 | Test Mode |
| 1 | 0 | 66 MHz | 100 MHz | 66 MHz | 33 MHz | 48 MHz | 14.318MHz | 16.67MHz | |
| 1 | 1 | 100 MHz | 100 MHz | 66 MHz | 33MHz | 48 MHz | 14.318MHZ | 16.67MHz | |

Clock Enable Configuration

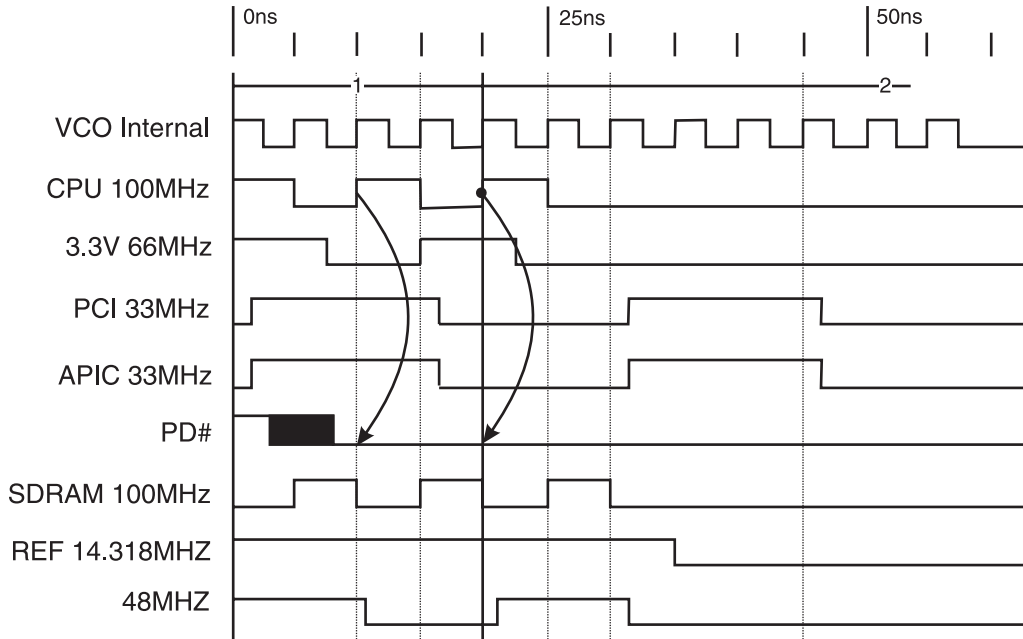
| PD# | CPUCLK | SDRAM | IOAPIC | 66MHz | PCICLK | REF, 48MHz | Osc | VCOs |
|-----|--------|-------|--------|-------|--------|---------------|-----|------|
| 0 | LOW | LOW | LOW | LOW | LOW | LOW | OFF | OFF |
| 1 | ON | ON | ON | ON | ON | ON | ON | ON |

Select Functions

| FS1 | FS0 | Notes |
|-----|-----|---------------------|
| 0 | 0 | Tristate |
| 0 | 1 | Test Mode |
| 1 | 0 | Active CPU = 66MHz |
| 1 | 1 | Active CPU = 100MHz |



Power Down Waveform



Note

1. After PD# is sampled active (Low) for 2 consecutive rising edges of CPUCLKs, all the output clocks are driven Low on their next High to Low transition.
2. Power-up latency < 3ms.
3. Waveform shown for 100MHz

Maximum Allowed Current

| 810E Condition | Max 2.5V supply consumption Max discrete cap loads, Vddq2 = 2.625V All static inputs = Vddq3 or GND | Max 2.5V supply consumption Max discrete cap loads, Vddq2 = 3.465V All static inputs = Vddq3 or GND |
|------------------------------------|--|--|
| Powerdown Mode (PWRDWN# = 0) | 10mA | 10mA |
| Full Active 66MHz SEL1, 0 = 10 | 70mA | 280mA |
| Full Active 100MHz SEL1, 0 = 11 | 100mA | 280mA |



General I²C serial interface information

The information in this section assumes familiarity with I²C programming.
For more information, contact ICS for an I²C programming application note.

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2_(H)
- ICS clock will **acknowledge**
- Controller (host) sends a dummy command code
- ICS clock will **acknowledge**
- Controller (host) sends a dummy byte count
- ICS clock will **acknowledge**
- Controller (host) starts sending first byte (Byte 0) through byte 5
- ICS clock will **acknowledge** each byte *one at a time*.
- Controller (host) sends a Stop bit

| How to Write: | |
|------------------------------|----------------------|
| Controller (Host) | ICS (Slave/Receiver) |
| Start Bit | |
| Address D2 _(H) | |
| | ACK |
| Dummy Command Code | |
| | ACK |
| Dummy Byte Count | |
| | ACK |
| Byte 0 | |
| | ACK |
| Byte 1 | |
| | ACK |
| Byte 2 | |
| | ACK |
| Byte 3 | |
| | ACK |
| Byte 4 | |
| | ACK |
| Byte 5 | |
| | ACK |
| Stop Bit | |

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address D3_(H)
- ICS clock will **acknowledge**
- ICS clock will send the **byte count**
- Controller (host) acknowledges
- ICS clock sends first byte (**Byte 0**) through **byte 5**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

| How to Read: | |
|------------------------------|----------------------|
| Controller (Host) | ICS (Slave/Receiver) |
| Start Bit | |
| Address D3 _(H) | |
| | ACK |
| | Byte Count |
| ACK | |
| | Byte 0 |
| ACK | |
| | Byte 1 |
| ACK | |
| | Byte 2 |
| ACK | |
| | Byte 3 |
| ACK | |
| | Byte 4 |
| ACK | |
| | Byte 5 |
| ACK | |
| Stop Bit | |

Notes:

1. The ICS clock generator is a slave/receiver, I²C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol.**
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I²C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.



Byte 5: ICS Reserved Functionality and frequency select register (Default=0)

| Bit | Description | | | | | | | | PWD |
|----------------|--|----------------|----------------|----------------|---------------|--------------|-------------|---------------|----------------|
| Bit7 | ICS RESERVED BIT (Needs to be 0 clock to operate normal) | | | | | | | | 0 |
| Bit6 | ICS RESERVED BIT (Needs to be 0 clock to operate normal) | | | | | | | | 0 |
| Bit5 | ICS RESERVED BIT (Needs to be 0 clock to operate normal) | | | | | | | | 0 |
| Bit (4,3,0) | Bit (4,3,0) | | | | CPUCLK MHz | SDRAM MHz | 3V66 MHz | PCICLK MHz | XXXX Note 1 |
| | FS0 (HW) | SEL3 (Bit4) | SEL2 (Bit3) | SEL1 (Bit0) | | | | | |
| | 0 | 0 | 0 | 0 | 66.67 | 100 | 66.67 | 33.33 | |
| | 0 | 0 | 0 | 1 | 70.67 | 106 | 70.67 | 35.33 | |
| | 0 | 0 | 1 | 0 | 74.66 | 112 | 74.67 | 37.33 | |
| | 0 | 0 | 1 | 1 | 82.66 | 124 | 82.66 | 41.33 | |
| | 0 | 1 | 0 | 0 | 63.5 | 95.25 | 63.5 | 31.75 | |
| | 0 | 1 | 0 | 1 | 68.67 | 103 | 68.67 | 34.33 | |
| | 0 | 1 | 1 | 0 | 72.67 | 109 | 72.67 | 36.33 | |
| | 0 | 1 | 1 | 1 | 88.66 | 133 | 88.66 | 44.33 | |
| | 1 | 0 | 0 | 0 | 100 | 100 | 66.67 | 33.33 | |
| | 1 | 0 | 0 | 1 | 106 | 106 | 70.67 | 35.33 | |
| | 1 | 0 | 1 | 0 | 112 | 112 | 74.67 | 37.33 | |
| | 1 | 0 | 1 | 1 | 124 | 124 | 82.66 | 41.33 | |
| | 1 | 1 | 0 | 0 | 95.25 | 95.25 | 63.5 | 31.75 | |
| | 1 | 1 | 0 | 1 | 103 | 103 | 68.67 | 34.33 | |
| | 1 | 1 | 1 | 0 | 109 | 109 | 72.67 | 36.33 | |
| 1 | 1 | 1 | 1 | 133 | 133 | 88.66 | 44.33 | | |
| Bit2 | Not used (Needs to be 1 for normal clock operation) | | | | | | | | 1 |
| Bit1 | Not used (Needs to be 1 for normal clock operation) | | | | | | | | 1 |

Note1: Default at power-up will be for latched logic inputs to define frequency, as displayed by Bit 3.

**Byte 0: Control Register**

(1 = enable, 0 = disable)

| Bit | Pin# | Name | PWD | Description |
|-------|------|--------------------------------|-----|-------------------|
| Bit 7 | | Reserved | 0 | (Active/Inactive) |
| Bit 6 | | Reserved | 0 | (Active/Inactive) |
| Bit 5 | | Reserved | 0 | (Active/Inactive) |
| Bit 4 | | Reserved | 1 | (Active/Inactive) |
| Bit 3 | | SpreadSpectrum (1=On/0=Off) | 1 | (Active/Inactive) |
| Bit 2 | 26 | 48MHz 1 | 1 | (Active/Inactive) |
| Bit 1 | 25 | 48MHz 0 | 1 | (Active/Inactive) |
| Bit 0 | 49 | CPUCLK2 | 1 | (Active/Inactive) |

Byte 1: Control Register

(1 = enable, 0 = disable)

| Bit | Pin# | Name | PWD | Description |
|-------|------|--------|-----|-------------------|
| Bit 7 | 36 | SDRAM7 | 1 | (Active/Inactive) |
| Bit 6 | 37 | SDRAM6 | 1 | (Active/Inactive) |
| Bit 5 | 39 | SDRAM5 | 1 | (Active/Inactive) |
| Bit 4 | 40 | SDRAM4 | 1 | (Active/Inactive) |
| Bit 3 | 42 | SDRAM3 | 1 | (Active/Inactive) |
| Bit 2 | 43 | SDRAM2 | 1 | (Active/Inactive) |
| Bit 1 | 45 | SDRAM1 | 1 | (Active/Inactive) |
| Bit 0 | 46 | SDRAM0 | 1 | (Active/Inactive) |

Byte 2: Control Register

(1 = enable, 0 = disable)

| Bit | Pin# | Name | PWD | Description |
|-------|------|----------|-----|-------------------|
| Bit 7 | 20 | PCICLK7 | 1 | (Active/Inactive) |
| Bit 6 | 19 | PCICLK6 | 1 | (Active/Inactive) |
| Bit 5 | 18 | PCICLK5 | 1 | (Active/Inactive) |
| Bit 4 | 16 | PCICLK4 | 1 | (Active/Inactive) |
| Bit 3 | 15 | PCICLK3 | 1 | (Active/Inactive) |
| Bit 2 | 13 | PCICLK2 | 1 | (Active/Inactive) |
| Bit 1 | 12 | PCICLK1 | 1 | (Active/Inactive) |
| Bit 0 | - | Reserved | 0 | (Active/Inactive) |

Notes:

1. Inactive means outputs are held LOW and are disabled from switching. These outputs are designed to be configured at power-on and are not expected to be configured during the normal modes of operation.
2. PWD = Power on Default



Byte 3: Reserved Register

(1 = enable, 0 = disable)

| Bit | Pin# | Name | PWD | Description |
|-------|------|----------|-----|-------------------|
| Bit 7 | - | Reserved | 0 | (Active/Inactive) |
| Bit 6 | - | Reserved | 0 | (Active/Inactive) |
| Bit 5 | - | Reserved | 0 | (Active/Inactive) |
| Bit 4 | - | Reserved | 0 | (Active/Inactive) |
| Bit 3 | - | Reserved | 0 | (Active/Inactive) |
| Bit 2 | - | Reserved | 0 | (Active/Inactive) |
| Bit 1 | - | Reserved | 0 | (Active/Inactive) |
| Bit 0 | - | Reserved | 0 | (Active/Inactive) |

Byte 4: Reserved Register

(1 = enable, 0 = disable)

| Bit | Pin# | Name | PWD | Description |
|-------|------|----------|-----|-------------------|
| Bit 7 | - | Reserved | 0 | (Active/Inactive) |
| Bit 6 | - | Reserved | 0 | (Active/Inactive) |
| Bit 5 | - | Reserved | 0 | (Active/Inactive) |
| Bit 4 | - | Reserved | 0 | (Active/Inactive) |
| Bit 3 | - | Reserved | 0 | (Active/Inactive) |
| Bit 2 | - | Reserved | 0 | (Active/Inactive) |
| Bit 1 | - | Reserved | 0 | (Active/Inactive) |
| Bit 0 | - | Reserved | 0 | (Active/Inactive) |

Notes:

1. Inactive means outputs are held LOW and are disabled from switching. These outputs are designed to be configured at power-on and are not expected to be configured during the normal modes of operation.
2. PWD = Power on Default

Absolute Maximum Ratings

| | |
|-------------------------------------|-------------------------------------|
| Core Supply Voltage | 4.6 V |
| I/O Supply Voltage | 3.6V |
| Logic Inputs | GND-0.5 V to V _{DD} +0.5 V |
| Ambient Operating Temperature | 0°C to +70°C |
| Storage Temperature | -65°C to +150°C |

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.



Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70°C; Supply Voltage V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5% (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | |
|--------------------------------|-------------------------------------|---|----------------------|-------|----------------------|-------|----|
| Input High Voltage | V _{IH} | | 2 | | V _{DD} +0.3 | V | |
| Input Low Voltage | V _{IL} | | V _{SS} -0.3 | | 0.8 | V | |
| Input High Current | I _{IH} | V _{IN} = V _{DD} | -5 | | 5 | μA | |
| Input Low Current | I _{IL1} | V _{IN} = 0 V; Inputs with no pull-up resistors | -5 | 2 | | μA | |
| | I _{IL2} | V _{IN} = 0 V; Inputs with pull-up resistors | -200 | -100 | | | |
| Operating Supply Current | I _{DD3.3OP} | C _L = 0 pF; Select @ 66 MHz | | 97 | 110 | mA | |
| | | C _L = 0 pF; Select @ 100 MHz | | 91 | 105 | | |
| | | C _L = 0 pF; Select @ 133 MHz | | 100 | 130 | | |
| | | C _L = Max loads; Select @ 66 MHz | | 275 | 310 | mA | |
| | | C _L = Max loads; Select @ 100 MHz | | 267 | 300 | | |
| | | C _L = Max loads; Select @ 133 MHz | | 278 | 350 | | |
| | I _{DD2.5OP} | C _L = 0 pF; Select @ 66 MHz | | | 8 | 10 | mA |
| | | C _L = 0 pF; Select @ 100 MHz | | | 11 | 15 | |
| | | C _L = 0 pF; Select @ 133 MHz | | | 13 | 20 | |
| | | C _L = Max loads; Select @ 66 MHz | | | 22 | 70 | mA |
| | | C _L = Max loads; Select @ 100 MHz | | | 31 | 100 | |
| | | C _L = Max loads; Select @ 133 MHz | | | 37 | 130 | |
| Powerdown Current | I _{DD3.3PD} | C _L = Max loads | | 220 | 400 | μA | |
| | I _{DD.25PD} | Input address VDD or GND | | <1 | 10 | | |
| Input Frequency | F _i | V _{DD} = 3.3 V | 12 | 14.32 | 16 | MHz | |
| Pin Inductance | L _{pin} | | | 7 | | nH | |
| Input Capacitance ¹ | C _{IN} | Logic Inputs | | | 5 | pF | |
| | C _{OUT} | Output pin capacitance | | 6 | | pF | |
| | C _{INX} | X1 & X2 pins | 27 | | 45 | pF | |
| Transition time ¹ | T _{trans} | To 1st crossing of target frequency | | | 5 | ms | |
| Settling time ¹ | T _s | From 1st crossing to 1% target frequency | | | 5 | ms | |
| Clk Stabilization ¹ | T _{STAB} | From V _{DD} = 3.3 V to 1% target frequency | | | 5 | ms | |
| Delay ¹ | t _{PZH} , t _{PZL} | Output enable delay (all outputs) | 1 | | 10 | ns | |
| | t _{PHZ} , t _{PLZ} | Output disable delay (all outputs) | 1 | | 10 | ns | |

¹Guaranteed by design, not 100% tested in production.



Electrical Characteristics - CPU

$T_A = 0 - 70^\circ\text{C}$; $V_{DDL} = 2.5 \text{ V} \pm 5\%$; $C_L = 10\text{-}20 \text{ pF}$ (unless otherwise specified)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------------------|-----------------|--|------|------|-----|----------|
| Output Impedance | R_{DSP2B}^1 | $V_O = V_{DD}*(0.5)$ | 13.5 | 16 | 45 | Ω |
| Output Impedance | R_{DSN2B}^1 | $V_O = V_{DD}*(0.5)$ | 13.5 | 21 | 45 | Ω |
| Output High Voltage | V_{OH2B} | $I_{OH} = -1 \text{ mA}$ | 2 | | | V |
| Output Low Voltage | V_{OL2B} | $I_{OL} = 1 \text{ mA}$ | | | 0.4 | V |
| Output High Current | I_{OH2B} | $V_{OH @ MIN} = 1.0 \text{ V}$ | -27 | -68 | | mA |
| | | $V_{OH @ MAX} = 2.375 \text{ V}$ | | -9 | -27 | |
| Output Low Current | I_{OL2B} | $V_{OL @ MIN} = 1.2 \text{ V}$ | 27 | 54 | | mA |
| | | $V_{OL @ MAX} = 0.3 \text{ V}$ | | 11 | 30 | |
| Rise Time ¹ | t_{r2B} | $V_{OL} = 0.4 \text{ V}, V_{OH} = 2.0 \text{ V}$ | 0.4 | 1.45 | 1.6 | ns |
| Fall Time ¹ | t_{f2B} | $V_{OH} = 2.0 \text{ V}, V_{OL} = 0.4 \text{ V}$ | 0.4 | 1.35 | 1.6 | ns |
| Duty Cycle ¹ | d_{t2B} | $V_T = 1.25 \text{ V}$ | 45 | 51 | 55 | % |
| Skew window ¹ | t_{sk2B} | $V_T = 1.25 \text{ V}$ | | 114 | 175 | ps |
| Jitter, Cycle-to-cycle ¹ | $t_{jyc-cyc2B}$ | $V_T = 1.25 \text{ V}$ | | 157 | 250 | ps |

¹Guaranteed by design, not 100% tested in production.

Electrical Characteristics - 3V66

$T_A = 0 - 70^\circ\text{C}$; $V_{DD} = 3.3 \text{ V} \pm 5\%$; $C_L = 10\text{-}20 \text{ pF}$ (unless otherwise specified)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------------------|----------------|--|-----|------|------|----------|
| Output Impedance | R_{DSP1B}^1 | $V_O = V_{DD}*(0.5)$ | 12 | 14 | 55 | Ω |
| Output Impedance | R_{DSN1B}^1 | $V_O = V_{DD}*(0.5)$ | 12 | 14.5 | 55 | Ω |
| Output High Voltage | V_{OH1} | $I_{OH} = -1 \text{ mA}$ | 2.4 | | | V |
| Output Low Voltage | V_{OL1} | $I_{OL} = 1 \text{ mA}$ | | | 0.55 | V |
| Output High Current | I_{OH1} | $V_{OH @ MIN} = 1.0 \text{ V}$ | -33 | -108 | | mA |
| | | $V_{OH @ MAX} = 3.135 \text{ V}$ | | -9 | -33 | |
| Output Low Current | I_{OL1} | $V_{OL @ MIN} = 1.95 \text{ V}$ | 30 | 95 | | mA |
| | | $V_{OL @ MAX} = 0.4 \text{ V}$ | | 29 | 38 | |
| Rise Time ¹ | t_{r1} | $V_{OL} = 0.4 \text{ V}, V_{OH} = 2.4 \text{ V}$ | 0.4 | 1.3 | 1.6 | ns |
| Fall Time ¹ | t_{f1} | $V_{OH} = 2.4 \text{ V}, V_{OL} = 0.4 \text{ V}$ | 0.4 | 1.29 | 1.6 | ns |
| Duty Cycle ¹ | d_{t1} | $V_T = 1.5 \text{ V}$ | 45 | 51.9 | 55 | % |
| Skew window ¹ | t_{sk1} | $V_T = 1.5 \text{ V}$ | | 77 | 175 | ps |
| Jitter, Cycle-to-cycle ¹ | $t_{jyc-cyc1}$ | $V_T = 1.5 \text{ V}$ | | 129 | 500 | ps |

¹Guaranteed by design, not 100% tested in production.



Electrical Characteristics - IOAPIC

$T_A = 0 - 70^\circ\text{C}$; $V_{DDL} = 2.5 \text{ V} \pm 5\%$; $C_L = 10\text{-}20 \text{ pF}$ (unless otherwise specified)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------------|---------------|--|-----|------|-----|----------|
| Output Impedance | R_{DSP4B}^1 | $V_O = V_{DD}*(0.5)$ | 9 | 16 | 30 | Ω |
| Output Impedance | R_{DSN4B}^1 | $V_O = V_{DD}*(0.5)$ | 9 | 20 | 30 | Ω |
| Output High Voltage | V_{OH4B} | $I_{OH} = -1 \text{ mA}$ | 2 | | | V |
| Output Low Voltage | V_{OL4B} | $I_{OL} = 1 \text{ mA}$ | | | 0.4 | V |
| Output High Current | I_{OH4B} | $V_{OH @ MIN} = 1.0 \text{ V}$ | -27 | -68 | | mA |
| | | $V_{OH @ MAX} = 2.375 \text{ V}$ | | -9 | -27 | |
| Output Low Current | I_{OL4B} | $V_{OL @ MIN} = 1.2 \text{ V}$ | 27 | 54 | | mA |
| | | $V_{OL @ MAX} = 0.3 \text{ V}$ | | 11 | 30 | |
| Rise Time ¹ | t_{r4B} | $V_{OL} = 0.4 \text{ V}, V_{OH} = 2.0 \text{ V}$ | 0.4 | 1.4 | 1.6 | ns |
| Fall Time ¹ | t_{f4B} | $V_{OH} = 2.0 \text{ V}, V_{OL} = 0.4 \text{ V}$ | 0.4 | 1.45 | 1.6 | ns |
| Duty Cycle ¹ | d_{t4B} | $V_T = 1.25 \text{ V}$ | 45 | 49.9 | 55 | % |
| Skew window ¹ | t_{sk4B} | $V_T = 1.25 \text{ V}$ | | 20 | 250 | ps |
| Jitter, Absolute ¹ | t_{abs} | $V_T = 1.25 \text{ V}$ | | 127 | 500 | ps |

¹Guaranteed by design, not 100% tested in production.

Electrical Characteristics - SDRAM

$T_A = 0 - 70^\circ\text{C}$; $V_{DD} = 3.3 \text{ V} \pm 5\%$; $C_L = 20\text{-}30 \text{ pF}$ (unless otherwise specified)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------------------|----------------|--|-----|------|-----|----------|
| Output Impedance | R_{DSP3B}^1 | $V_O = V_{DD}*(0.5)$ | 10 | 12 | 24 | Ω |
| Output Impedance | R_{DSN3B}^1 | $V_O = V_{DD}*(0.5)$ | 10 | 15 | 24 | Ω |
| Output High Current | I_{OH3} | $V_{OH @ MIN} = 2.0 \text{ V}$ | -54 | -92 | | mA |
| | | $V_{OH @ MAX} = 3.135 \text{ V}$ | | -16 | -46 | |
| Output Low Current | I_{OL3} | $V_{OL @ MIN} = 1.0 \text{ V}$ | 54 | 68 | | mA |
| | | $V_{OL @ MAX} = 0.4 \text{ V}$ | | 29 | 53 | |
| Rise Time ¹ | t_{r3} | $V_{OL} = 0.4 \text{ V}, V_{OH} = 2.4 \text{ V}$ | 0.4 | 1 | 1.6 | ns |
| Fall Time ¹ | t_{f3} | $V_{OH} = 2.4 \text{ V}, V_{OL} = 0.4 \text{ V}$ | 0.4 | 1.1 | 1.6 | ns |
| Duty Cycle ¹ | d_{t3} | $V_T = 1.5 \text{ V}$ | 45 | 50.5 | 55 | % |
| Skew window ¹ | t_{sk3} | $V_T = 1.5 \text{ V}$ | | 148 | 250 | ps |
| Jitter, Cycle-to-cycle ¹ | $t_{jcc-cyc3}$ | $V_T = 1.5 \text{ V}, 66, 100 \text{ MHz}$ | | 152 | 250 | ps |

¹Guaranteed by design, not 100% tested in production.



Electrical Characteristics - PCI

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%; C_L = 10-30 pF (unless otherwise specified)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------------------|---------------------------------|--|-----|------|------|-------|
| Output Impedance | R _{DSP1B} ¹ | V _O = V _{DD} *(0.5) | 12 | 15 | 55 | Ω |
| Output Impedance | R _{D5N1B} ¹ | V _O = V _{DD} *(0.5) | 12 | 15 | 55 | Ω |
| Output High Voltage | V _{OH1} | I _{OH} = -1 mA | 2.4 | | | V |
| Output Low Voltage | V _{OL1} | I _{OL} = 1 mA | | | 0.55 | V |
| Output High Current | I _{OH1} | V _{OH} @ MIN = 1.0 V | -33 | -106 | | mA |
| | | V _{OH} @ MAX = 3.135 V | | -14 | -33 | |
| Output Low Current | I _{OL1} | V _{OL} @ MIN = 1.95 V | 30 | 94 | | mA |
| | | V _{OL} @ MAX = 0.4 V | | 29 | 38 | |
| Rise Time ¹ | t _{r1} | V _{OL} = 0.4 V, V _{OH} = 2.4 V | 0.4 | 1.75 | 2 | ns |
| Fall Time ¹ | t _{f1} | V _{OH} = 2.4 V, V _{OL} = 0.4 V | 0.4 | 1.55 | 2 | ns |
| Duty Cycle ¹ | d _{t1} | V _T = 1.5 V | 45 | 50.5 | 55 | % |
| Skew window ¹ | t _{sk1} | V _T = 1.5 V | | 270 | 500 | ps |
| Jitter, Cycle-to-cycle ¹ | t _{jcc-cycl} | V _T = 1.5 V | | 160 | 500 | ps |

¹Guaranteed by design, not 100% tested in production.

Electrical Characteristics - REF, 48MHz_0(Pin25)

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%; C_L = 10-20 pF (unless otherwise specified)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------|---------------------------------|--|-----|------|------|-------|
| Output Impedance | R _{DSP5B} ¹ | V _O = V _{DD} *(0.5) | 20 | 29 | 60 | Ω |
| Output Impedance | R _{D5N5B} ¹ | V _O = V _{DD} *(0.5) | 20 | 27 | 60 | Ω |
| Output High Voltage | V _{OH15} | I _{OH} = -1 mA | 2.4 | | | V |
| Output Low Voltage | V _{OL5} | I _{OL} = 1 mA | | | 0.55 | V |
| Output High Current | I _{OH5} | V _{OH} @ MIN = 1.0 V | -29 | -54 | | mA |
| | | V _{OH} @ MAX = 3.135 V | | -11 | -23 | |
| Output Low Current | I _{OL5} | V _{OL} @ MIN = 1.95 V | 29 | 54 | | mA |
| | | V _{OL} @ MAX = 0.4 V | | 16 | 27 | |
| Rise Time ¹ | t _{r5} | V _{OL} = 0.4 V, V _{OH} = 2.4 V | 0.4 | 2.35 | 4 | ns |
| Fall Time ¹ | t _{f5} | V _{OH} = 2.4 V, V _{OL} = 0.4 V | 0.4 | 2.65 | 4 | ns |
| Duty Cycle ¹ | d _{t5} | V _T = 1.5 V | 45 | 52 | 55 | % |
| Jitter, absolute | t _{abs} | V _T = 1.5 V, | | 332 | 500 | ps |

¹Guaranteed by design, not 100% tested in production.

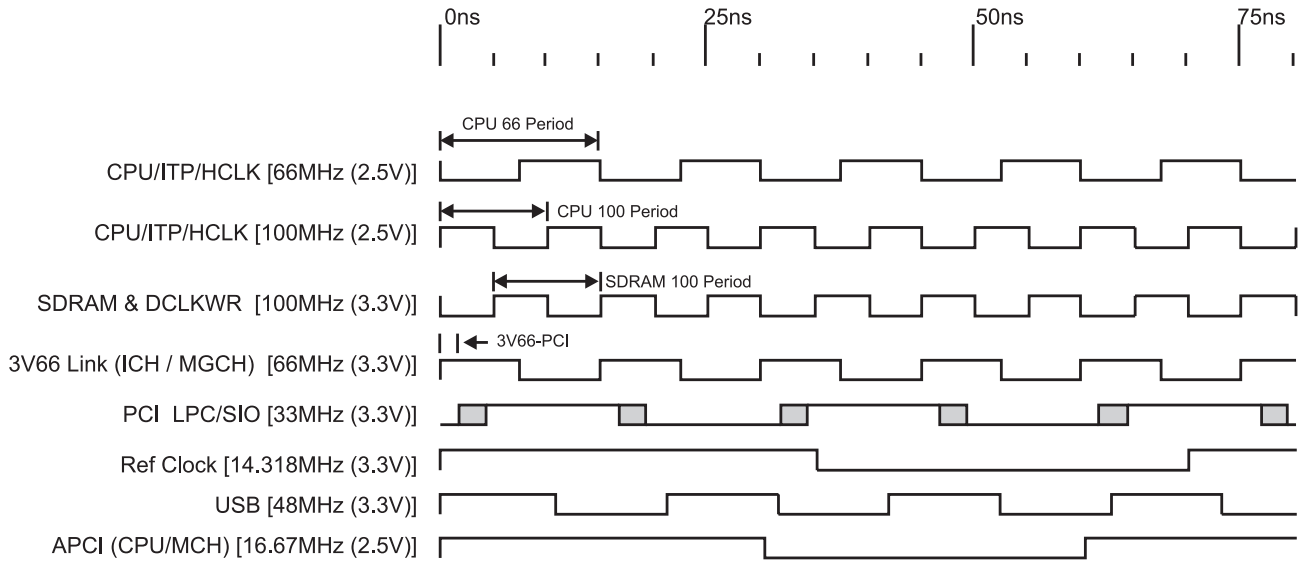


Electrical Characteristics - 48MHz_1 (Pin 26)

$T_A = 0 - 70^\circ\text{C}$; $V_{DD} = 3.3 \text{ V} \pm 5\%$; $C_L = 20\text{-}30 \text{ pF}$ (unless otherwise specified)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------------------|-------------------------|--|-----|-----|------|----------|
| Output Impedance | R_{DSP3B}^1 | $V_O = V_{DD} * (0.5)$ | 10 | 15 | 24 | Ω |
| Output Impedance | R_{DSN3B}^1 | $V_O = V_{DD} * (0.5)$ | 10 | 15 | 24 | Ω |
| Output High Voltage | V_{OH3} | $I_{OH} = -1 \text{ mA}$ | 2.4 | | | V |
| Output Low Voltage | V_{OL3} | $I_{OL} = 1 \text{ mA}$ | | | 0.55 | V |
| Output High Current | I_{OH3} | $V_{OH} @ \text{MIN} = 2.0 \text{ V}$ | -54 | -82 | | mA |
| | | $V_{OH} @ \text{MAX} = 3.135 \text{ V}$ | | -20 | -46 | |
| Output Low Current | I_{OL3} | $V_{OL} @ \text{MIN} = 1.0 \text{ V}$ | 54 | 95 | | mA |
| | | $V_{OL} @ \text{MAX} = 0.4 \text{ V}$ | | 28 | 53 | |
| Rise Time ¹ | t_{r3} | $V_{OL} = 0.4 \text{ V}, V_{OH} = 2.4 \text{ V}$ | 0.4 | 1.1 | 1.6 | ns |
| Fall Time ¹ | t_{f3} | $V_{OH} = 2.4 \text{ V}, V_{OL} = 0.4 \text{ V}$ | 0.4 | 1.3 | 1.6 | ns |
| Duty Cycle ¹ | d_{t3} | $V_T = 1.5 \text{ V}$ | 45 | 53 | 55 | % |
| Jitter, Cycle-to-cycle ¹ | $t_{j\text{cyc-cyc}3B}$ | $V_T = 1.5 \text{ V}$ | | 130 | 250 | ps |

¹Guaranteed by design, not 100% tested in production.



Group Offset Waveforms

Group Skews at Common Transition Edges: (CPU = 66MHz)

CPU & IOAPIC load (lumped) = 20pf; PCI, SDRAM, 3V66 LOAD (LUMPED) = 30pf.

| GROUP | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------|--------------------------|--|-----|-----|-----|-------|
| CPU to 3V66 | S _{CPUI-3V66} | CPU @ 1.25V, 3V66 @ 1.5V (Note: 180° offset between CPU & 66MHz) | 0 | | 500 | ps |
| CPU to SDRAM | S _{CPUI2-SDRAM} | CPU @ 1.25V, SDRAM @ 1.5V (Note: 180° offset between CPU & 66MHz) | 0 | | 500 | ps |
| 3V66 to PCI | S _{3V66-PCI} | 3V66 @ 1.5V, PCI @ 1.5V | 1.5 | | 4 | ns |
| IOAPIC to PCI | S _{IOAPIC-PCI} | IOAPIC @ 1.25V, PCI @ 1.5V | 0 | | 500 | ps |

¹Guaranteed by design, not 100% tested in production.

Group Skews at Common Transition Edges: (CPU = 100MHz)

CPU & IOAPIC load (lumped) = 20pf; PCI, SDRAM, 3V66 LOAD (LUMPED) = 30pf.

| GROUP | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------|--------------------------|---|-----|-----|-----|-------|
| CPU to 3V66 | S _{CPUI-3V66} | CPU @ 1.25V, 3V66 @ 1.5V (Note: 180° offset between CPU & 100MHz) | 0 | | 500 | ps |
| CPU to SDRAM | S _{CPUI2-SDRAM} | CPU @ 1.25V, SDRAM @ 1.5V (Note: 180° offset between CPU & 100MHz) | 0 | | 500 | ps |
| 3V66 to PCI | S _{3V66-PCI} | 3V66 @ 1.5V, PCI @ 1.5V | 1.5 | | 4 | ns |
| IOAPIC to PCI | S _{IOAPIC-PCI} | IOAPIC @ 1.25V, PCI @ 1.5V | 0 | | 500 | ps |

¹Guaranteed by design, not 100% tested in production.



General Layout Precautions:

- 1) Use a ground plane on the top layer of the PCB in all areas not used by traces.
- 2) Make all power traces and vias as wide as possible to lower inductance.

Notes:

- 1) All clock outputs should have series terminating resistor. Not shown in all places to improve readability of diagram.
- 2) 47 ohm / 56pf RC termination should be used on all over 50MHz outputs.
- 3) Optional crystal load capacitors are recommended.

Capacitor Values:

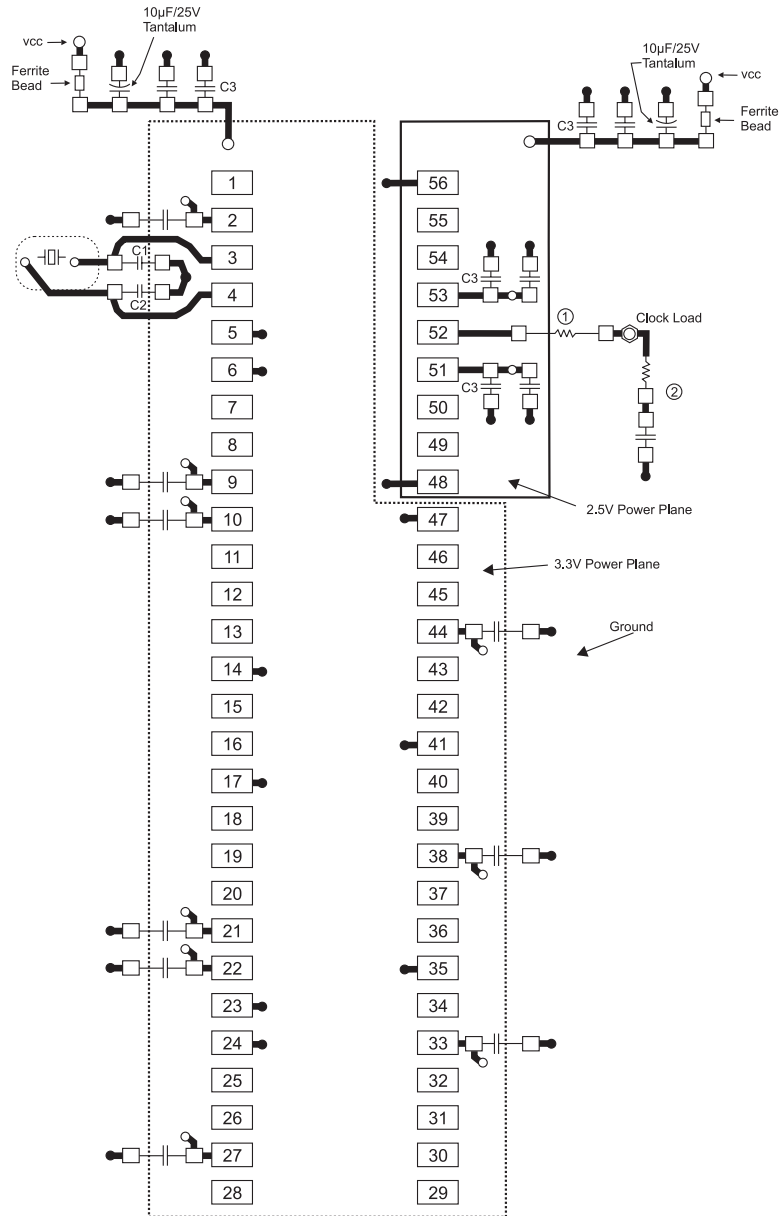
C1, C2 : Crystal load values determined by user

C3 : 100pF ceramic

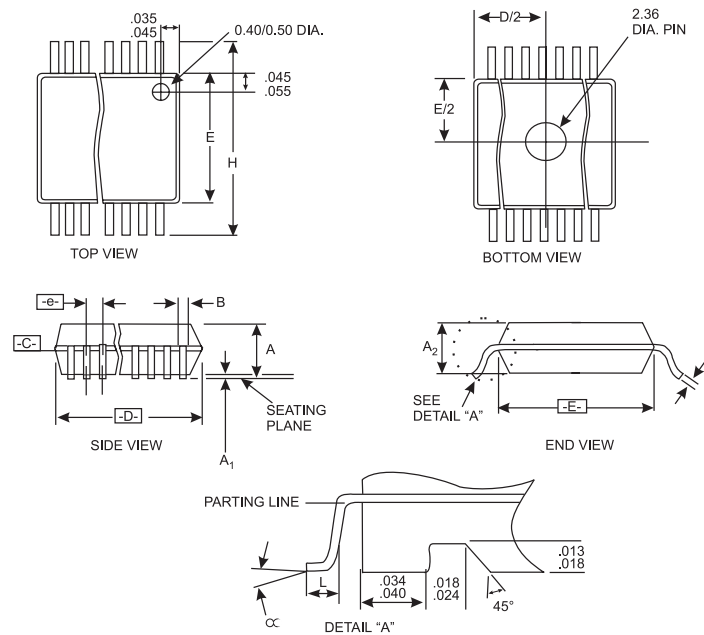
All unmarked capacitors are 0.01μF ceramic

Connections to VDD:

- Best
- Okay
- Avoid
- Avoid



- = Ground Plane Connection
- = Power Plane Connection
- = Solder Pads
- ⊗ = Clock Load



SSOP Package

| SYMBOL | COMMON DIMENSIONS | | | VARIATIONS | D | | | N |
|--------|-------------------|------|-------|------------|------|------|------|----|
| | MIN. | NOM. | MAX. | | MIN. | NOM. | MAX. | |
| A | .095 | .101 | .110 | AC | .620 | .625 | .630 | 48 |
| A1 | .008 | .012 | .016 | AD | .720 | .725 | .730 | 56 |
| A2 | .088 | .090 | .092 | | | | | |
| B | .008 | .010 | .0135 | | | | | |
| C | .005 | .006 | .0085 | | | | | |
| D | See Variations | | | | | | | |
| E | .292 | .296 | .299 | | | | | |
| e | 0.025 BSC | | | | | | | |
| H | .400 | .406 | .410 | | | | | |
| h | .010 | .013 | .016 | | | | | |
| L | .024 | .032 | .040 | | | | | |
| N | See Variations | | | | | | | |
| ∞ | 0° | 5° | 8° | | | | | |
| X | .085 | .093 | .100 | | | | | |

Ordering Information

ICS9250yF-10

Example:

ICS XXXX y F - PPP

