MAXM17516

6A, 2.4V to 5.5V Input, High-Efficiency Power Module

General Description

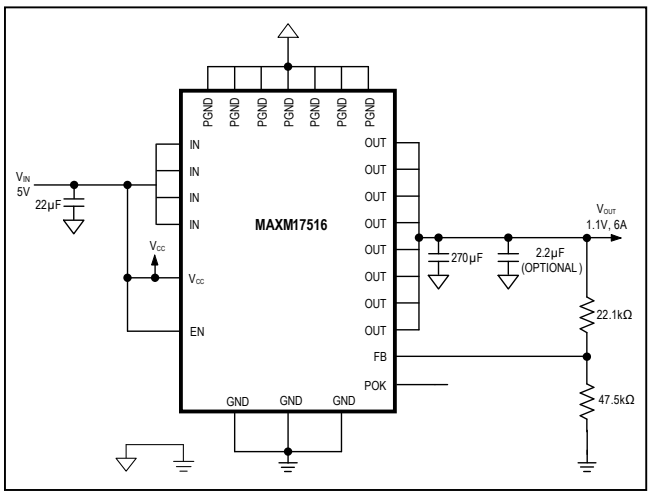
The *Himalaya* series of voltage regulator ICs and power modules enable cooler, smaller, and simpler power supply solutions. The MAXM17516 is a fixed-frequency, step-down power module in a thermally-efficient system-in-package (SiP) package that operates from a 2.4V to 5.5V input supply voltage and supports output currents up to 6A. The device includes a switch-mode power-supply controller, dual n-channel MOSFET power switches, a fully-shielded inductor, as well as compensation components. The device supports 0.75V to 1.8V programmable output voltage. The high level of integration significantly reduces design complexity, manufacturing risks, and offers a true plug-and-play power-supply solution, reducing the time to market.

The MAXM17516 is available in a thermally-enhanced, compact 28-pin, 10mm x 6.5mm x 2.8mm SiP and can operate over the -40°C to +125°C industrial temperature range.

Applications

- FPGA and DSP Point-of-Load Regulator
- Base Station Point-of-Load Regulator
- Industrial Control Equipment
- Servers
- ATE Equipment
- Medical Equipment

Typical Application Circuit



Benefits and Features

- Reduces Design Complexity, Manufacturing Risks, and Time-to-Market
  - Complete Integrated Step-Down Power Supply in a Single Package
- Saves Board Space in Space-Constrained Applications
  - Small Form Factor 6.5mm x 10mm x 2.8mm SiP Package
  - Simplified PCB Design with as Few as Four External Components
- Offers Flexibility for Power-Design Optimization
  - 2.4V to 5.5V Input Voltage Range
  - 0.75V to 1.8V Programmable Output Voltage
  - 6A Output Current
  - Fixed 1MHz Switching Frequency
  - Enable Input
  - Power-Good Output
- Reduces Power Dissipation
  - Up to 94% Efficiency
  - Autoswitch, Light-Load, Pulse-Skipping Mode
  - High Impedance Shutdown
  - < 1µA Shutdown Current
- Operates Reliably and Reduces System Downtime
  - Voltage-Controlled Internal Soft-Start
  - Fault Protection
  - Output Undervoltage/Overvoltage Protection
  - Thermal-Fault Protection
  - Peak Current Limit
  - -40°C to +125°C Operation

***Ordering Information* appears at end of data sheet.**

maxim integrated™

Absolute Maximum Ratings

IN to PGND .....-0.3V to +6V
V_{CC} to GND .....-0.3V to +6V
V_{CC} to IN.....-0.3V to +6V
EN to GND .....-0.3V to +6V
FB, POK to GND .....-0.3V to (V_{CC} + 0.3V)
OUT, EP3 to GND .....-0.6V to (V_{IN} + 0.3V)
PGND to GND .....-0.3V to +0.3V
EP1 to GND.....-0.3V to +0.3V
EP2 to PGND ..... -0.3V to + (V_{IN} + 0.3V)
EP2 to GND..... -0.6V to + (V_{IN} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
28-Pin SIP (derate 37mW/°C above +70°C) 2000mW
Operating Temperature Range..... -40°C to +125°C
Junction Temperature.....+125°C
Storage Temperature Range..... -55°C to +150°C
Lead Temperature (soldering, 10s) .....+245°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

SiP
Junction-to-Ambient Thermal Resistance (θ_{JA}).....25°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) .....6°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{IN} = V_{CC} = V_{EN} = 5V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted. See *Typical Application Circuit.*) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY (V_{IN})						
IN Input Voltage Range	V_{IN}		2.4		5.5	V
		V_{IN} = V_{CC}	4.5		5.5	
IN Undervoltage Threshold		Rising edge (100mV hysteresis)	2.05	2.19	2.4	V
IN Standby Supply Current	I_Q	V_{IN} = V_{CC} = 4.5V, no load		1	5.5	µA
V_{CC} SUPPLY						
V_{CC} Input Voltage Range	V_{CC}		4.5		5.5	V
V_{CC} Undervoltage Threshold		Rising edge (160mV hysteresis)	3.9	4.2	4.5	V
V_{CC} Shutdown Supply Current	I_{VCC_SHD}	EN = GND, POK unconnected, measured at V_{CC}, T_A = +25°C		0.1	1.0	µA
V_{CC} Supply Current	I_{VCC}	Regulator enabled, no load, no switching (V_{FB} = 1V)		62	135	µA
OUTPUT						
Output Voltage Programmable Range	V_{OUT}	V_{IN} = V_{CC} = 5.2V, I_{LOAD} = 2A (see derating curve)	0.754		1.8	V
Unity Gain Output-Voltage Tolerance/FB accuracy		FB = OUT, no load	0.757	0.765	0.783	V
FB Load Regulation Accuracy (RDROOP)		2A < I_{OUT} < 5A, FB = OUT	-7.5	-4.4	-1	mV/A
FB Line Regulation Accuracy		FB = OUT, no load, 2.4V < V_{IN} < 5.5V		1.253	4.5	mV/V
FB Input Bias Current		T_A = -40°C to +125°C (Note 3)	-0.1	-0.015	+0.1	µA

Electrical Characteristics (continued)

(V_{IN} = V_{CC} = V_{EN} = 5V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted. See *Typical Application Circuit.*) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Average Output Current Limit		V_{IN} = 5V	6		9	A
EFFICIENCY						
Efficiency		V_{IN} = 5V, V_{OUT} = 1.1V, I_{OUT} = 2A		86		%
		V_{IN} = 5V, V_{OUT} = 1.1V, I_{OUT} = 6A		74		
SWITCHING FREQUENCY						
Switching Frequency	f_{SW}		0.9	1	1.1	MHz
SOFT-START						
Soft-Start Ramp Time	t_{SS}			1.79		ms
Soft-Start Fault Blanking Time	t_{SSLT}			3		ms
POWER-GOOD OUTPUT (POK)						
POK Upper Trip Threshold and Overvoltage-Fault Threshold		Rising edge, 50mV hysteresis	830	850	870	mV
POK Lower Trip Threshold		Falling edge, 50mV hysteresis	658	690	725	mV
POK Leakage Current	I_{POK}	T_A = +25°C, V_{POK} = 5.5V		0.1	1	µA
POK Propagation Delay Time	t_{POK}	FB forced 50mV beyond POK trip threshold		2		µs
POK Output Low Voltage		I_{SINK} = 3mA			100	mV
Overvoltage Fault Latch Delay Time		FB forced 50mV above POK upper-trip threshold		2		µs
Undervoltage Fault Latch Delay Time		FB forced 50mV below POK lower-trip threshold, TUV		1.6		ms
LOGIC INPUTS						
EN Input High Threshold		Rising, hysteresis = 215mV (typ)	1.0	1.4	1.6	V
EN Input Leakage Current		T_A = +25°C		0.1	1	µA
THERMAL SHUTDOWN						
Thermal-Shutdown Threshold	TSHDN	Hysteresis = 15°C		+160		°C

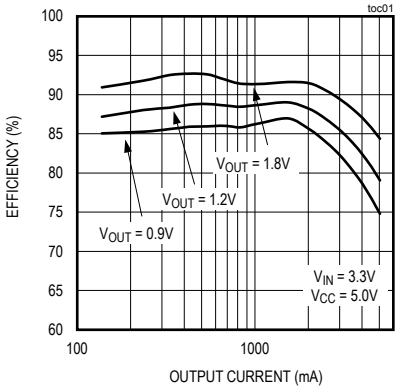
Note 2: Limits are 100% tested at T_A = +25°C. Maximum and minimum limits are guaranteed by design and characterization over temperature.

Note 3: Design guaranteed by ATE characterization. Limits are not production tested.

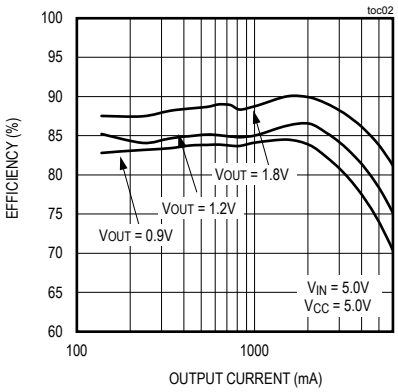
Typical Operating Characteristics

(V_{CC} = 5V, V_{IN} = 3.3V - 5V, V_{OUT} = 0.9V - 1.8V, I_{OUT} = 0–6A, T_A = +25°C, unless otherwise noted.)

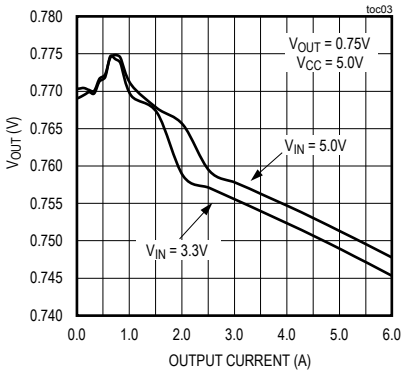
EFFICIENCY vs OUTPUT CURRENT



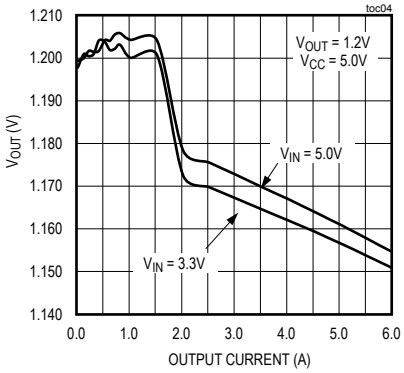
EFFICIENCY vs OUTPUT CURRENT



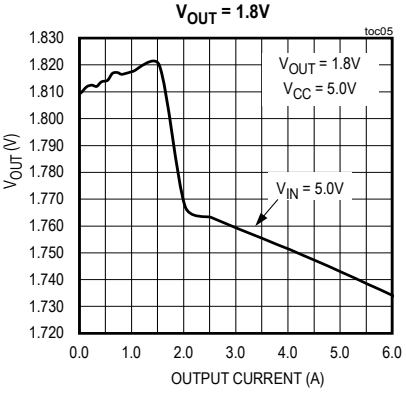
LOAD REGULATION V_{OUT} = 0.75V



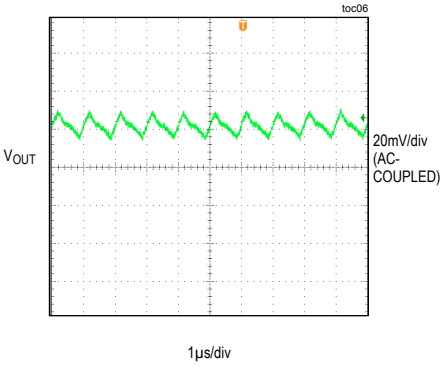
LOAD REGULATION V_{OUT} = 1.2V



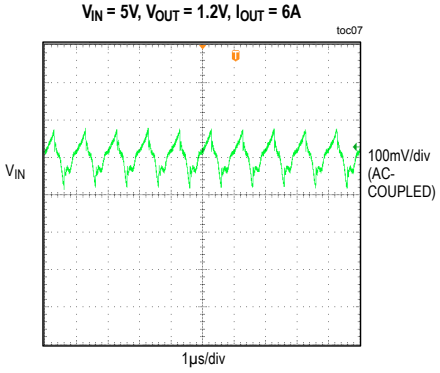
LOAD REGULATION V_{OUT} = 1.8V



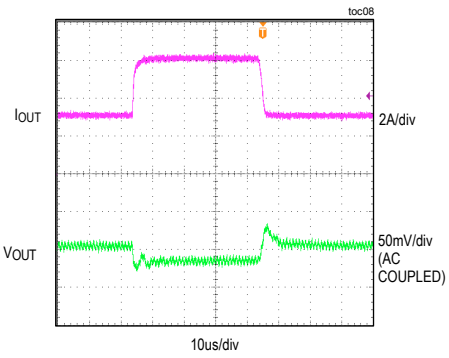
OUTPUT VOLTAGE RIPPLE V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 6A



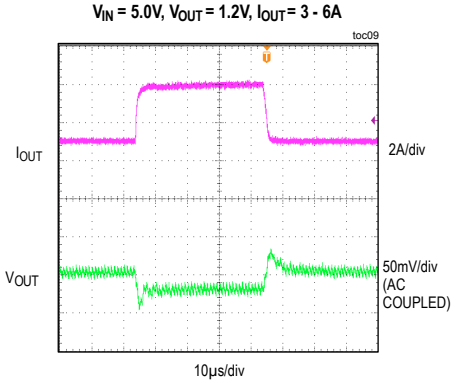
INPUT VOLTAGE RIPPLE V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 6A



LOAD CURRENT TRANSIENT RESPONSE V_{IN} = 3.3V, V_{OUT} = 1.2V, I_{OUT} = 3 - 6A



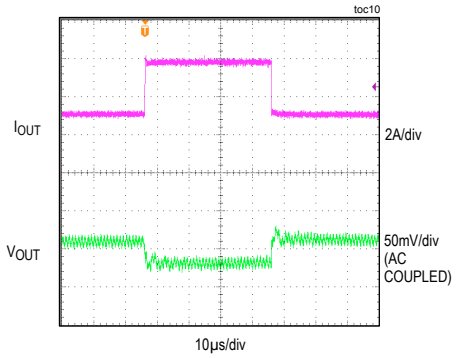
LOAD CURRENT TRANSIENT RESPONSE V_{IN} = 5.0V, V_{OUT} = 1.2V, I_{OUT} = 3 - 6A



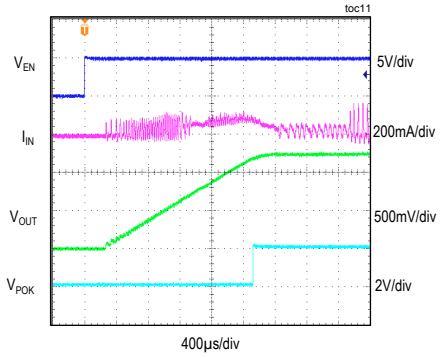
Typical Operating Characteristics (continued)

(V_{CC} = 5V, V_{IN} = 3.3V - 5V, V_{OUT} = 0.9V - 1.8V, I_{OUT} = 0–6A, T_A = +25°C, unless otherwise noted.)

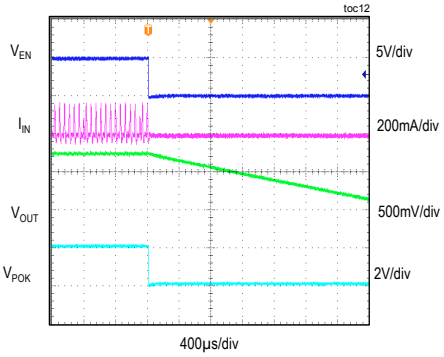
LOAD CURRENT TRANSIENT RESPONSE
V_{IN} = 5.0V, V_{OUT} = 1.8V, I_{OUT} = 3 - 6A



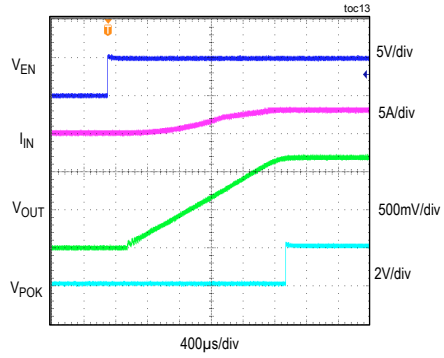
STARTUP WAVEFORM
V_{IN} = 3.3V, V_{OUT} = 1.2V, I_{OUT} = 0A



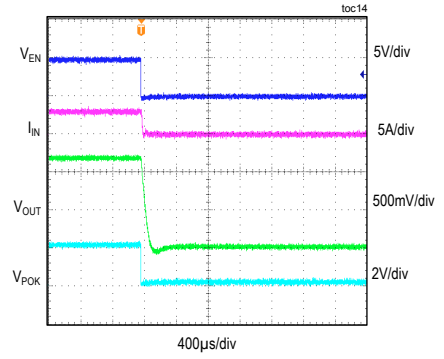
SHUTDOWN WAVEFORM
V_{IN} = 3.3V, V_{OUT} = 1.2V, I_{OUT} = 30mA



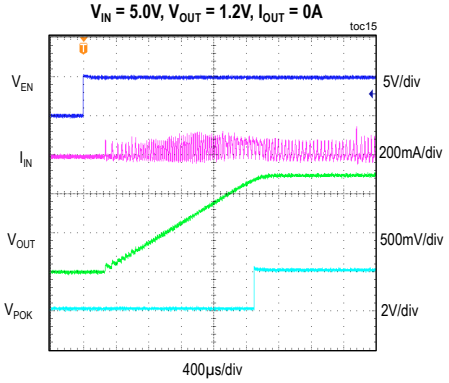
STARTUP WAVEFORM
V_{IN} = 3.3V, V_{OUT} = 1.2V, I_{OUT} = 6A



SHUTDOWN WAVEFORM
V_{IN} = 3.3V, V_{OUT} = 1.2V, I_{OUT} = 6A



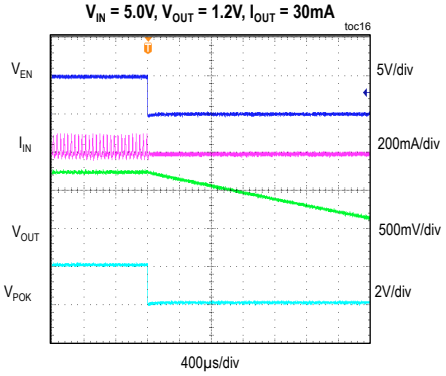
STARTUP WAVEFORM
V_{IN} = 5.0V, V_{OUT} = 1.2V, I_{OUT} = 0A



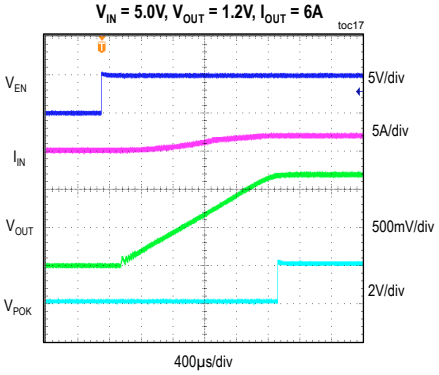
Typical Operating Characteristics (continued)

(V_{CC} = 5V, V_{IN} = 3.3V - 5V, V_{OUT} = 0.9V - 1.8V, I_{OUT} = 0–6A, T_A = +25°C, unless otherwise noted.)

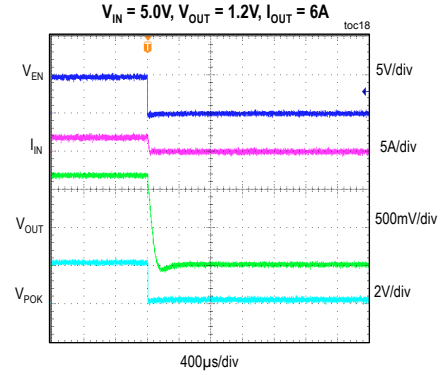
SHUTDOWN WAVEFORM
V_{IN} = 5.0V, V_{OUT} = 1.2V, I_{OUT} = 30mA



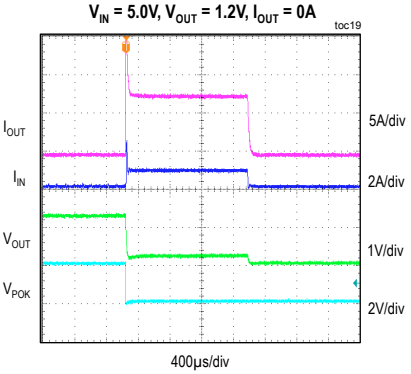
STARTUP WAVEFORM
V_{IN} = 5.0V, V_{OUT} = 1.2V, I_{OUT} = 6A



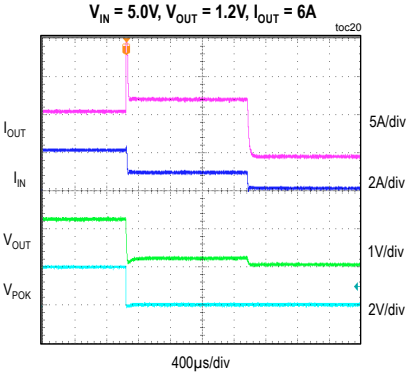
SHUTDOWN WAVEFORM
V_{IN} = 5.0V, V_{OUT} = 1.2V, I_{OUT} = 6A



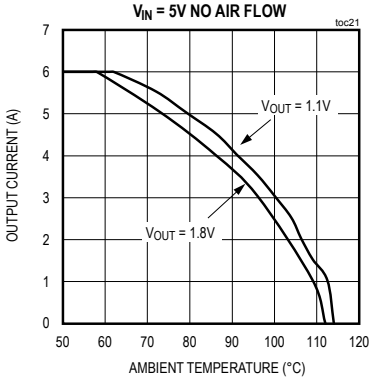
LOAD SHORT CIRCUIT
V_{IN} = 5.0V, V_{OUT} = 1.2V, I_{OUT} = 0A



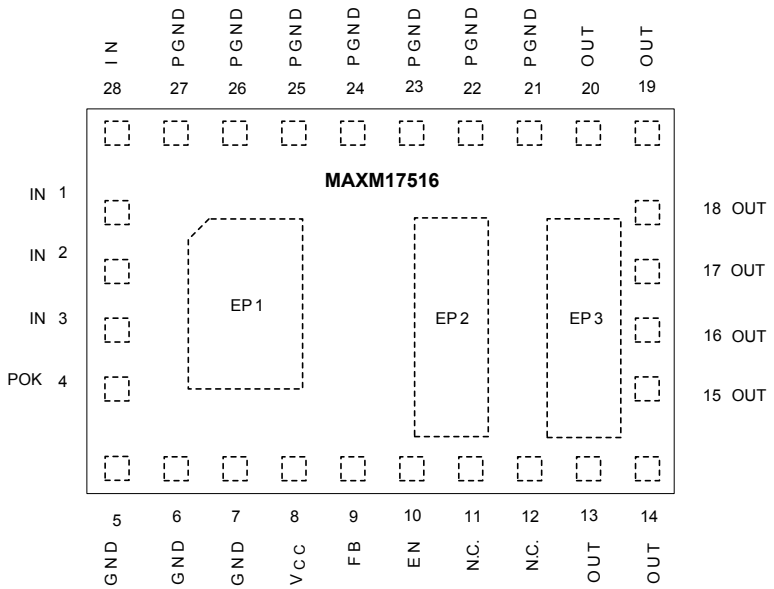
LOAD SHORT CIRCUIT
V_{IN} = 5.0V, V_{OUT} = 1.2V, I_{OUT} = 6A



OUTPUT CURRENT
vs. AMBIENT TEMPERATURE
V_{IN} = 5V NO AIR FLOW



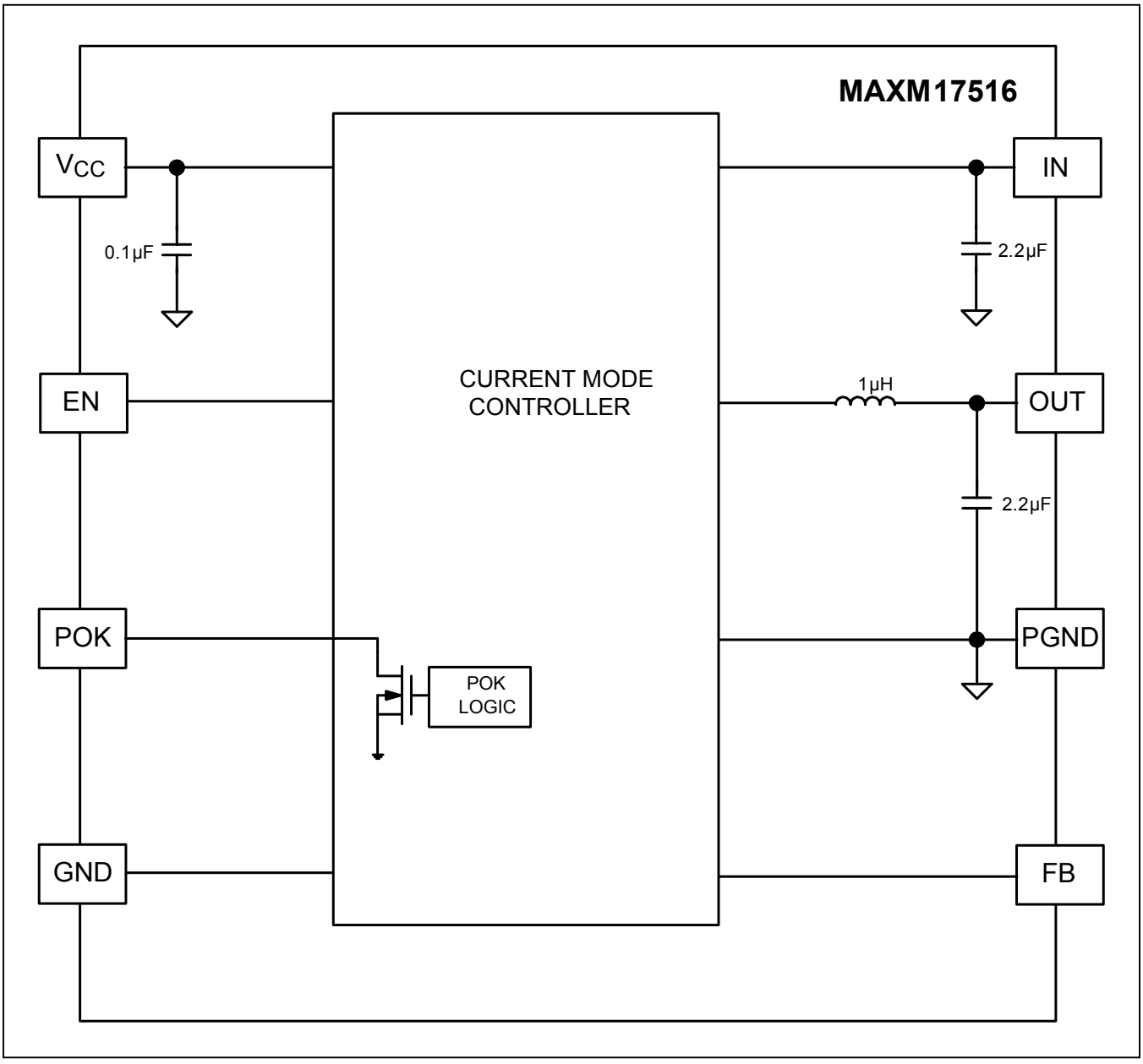
Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1–3, 28	IN	Input Supply Connection. Bypass to GND with a 22µF or 2 x 10µF ceramic capacitor. Supply range for this pin is 4.5V to 5.5V. When V_{CC} can be supplied separately from a 4.5V to 5.5V source, the IN pin can then be powered from a 2.4V to 5.5V supply.
4	POK	Open-Drain Power-Good Output. POK is pulled low if FB is more than 12% (typ) above or below the nominal regulation threshold. POK is held low in shutdown. POK becomes high impedance when FB is in regulation range. Pull this pin up with 10kΩ (typ) resistor value.
5–7	GND	GND. Connect PGND and GND together at a single point.
8	V_{CC}	5V Bias Supply Input for the Internal Switching Regulator Drivers. For IN from 4.5V to 5.5V, V_{CC} can be connected to the IN supply. For IN supply voltages lower than the above range, V_{CC} should be powered from a separate 5V ±10% supply and bypassed with a 1µF or greater ceramic capacitor.
9	FB	Feedback Input for the Internal Step-Down Converter. Connect FB to a resistive divider between OUT and GND to adjust the typical output voltage between 0.765V to 1.8V. Keep equivalent divider resistance lower than 50kΩ.
10	EN	Regulator Enable Input. When EN is pulled low, the regulator is disabled. When EN is driven high, the regulator is enabled.
11, 12	N.C.	No Connection
13–20	OUT	Regulator Output Pins. Connect an output capacitor between OUT and PGND with a 220µF (typ) POSCAP low-ESR capacitor.
21–27	PGND	Power GND Return. Connect to GND.
—	EP1	Exposed Pad 1. Connect this pad to the PGND ground plane of 1in by 1in copper for cooling.
—	EP2	Exposed Pad 2. Connect this pad to the PCB for better thermal performance, but do not connect to any other node. Minimize area of copper island.
—	EP3	Exposed Pad 3. Connect this pad to the OUT pins and the copper area of 1in by 1in.

Functional Diagram



Design Procedure

Adjusting Output Voltage

The MAXM17516 produces an adjustable 0.75V to 1.8V output voltage from a 2.4V to 5.5V input voltage range by using a resistive feedback divider from OUT to FB.

Adjusting the output voltage of the device requires a resistive divider network from OUT to FB, according to the equation below. From the initial output voltage, the load-line regulation reduces the effective feedback voltage by a typical 5mV/A as the output current increases.

$$R_U = R_B \times \left[\frac{V_{OUT}}{0.765} - 1\right] k\Omega, \text{ where } R_B \text{ is in } k\Omega.$$

Input Voltage Range

The maximum value ($V_{IN(MAX)}$) and minimum value ($V_{IN(MIN)}$) must accommodate the worst-case conditions accounting for the input voltage soars and drops. If there is a choice at all, lower input voltages result in better efficiency. With a maximum duty cycle of 87.5%, V_{OUT} is limited to 0.875 x V_{IN}. To operate with a 6A output current, the minimum input voltage given an output voltage is shown in Figure 1.

Input Capacitor Selection

The input capacitor must meet the ripple-current requirement (I_{RMS}) imposed by the switching currents. The I_{RMS} requirements of the regulator can be determined by the following equation:

$$I_{RMS} = I_{OUT} \times \sqrt{D \times (1 - D)}$$

The worst-case RMS current requirement occurs when operating with D = 0.5. At this point, the above equation simplifies to I_{RMS} = 0.5 x I_{OUT}.

The minimum input capacitor required can be calculated by the following equation:

$$C_{IN} = \frac{(I_{IN\_AVG}) \times (1 - D)}{(\Delta V_{IN}) \times f_{SW}}$$

where,

I_{IN_AVG} is the average input current given by:

$$I_{IN\_Avg} = \frac{P_{OUT}}{\eta \times V_{IN}}$$

D is the operating duty cycle, which is approximately equal to V_{OUT}/V_{IN} where:

ΔV_{IN} is the required input-voltage ripple,

f_{SW} is the operating switching frequency,

P_{OUT} is the output power, which is equal to V_{OUT} x I_{OUT},

η is the efficiency.

For the device's system (IN) supply, ceramic capacitors are preferred due to their resilience to inrush surge currents typical of systems, and due to their low parasitic inductance, which helps reduce the high-frequency ringing on the IN supply when the internal MOSFETs are turned off. Choose an input capacitor that exhibits less than +10°C temperature rise at the RMS input current for optimal circuit longevity.

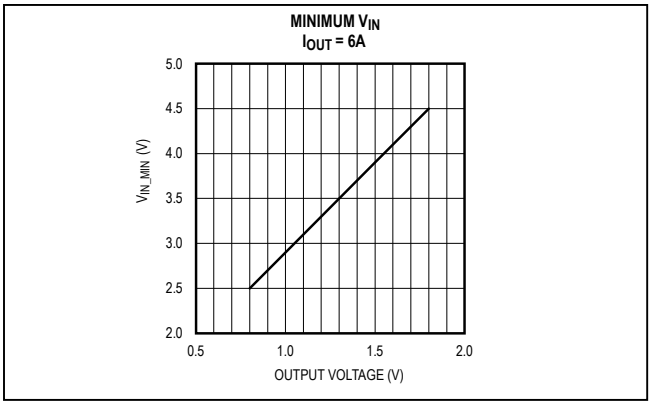


Figure 1. Minimum V_{IN}

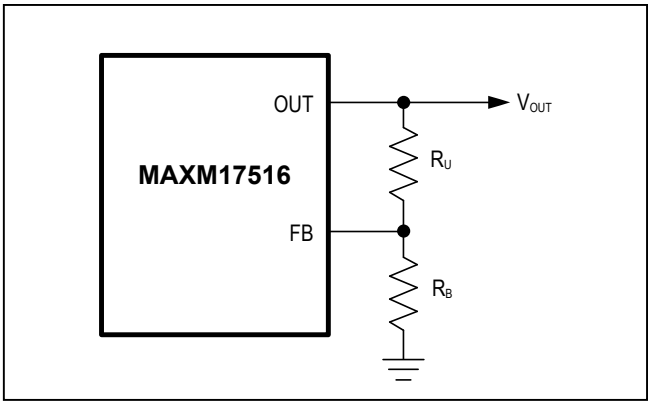


Figure 2. Adjusting Output Voltage

Output Capacitor Selection

The output capacitor selection requires careful evaluation of several different design requirements (e.g., stability, transient response, and output ripple voltage) that place limits on the output capacitance and the effective series resistance (ESR). Based on these requirements, a combination of low-ESR polymer capacitors (lower cost but higher output ripple voltage) and ceramic capacitors (higher cost but low output ripple voltage) should be used to achieve stability with low output ripple.

Loop Compensation

The gain portion of the loop gain is a result of error-amplifier gain, current-sensing gain, and load with an overall typical value at 1kHz of 36dB at V_{IN} = 5V, and 46dB at V_{IN} = 3V, with a typical limit to the gain-bandwidth (GBW) product of 120,000. The crossover should occur before this error-amplifier bandwidth limit of 120kHz (gain = 1). The output capacitor and load introduces a pole with the worst case at the maximum load (6A). If the load pole location is further than a frequency where the gain exceeds the GBW, the gain drop starts earlier at the location where the loop gain is limited. This situation applies typically to an output voltage less than 1.8V, so zero frequency from the ESR is needed to increase the phase margin at the crossover frequency.

The recommended relationship between ESR and total output capacitance values are shown in Table 1. When a low-ESR type capacitor is used with a ceramic capacitor, a recommended value of 44µF to 100µF ceramic capacitor should be used to make up the total capacitance value with the relationship between ESR and total output capacitance value, such that the zero frequency is between 32kHz and 40kHz. When only a low-ESR type capacitor is used, the zero frequency should be between 62kHz and 80kHz. Optionally, a small 10µF–22µF ceramic capacitor can be used to reduce output ripple.

Optionally, for an output greater than or equal to 1.8V, an all-ceramic capacitor solution can be used with a minimum capacitance value that locates the pole location below 1kHz with resistive load (6A), and with a simplified equation given by C_{OUTMIN} (µF) = 900/V_{OUT}.

Output Ripple Voltage

With polymer capacitors, the ESR dominates and determines the output ripple voltage. The step-down regulator's output ripple voltage (V_{RIPPLE}) equals the total inductor ripple current (ΔI_L) multiplied by the output capacitor's ESR. Therefore, the maximum ESR to meet the output ripple-voltage requirement is:

$$R_{ESR} \le \frac{V_{RIPPLE}}{\Delta I_L}$$

where,

$$\Delta I_L = \left(\frac{V_{IN} - V_{OUT}}{L}\right) \times \left(\frac{V_{OUT}}{V_{IN}}\right) \times \frac{1}{f_{SW}}$$

where, f_{SW} is the switching frequency and L is the inductor (1µH).

The actual capacitance value required relates to the physical case size needed to achieve the ESR requirement, as well as to the capacitor chemistry. Thus, polymer capacitor selection is usually limited by ESR and voltage rating rather than by capacitance value.

With ceramic capacitors, the ripple voltage due to capacitance dominates the output ripple voltage. Therefore, the minimum capacitance needed with ceramic output capacitors is:

$$C_{OUT} = \left(\frac{\Delta I_L}{8 \times f_{SW}}\right) \times \frac{1}{V_{RIPPLE}}$$

Alternatively, combining ceramics (for the low ESR) and polymers (for the bulk capacitance) helps balance the output capacitance vs. output ripple-voltage requirements.

Table 1. Output Capacitor Selection vs. ESR

TOTAL C_{OUT} (µF)	LOW-ESR TYPE WITH CERAMIC-TYPE ESR (mΩ)	LOW-ESR TYPE WITHOUT CERAMIC-TYPE ESR (mΩ)
250	16–20	8–10
300	13–17	7–9
350	11–14	6, 7
400	10–12	5, 6
450	9–11	4–6
500	8–10	4, 5
550	7–9	4, 5
600	7, 8	3, 4

Load-Transient Response

The load-transient response depends on the overall output impedance over frequency, and the overall amplitude and slew rate of the load step. In applications with large, fast-load transients (load step > 80% of full load and slew rate > 10A/µs), the output capacitor's high-frequency response (ESL and ESR) needs to be considered. To prevent the output voltage from spiking too low under a load-transient event, the ESR is limited by the following equation (ignoring the sag due to finite capacitance):

$$R_{ESR} \le \frac{V_{RIPPLESTEP}}{\Delta I_{OUTSTEP}}$$

where, $V_{RIPPLESTEP}$ is the allowed voltage drop during load current transient, and $I_{OUTSTEP}$ is the maximum load current step.

The capacitance value dominates the mid-frequency output impedance and continues to dominate the load-transient response as long as the load transient's slew rate is fewer than two switching cycles. Under these conditions, the sag and soar voltages depend on the output capacitance, inductance value, and delays in the transient response. Low inductor values allow the inductor current to slew faster, replenishing charge removed from or added to the output filter capacitors by a sudden load step, especially with low differential voltages across the inductor. The minimum capacitance needed to handle the sag voltage (V_{SAG}) that occurs after applying the load current can be estimated by the following equation:

$$C_{OUT\_SAG} = \frac{1}{V_{SAG}} \times \left[\frac{1}{2}\left(\frac{L \times \Delta IOUT_{STEP}^{2}}{(VIN \times D_{MAX}) - VOUT}\right) + \left(\Delta IOUT_{STEP} \times (t_{sw} - \Delta T)\right)\right]$$

where:

D_{MAX} is the maximum duty factor (87.5%),

t_{SW} is the switching period ($1/f_{SW}$),

ΔT equals V_{OUT}/V_{IN} x t_{SW} when in PWM mode, or L x $I_{IDLE}/(V_{IN} - V_{OUT})$ when in Idle Mode (1.5A).

The minimum capacitance needed to handle the overshoot voltage (V_{SOAR}) that occurs after load removal (due to stored inductor energy) can be calculated as:

$$C_{OUT\_SOAR} \approx \frac{(\Delta IOUT_{STEP})^2 L}{2 V_{OUT} V_{SOAR}}$$

When the device is operating under low duty cycle, the output capacitor size is usually determined by the C_{OUT_SOAR}.

Detailed Description

The MAXM17516 is a complete step-down switch-mode power-supply solution that can deliver up to 6A output current and up to 1.8V output voltage from a 2.4V to 5.5V input voltage range. The device includes switch-mode power-supply controller, dual n-channel MOSFET power switches, and an inductor. The device uses a fixed-frequency current-mode control scheme.

The device provides peak current-limit protection, output undervoltage protection, output overvoltage protection, and thermal protection. The device operates in skip mode at light loads to improve the light-load efficiency. Independent enable and an open-drain power-good output allow flexible system power sequencing. The fixed voltage soft-start reduces the inrush current by gradually ramping up the internal reference voltage.

Fixed-Frequency Current-Mode Controller

The heart of the current-mode PWM controller is a multistage, open-loop comparator that compares the output voltage-error signal with respect to the reference voltage, the current-sense signal, and the slope-compensation ramp (see the *Functional Diagram*). The device uses a direct summing configuration, approaching ideal cycle-to-cycle control over the output voltage without a traditional error amplifier and the phase shift associated with it.

Light-Load Operation

The device features an inherent automatic switchover to pulse skipping (PFM operation) at light loads. This switchover is affected by a comparator that truncates the low-side switch on-time at the inductor current's zero crossing. The zero-crossing comparator senses the inductor current during the off-time. Once the current through the low-side MOSFET drops below the zero-crossing trip level, it turns off the low-side MOSFET. This prevents the inductor from discharging the output capacitors and forces the switching regulator to skip pulses under light-load conditions to avoid overcharging the output. Therefore, the controller regulates the valley of the output ripple under light-load conditions. The switching waveforms can appear noisy and asynchronous at light-load pulse-skipping operation, but this is a normal operating condition that results in high light-load efficiency.

Idle Mode is a trademark of Maxim Integrated Products, Inc

Idle Mode™ Current-Sense Threshold

In Idle Mode, the on-time of the step-down controller terminates when both the output voltage exceeds the feedback threshold, and the internal current-sense voltage falls below the Idle Mode current-sense threshold (I_{IDLE} = 1.5A). Another on-time cannot be initiated until the output voltage drops below the feedback threshold. In this mode, the behavior appears like PWM operation with occasional pulse skipping, where inductor current does not need to reach the light-load level.

Power-On Reset (POR) and UVLO

Power-on reset (POR) occurs when V_{CC} rises above approximately 2.1V, resetting the undervoltage, overvoltage, and thermal-shutdown fault latches. The V_{CC} input undervoltage-lockout (UVLO) circuitry prevents the switching regulators from operating if the 5V bias supply (V_{CC}) is below its 4V UVLO threshold.

Soft-Start

The internal step-down controller starts switching and the output voltage ramps up using soft-start. If the V_{CC} bias supply voltage drops below the UVLO threshold, the controller stops switching and disables the drivers (LX becomes high impedance) until the bias supply voltage recovers.

Once the 5V V_{CC} bias supply and V_{IN} rise above their respective input UVLO thresholds, and EN is pulled high, the internal step-down controller becomes enabled and begins switching. The internal voltage soft-starts gradually increment the feedback voltage by approximately 25mV every 61 switching cycles, making the output voltage reach its nominal regulation voltage 1.79ms after the regulator is enabled (see the Soft-Start Waveforms in the *Typical Operating Characteristics* section).

Power-Good Output (POK)

POK is the open-drain output of the window comparator that continuously monitors the output for undervoltage and overvoltage conditions. POK is actively held low in shutdown (EN = GND). POK becomes high impedance after the device is enabled and the output remains within ±10% of the nominal regulation voltage set by FB. POK goes low once the output drops 12% (typ) below or rises 12% (typ) above its nominal regulation point, or the output shuts down. For a logic-level POK output voltage, connect an external pullup resistor between POK and V_{CC}. A 10kΩ pullup resistor works well in most applications.

Output Overvoltage Protection (OVP)

If the output voltage rises to 112% (typ) of its nominal regulation voltage, the controller sets the fault latch, pulls POK low, shuts down the regulator, and immediately pulls the output to ground through its low-side MOSFET. Turning on the low-side MOSFET with 100% duty cycle rapidly discharges the output capacitors and clamps the output to ground. However, this commonly undamped response causes negative output voltages due to the energy stored in the output LC at the instant of 0V fault. If the load cannot tolerate a negative voltage, place a power Schottky diode across the output to act as a reverse-polarity clamp. If the condition that caused the overvoltage persists (such as a shorted high-side MOSFET), the input source also fails (short-circuit fault). Cycle V_{CC} below 1V or toggle the enable input to clear the fault latch and restart the regulator.

Output Undervoltage Protection (UVP)

The device includes an output undervoltage-protection (UVP) circuit that begins to monitor the output once the startup blanking period has ended. If the output voltage drops below 88% (typ) of its nominal regulation voltage, the regulator pulls the POK output low and begins the UVP fault timer. Once the timer expires after 1.6ms, the regulator shuts down, forcing the high-side MOSFET off and disabling the low-side MOSFET once the zero-crossing threshold has been reached. Cycle V_{CC} below 1V, or toggle the enable input to clear the fault latch and restart the regulator.

Thermal-Fault Protection

The device features a thermal-fault protection circuit. When the junction temperature rises above +160°C (typ), a thermal sensor activates the fault latch, pulls down the POK output, and shuts down the regulator. Toggle EN to clear the fault latch, and restart the controllers after the junction temperature cools by 15°C (typ).

Power Dissipation

The device output current needs to be derated if the device needs to operate in high ambient temperature. The amount of current derating depends upon the input voltage, output voltage, and ambient temperature. The derating curves given in the *Typical Operating Characteristics* section can be used as a guide.

The maximum allowable power losses can be calculated using the following equation:

$$PD_{MAX} = \frac{T_{JMAX} - T_A}{\theta_{JA}}$$

where:

PD_{MAX} is the maximum allowed power losses with maximum allowed junction temperature,

T_{JMAX} is the maximum allowed junction temperature,

T_A is operating ambient temperature,

θ_{JA} is the junction-to-ambient thermal resistance.

PCB Layout Guidelines

Careful PCB layout is critical to achieving low switching losses and clean, stable operation. Use the following guidelines for good PCB layout:

- Keep the input capacitors as close as possible to the IN and PGND pins.
- Keep the output capacitors as close as possible to the OUT and PGND pins.
- Connect all the PGND connections to as large a copper plane area as possible on the top layer.
- Connect EP1 to the PGND and GND planes on the top layer.
- Use multiple vias to connect internal PGND planes to the top-layer PGND plane.
- Do not keep any solder mask on EP1–EP3 on bottom layer. Keeping solder mask on exposed pads decreases the heat-dissipating capability.
- Keep the power traces and load connections short. This practice is essential for high efficiency. Using thick copper PCBs (2oz vs. 1oz) can enhance full-load efficiency. Correctly routing PCB traces is a difficult task that must be approached in terms of fractions of centimeters, where a single milliohm of excess trace resistance causes a measurable efficiency penalty.

Ordering Information

PART	TEMP RANGE	MSL	PIN-PACKAGE
MAXM17516ALI+T	-40°C to +125°C	3	28 SiP

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Chip Information

PROCESS: BiCMOS

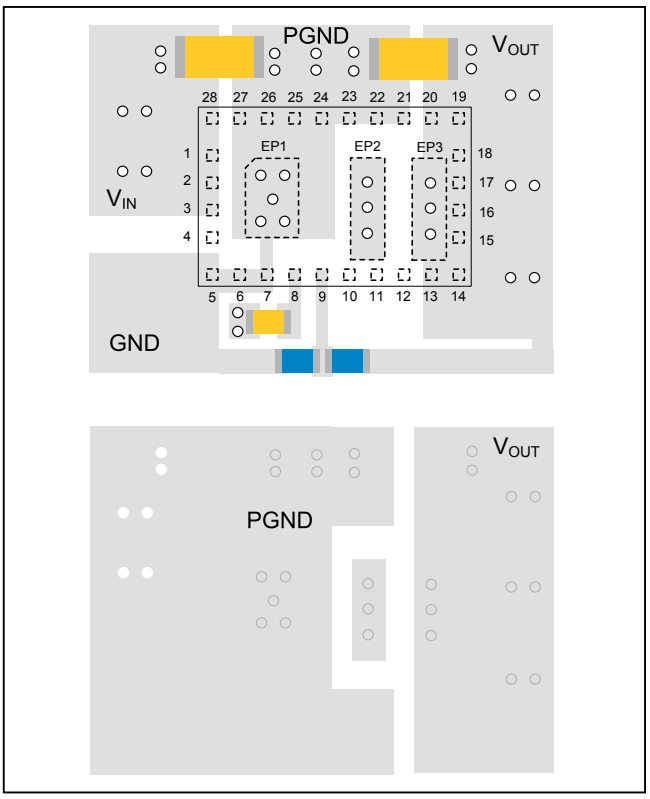


Figure 3. Layout Recommendation

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
28 SiP	L286510+1	21-0701	90-0445

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/14	Initial release	—
1	4/15	Tightened FB accuracy and added MSL 3 rating	2, 13

