

# NDD60N550U1

## N-Channel Power MOSFET 600 V, 550 mΩ

### Features

- 100% Avalanche Tested
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### ABSOLUTE MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	NDD	Unit
Drain-to-Source Voltage	$V_{DS}$	600	V
Gate-to-Source Voltage	$V_{GS}$	$\pm 25$	V
Continuous Drain Current $R_{\theta JC}$	Steady State	$T_C = 25^\circ\text{C}$	8.2
		$T_C = 100^\circ\text{C}$	5.2
Power Dissipation – $R_{\theta JC}$	Steady State	$T_C = 25^\circ\text{C}$	94
Pulsed Drain Current	$t_p = 10 \mu\text{s}$	$I_{DM}$	34
Operating Junction and Storage Temperature	$T_J, T_{STG}$	-55 to +150	$^\circ\text{C}$
Source Current (Body Diode)	$I_S$	8.2	A
Single Pulse Drain-to-Source Avalanche Energy ( $I_D = 4 \text{ A}$ )	EAS	54	mJ
Peak Diode Recovery (Note 1)	$dv/dt$	15	V/ns
Lead Temperature for Soldering Leads	$T_L$	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1.  $I_{SD} < 8.2 \text{ A}$ ,  $di/dt \leq 400 \text{ A}/\mu\text{s}$ ,  $V_{DS \text{ peak}} \leq V_{(BR)DSS}$ ,  $V_{DD} = 80\% V_{(BR)DSS}$

### THERMAL RESISTANCE

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain) NDD60N550U1	$R_{\theta JC}$	1.3	$^\circ\text{C}/\text{W}$
Junction-to-Ambient Steady State (Note 3)	$R_{\theta JA}$	NDD60N550U1	47
		NDD60N550U1-1	98
		NDD60N550U1-35	95

2. Insertion mounted
3. Surface mounted on FR4 board using 1" sq. pad size (Cu area = 1.127 in sq [2 oz] including traces)

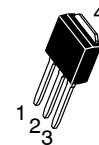
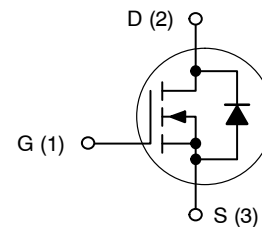


ON Semiconductor®

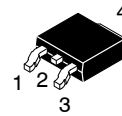
<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(ON) \text{ MAX}}$
600 V	550 mΩ @ 10 V

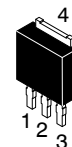
### N-Channel MOSFET



IPAK  
CASE 369D  
STYLE 2



DPAK  
CASE 369C  
STYLE 2



IPAK  
CASE 369AD  
STYLE 2

### MARKING AND ORDERING INFORMATION

See detailed ordering and shipping information on page 3 of this data sheet.

# NDD60N550U1

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
----------------	--------	-----------------	-----	-----	-----	------

### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 1 mA	600			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /T <sub>J</sub>			540		mV/°C
Drain-to-Source Leakage Current	I <sub>DSS</sub>	V <sub>DS</sub> = 600 V, V <sub>GS</sub> = 0 V	T <sub>J</sub> = 25°C		1	μA
			T <sub>J</sub> = 125°C		100	
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±25 V			±100	nA

### ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2	3.2	4	V
Negative Threshold Temperature Coefficient	V <sub>GS(TH)</sub> /T <sub>J</sub>	Reference to 25°C, I <sub>D</sub> = 250 μA		7.6		mV/°C
Static Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 4 A		510	550	mΩ
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 4 A		7.0		S

### DYNAMIC CHARACTERISTICS

Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 0 V, f = 1 MHz		540		pF
Output Capacitance	C <sub>oss</sub>			33		
Reverse Transfer Capacitance	C <sub>rss</sub>			1.6		
Effective output capacitance, energy related (Note 6)	C <sub>o(er)</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 0 to 480 V		24		
Effective output capacitance, time related (Note 7)	C <sub>o(tr)</sub>	I <sub>D</sub> = constant, V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 0 to 480 V		84		
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 300 V, I <sub>D</sub> = 9.5 A, V <sub>GS</sub> = 10 V		18		nC
Gate-to-Source Charge	Q <sub>gs</sub>			3.4		
Gate-to-Drain Charge	Q <sub>gd</sub>			8.7		
Plateau Voltage	V <sub>GP</sub>			5.4		V
Gate Resistance	R <sub>g</sub>			5.5		Ω

### RESISTIVE SWITCHING CHARACTERISTICS (Note 5)

Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 300 V, I <sub>D</sub> = 9.5 A, V <sub>GS</sub> = 10 V, R <sub>G</sub> = 0 Ω		8		ns
Rise Time	t <sub>r</sub>			14		
Turn-off Delay Time	t <sub>d(off)</sub>			20		
Fall Time	t <sub>f</sub>			17		

### SOURCE-DRAIN DIODE CHARACTERISTICS

Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> = 8.2 A, V <sub>GS</sub> = 0 V	T <sub>J</sub> = 25°C		0.9	1.3	V
			T <sub>J</sub> = 100°C		0.82		
Reverse Recovery Time	t <sub>rr</sub>	V <sub>GS</sub> = 0 V, V <sub>DD</sub> = 30 V, I <sub>S</sub> = 9.5 A, d <sub>i</sub> /d <sub>t</sub> = 100 A/μs		290		ns	
Charge Time	t <sub>a</sub>			160			
Discharge Time	t <sub>b</sub>			130			
Reverse Recovery Charge	Q <sub>rr</sub>			2.6			μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

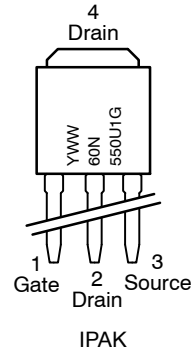
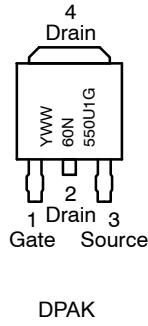
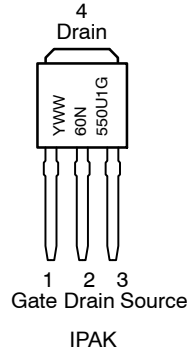
5. Switching characteristics are independent of operating junction temperatures.

6. C<sub>o(er)</sub> is a fixed capacitance that gives the same stored energy as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>(BR)DSS</sub>

7. C<sub>o(tr)</sub> is a fixed capacitance that gives the same charging time as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>(BR)DSS</sub>

# NDD60N550U1

## MARKING DIAGRAMS



Y = Year  
 WW = Work Week  
 G = Pb-Free Package

## ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
NDD60N550U1-1G	IPAK (Pb-Free, Halogen-Free)	75 Units / Rail
NDD60N550U1-35G	IPAK (Pb-Free, Halogen-Free)	75 Units / Rail
NDD60N550U1T4G	DPAK (Pb-Free, Halogen-Free)	2500 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NDD60N550U1

## TYPICAL CHARACTERISTICS

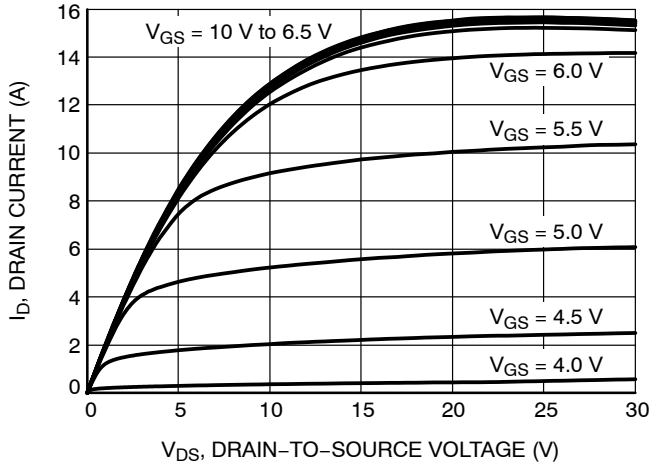


Figure 1. On-Region Characteristics

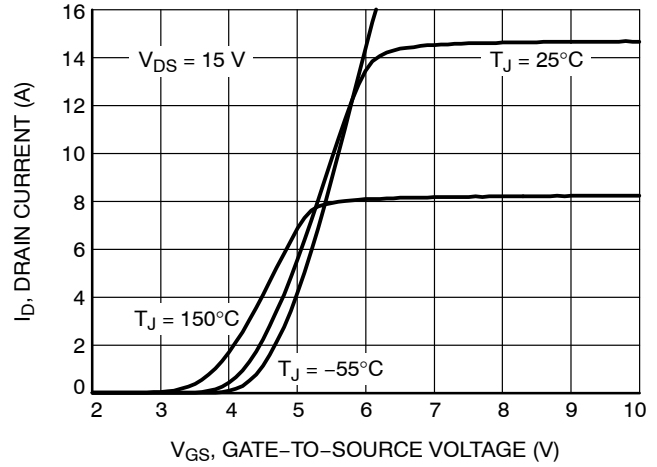


Figure 2. Transfer Characteristics

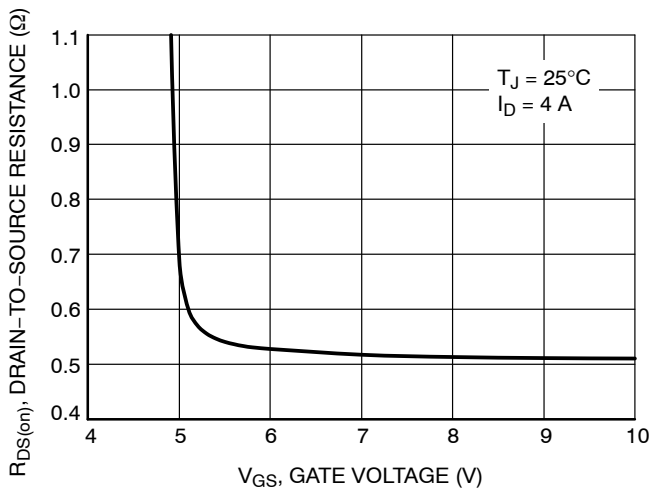


Figure 3. On-Resistance vs. Gate-to-Source Voltage

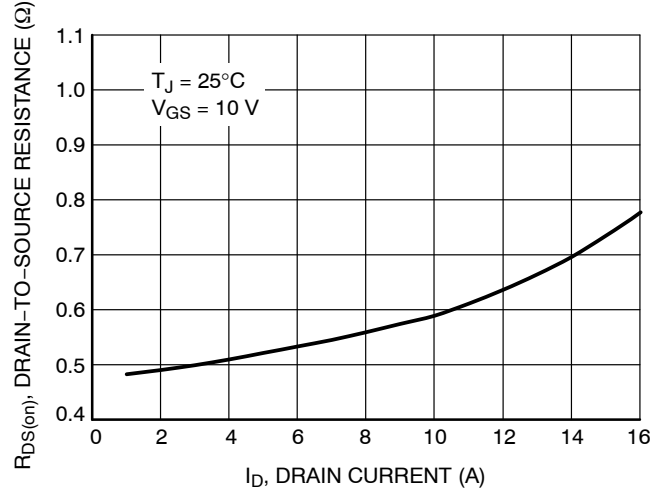


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

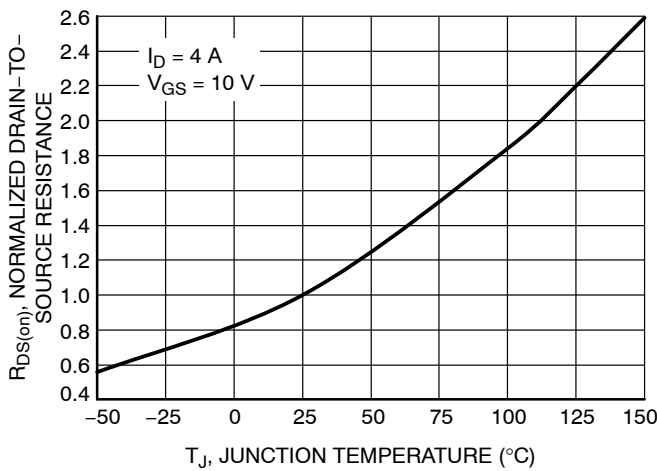


Figure 5. On-Resistance Variation with Temperature

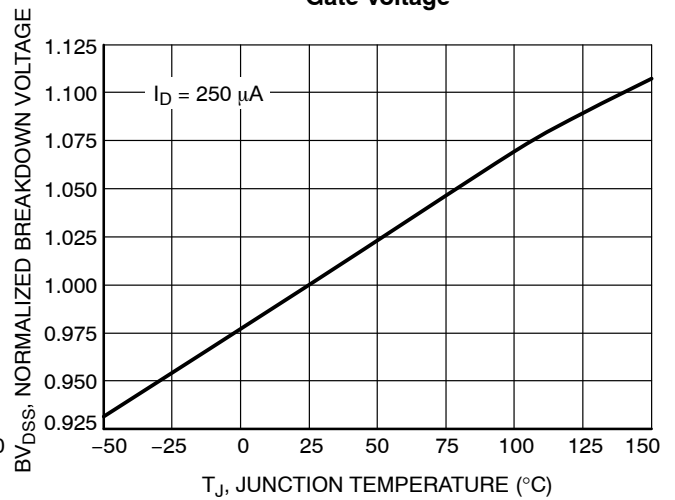
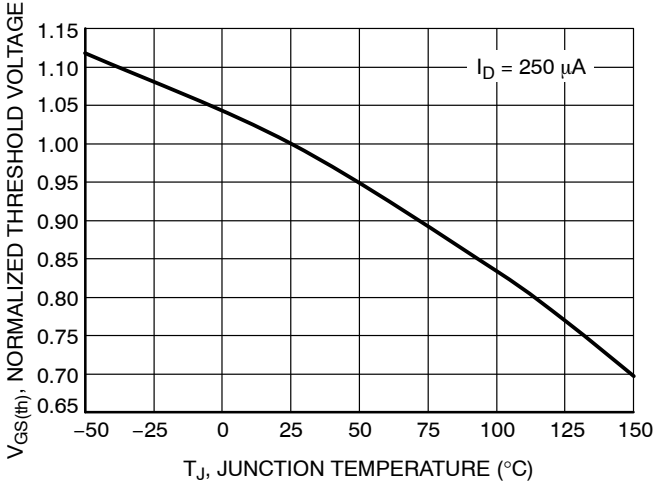


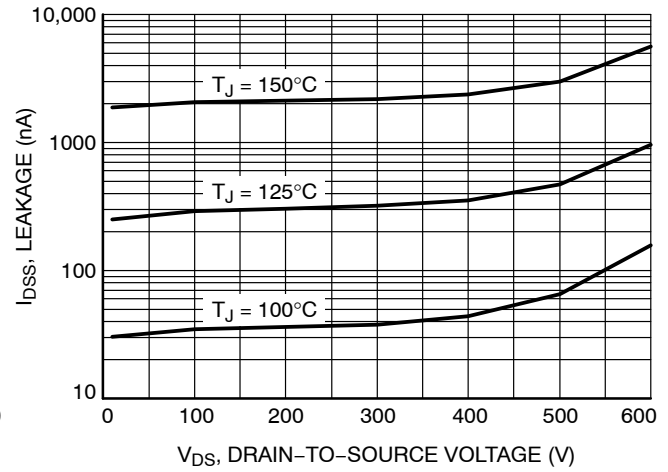
Figure 6. Breakdown Voltage Variation with Temperature

# NDD60N550U1

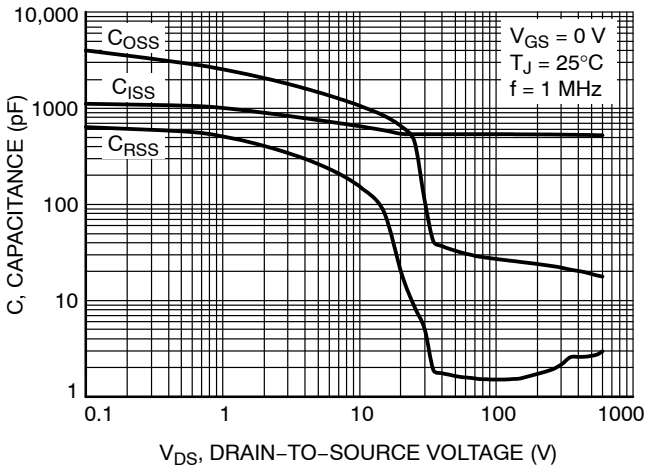
## TYPICAL CHARACTERISTICS



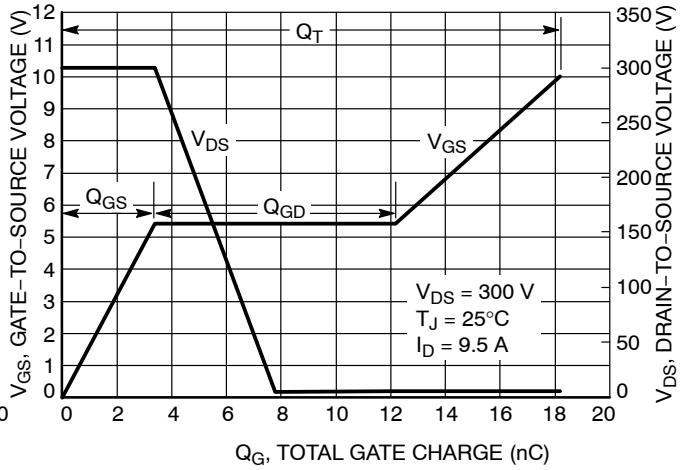
**Figure 7. Threshold Voltage Variation with Temperature**



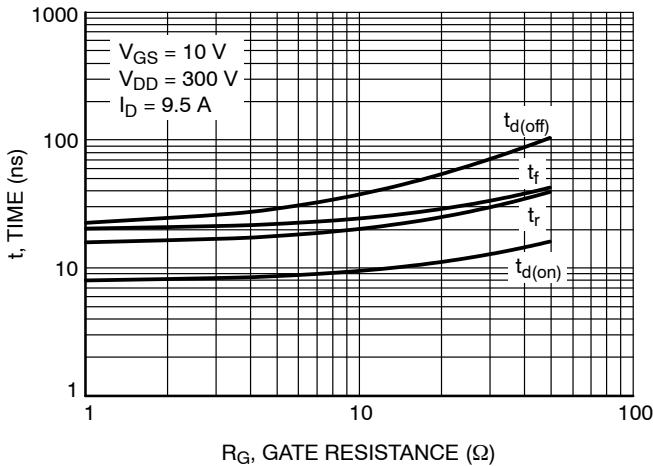
**Figure 8. Drain-to-Source Leakage Current vs. Voltage**



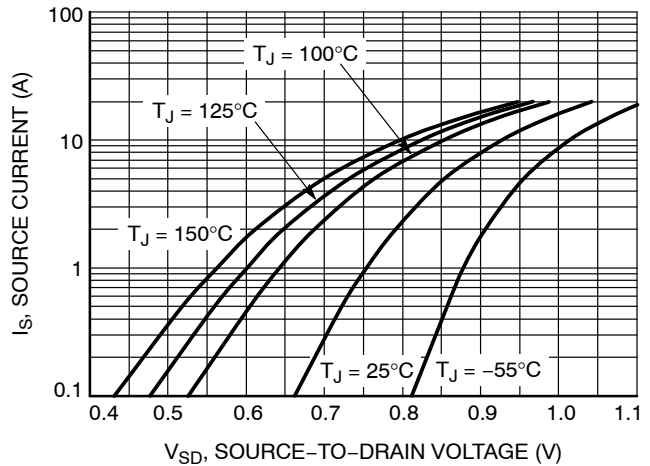
**Figure 9. Capacitance Variation**



**Figure 10. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge**



**Figure 11. Resistive Switching Time Variation vs. Gate Resistance**



**Figure 12. Diode Forward Voltage vs. Current**

# NDD60N550U1

## TYPICAL CHARACTERISTICS

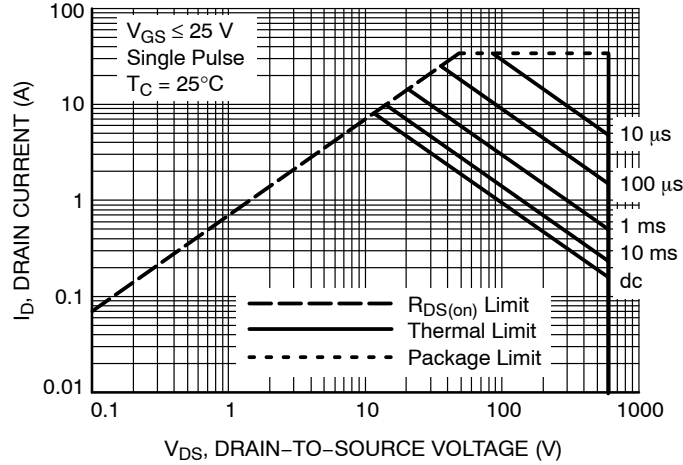


Figure 13. Maximum Rated Forward Biased Safe Operating Area

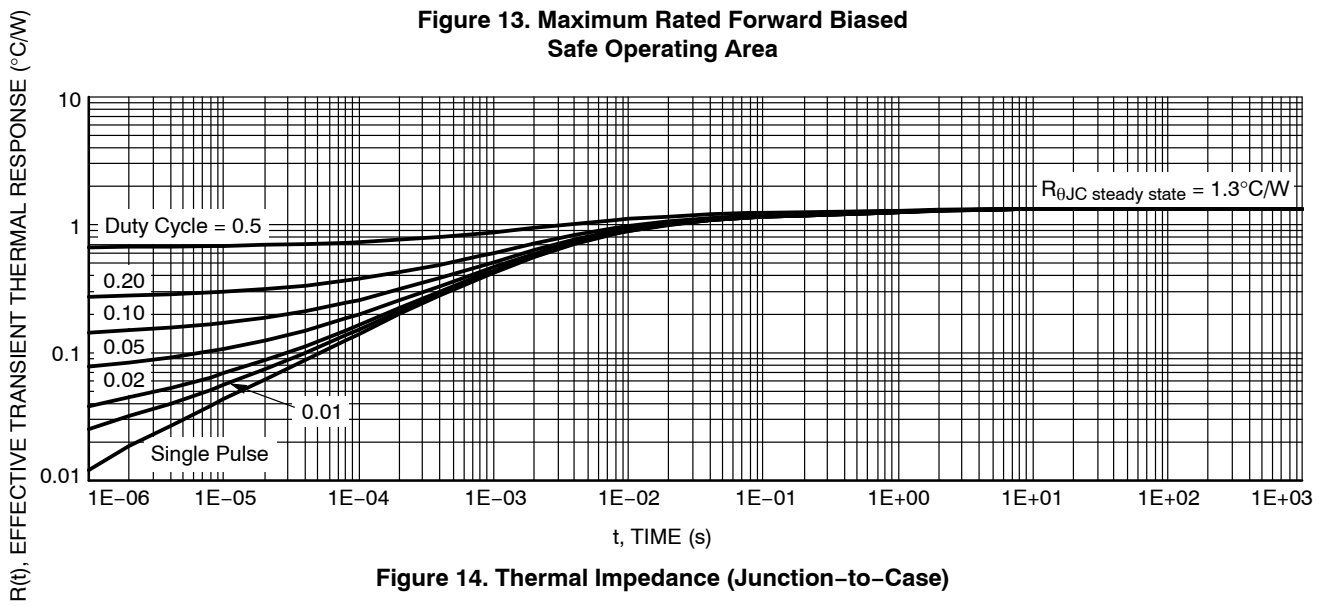
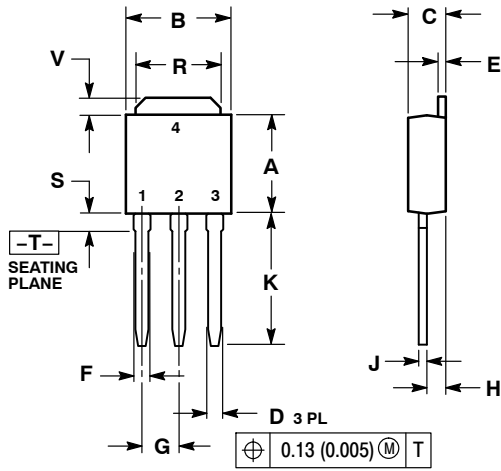


Figure 14. Thermal Impedance (Junction-to-Case)

# NDD60N550U1

## PACKAGE DIMENSIONS

### IPAK CASE 369D ISSUE C

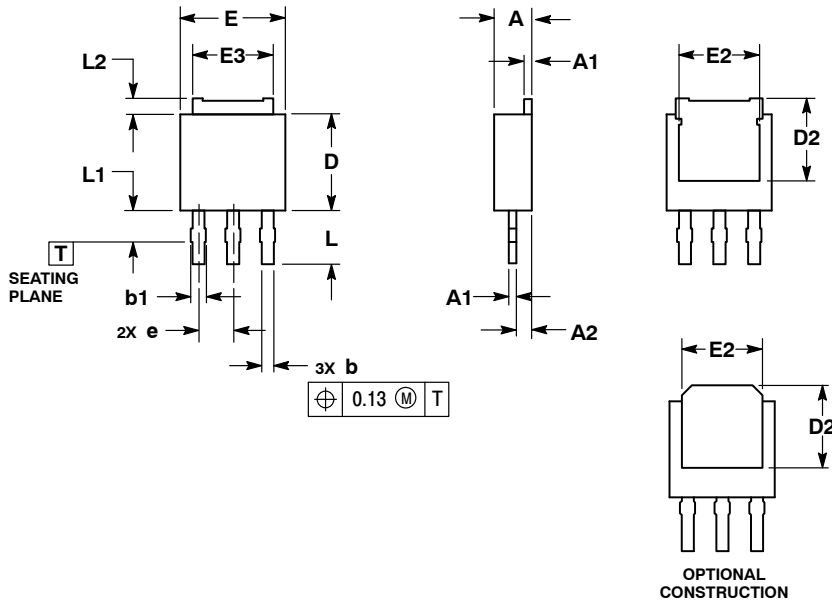


- NOTES:  
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
 2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

- STYLE 2:  
 PIN 1. GATE  
 2. DRAIN  
 3. SOURCE  
 4. DRAIN

### 3.5 MM IPAK, STRAIGHT LEAD CASE 369AD ISSUE B



- NOTES:  
 1.. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.  
 2.. CONTROLLING DIMENSION: MILLIMETERS.  
 3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP.  
 4. DIMENSIONS D AND E DO NOT INCLUDE MOLD GATE OR MOLD FLASH.

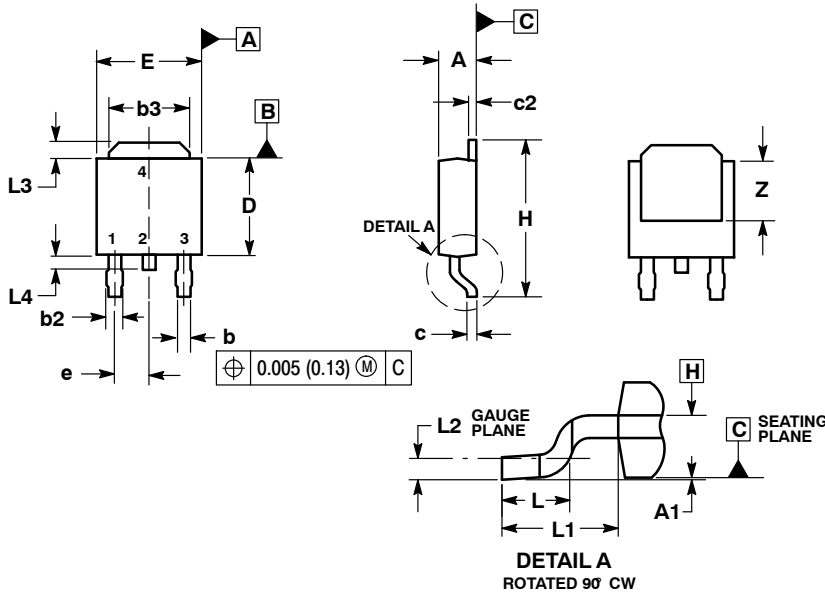
DIM	MILLIMETERS	
	MIN	MAX
A	2.19	2.38
A1	0.46	0.60
A2	0.87	1.10
b	0.69	0.89
b1	0.77	1.10
D	5.97	6.22
D2	4.80	---
E	6.35	6.73
E2	4.57	5.45
E3	4.45	5.46
e	2.28 BSC	
L	3.40	3.60
L1	---	2.10
L2	0.89	1.27

- STYLE 2:  
 PIN 1. GATE  
 2. DRAIN  
 3. SOURCE  
 4. DRAIN

# NDD60N550U1

## PACKAGE DIMENSIONS

### DPAK (SINGLE GAUGE) CASE 369C ISSUE D

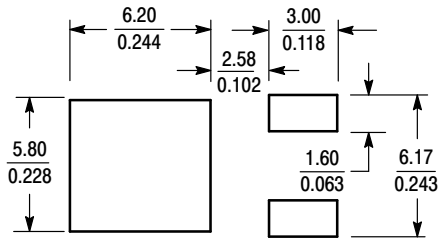


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108 REF		2.74 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

### SOLDERING FOOTPRINT\*




SCALE 3:1  $\left(\frac{\text{mm}}{\text{inches}}\right)$

**STYLE 2:**

1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

### PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT:**

Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
Email: [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5817-1050

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)

**Order Literature:** <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative