Si4736/37/38/39-B20

BROADCAST WEATHER BAND RADIO RECEIVER

Features

- NOAA weather band support (162.4–162.55 MHz)
- Worldwide FM band support (76–108 MHz)
- Worldwide AM band support (520–1710 kHz) (Si4736/37 only)
- 1050 Hz alert tone detection
- Excellent real-world performance
- Freq synthesizer with integrated VCO
- Advanced AM/FM seek tuning
- Automatic frequency control (AFC)
- Automatic gain control (AGC)
- Integrated LDO regulator
- Digital FM stereo decoder
- Adaptive noise suppression
- AM/FM/WB digital tuning
- No manual alignment necessary
- Programmable reference clock
- Volume control
- Programmable soft mute control
- Programmable de-emphasis
- RDS/RBDS processor (Si4737/39 only)
- Optional digital audio output (Si47/39 only)
- Optional digital audio output (Si4737/39 only)
- 2-wire and 3-wire control interface
- 2.7 to 5.5 V supply voltage
- Firmware upgradeable
- 3 x 3 x 0.55 mm 20-pin QFN package
  - Pb-free/RoHS compliant

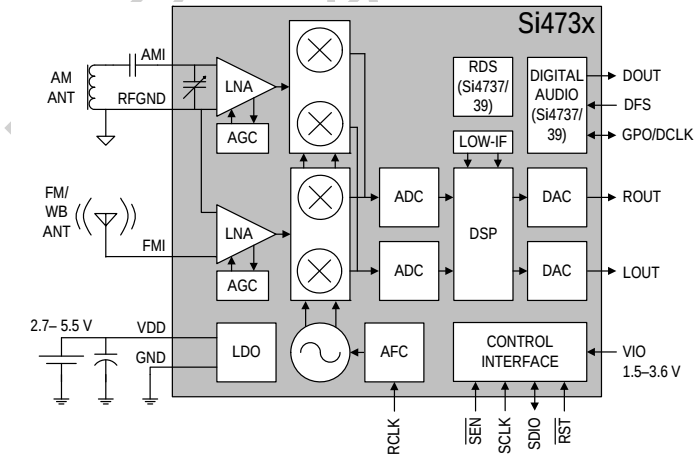
Applications

- Emergency radios
- Table and portable radios
- Stereos
- Mini/micro systems
- Portable media players
- Boom boxes
- Cellular handsets
- Modules
- Clock radios
- Mini HiFi

Description

The Si4736/37/38/39 is the first digital CMOS AM/FM/WB radio receiver IC that integrates the complete tuner function from antenna input to audio output.

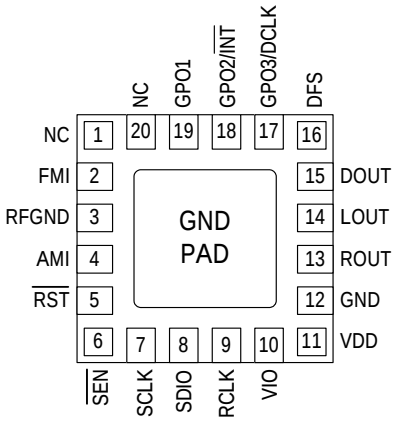
Functional Block Diagram



Ordering Information:
See page 30.

Pin Assignments

Si4736/37/38/39-GM
(Top View)



Patents pending

Notes:

1. To ensure proper operation and receiver performance, follow the guidelines in “AN383: Universal Antenna Selection and Layout Guidelines.” Silicon Laboratories will evaluate schematics and layouts for qualified customers.
2. Place Si4736/37/38/39 as close as possible to antenna jack and keep the FMI and AMI traces as short as possible.

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1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Voltage	V_{DD}		2.7	—	5.5	V
Interface Supply Voltage	V_{IO}		1.5	—	3.6	V
Power Supply Power-Up Rise Time	V_{DDRISE}		10	—	—	µs
Interface Power Supply Power-Up Rise Time	V_{IORISE}		10	—	—	µs
Ambient Temperature	T_A		–20	25	85	°C

Note: All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at VDD = 3.3 V and 25 °C unless otherwise stated. Parameters are tested in production unless otherwise stated.

Table 2. Absolute Maximum Ratings[1,2]

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	–0.5 to 5.8	V
Interface Supply Voltage	V_{IO}	–0.5 to 3.9	V
Input Current[3]	I_{IN}	10	mA
Input Voltage[3]	V_{IN}	–0.3 to (VIO + 0.3)	V
Operating Temperature	T_{OP}	–40 to 95	°C
Storage Temperature	T_{STG}	–55 to 150	°C
RF Input Level[4]		0.4	V_{pK}

Notes:

1. Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure beyond recommended operating conditions for extended periods may affect device reliability.
2. The Si4736/37/38/39 devices are high-performance RF integrated circuits with certain pins having an ESD rating of < 2 kV HBM. Handling and assembly of these devices should only be done at ESD-protected workstations.
3. For input pins SCLK, SEN, SDIO, RST, RCLK, DCLK, DFS, GPO1, GPO2, and GPO3.
4. At RF input pins, FMI and AMI.

Table 3. DC Characteristics

(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
FM Mode						
Supply Current	I_{FM}		—	19.2	22	mA
Supply Current[1]	I_{FM}	Low SNR level	—	19.8	23	mA
RDS Supply Current[2]	I_{FM}		—	19.9	23	mA
Supply Current[2]	I_{FMD}	Digital Output Mode	—	18.0	20.5	mA
WB Mode						
Supply Current	I_{FM}		—	19.2	22	mA
Supply Current	I_{FM}	Low SNR level	—	19.8	23	mA
Supply Current	I_{FMD}		—	17.2	20.5	mA
AM Mode						
Supply Current	I_{AM}	Analog Output Mode	—	17.3	20.5	mA
Supply Current[2]	I_{AMD}	Digital Output Mode	—	15.5	20.5	mA
Supplies and Interface						
Interface Supply Current	I_{IO}		—	320	600	µA
V_{DD} Powerdown Current	I_{DDPD}		—	10	20	µA
V_{IO} Powerdown Current	I_{IOPD}	SCLK, RCLK inactive	—	1	10	µA
High Level Input Voltage[3]	V_{IH}		0.7 x V_{IO}	—	V_{IO} + 0.3	V
Low Level Input Voltage[3]	V_{IL}		–0.3	—	0.3 x V_{IO}	V
High Level Input Current[3]	I_{IH}	V_{IN} = V_{IO} = 3.6 V	–10	—	10	µA
Low Level Input Current[3]	I_{IL}	V_{IN} = 0 V, V_{IO} = 3.6 V	–10	—	10	µA
High Level Output Voltage[4]	V_{OH}	I_{OUT} = 500 µA	0.8 x V_{IO}	—	—	V
Low Level Output Voltage[4]	V_{OL}	I_{OUT} = –500 µA	—	—	0.2 x V_{IO}	V

Notes:
1. LNA is automatically switched to higher current mode for optimum sensitivity in weak signal conditions.
2. Specifications are guaranteed by characterization.
3. For input pins SCLK, SEN, SDIO, RST, RCLK, DCLK, and DFS.
4. For output pins SDIO, DOUT, GPO1, GPO2, and GPO3.

Table 4. Reset Timing Characteristics[1,2,3]

(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Min	Typ	Max	Unit
$\overline{RST}$ Pulse Width and GPO1, GPO2/$\overline{INT}$ Setup to $\overline{RST}$↑[4]	t_{SRST}	100	—	—	µs
GPO1, GPO2/$\overline{INT}$ Hold from $\overline{RST}$↑	t_{HRST}	30	—	—	ns

Important Notes:

1. When selecting 2-wire mode, the user must ensure that a 2-wire start condition (falling edge of SDIO while SCLK is high) does not occur within 300 ns before the rising edge of $\overline{RST}$.
2. When selecting 2-wire mode, the user must ensure that SCLK is high during the rising edge of $\overline{RST}$, and stays high until after the first start condition.
3. When selecting 3-wire or SPI modes, the user must ensure that a rising edge of SCLK does not occur within 300 ns before the rising edge of $\overline{RST}$.
4. If GPO1 and GPO2 are actively driven by the user, then minimum t_{SRST} is only 30 ns. If GPO1 or GPO2 is hi-Z, then minimum t_{SRST} is 100 µs, to provide time for on-chip 1 MΩ devices (active while $\overline{RST}$ is low) to pull GPO1 high and GPO2 low.

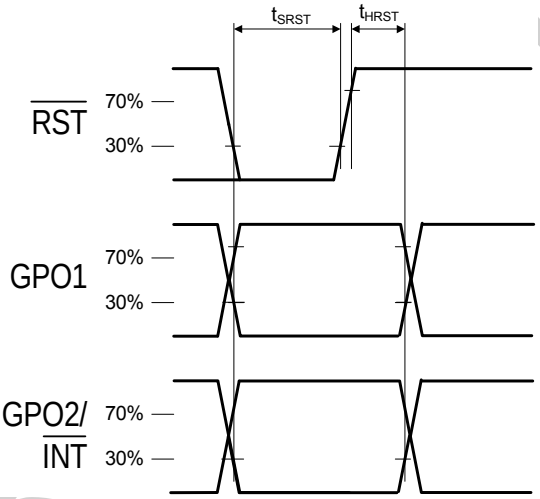


Figure 1. Reset Timing Parameters for Busmode Select

Table 5. 2-Wire Control Interface Characteristics[1,2,3]

(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK Frequency	f_{SCL}		0	—	400	kHz
SCLK Low Time	t_{LOW}		1.3	—	—	µs
SCLK High Time	t_{HIGH}		0.6	—	—	µs
SCLK Input to SDIO ↓ Setup (START)	$t_{SU:STA}$		0.6	—	—	µs
SCLK Input to SDIO ↓ Hold (START)	$t_{HD:STA}$		0.6	—	—	µs
SDIO Input to SCLK ↑ Setup	$t_{SU:DAT}$		100	—	—	ns
SDIO Input to SCLK ↓ Hold[4,5]	$t_{HD:DAT}$		0	—	900	ns
SCLK input to SDIO ↑ Setup (STOP)	$t_{SU:STO}$		0.6	—	—	µs
STOP to START Time	t_{BUF}		1.3	—	—	µs
SDIO Output Fall Time	$t_{f:OUT}$		$20 + 0.1\frac{C_b}{1pF}$	—	250	ns
SDIO Input, SCLK Rise/Fall Time	$t_{f:IN}$ $t_{r:IN}$		$20 + 0.1\frac{C_b}{1pF}$	—	300	ns
SCLK, SDIO Capacitive Loading	C_b		—	—	50	pF
Input Filter Pulse Suppression	t_{SP}		—	—	50	ns

Notes:

1. When V_{IO} = 0 V, SCLK and SDIO are low impedance.
2. When selecting 2-wire mode, the user must ensure that a 2-wire start condition (falling edge of SDIO while SCLK is high) does not occur within 300 ns before the rising edge of $\overline{RST}$.
3. When selecting 2-wire mode, the user must ensure that SCLK is high during the rising edge of $\overline{RST}$, and stays high until after the first start condition.
4. The Si4736/37/38/39 delays SDIO by a minimum of 300 ns from the V_{IH} threshold of SCLK to comply with the minimum $t_{HD:DAT}$ specification.
5. The maximum $t_{HD:DAT}$ has only to be met when f_{SCL} = 400 kHz. At frequencies below 400 kHz, $t_{HD:DAT}$ may be violated as long as all other timing parameters are met.

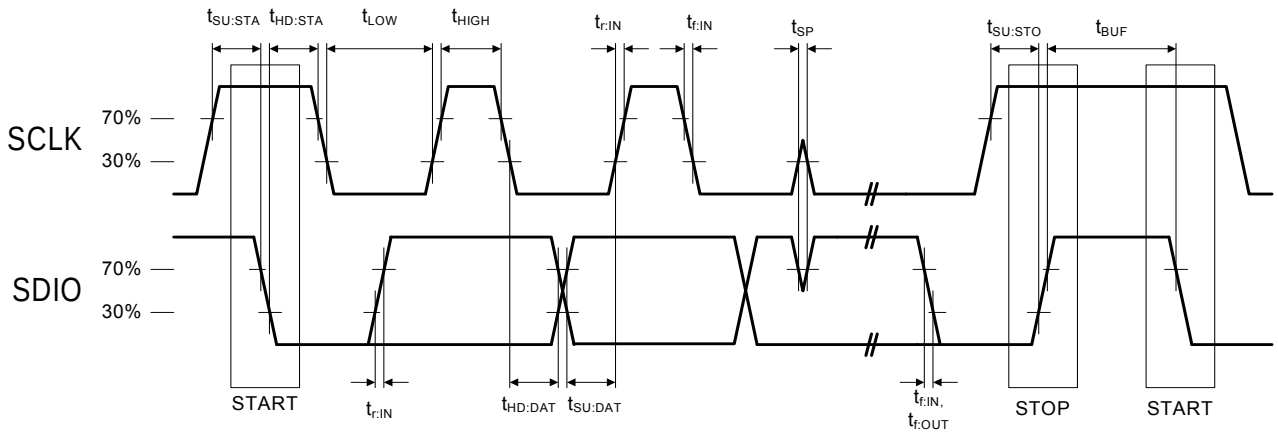


Figure 2. 2-Wire Control Interface Read and Write Timing Parameters

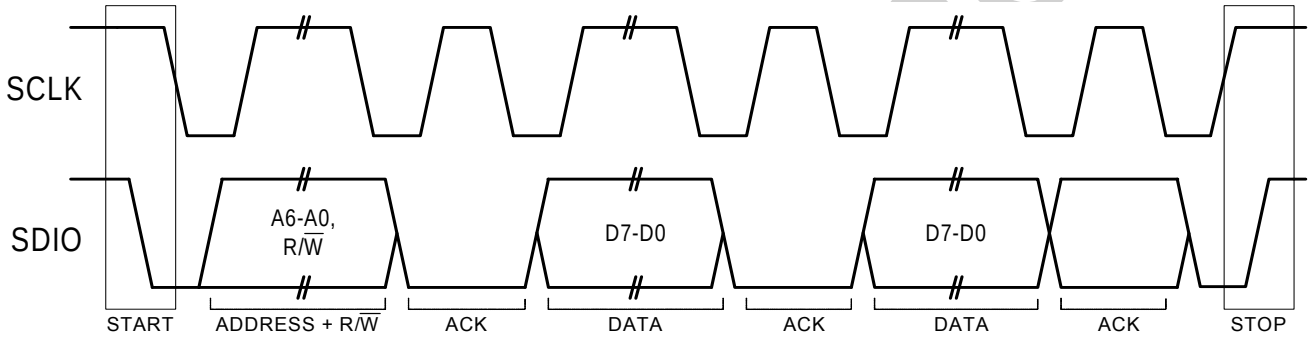


Figure 3. 2-Wire Control Interface Read and Write Timing Diagram

Table 6. 3-Wire Control Interface Characteristics

(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK Frequency	f_{CLK}		0	—	2.5	MHz
SCLK High Time	t_{HIGH}		25	—	—	ns
SCLK Low Time	t_{LOW}		25	—	—	ns
SDIO Input, $\overline{SEN}$ to SCLK↑ Setup	t_S		20	—	—	ns
SDIO Input to SCLK↑ Hold	t_{HSDIO}		10	—	—	ns
$\overline{SEN}$ Input to SCLK↓ Hold	t_{HSEN}		10	—	—	ns
SCLK↑ to SDIO Output Valid	t_{CDV}	Read	2	—	25	ns
SCLK↑ to SDIO Output High Z	t_{CDZ}	Read	2	—	25	ns
SCLK, $\overline{SEN}$, SDIO, Rise/Fall time	t_R, t_F		—	—	10	ns

Note: When selecting 3-wire mode, the user must ensure that a rising edge of SCLK does not occur within 300 ns before the rising edge of $\overline{RST}$.

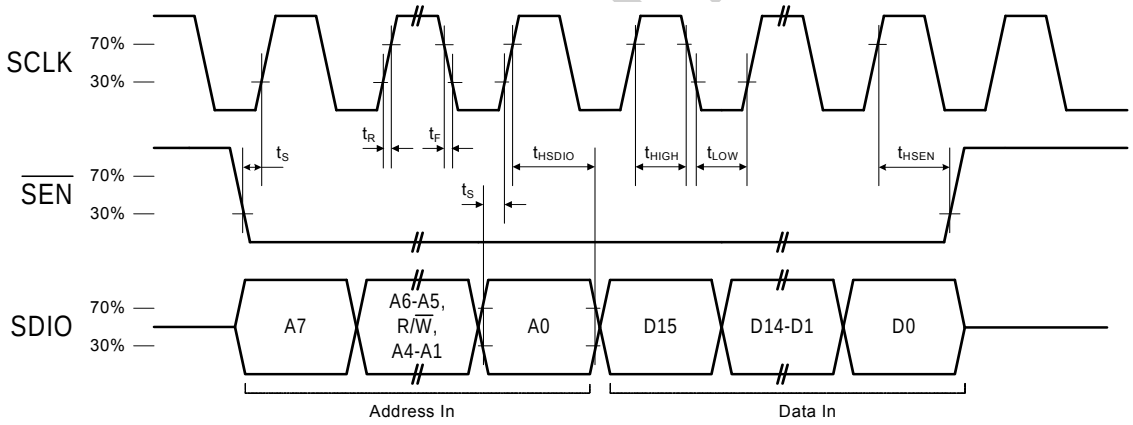


Figure 4. 3-Wire Control Interface Write Timing Parameters

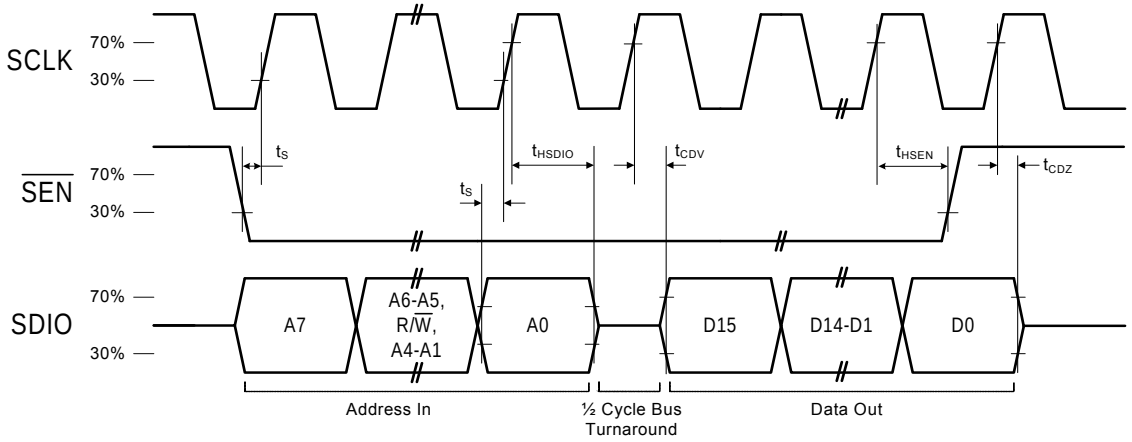


Figure 5. 3-Wire Control Interface Read Timing Parameters

Table 7. SPI Control Interface Characteristics

(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK Frequency	f_{CLK}		0	—	2.5	MHz
SCLK High Time	t_{HIGH}		25	—	—	ns
SCLK Low Time	t_{LOW}		25	—	—	ns
SDIO Input, $\overline{SEN}$ to SCLK↑ Setup	t_S		15	—	—	ns
SDIO Input to SCLK↑ Hold	t_{HSDIO}		10	—	—	ns
$\overline{SEN}$ Input to SCLK↓ Hold	t_{HSEN}		5	—	—	ns
SCLK↓ to SDIO Output Valid	t_{CDV}	Read	2	—	25	ns
SCLK↓ to SDIO Output High Z	t_{CDZ}	Read	2	—	25	ns
SCLK, $\overline{SEN}$, SDIO, Rise/Fall time	t_R, t_F		—	—	10	ns

Note: When selecting SPI mode, the user must ensure that a rising edge of SCLK does not occur within 300 ns before the rising edge of $\overline{RST}$.

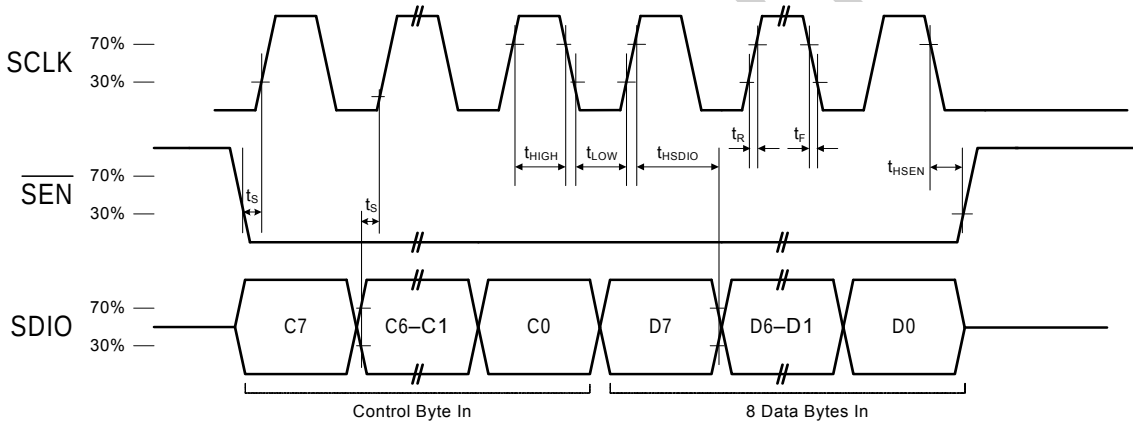


Figure 6. SPI Control Interface Write Timing Parameters

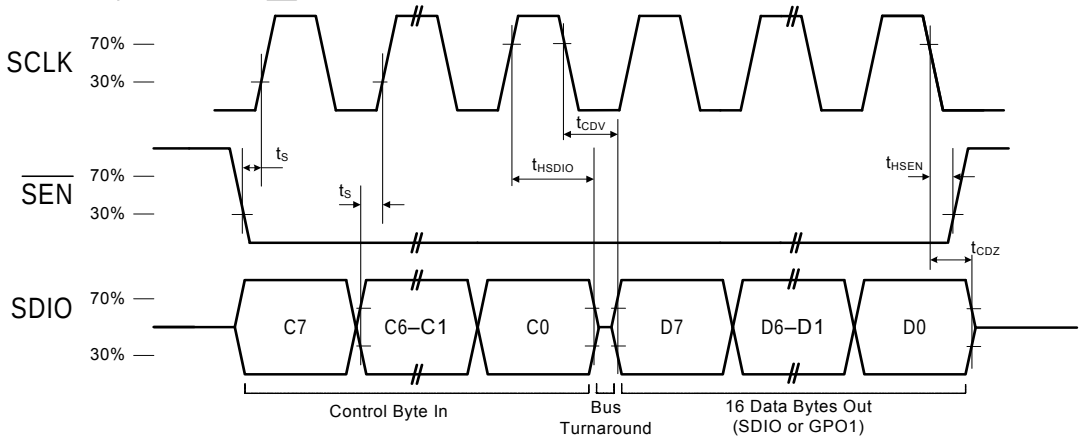


Figure 7. SPI Control Interface Read Timing Parameters

Table 8. Digital Audio Interface Characteristics
(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DCLK Cycle Time	t_{DCT}		26	—	1000	ns
DCLK Pulse Width High	t_{DCH}		10	—	—	ns
DCLK Pulse Width Low	t_{DCL}		10	—	—	ns
DFS Set-up Time to DCLK Rising Edge	$t_{SU:DFS}$		5	—	—	ns
DFS Hold Time from DCLK Rising Edge	$t_{HD:DFS}$		5	—	—	ns
DOUT Propagation Delay from DCLK Falling Edge	$t_{PD:DOUT}$		0	—	12	ns

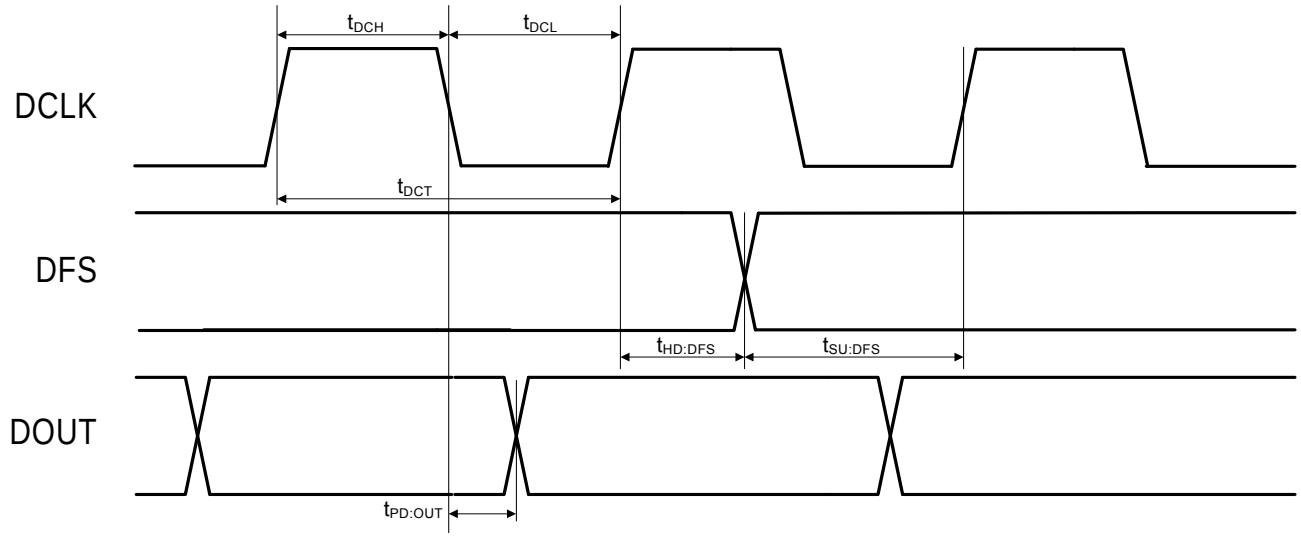


Figure 8. Digital Audio Interface Timing Parameters, I^2S Mode

Table 9. FM Receiver Characteristics[1,2]

(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Frequency	f_{RF}		76	—	108	MHz
Sensitivity with Headphone Network[3,4,5]		(S+N)/N = 26 dB	—	2.2	3.5	µV EMF
Sensitivity with 50 Ω Network[3,4,5,6]		(S+N)/N = 26 dB	—	1.1	—	µV EMF
RDS Sensitivity[6]		Δf = 2 kHz, RDS BLER < 5%	—	15	—	µV EMF
LNA Input Resistance[6,7]			3	4	5	kΩ
LNA Input Capacitance[6,7]			4	5	6	pF
Input IP3[6,8]			100	105	—	dBµV EMF
AM Suppression[3,4,6,7]		m = 0.3	40	50	—	dB
Adjacent Channel Selectivity		±200 kHz	35	50	—	dB
Alternate Channel Selectivity		±400 kHz	60	70	—	dB
Spurious Response Rejection[6]		In-band	35	—	—	dB
Audio Output Voltage[3,4,7]			72	80	90	mV_{RMS}
Audio Output L/R Imbalance[3,7,9]			—	—	1	dB
Audio Frequency Response Low[6]		–3 dB	—	—	30	Hz
Audio Frequency Response High[6]		–3 dB	15	—	—	kHz
Audio Stereo Separation[7,9]			25	—	—	dB
Audio Mono S/N[3,4,5,7,10]			55	63	—	dB
Audio Stereo S/N[4,5,7,10,11]			—	58	—	dB
Audio THD[3,7,9]			—	0.1	0.5	%
De-emphasis Time Constant[6]		FM_DEEMPHASIS = 2	70	75	80	µs
		FM_DEEMPHASIS = 1	45	50	54	µs
Audio Output Load Resistance[6,10]	R_L	Single-ended	10	—	—	kΩ
Audio Output Load Capacitance[6,10]	C_L	Single-ended	—	—	50	pF

Notes:

1. Additional testing information is available in Application Note AN388. Volume = maximum for all tests. Tested at RF = 98.1 MHz.
2. To ensure proper operation and receiver performance, follow the guidelines in “AN383: Antenna Selection and Universal Layout Guidelines.” Silicon Laboratories will evaluate schematics and layouts for qualified customers.
3. F_{MOD} = 1 kHz, 75 µs de-emphasis, MONO = enabled, and L = R unless noted otherwise.
4. Δf = 22.5 kHz.
5. B_{AF} = 300 Hz to 15 kHz, A-weighted.
6. Guaranteed by characterization.
7. V_{EMF} = 1 mV.
8. $|f_2 – f_1| > 2$ MHz, $f_0 = 2 \times f_1 – f_2$. AGC is disabled. Refer to "6. Pin Descriptions: Si4736/37/38/39-GM" on page 29.
9. Δf = 75 kHz.
10. At L_{OUT} and R_{OUT} pins.
11. Analog audio output mode.
12. At temperature (25 °C).

Table 9. FM Receiver Characteristics[1,2] (Continued)

(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Seek/Tune Time[6]		RCLK tolerance = 100 ppm	—	—	80	ms/channel
Powerup Time[6]		From powerdown	—	—	110	ms
RSSI Offset[12]		Input levels of 8 and 60 dBµV at RF Input	–3	—	3	dB

Notes:
1. Additional testing information is available in Application Note AN388. Volume = maximum for all tests. Tested at RF = 98.1 MHz.
2. To ensure proper operation and receiver performance, follow the guidelines in "AN383: Antenna Selection and Universal Layout Guidelines." Silicon Laboratories will evaluate schematics and layouts for qualified customers.
3. F_{MOD} = 1 kHz, 75 µs de-emphasis, MONO = enabled, and L = R unless noted otherwise.
4. Δf = 22.5 kHz.
5. B_{AF} = 300 Hz to 15 kHz, A-weighted.
6. Guaranteed by characterization.
7. V_{EMF} = 1 mV.
8. $|f_2 - f_1| > 2$ MHz, $f_0 = 2 \times f_1 - f_2$. AGC is disabled. Refer to "6. Pin Descriptions: Si4736/37/38/39-GM" on page 29.
9. Δf = 75 kHz.
10. At L_{OUT} and R_{OUT} pins.
11. Analog audio output mode.
12. At temperature (25 °C).

Table 10. WB Receiver Characteristics[1]

(V_{DD} = 2.7 to 5.5 V, VIO = 1.5 to 3.6V, T_A = 25 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Frequency	f_R		162.4	—	162.55	MHz
Sensitivity[2,3]		SINAD = 12 dB	—	0.9	—	µV EMF
Adjacent Channel Selectivity		+/-25 kHz	—	52	—	dB
Audio S/N[2,3,4,5]		Mono	—	45	—	dB
Audio Frequency Response Low[6]		–3 dB	—	—	300	Hz
Audio Frequency Response High[6]		–3 dB	3	—	—	kHz

Notes:
1. To ensure proper operation and receiver performance, follow the guidelines in "AN383: Universal Antenna Selection and Layout Guidelines." Silicon Laboratories will evaluate schematics and layouts for qualified customers.
2. F_{MOD} = 1 kHz.
3. Δf = 3 kHz.
4. V_{EMF} = 1 mV.
5. A-weighted.
6. Guaranteed by characterization

Table 11. AM Receiver Characteristics[1]

(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, TA = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Frequency	f_{RF}		520	—	1710	kHz
Sensitivity[2,3,4,5, 6]		(S+N)/N = 26 dB	—	25	35	µV EMF
Large Signal Voltage Handling[5,7]		THD < 8%	—	300	—	mV_{RMS}
Power Supply Rejection Ratio		ΔV_{DD} = 100 mV_{RMS}, 100 Hz	—	40	—	dB
Audio Output Voltage[2,8]			54	60	67	mV_{RMS}
Audio S/N[2,3,4,6,8]			50	56	—	dB
Audio THD[2,4,8]			—	0.1	0.5	%
Antenna Inductance[5,9]			180	—	450	µH
Powerup Time		From powerdown	—	—	110	ms

Notes:

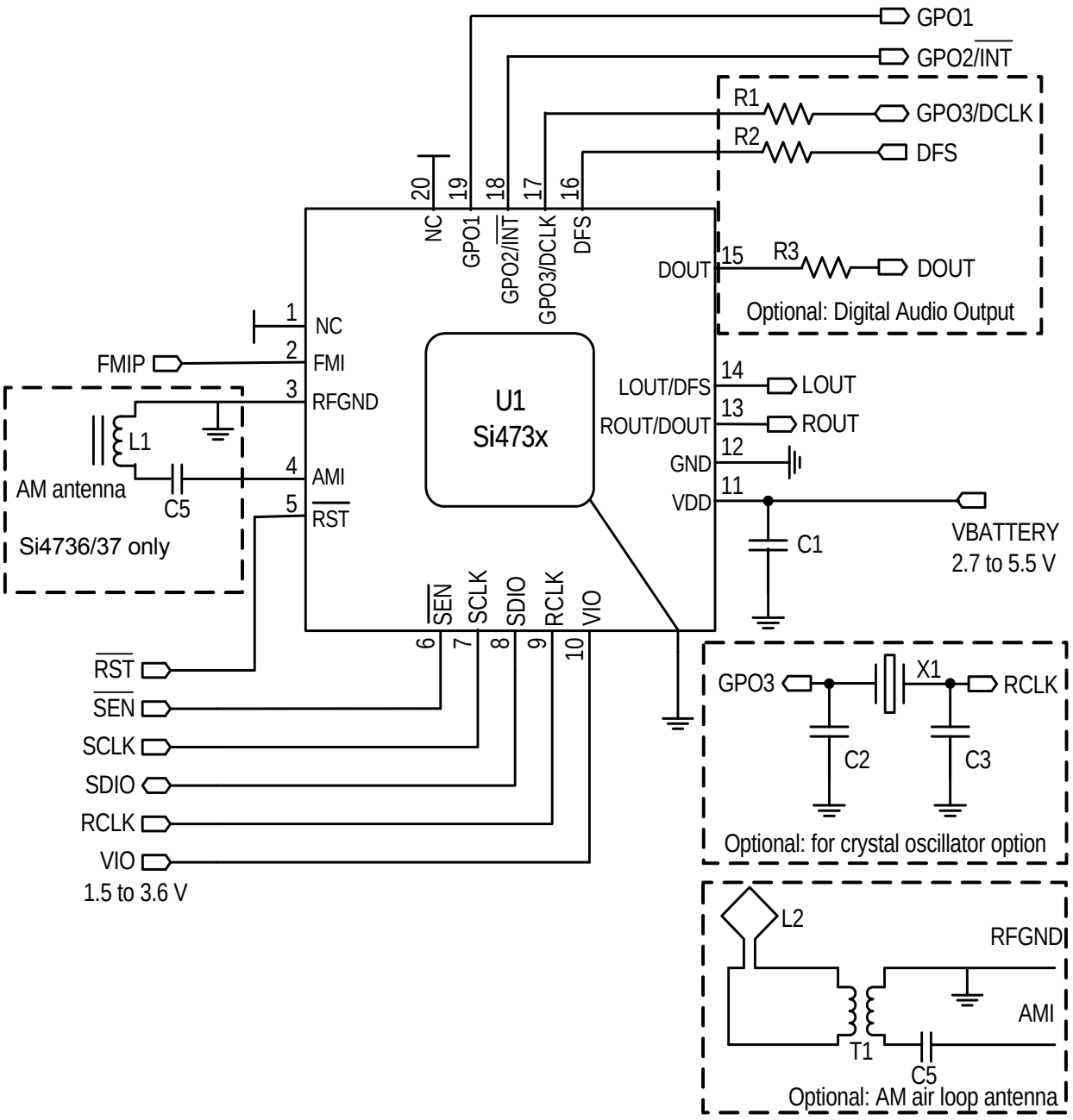
1. To ensure proper operation and receiver performance, follow the guidelines in “AN383: Antenna Selection and Universal Layout Guidelines.” Silicon Laboratories will evaluate schematics and layouts for qualified customers.
2. FMOD = 1 kHz, 30% modulation, A-weighted, 2 kHz channel filter.
3. B_{AF} = 300 Hz to 15 kHz, A-weighted.
4. f_{RF} = 1000 kHz, Δf = 10 kHz.
5. Guaranteed by characterization.
6. Analog audio output mode.
7. See “AN388: Evaluation Board Test Procedure” for evaluation method.
8. V_{IN} = 5 mVrms.
9. Stray capacitance on antenna and board must be < 10 pF to achieve full tuning range at higher inductance levels.

Table 12. Reference Clock and Crystal Characteristics
(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Reference Clock						
RCLK Supported Frequencies*			31.130	32.768	40000.0	kHz
RCLK Frequency Tolerance			–50	—	50	ppm
REFCLK_PRESCALE			1	—	4095	
REFCLK			31.130	32.768	34.406	kHz
Crystal Oscillator						
Crystal Oscillator Frequency			—	32.768	—	kHz
Crystal Frequency Tolerance*			–100	—	100	ppm
Board Capacitance			—	—	3.5	pF

***Note:** The Si4736/37/38/39 divides the RCLK input by REFCLK_PRESCALE to obtain REFCLK. There are some RCLK frequencies between 31.130 kHz and 40 MHz that are not supported. See AN332, Table 6 for more details.

2. Typical Application Schematic



Notes:

1. Place C1 close to V_{DD} pin.
2. All grounds connect directly to GND plane on PCB.
3. Pins 1 and 20 are no connects, leave floating.
4. To ensure proper operation and receiver performance, follow the guidelines in "AN383: Universal Antenna Selection and Layout Guidelines." Silicon Laboratories will evaluate schematics and layouts for qualified customers.
5. Pin 2 connects to the FM antenna interface, and pin 4 connects to the AM antenna interface.
6. RFGND should be locally isolated from GND.
7. Place Si4736/37/38/39 as close as possible to antenna jack and keep the FMI and AMI traces as short as possible.

3. Bill of Materials

Component(s)	Value/Description	Supplier
C1	Supply bypass capacitor, 22 nF, ±20%, Z5U/X7R	Murata
C5	Coupling capacitor, 0.47 µF, ±20%, Z5U/X7R	Murata
L1	Ferrite loop stick, 180–450 µH	Jiaxin
U1	Si4736/37/38/39 AM/FM/WB Radio Tuner	Silicon Laboratories
Optional Components		
T1	Transformer, 1–5 turns ratio	Jiaxin, UMEC
L2	Air loop antenna, 10–20 µH	Various
C2, C3	Crystal load capacitors, 22 pF, ±5%, COG (Optional: for crystal oscillator option)	Venkel
X1	32.768 kHz crystal (Optional: for crystal oscillator option)	Epson
R1	Resistor, 2 kΩ (Optional: for digital audio)	Venkel
R2	Resistor, 2 kΩ (Optional: for digital audio)	Venkel
R3	Resistor, 600 Ω (Optional: for digital audio)	Venkel

4. Functional Description

4.1. Overview

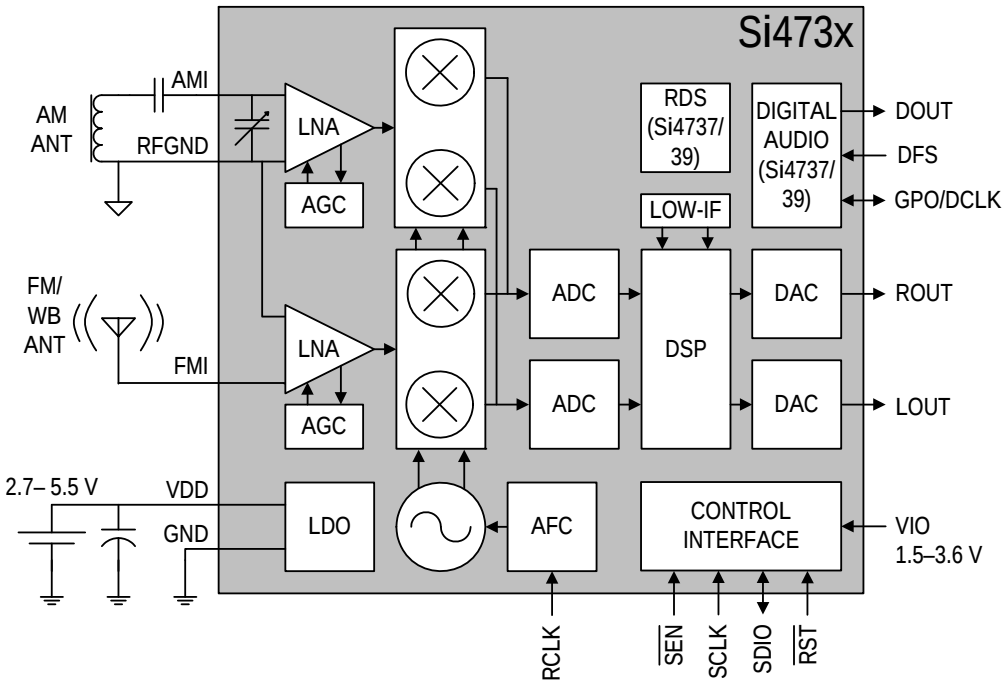


Figure 9. Functional Block Diagram

The Si4736/37 and Si4738/39 are the industry's first fully integrated, 100% CMOS AM/FM/WB and FM/WB radio receiver ICs. Offering unmatched integration and PCB space savings, the Si4736/37/38/39 requires only two external components and less than 15 mm^2 of board area, excluding the antenna inputs. The Si4736/37/38/39 AM/FM/WB radio provides the space savings and low power consumption necessary for portable devices while delivering the high performance and design simplicity desired for all AM/FM/WB solutions.

Leveraging Silicon Laboratories' proven and patented Si4700/01 FM tuner's digital low intermediate frequency (low-IF) receiver architecture, the Si4736/37/38/39 delivers superior RF performance and interference rejection in both AM and FM bands. The high integration and complete system production test simplifies design-in, increases system quality, and improves manufacturability.

The Si4736/37/38/39 is a feature-rich solution including 1050 Hz tone detection, advanced seek algorithms, soft mute, auto-calibrated digital tuning, and FM stereo processing. In addition, the Si4736/37/38/39 provides analog and digital audio outputs and a programmable reference clock. The device supports I^2C-compatible, 2-wire control interface, SPI, and a Si4700/01 backwards-compatible, 3-wire control interface.

The Si4736/37/38/39 utilizes digital processing to achieve high fidelity, optimal performance, and design flexibility. The chip provides excellent pilot rejection, selectivity, and unmatched audio performance, and offers both the manufacturer and the end-user extensive programmability and flexibility in listening experience.

The Si4737/39 incorporates a digital processor for the European Radio Data System (RDS) and the North American Radio Broadcast Data System (RBDS), and includes all required symbol decoding, block synchronization, error detection, and error correction functions. Using this feature, the Si4737/39 enables broadcast data such as station identification and song name to be displayed to the user.

4.2. Operating Modes

The Si4736/37/38/39 operates in an FM receive, an AM receive, or a weather band receive mode. In FM mode and WB mode, radio signals are received on FMI (pin 2) and processed by the FM front-end circuitry. In AM mode, radio signals are received on AMI (pin 4) and processed by the AM front-end circuitry. In addition to the receiver mode, there is a clocking mode to choose to clock the Si473x from a reference clock or crystal. On the Si4737/39, there is an audio output mode to choose between an analog and/or digital audio output. In the analog audio output mode, pin 13 is ROUT, pin 14 is LOUT, and pin 17 is GPO3. In the digital audio mode, pin 15 is DOUT, pin 16 is DFS, and pin 17 is DCLK. Concurrent analog/digital audio output mode requires pins 13, 14, 15, 16, and 17. The receiver mode and the audio output mode are set by the POWER_UP command listed in Table 12. Si473x Command Summary.

4.3. FM Receiver

The Si4736/37/38/39 FM receiver is based on the proven Si4700/01 FM tuner. The receiver uses a digital low-IF architecture, allowing the elimination of external components and factory adjustments. The Si4736/37/38/39 integrates a low noise amplifier (LNA) supporting the worldwide FM broadcast band (76 to 108 MHz). An AGC circuit controls the gain of the LNA to optimize sensitivity and rejection of strong interferers. For testing purposes, the AGC can be disabled. Refer to Section "5. Commands and Properties" on page 25 for additional programming and configuration information. An image-reject mixer downconverts the RF signal to low-IF. The quadrature mixer output is amplified, filtered, and digitized with high resolution analog-to-digital converters (ADCs). This advanced architecture allows the Si4736/37/38/39 to perform channel selection, FM demodulation, and stereo audio processing to achieve superior performance compared to traditional analog architectures.

4.4. AM Receiver (Si4736/37)

The highly integrated Si4736/37 supports worldwide AM band reception from 520 to 1710 kHz using a digital low-IF architecture with a minimum number of external components and no manual alignment required. This digital low-IF architecture allows for high-precision filtering and offers excellent selectivity and noise suppression. The DSP also provides 9 or 10 kHz channel selection, AM demodulation, soft mute, and additional features such as adjustable channel bandwidth settings. Similar to the FM receiver, the integrated LNA and AGC optimize sensitivity and rejection of strong interferers allowing better reception of weak stations.

The Si4736/37 provides highly accurate digital AM tuning without factory adjustments. To offer maximum flexibility, the receiver supports a wide range of ferrite loop sticks from 180–450 µH. An air loop antenna is supported by using a transformer to increase the effective inductance from the air loop. Using a 1:5 turn ratio inductor, the inductance is increased by 25 times and easily supports all typical AM air loop antennas, which generally vary between 10 and 20 µH.

4.5. Weather Band Receiver

The Si4736/37/38/39 supports weather band reception from 162.4 to 162.55 MHz. The highly integrated Si4736/37/38/39 meets NOAA specification, receives all seven NOAA specified frequencies, implements narrow-band FM de-emphasis, and supports 1050 Hz alert tone detection. In addition, the Si4736/37/38/39 provides advanced features not available on conventional radios, such as an AFC and a dynamic channel bandwidth filter.

The AFC locks on to the strongest signal within a narrow, adjustable frequency range to compensate for any potential frequency errors such as crystal tolerance or transmit frequency errors. The AFC ensures the channel filter is always centered on the desired channel providing optimal reception. The dynamic channel bandwidth feature utilizes a wide filter in strong signal conditions to provide best sound quality and a narrower filter in weak conditions to provide best sensitivity.

4.6. Digital Audio Interface (Si4737/39 Only)

The digital audio interface operates in slave mode and supports three different audio data formats:

- I^2S
- Left-Justified
- DSP Mode

4.6.1. Audio Data Formats

In I^2S mode, by default the MSB is captured on the second rising edge of DCLK following each DFS transition. The remaining bits of the word are sent in order, down to the LSB. The left channel is transferred first when the DFS is low, and the right channel is transferred when the DFS is high.

In Left-Justified mode, by default the MSB is captured on the first rising edge of DCLK following each DFS transition. The remaining bits of the word are sent in order, down to the LSB. The left channel is transferred first when the DFS is high, and the right channel is transferred when the DFS is low.

In DSP mode, the DFS becomes a pulse with a width of 1DCLK period. The left channel is transferred first, followed right away by the right channel. There are two options in transferring the digital audio data in DSP mode: the MSB of the left channel can be transferred on the first rising edge of DCLK following the DFS pulse or on the second rising edge.

In all audio formats, depending on the word size, DCLK frequency and sample rates, there may be unused DCLK cycles after the LSB of each word before the next DFS transition and MSB of the next word. In addition, if preferred, the user can configure the MSB to be captured on the falling edge of DCLK via properties. The number of audio bits can be configured for 8, 16, 20, or 24 bits.

4.6.2. Audio Sample Rates

The device supports a number of industry-standard sampling rates including 32, 40, 44.1, and 48 kHz. The digital audio interface enables low-power operation by eliminating the need for redundant DACs on the audio baseband processor.

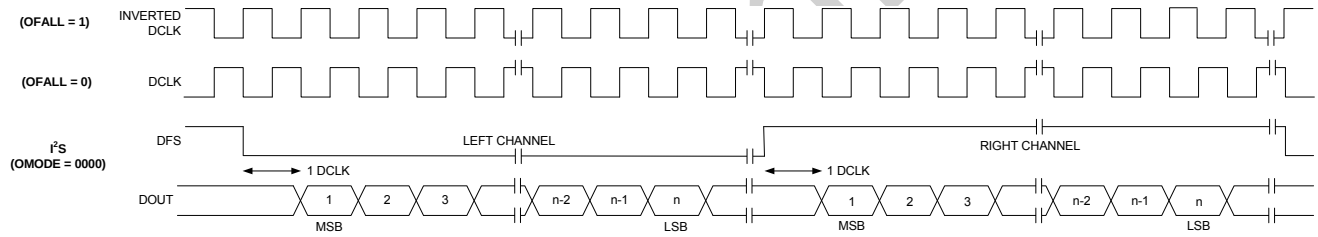


Figure 10. I^2S Digital Audio Format

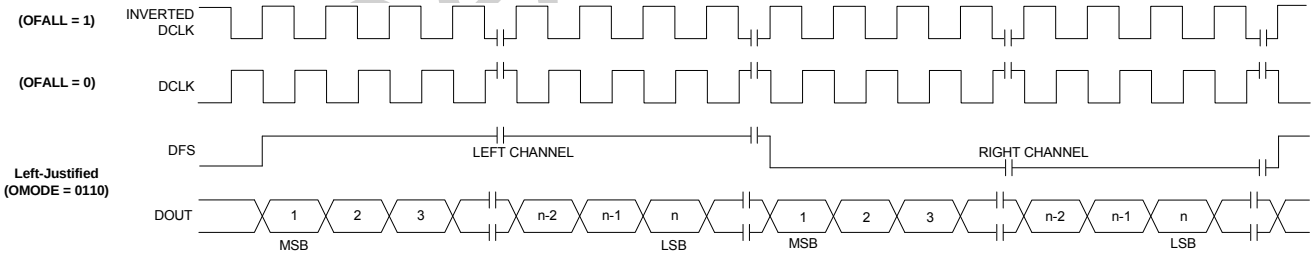


Figure 11. Left-Justified Digital Audio Format

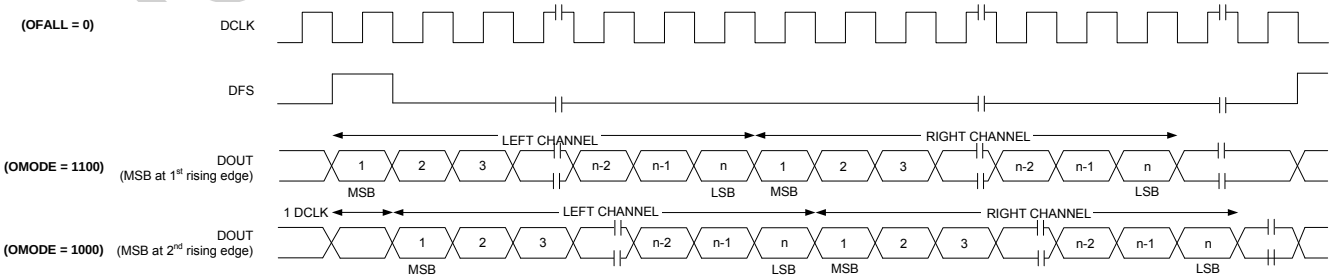


Figure 12. DSP Digital Audio Format

4.7. Stereo Audio Processing

The output of the FM demodulator is a stereo multiplexed (MPX) signal. The MPX standard was developed in 1961, and is used worldwide. Today's MPX signal format consists of left + right (L+R) audio, left – right (L–R) audio, a 19 kHz pilot tone, and RDS/RBDS data as shown in Figure 13 below.

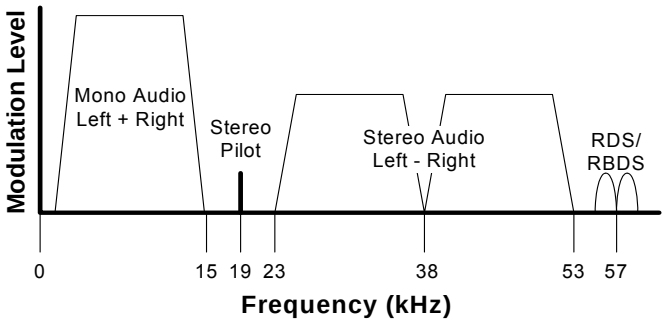


Figure 13. MPX Signal Spectrum

4.7.1. Stereo Decoder

The Si4736/37/38/39's integrated stereo decoder automatically decodes the MPX signal using DSP techniques. The 0 to 15 kHz (L+R) signal is the mono output of the FM tuner. Stereo is generated from the (L+R), (L–R), and a 19 kHz pilot tone. The pilot tone is used as a reference to recover the (L–R) signal. Output left and right channels are obtained by adding and subtracting the (L+R) and (L–R) signals respectively. The Si4737/39 uses frequency information from the 19 kHz stereo pilot to recover the 57 kHz RDS/RBDS signal.

4.7.2. Stereo-Mono Blending

Adaptive noise suppression is employed to gradually combine the stereo left and right audio channels to a mono (L+R) audio signal as the signal quality degrades to maintain optimum sound fidelity under varying reception conditions. Stereo/mono status can be monitored with the FM_RSQ_STATUS command. Mono operation can be forced with the FM_BLEND_MONO_THRESHOLD property.

4.8. De-emphasis

Pre-emphasis and de-emphasis is a technique used by FM broadcasters to improve the signal-to-noise ratio of FM receivers by reducing the effects of high-frequency interference and noise. When the FM signal is transmitted, a pre-emphasis filter is applied to accentuate the high audio frequencies. The Si4736/37/38/39 incorporates a de-emphasis filter which attenuates high frequencies to restore a flat frequency response. Two time constants are used in various regions. The de-emphasis time constant is programmable to 50 or 75 µs and is set by the FM_DEEMPHASIS property.

4.9. Stereo DAC

High-fidelity stereo digital-to-analog converters (DACs) drive analog audio signals onto the LOUT and ROUT pins. The audio output may be muted. Volume is adjusted digitally with the RX_VOLUME property.

4.10. Soft Mute

The soft mute feature is available to attenuate the audio outputs and minimize audible noise in very weak signal conditions. The softmute attenuation level is adjustable using the FM_SOFT_MUTE_MAX_ATTENUATION and AM_SOFT_MUTE_MAX_ATTENUATION properties.

4.11. RDS/RBDS Processor (Si4737/39 Only)

The Si4737/39 implements an RDS/RBDS* processor for symbol decoding, block synchronization, error detection, and error correction.

The Si4737/39 device is user configurable and provides an optional interrupt when RDS is synchronized, loses synchronization, and/or the user configurable RDS FIFO threshold has been met.

The Si4737/39 reports RDS decoder synchronization status, and detailed bit errors in the information word for each RDS block with the FM_RDS_STATUS command. The range of reportable block errors is 0, 1–2, 3–5, or 6+. More than six errors indicates that the corresponding block information word contains six or more non-correctable errors, or that the block checkword contains errors.

***Note:** RDS/RBDS is referred to only as RDS throughout the remainder of this document.

4.12. Tuning

The frequency synthesizer uses Silicon Laboratories' proven technology, including a completely integrated VCO. The frequency synthesizer generates the quadrature local oscillator signal used to downconvert the RF input to a low intermediate frequency. The VCO frequency is locked to the reference clock and adjusted with an AFC servo loop during reception. The tuning frequency can be directly programmed using the WB_TUNE_FREQ, FM_TUNE_FREQ, and AM_TUNE_FREQ commands. The Si4736/37/38/39 supports channel spacing of 25 kHz in WB mode; 50, 100, or 200 kHz in FM mode; and 9 or 10 kHz in AM mode.

4.13. Seek

Seek tuning will search up or down for a valid channel. Valid channels are found when the receive signal strength indicator (RSSI) and the signal-to-noise ratio (SNR) values exceed the set threshold. Using the SNR qualifier rather than solely relying on the more traditional RSSI qualifier can reduce false stops and increase the number of valid stations detected. Seek is initiated using the FM_SEEK_START and AM_SEEK_START commands. The RSSI and SNR threshold settings are adjustable using properties (see Table 15).

Two seek options are available. The device will either wrap or stop at the band limits. If the seek operation is unable to find a channel, the device will indicate failure and return to the channel selected before the seek operation began.

Seek is not available for weather band.

4.14. Reference Clock

The Si4736/37/38/39 reference clock is programmable, supporting RCLK frequencies in Table 12. Refer to Table 3, "DC Characteristics," on page 5 for switching voltage levels and Table 9, "FM Receiver Characteristics" on page 12 for frequency tolerance information.

An onboard crystal oscillator is available to generate the 32.768 kHz reference when an external crystal and load capacitors are provided. Refer to "2. Typical Application Schematic" on page 16. This mode is enabled using the POWER_UP command, see Table 14, "Si473x Command Summary," on page 25.

The Si4736/37/38/39 performance may be affected by data activity on the SDIO bus when using the integrated internal oscillator. SDIO activity results from polling the tuner for status or communicating with other devices that share the SDIO bus. If there is SDIO bus activity while the Si4736/37/38/39 is performing the seek/tune function, the crystal oscillator may experience jitter, which may result in mistunes, false stops, and/or lower SNR.

For best seek/tune results, Silicon Laboratories recommends that all SDIO data traffic be suspended during Si4736/37/38/39 seek and tune operations. This is achieved by keeping the bus quiet for all other devices on the bus, and delaying tuner polling until the tune or seek operation is complete. The STC (seek/tune complete) interrupt should be used instead of polling to determine when a seek/tune operation is complete.

4.15. Control Interface

A serial port slave interface is provided, which allows an external controller to send commands to the Si4736/37/38/39 and receive responses from the device. The serial port can operate in three bus modes: 2-wire mode, 3-wire mode, or SPI mode. The Si4736/37/38/39 selects the bus mode by sampling the state of the GPO1 and GPO2 pins on the rising edge of $\overline{RST}$. The GPO1 pin includes an internal pull-up resistor, which is connected while $\overline{RST}$ is low, and the GPO2 pin includes an internal pull-down resistor, which is connected while $\overline{RST}$ is low. Therefore, it is only necessary for the user to actively drive pins which differ from these states. See Table 13.

Table 13. Bus Mode Select on Rising Edge of $\overline{RST}$

Bus Mode	GPO1	GPO2
2-Wire	1	0
SPI	1	1 (must drive)
3-Wire	0 (must drive)	0

After the rising edge of $\overline{RST}$, the pins GPO1 and GPO2 are used as general purpose output (O) pins, as described in Section "4.16. GPO Outputs". In any bus mode, commands may only be sent after V_{IO} and V_{DD} supplies are applied.

In any bus mode, before sending a command or reading a response, the user must first read the status byte to ensure that the device is ready (CTS bit is high).

4.15.1. 2-Wire Control Interface Mode

When selecting 2-wire mode, the user must ensure that SCLK is high during the rising edge of $\overline{RST}$, and stays high until after the first start condition. Also, a start condition must not occur within 300 ns before the rising edge of $\overline{RST}$.

The 2-wire bus mode uses only the SCLK and SDIO pins for signaling. A transaction begins with the START condition, which occurs when SDIO falls while SCLK is high. Next, the user drives an 8-bit control word serially

on SDIO, which is captured by the device on rising edges of SCLK. The control word consists of a 7-bit device address, followed by a read/write bit (read = 1, write = 0). The Si4736/37/38/39 acknowledges the control word by driving SDIO low on the next falling edge of SCLK.

Although the Si4736/37/38/39 will respond to only a single device address, this address can be changed with the SEN pin (note that the SEN pin is not used for signaling in 2-wire mode). When SEN = 0, the 7-bit device address is 0010001b. When SEN = 1, the address is 1100011b.

For write operations, the user then sends an 8-bit data byte on SDIO, which is captured by the device on rising edges of SCLK. The Si4736/37/38/39 acknowledges each data byte by driving SDIO low for one cycle, on the next falling edge of SCLK. The user may write up to 8 data bytes in a single 2-wire transaction. The first byte is a command, and the next seven bytes are arguments.

For read operations, after the Si4736/37/38/39 has acknowledged the control byte, it will drive an 8-bit data byte on SDIO, changing the state of SDIO on the falling edge of SCLK. The user acknowledges each data byte by driving SDIO low for one cycle, on the next falling edge of SCLK. If a data byte is not acknowledged, the transaction will end. The user may read up to 16 data bytes in a single 2-wire transaction. These bytes contain the response data from the Si4736/37/38/39.

A 2-wire transaction ends with the STOP condition, which occurs when SDIO rises while SCLK is high.

For details on timing specifications and diagrams, refer to Table 5, “2-Wire Control Interface Characteristics” on page 7; Figure 2, “2-Wire Control Interface Read and Write Timing Parameters,” on page 8, and Figure 3, “2-Wire Control Interface Read and Write Timing Diagram,” on page 8.

4.15.2. 3-Wire Control Interface Mode

When selecting 3-wire mode, the user must ensure that a rising edge of SCLK does not occur within 300 ns before the rising edge of RST.

The 3-wire bus mode uses the SCLK, SDIO, and SEN pins. A transaction begins when the user drives SEN low. Next, the user drives a 9-bit control word on SDIO, which is captured by the device on rising edges of SCLK. The control word consists of a 9-bit device address (A7:A5 = 101b), a read/write bit (read = 1, write = 0), and a 5-bit register address (A4:A0).

For write operations, the control word is followed by a 16-bit data word, which is captured by the device on rising edges of SCLK.

For read operations, the control word is followed by a delay of one-half SCLK cycle for bus turn-around. Next, the Si4736/37/38/39 will drive the 16-bit read data word serially on SDIO, changing the state of SDIO on each rising edge of SCLK.

A transaction ends when the user sets SEN high, then pulses SCLK high and low one final time. SCLK may either stop or continue to toggle while SEN is high.

In 3-wire mode, commands are sent by first writing each argument to register(s) 0xA1–0xA3, then writing the command word to register 0xA0. A response is retrieved by reading registers 0xA8–0xAF.

For details on timing specifications and diagrams, refer to Table 6, “3-Wire Control Interface Characteristics,” on page 9; Figure 4, “3-Wire Control Interface Write Timing Parameters,” on page 9, and Figure 5, “3-Wire Control Interface Read Timing Parameters,” on page 9.

4.15.3. SPI Control Interface Mode

When selecting SPI mode, the user must ensure that a rising edge of SCLK does not occur within 300 ns before the rising edge of RST.

SPI bus mode uses the SCLK, SDIO, and SEN pins for read/write operations. The system controller can choose to receive read data from the device on either SDIO or GPO1. A transaction begins when the system controller drives SEN = 0. The system controller then pulses SCLK eight times, while driving an 8-bit control byte serially on SDIO. The device captures the data on rising edges of SCLK. The control byte must have one of five values:

- 0x48 = write a command (controller drives 8 additional bytes on SDIO).
- 0x80 = read a response (device drives 1additional byte on SDIO).
- 0xC0 = read a response (device drives 16 additional bytes on SDIO).
- 0xA0 = read a response (device drives 1 additional byte on GPO1).
- 0xE0 = read a response (device drives 16 additional bytes on GPO1).

For write operations, the system controller must drive exactly 8 data bytes (a command and seven arguments) on SDIO after the control byte. The data is captured by the device on the rising edge of SCLK.

For read operations, the controller must read exactly 1 byte (STATUS) after the control byte or exactly 16 data bytes (STATUS and RESP1–RESP15) after the control byte. The device changes the state of SDIO (or GPO1, if specified) on the falling edge of SCLK. Data must be captured by the system controller on the rising edge of SCLK.

Keep SEN low until all bytes have transferred. A transaction may be aborted at any time by setting SEN

high and toggling SCLK high and then low. Commands will be ignored by the device if the transaction is aborted.

For details on timing specifications and diagrams, refer to Figure 6 and Figure 7 on page 10.

4.16. GPO Outputs

The Si4736/37/38/39 provides three general-purpose output pins. The GPO pins can be configured to output a constant low, constant high, or high-impedance. The GPO pins can be reconfigured as specialized functions. GPO2/INT can be configured to provide interrupts and GPO3 can be configured to provide external crystal support or as DCLK in digital audio output mode. In digital output mode (Si4737/39 only), pin 16 and pin 17 can be configured as DFS and DOUT, respectively.

4.17. Firmware Upgrades

The Si4736/37/38/39 contains on-chip program RAM to accommodate minor changes to the firmware. This allows Silicon Laboratories to provide future firmware updates to optimize the characteristics of new radio designs and those already deployed in the field.

4.18. Reset, Power Up, and Power Down

Setting the RST pin low will disable analog and digital circuitry, reset the registers to their default settings, and disable the bus. Setting the RST pin high will bring the device out of reset.

A power down mode is available to reduce power consumption when the part is idle. Putting the device in power down mode will disable analog and digital circuitry while keeping the bus active.

4.19. Programming with Commands

To ease development time and offer maximum customization, the Si4736/37/38/39 provides a simple yet powerful software interface to program the receiver. The device is programmed using commands, arguments, properties and responses.

To perform an action, the user writes a command byte and associated arguments causing the chip to execute the given command. Commands control an action such as power up the device, shut down the device, or tune to a station. Arguments are specific to a given command and are used to modify the command. A complete list of commands is available in Table 14, “Si473x Command Summary,” on page 25.

Properties are a special command argument used to modify the default chip operation and are generally configured immediately after power up. Examples of properties are de-emphasis level, RSSI seek threshold, and soft mute attenuation threshold. A complete list of properties is available in Table 15, “Si473x Property Summary,” on page 26.

Responses provide the user information and are echoed after a command and associated arguments are issued. All commands provide a one-byte status update indicating interrupt and clear-to-send status information. For a detailed description of the commands and properties for the Si4736/37/38/39, see “AN332: Universal Programming Guide.”

5. Commands and Properties

Table 14. Si473x Command Summary

Cmd	Name	Description
0x01	POWER_UP	Power up device and mode selection. Modes include AM or FM receive, analog or digital output, and reference clock or crystal support.
0x10	GET_REV	Returns revision information on the device.
0x11	POWER_DOWN	Power down device.
0x12	SET_PROPERTY	Sets the value of a property.
0x13	GET_PROPERTY	Retrieves a property's value.
0x14	GET_INT_STATUS	Read interrupt status bits.
0x15	PATCH_ARGS	Reserved command used for firmware file downloads.
0x16	PATCH_DATA	Reserved command used for firmware file downloads.
0x20	FM_TUNE_FREQ	Selects the FM tuning frequency.
0x21	FM_SEEK_START	Begins searching for a valid frequency.
0x22	FM_TUNE_STATUS	Queries the status of previous FM_TUNE_FREQ or FM_SEEK_START command.
0x23	FM_RSQ_STATUS	Queries the status of the Received Signal Quality (RSQ) of the current channel.
0x24	FM_RDS_STATUS	Returns RDS information for current channel and reads an entry from the RDS FIFO (Si4737/39 only).
0x40	AM_TUNE_FREQ	Tunes to a given AM frequency.
0x41	AM_SEEK_START	Begins searching for a valid frequency.
0x42	AM_TUNE_STATUS	Queries the status of the already issued AM_TUNE_FREQ or AM_-SEEK_START command.
0x43	AM_RSQ_STATUS	Queries the status of the RSQ for the current channel.
0x50	WB_TUNE_FREQ	Selects the WB tuning frequency.
0x52	WB_TUNE_STATUS	Queries the status of the previous WB_TUNE_FREQ command.
0x53	WB_RSQ_STATUS	Queries the status of the Received Signal Quality (RSQ) of the current channel.
0x55	WB_ASQ_STATUS	Queries the status of the 1050 Hz alert tone.
0x57	WB_AGC_STATUS	Queries the status of the AGC.
0x58	WB_AGC_OVERRIDE	Enable or disable the WB AGC.
0x80	GPO_CTL	Configures GPO3 as output or Hi-Z.
0x81	GPO_SET	Sets GPO3 output level (low or high).

Table 15. Si473x Property Summary

Prop	Name	Description	Default
0x0001	GPO_IEN	Enables interrupt sources.	0x0000
0x0102	DIGITAL_OUTPUT_FORMAT	Configures the digital output format (Si4737/39 only).	0x0000
0x0104	DIGITAL_OUTPUT_ SAMPLE_RATE	Configures the digital output sample rate in 100 Hz steps. The digital output sample rate is disabled by default (Si4737/39 only).	0x0000
0x0201	REFCLK_FREQ	Sets frequency of reference clock in Hz. The range is 31130 to 34406 Hz, or 0 to disable the AFC. Default is 32768 Hz.	0x8000
0x0202	REFCLK_PRESCALE	Sets the prescaler value for RCLK input.	0x0001
0x1100	FM_DEEMPHASIS	Sets de-emphasis time constant. Default is 75 us.	0x0002
0x1105	FM_BLEND_STEREO_ THRESHOLD	Sets RSSI threshold for stereo blend (Full stereo above threshold, blend below threshold). To force stereo set this to 0. To force mono set this to 127. Default value is 49 dBuV.	0x0031
0x1106	FM_BLEND_MONO_ THRESHOLD	Sets RSSI threshold for mono blend (full mono below threshold, blend above threshold). To force stereo set this to 0. To force mono set this to 127. Default value is 30 dBuV.	0x001E
0x1108	FM_MAX_TUNE_ ERROR	Sets the maximum freq error allowed before setting the AFC rail (AFCRL) indicator. Default value is 30 kHz.	0x001E
0x1200	FM_RSQ_INT_ SOURCE	Configures interrupt related to RSQ metrics.	0x0000
0x1201	FM_RSQ_SNR_HI_ THRESHOLD	Sets high threshold for SNR interrupt.	0x007F
0x1202	FM_RSQ_SNR_LO_ THRESHOLD	Sets low threshold for SNR interrupt.	0x0000
0x1203	FM_RSQ_RSSI_HI_ THRESHOLD	Sets high threshold for RSSI interrupt.	0x007F
0x1204	FM_RSQ_RSSI_LO_ THRESHOLD	Sets low threshold for RSSI interrupt.	0x0000
0x1207	FM_RSQ_BLEND_ THRESHOLD	Sets the blend threshold for blend interrupt when boundary is crossed.	0x0081
0x1300	FM_SOFT_MUTE_RATE	Sets the attack and decay rates when entering and leaving soft mute.	0x0040
0x1302	FM_SOFT_MUTE_ MAX_ATTENUATION	Sets maximum attenuation during soft mute (dB). Set to 0 to disable soft mute. Default is 16 dB.	0x0010
0x1303	FM_SOFT_MUTE_ SNR_THRESHOLD	Sets SNR threshold to engage soft mute. Default is 4 dB.	0x0004
0x1400	FM_SEEK_BAND_ BOTTOM	Sets the bottom of the FM band for seek. Default is 8750.	0x222E
0x1401	FM_SEEK_BAND_TOP	Sets the top of the FM band for seek. Default is 10790.	0x2A26
0x1402	FM_SEEK_FREQ_ SPACING	Selects frequency spacing for FM seek.	0x000A
0x1403	FM_SEEK_TUNE_ SNR_THRESHOLD	Sets the SNR threshold for a valid FM Seek/Tune. Default value is 3 dB.	0x0003
0x1404	FM_SEEK_TUNE_ RSSI_TRESHOLD	Sets the RSSI threshold for a valid FM Seek/Tune. Default value is 20 dBuV.	0x0014

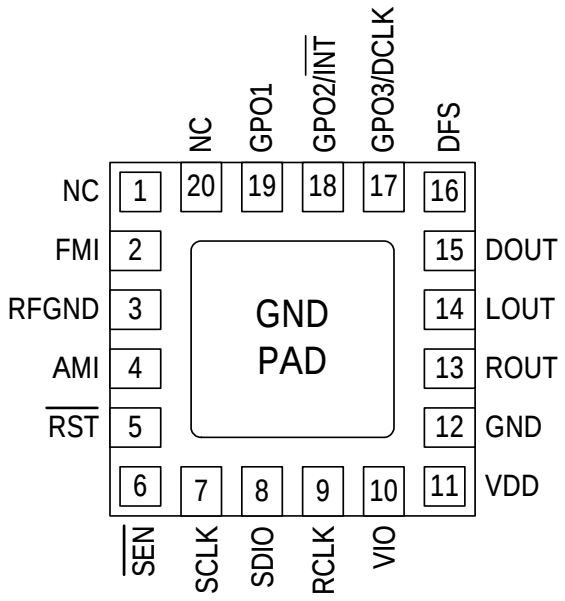
Table 15. Si473x Property Summary (Continued)

Prop	Name	Description	Default
0x1500	RDS_INT_SOURCE	Configures RDS interrupt behavior.	0x0000
0x1501	RDS_INT_FIFO_COUNT	Sets the minimum number of RDS groups stored in the receive RDS FIFO required before RDS RECV is set.	0x0000
0x1502	RDS_CONFIG	Configures RDS setting.	0x0000
0x3100	AM_DEEMPHASIS	Sets de-emphasis time constant. Can be set to 50 us. De-emphasis is disabled by default.	0x0000
0x3102	AM_CHANNEL_FILTER	Selects the bandwidth of the channel filter for AM reception. The choices are 6, 4, 3, or 2 (kHz). The default bandwidth is 2 kHz.	0x0003
0x3200	AM_RSQ_INTERRUPTS	Configures interrupt related to RSQ metrics. All interrupts are disabled by default.	0x0000
0x3201	AM_RSQ_SNR_HIGH_THRESHOLD	Sets high threshold for SNR interrupt. The default is 0 dB.	0x0000
0x3202	AM_RSQ_SNR_LOW_THRESHOLD	Sets low threshold for SNR interrupt. The default is 0 dB.	0x0000
0x3203	AM_RSQ_RSSI_HIGH_THRESHOLD	Sets high threshold for RSSI interrupt. The default is 0 dB.	0x0000
0x3204	AM_RSQ_RSSI_LOW_THRESHOLD	Sets low threshold for RSSI interrupt. The default is 0 dB.	0x0000
0x3300	AM_SOFT_MUTE_RATE	Sets the rate of attack when entering or leaving soft mute. The default is 278 dB/s.	0x0040
0x3301	AM_SOFT_MUTE_SLOPE	Sets the AM soft mute slope. The bigger the number, the higher the max attenuation level. Default value is a slope of 2.	0x0002
0x3302	AM_SOFT_MUTE_MAX_ATTENUATION	Sets maximum attenuation during soft mute (dB). Set to 0 to disable soft mute. Default is 16 dB.	0x0010
0x3303	AM_SOFT_MUTE_SNR_THRESHOLD	Sets SNR threshold to engage soft mute. Default is 10 dB.	0x000A
0x3400	AM_SEEK_BAND_BOTTOM	Sets the bottom of the AM band for seek. Default is 520.	0x0208
0x3401	AM_SEEK_BAND_TOP	Sets the top of the AM band for seek. Firmware 1.0 incorrectly defaults to 1721 kHz instead of 1710.	0x06AE
0x3402	AM_SEEK_FREQ_SPACING	Selects frequency spacing for AM seek. Default is 10 kHz spacing.	0x000A
0x3403	AM_SEEK_SNR_THRESHOLD	Sets the SNR threshold for a valid AM Seek/Tune. If the value is zero then SNR threshold is not considered when doing a seek. Default value is 5 dB.	0x0005
0x3404	AM_SEEK_RSSI_THRESHOLD	Sets the RSSI threshold for a valid AM Seek/Tune. If the value is zero then RSSI threshold is not considered when doing a seek. Default value is 25 dBuV.	0x0019
0x4000	RX_VOLUME	Sets the output volume.	0x003F
0x4001	RX_HARD_MUTE	Mutes the audio output. L and R audio outputs may be muted independently in FM mode.	0x0000
0x5108	WB_MAX_TUNE_ERROR	Maximum change in frequencies from the WB_TUNE_FREQ to which the AFC will lock.	0x000F

Table 15. Si473x Property Summary (Continued)

Prop	Name	Description	Default
0x5200	WB_RSQ_INTERRUPT_SOURCE	Configures interrupts related to RSQ metrics. All interrupts are disabled by default.	0x0000
0x5201	WB_RSQ_SNR_HIGH_THRESHOLD	Sets high threshold for SNR interrupt. The default is 0 dB.	0x007F
0x5202	WB_RSQ_SNR_LOW_THRESHOLD	Sets low threshold for SNR interrupt. The default is 0 dB.	0x0000
0x5203	WB_RSQ_RSSI_HIGH_THRESHOLD	Sets high threshold for RSSI interrupt. The default is 0 dB.	0x007F
0x5204	WB_RSQ_RSSI_LOW_THRESHOLD	Sets low threshold for RSSI interrupt. The default is 0 dB.	0x0000
0x5600	WB_ASQ_INTERRUPT_SOURCE	Configures 1050 Hz alert tone interrupts. All interrupts are disabled by default.	0x0000

6. Pin Descriptions: Si4736/37/38/39-GM



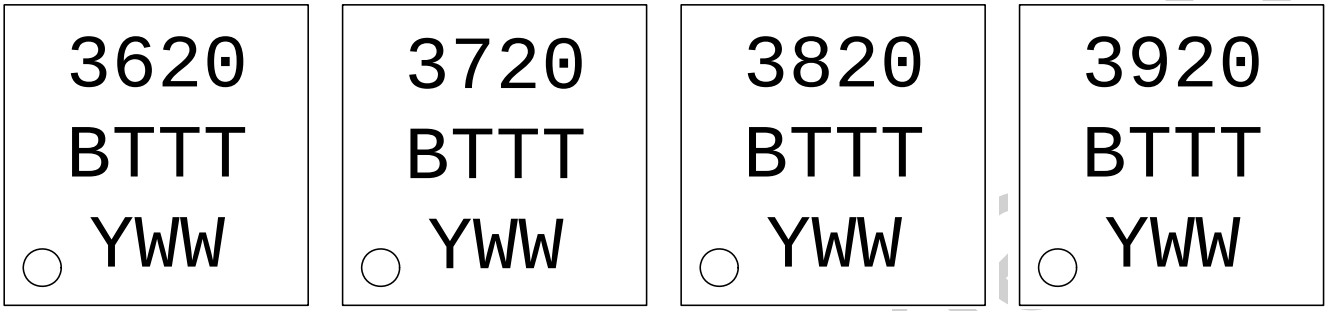
Pin Number(s)	Name	Description
1, 20	NC	No connect. Leave floating.
2	FMI	FM/WB RF inputs. FMI should be connected to the antenna trace.
3	RFGND	RF ground. Connect to ground plane on PCB.
4	AMI	AM RF input. AMI should be connected to the AM antenna.
5	$\overline{\text{RST}}$	Device reset (active low) input.
6	$\overline{\text{SEN}}$	Serial enable input (active low).
7	SCLK	Serial clock input.
8	SDIO	Serial data input/output.
9	RCLK	External reference oscillator input.
10	V_{IO}	I/O supply voltage.
11	V_{DD}	Supply voltage. May be connected directly to battery.
12, GND PAD	GND	Ground. Connect to ground plane on PCB.
13	ROUT	Right audio line output in analog output mode.
14	LOUT	Left audio line output in analog output mode.
15	DOUT	Digital output data in digital output mode.
16	DFS	Digital frame synchronization input in digital output mode.
17	GPO3/DCLK	General purpose output, crystal oscillator, or digital bit synchronous clock input in digital output mode.
18	GPO2/$\overline{\text{INT}}$	General purpose output or interrupt pin.
19	GPO1	General purpose output.

7. Ordering Guide

Part Number*	Description	Package Type	Operating Temperature
Si4736-B20-GM	AM/FM/WB Broadcast Radio Receiver	QFN Pb-free	–20 to 85 °C
Si4737-B20-GM	AM/FM/WB Broadcast Radio Receiver with RDS/RBDS	QFN Pb-free	–20 to 85 °C
Si4738-B20-GM	FM/WB Broadcast Radio Receiver	QFN Pb-free	–20 to 85 °C
Si4739-B20-GM	FM/WB Broadcast Radio Receiver with RDS/RBDS	QFN Pb-free	–20 to 85 °C
***Note:** Add an “(R)” at the end of the device part number to denote tape and reel option; 2500 quantity per reel.			

8. Package Markings (Top Marks)

8.1. Top Mark



8.2. Top Mark Explanation

Mark Method:	YAG Laser	
Line 1 Marking:	Part Number	36 = Si4736, 37 = Si4737, 38 = Si4738, 39 = Si4739
	Firmware Revision	20 = Firmware Revision 2.0
Line 2 Marking:	Die Revision	B = Revision B Die
	TTT = Internal Code	Internal tracking code
Line 3 Marking:	Circle = 0.5 mm Diameter (Bottom-Left Justified)	Pin 1 Identifier
	Y = Year WW = Workweek	Assigned by the Assembly House. Corresponds to the last significant digit of the year and workweek of the mold date.

9. Package Outline: Si4736/37/38/39 QFN

Figure 14 illustrates the package details for the Si4736/37/38/39. Table 16 lists the values for the dimensions shown in the illustration.

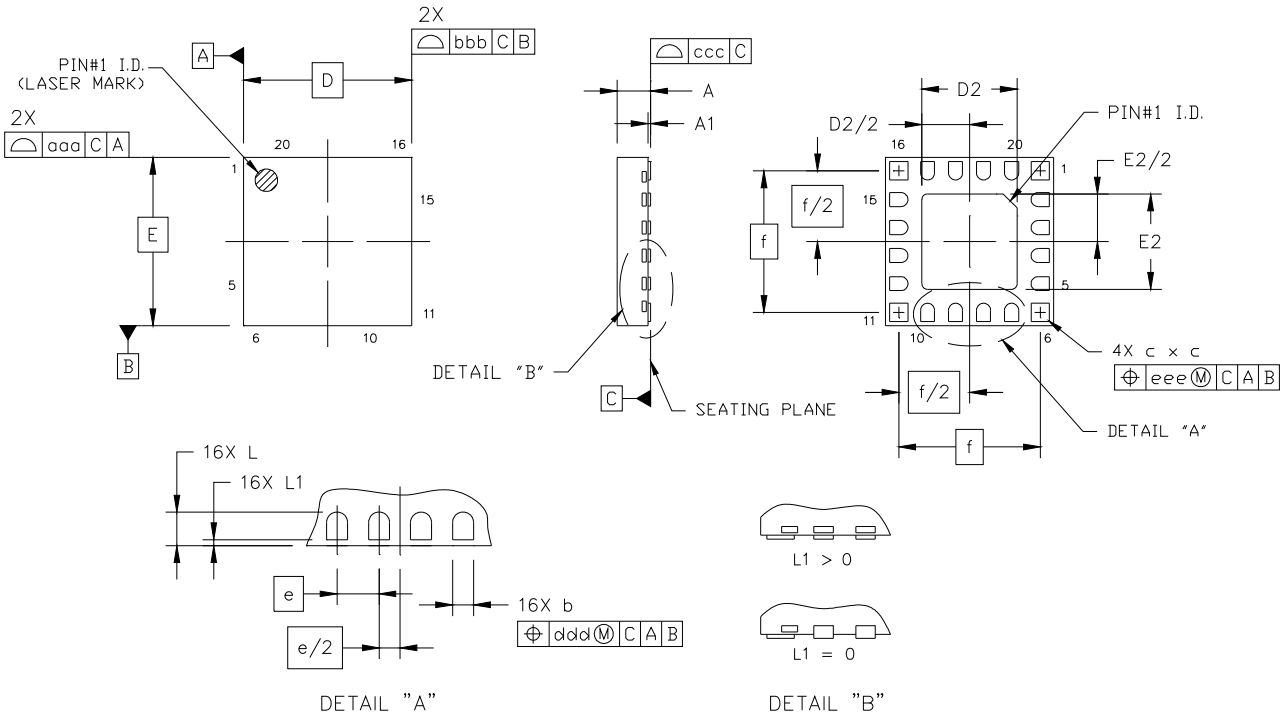


Figure 14. 20-Pin Quad Flat No-Lead (QFN)

Table 16. Package Dimensions

Symbol	Millimeters		
	Min	Nom	Max
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
b	0.20	0.25	0.30
c	0.27	0.32	0.37
D		3.00 BSC	
D2	1.65	1.70	1.75
e		0.50 BSC	
E		3.00 BSC	
E2	1.65	1.70	1.75

Symbol	Millimeters		
	Min	Nom	Max
f		2.53 BSC	
L	0.35	0.40	0.45
L1	0.00	—	0.10
aaa	—	—	0.05
bbb	—	—	0.05
ccc	—	—	0.08
ddd	—	—	0.10
eee	—	—	0.10

Notes:

1. All dimensions are shown in millimeters (mm) unless otherwise noted.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.

10. PCB Land Pattern: Si4736/37/38/39 QFN

Figure 15 illustrates the PCB land pattern details for the Si4736/37/38/39-GM. Table 17 lists the values for the dimensions shown in the illustration.

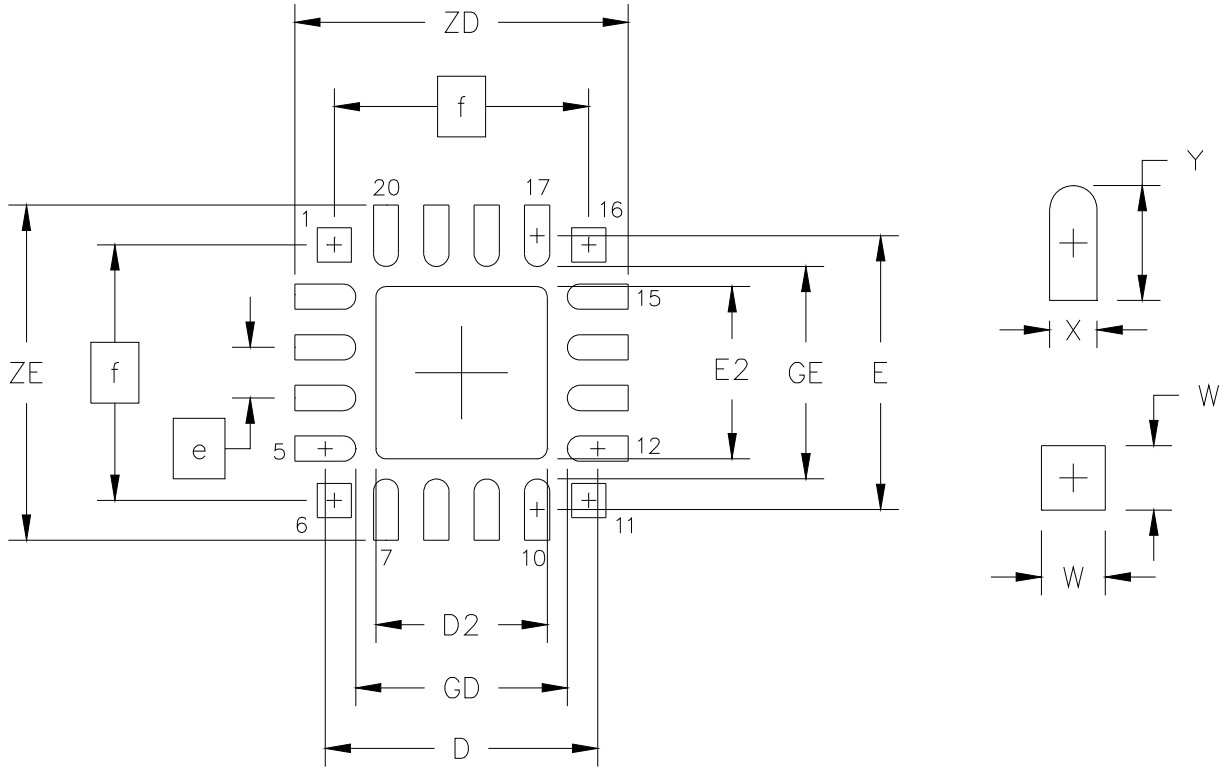


Figure 15. PCB Land Pattern

Table 17. PCB Land Pattern Dimensions

Symbol	Millimeters	
	Min	Max
D	2.71 REF	
D2	1.60	1.80
e	0.50 BSC	
E	2.71 REF	
E2	1.60	1.80
f	2.53 BSC	
GD	2.10	—

Symbol	Millimeters	
	Min	Max
GE	2.10	—
W	—	0.34
X	—	0.28
Y	0.61 REF	
ZE	—	3.31
ZD	—	3.31

Notes: General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on IPC-SM-782 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Notes: Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Notes: Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads.
4. A 1.45 x 1.45 mm square aperture should be used for the center pad. This provides approximately 70% solder paste coverage on the pad, which is optimum to assure correct component stand-off.

Notes: Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

11. Additional Reference Resources

- EN55020 Compliance Test Certificate
- AN231: Si4700/01 Headphone and Antenna Interface
- AN332: Universal Programming Guide
- AN383: Universal Antenna Selection and Layout Guidelines
- AN386: Si473x Ferrite Loop Stick Antenna Interface
- AN388: Si473x AM/FM Tuner Evaluation Board Test Procedure
- AN389: Si473x EVB Quick-Start Guide
- Si47xx Customer Support Site: http://www.mysilabs.com
  This site contains all application notes, evaluation board schematics and layouts, and evaluation software. NDA is required for access. To request access, register at http://www.mysilabs.com and send user's first and last name, company, NDA reference number, and mysilabs user name to fminfo@silabs.com. Silicon Labs recommends an all lower case user name.

Document Change List

Revision 0.4 to Revision 0.5

- Updated Table 3, “DC Characteristics,” on page 5.
- Updated Table 5, “2-Wire Control Interface Characteristics[1,2,3],” on page 7.
- Updated Table 8, “Digital Audio Interface Characteristics,” on page 11.
- Updated Table 9, “FM Receiver Characteristics[1,2],” on page 12.
- Updated Table 10, “WB Receiver Characteristics[1],” on page 13.
- Updated Table 11, “AM Receiver Characteristics[1],” on page 14.
- Updated Table 12, “Reference Clock and Crystal Characteristics,” on page 15.
- Updated "3. Bill of Materials" on page 17.
- Added GPO_CTL and GPO_SET commands to Table 13, “Bus Mode Select on Rising Edge of RST,” on page 22.
- Updated "11. Additional Reference Resources" on page 35..

NOTES:

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