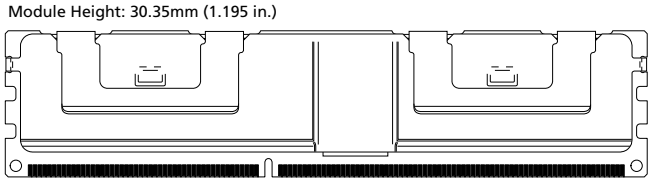
DDR3 SDRAM LRDIMM

MT72JSZS4G72LZ – 32GB

Features

- 240-pin, load-reduced dual in-line memory module (LRDIMM)
- Memory buffer (MB) isolates DRAM interface from card edge
- Single-load for all data, command, control, address, and clock signals
- Rank multiplication providing access to 4 physical ranks
- Fast data transfer rates: PC3-14900
- 32GB (4 Gig x 72)
- V_{DD} = 1.5V ±0.075V
- V_{DDSPD} = 3.0V–3.6V
- Supports ECC error detection and correction
- Nominal and dynamic on-die termination (ODT) for data and strobe signals
- Quad-rank, using 8Gb TwinDie™ devices
- 8 internal device banks
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the mode register set (MRS)
- Two on-board temperature sensors
- Gold edge contacts
- Full module heat spreader
- Halogen-free
- Terminated control, command, and address bus

Figure 1: 240-Pin LRDIMM (MO-269 RC/C)



Options	Marking
• Operating temperature	
– Commercial (0°C ≤ T_C ≤ +95°C)	None
• Package	
– 240-pin DIMM (halogen-free)	Z
• Frequency/CAS latency	
– 1.07ns @ CL = 13 (DDR3-1866)	-1G9

Table 1: Key Timing Parameters

Speed Grade	Industry Nomenclature	Data Rate (MT/s)								^tRCD (ns)	^tRP (ns)	^tRC (ns)
		CL = 13	CL = 11	CL = 10	CL = 9	CL = 8	CL = 7	CL = 6	CL = 5			
-1G9	PC3-14900	1866	1600	1333	1333	1066	1066	800	667	13.125	13.125	47.125
-1G6	PC3-12800	–	1600	1333	1333	1066	1066	800	667	13.125	13.125	48.125
-1G4	PC3-10600	–	–	1333	1333	1066	1066	800	667	13.125	13.125	49.125
-1G1	PC3-8500	–	–	–	–	1066	1066	800	667	13.125	13.125	50.625
-1G0	PC3-8500	–	–	–	–	1066	–	800	667	15	15	52.5
-80B	PC3-6400	–	–	–	–	–	–	800	667	15	15	52.5

Table 2: Addressing

Parameter	32GB
Refresh count	8K
Row address	64K A[15:0]
Device bank address	8 BA[2:0]
Device configuration	8Gb TwinDie (2 Gig x 4)
Column address	2K A[11, 9:0]
Module rank address	4 S#[3:0]

Table 3: Part Numbers and Timing Parameters – 32GB Modules

Base device: MT41J2G4[1], 8Gb TwinDie DDR3 SDRAM

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL-^{t}RCD-^{t}RP)
MT72JSZS4G72LZ-1G9__	32GB	4 Gig x 72	14.9 GB/s	1.07ns/1866 MT/s	13-13-13

Notes:
1. The data sheet for the base device can be found on Micron's Web site.
2. All LRDIMM part numbers end with a two-place code (not shown) that designates component and PCB revisions, and a two-place code (also not shown) that indicates buffer vendor and revision. Consult factory for current revision codes. Example: MT72JSZS4G72LZ-1G9N1A7.

Pin Assignments

Table 4: Pin Assignments

240-Pin DDR3 LRDIMM Front								240-Pin DDR3 LRDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{REFDQ}	31	DQ25	61	A2	91	DQ41	121	V_{SS}	151	V_{SS}	181	A1	211	V_{SS}
2	V_{SS}	32	V_{SS}	62	V_{DD}	92	V_{SS}	122	DQ4	152	DQS12	182	V_{DD}	212	DQS14
3	DQ0	33	DQS3#	63	NF	93	DQS5#	123	DQ5	153	DQS12#	183	V_{DD}	213	DQS14#
4	DQ1	34	DQS3	64	NF	94	DQS5	124	V_{SS}	154	V_{SS}	184	CK0	214	V_{SS}
5	V_{SS}	35	V_{SS}	65	V_{DD}	95	V_{SS}	125	DQS9	155	DQ30	185	CK0#	215	DQ46
6	DQS0#	36	DQ26	66	V_{DD}	96	DQ42	126	DQS9#	156	DQ31	186	V_{DD}	216	DQ47
7	DQS0	37	DQ27	67	V_{REFCA}	97	DQ43	127	V_{SS}	157	V_{SS}	187	EVENT#	217	V_{SS}
8	V_{SS}	38	V_{SS}	68	Par_In	98	V_{SS}	128	DQ6	158	CB4	188	A0	218	DQ52
9	DQ2	39	CB0	69	V_{DD}	99	DQ48	129	DQ7	159	CB5	189	V_{DD}	219	DQ53
10	DQ3	40	CB1	70	A10/AP	100	DQ49	130	V_{SS}	160	V_{SS}	190	BA1	220	V_{SS}
11	V_{SS}	41	V_{SS}	71	BA0	101	V_{SS}	131	DQ12	161	DQS17	191	V_{DD}	221	DQS15
12	DQ8	42	DQS8#	72	V_{DD}	102	DQS6#	132	DQ13	162	DQS17#	192	RAS#	222	DQS15#
13	DQ9	43	DQS8	73	WE#	103	DQS6	133	V_{SS}	163	V_{SS}	193	S0#	223	V_{SS}
14	V_{SS}	44	V_{SS}	74	CAS#	104	V_{SS}	134	DQS10	164	CB6	194	V_{DD}	224	DQ54
15	DQS1#	45	CB2	75	V_{DD}	105	DQ50	135	DQS10#	165	CB7	195	ODT0	225	DQ55
16	DQS1	46	CB3	76	S1#	106	DQ51	136	V_{SS}	166	V_{SS}	196	A13	226	V_{SS}
17	V_{SS}	47	V_{SS}	77	ODT1	107	V_{SS}	137	DQ14	167	NF	197	V_{DD}	227	DQ60
18	DQ10	48	V_{TT}	78	V_{DD}	108	DQ56	138	DQ15	168	RESET#	198	S3#	228	DQ61
19	DQ11	49	V_{TT}	79	S2#	109	DQ57	139	V_{SS}	169	CKE1	199	V_{SS}	229	V_{SS}
20	V_{SS}	50	CKE0	80	V_{SS}	110	V_{SS}	140	DQ20	170	V_{DD}	200	DQ36	230	DQS16
21	DQ16	51	V_{DD}	81	DQ32	111	DQS7#	141	DQ21	171	A15	201	DQ37	231	DQS16#
22	DQ17	52	BA2	82	DQ33	112	DQS7	142	V_{SS}	172	A14	202	V_{SS}	232	V_{SS}
23	V_{SS}	53	Err_Out#	83	V_{SS}	113	V_{SS}	143	DQS11	173	V_{DD}	203	DQS13	233	DQ62
24	DQS2#	54	V_{DD}	84	DQS4#	114	DQ58	144	DQS11#	174	A12	204	DQS13#	234	DQ63
25	DQS2	55	A11	85	DQS4	115	DQ59	145	V_{SS}	175	A9	205	V_{SS}	235	V_{SS}
26	V_{SS}	56	A7	86	V_{SS}	116	V_{SS}	146	DQ22	176	V_{DD}	206	DQ38	236	V_{DDSPD}
27	DQ18	57	V_{DD}	87	DQ34	117	SA0	147	DQ23	177	A8	207	DQ39	237	SA1
28	DQ19	58	A5	88	DQ35	118	SCL	148	V_{SS}	178	A6	208	V_{SS}	238	SDA
29	V_{SS}	59	A4	89	V_{SS}	119	SA2	149	DQ28	179	V_{DD}	209	DQ44	239	V_{SS}
30	DQ24	60	V_{DD}	90	DQ40	120	V_{TT}	150	DQ29	180	A3	210	DQ45	240	V_{TT}

Pin Descriptions

The pin description table below is a comprehensive list of all possible pins for all DDR3 modules. All pins listed may not be supported on this module. See Pin Assignments for information specific to this module.

Table 5: Pin Descriptions

Symbol	Type	Description
Ax	Input	**Address inputs:** Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BAx) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. See the Pin Assignments Table for density-specific addressing information.
BAx	Input	**Bank address inputs:** Define the device bank to which an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA define which mode register (MR0, MR1, MR2, or MR3) is loaded during the LOAD MODE command.
CKx, CKx#	Input	**Clock:** Differential clock inputs. All control, command, and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#.
CKEx	Input	**Clock enable:** Enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM.
DMx	Input	**Data mask (x8 devices only):** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with that input data, during a write access. Although DM pins are input-only, DM loading is designed to match that of the DQ and DQS pins.
ODTx	Input	**On-die termination:** Enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to the following pins: DQ, DQS, DQS#, DM, and CB. The ODT input will be ignored if disabled via the LOAD MODE command.
Par_In	Input	**Parity input:** Parity bit for Ax, RAS#, CAS#, and WE#.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with S#) define the command being entered.
RESET#	Input (LVCMOS)	**Reset:** RESET# is an active LOW asychronous input that is connected to each DRAM and the registering clock driver. After RESET# goes HIGH, the DRAM must be reinitialized as though a normal power-up was executed.
Sx#	Input	**Chip select:** Enables (registered LOW) and disables (registered HIGH) the command decoder.
SAx	Input	**Serial address inputs:** Used to configure the temperature sensor/SPD EEPROM address range on the I^2C bus.
SCL	Input	**Serial clock for temperature sensor/SPD EEPROM:** Used to synchronize communication to and from the temperature sensor/SPD EEPROM on the I^2C bus.
CBx	I/O	**Check bits:** Used for system error detection and correction.
DQx	I/O	**Data input/output:** Bidirectional data bus.
DQSx, DQSx#	I/O	**Data strobe:** Differential data strobes. Output with read data; edge-aligned with read data; input with write data; center-aligned with write data.

Table 5: Pin Descriptions (Continued)

Symbol	Type	Description
SDA	I/O	**Serial data:** Used to transfer addresses and data into and out of the temperature sensor/SPD EEPROM on the I^2C bus.
TDQSx, TDQSx#	Output	**Redundant data strobe (x8 devices only):** TDQS is enabled/disabled via the LOAD MODE command to the extended mode register (EMR). When TDQS is enabled, DM is disabled and TDQS and TDQS# provide termination resistance; otherwise, TDQS# are no function.
Err_Out#	Output (open drain)	**Parity error output:** Parity error found on the command and address bus.
EVENT#	Output (open drain)	**Temperature event:** The EVENT# pin is asserted by the temperature sensor when critical temperature thresholds have been exceeded.
V_{DD}	Supply	**Power supply:** 1.5V ±0.075V. The component V_{DD} and V_{DDQ} are connected to the module V_{DD}.
V_{DDSPD}	Supply	**Temperature sensor/SPD EEPROM power supply:** 3.0–3.6V.
V_{REFCA}	Supply	**Reference voltage:** Control, command, and address $V_{DD}/2$.
V_{REFDQ}	Supply	**Reference voltage:** DQ, DM $V_{DD}/2$.
V_{SS}	Supply	Ground.
V_{TT}	Supply	**Termination voltage:** Used for control, command, and address $V_{DD}/2$.
NC	–	**No connect:** These pins are not connected on the module.
NF	–	**No function:** These pins are connected within the module, but provide no functionality.

DQ Map

Table 6: Component-to-Module DQ Map, Front

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U1	0	19	28	U2	0	22	146
	1	18	27		1	20	140
	2	17	22		2	23	147
	3	16	21		3	21	141
U3	0	CB4	158	U4	0	10	18
	1	CB5	159		1	9	13
	2	CB6	164		2	8	12
	3	CB7	165		3	11	19
U5	0	13	132	U7	0	52	218
	1	14	137		1	53	219
	2	12	131		2	55	225
	3	15	138		3	54	224
U8	0	51	106	U9	0	44	209
	1	50	105		1	46	215
	2	48	99		2	45	210
	3	49	100		3	47	216
U10	0	43	97	U11	0	25	31
	1	42	96		1	27	37
	2	40	90		2	26	36
	3	41	91		3	24	30
U12	0	28	149	U13	0	CB0	39
	1	31	156		1	CB1	40
	2	29	150		2	CB2	45
	3	30	155		3	CB3	46
U14	0	2	9	U15	0	5	123
	1	0	3		1	7	129
	2	3	10		2	6	128
	3	1	4		3	4	122
U16	0	60	227	U17	0	56	108
	1	62	233		1	57	109
	2	61	228		2	58	114
	3	63	234		3	59	115

Table 6: Component-to-Module DQ Map, Front (Continued)

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U18	0	38	206	U19	0	33	82
	1	37	201		1	34	87
	2	36	200		2	32	81
	3	39	207		3	35	88

Table 7: Component-to-Module DQ Map, Back

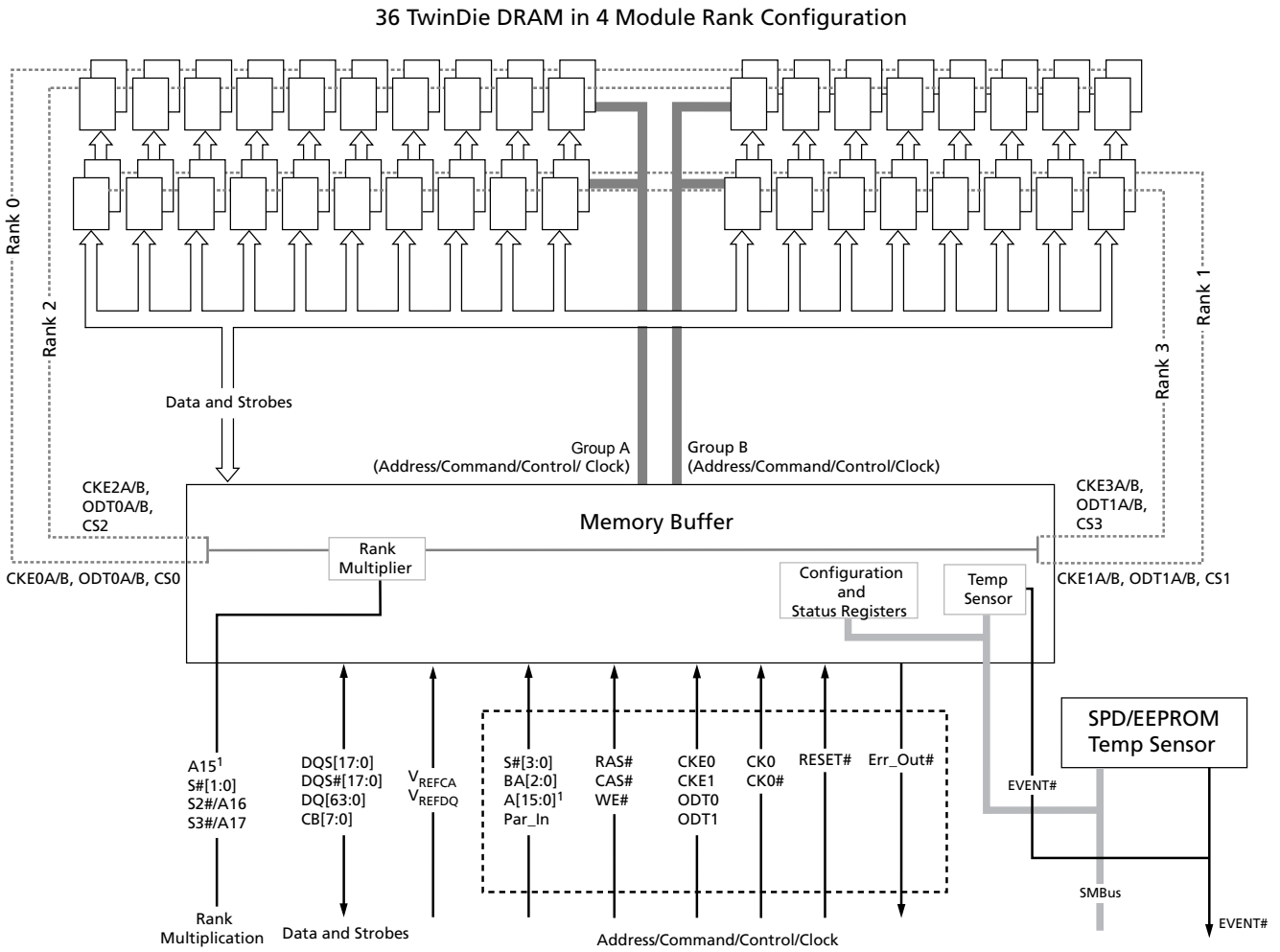
Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U20	0	42	96	U21	0	46	215
	1	40	90		1	45	210
	2	41	91		2	47	216
	3	43	97		3	44	209
U22	0	50	105	U23	0	53	219
	1	48	99		1	55	225
	2	49	100		2	54	224
	3	51	106		3	52	218
U25	0	14	137	U26	0	9	13
	1	12	131		1	8	12
	2	15	138		2	11	19
	3	13	132		3	10	18
U27	0	CB5	159	U28	0	20	140
	1	CB6	164		1	23	147
	2	CB7	165		2	21	141
	3	CB4	158		3	22	146
U29	0	18	27	U30	0	34	87
	1	17	22		1	32	81
	2	16	21		2	35	88
	3	19	28		3	33	82
U31	0	37	201	U32	0	57	109
	1	36	200		1	58	114
	2	39	207		2	59	115
	3	38	206		3	56	108

Table 7: Component-to-Module DQ Map, Back (Continued)

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U33	0	62	233	U34	0	7	129
	1	61	228		1	6	128
	2	63	234		2	4	122
	3	60	227		3	5	123
U35	0	0	3	U36	0	CB1	40
	1	3	10		1	CB2	45
	2	1	4		2	CB3	46
	3	2	9		3	CB0	39
U37	0	31	156	U38	0	27	37
	1	29	150		1	26	36
	2	30	155		2	24	30
	3	28	149		3	25	31

Functional Block Diagram

Figure 2: Functional Block Diagram



Notes:
1. The ZQ ball on each DDR3 die is connected to a separate external 240Ω ±1% resistor that is tied to V_{SS}. This supports ZQ calibration to the entire device with one command set. It is used for the calibration of the component's ODT and output driver.
2. A15 used for rank multiplication for 16GB module and for DRAM addressing for 32GB module.

General Description

The LRDIMM uses the same interface as the standard DDR3 RDIMM, but reduces the channel loading by buffering all signals that go to the DRAM. Like a standard RDIMM, the command, control, address, and clocks are redriven by the memory buffer and have similar characteristics to single-registered RDIMM. Additionally, the LRDIMM buffers all data and strobes through the memory buffer. This reduces the channel loading, as there is only a single load per signal, per module, for all DQ and DQS nodes.

The LRDIMM is a high-speed, CMOS dynamic random access memory module that uses internally configured 8-bank DDR3 SDRAM devices. DDR3 architecture is an 8*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR3 SDRAM module consists of a single 8*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and eight corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

For improved signal quality, the clock, control, command, and address buses have been routed in a fly-by topology, where each clock, control, command, and address pin on each DRAM is connected to a single trace and terminated (rather than a tree structure, where the termination is off the module near the connector). Inherent to fly-by topology, the timing skew between the clock and DQS signals can be easily accounted for by using the write-leveling feature of DDR3.

LRDIMMs use two sets of differential signals: DQS/DQS# to capture data and CK/CK# to capture commands, addresses, and control signals. Differential clocks and data strobes ensure exceptional noise immunity for these signals and provide precise crossing points to capture input signals.

The LRDIMM includes two temperature sensors:

- A temperature sensor located within the memory buffer monitors the temperature of that high-current device on the PCB.
- A temperature sensor integrated with the serial presence-detect (SPD) EEPROM monitors the temperature of the module PCB directly through a heat paddle under the EEPROM.

The DRAM temperature is related to these two indicators by a combination of heat spreader performance, ambient temperature, and air flow.

Memory Buffer Operation

LRDIMMs provide increased performance by presenting a single memory buffer to the system, rather than multiple DRAM. Additionally, increased capacity is achieved due to the well-defined topology and load that is achieved on the module because the memory buffer drives only the SDRAM.

Four chip selects are possible at the edge connector; however, the memory buffer provides an address multiplication feature to increase the number of ranks accessible to the system. The memory buffer uses one or two of the upper chip selects not directly usable by the SDRAM to generate additional chip selects. This feature is configurable within the memory buffer.

Control and Status Registers

The memory buffer contains control and status registers. All control and status registers are accessible through the SMBus, as well as through in-band channel commands. The

registers can be read by software from the SMBus host any time the memory buffer is powered, except when the memory buffer is in clock-stopped power-down mode, or when the device RESET# pin is asserted.

Temperature Sensor

The memory buffer contains a class-C temperature sensor that can be configured to assert the EVENT# pin when temperature thresholds are exceeded. The temperature sensor is accessible through the SMBus.

Parity Operations

The memory buffer can accept a parity bit from the system's memory controller, providing even parity for the control, command, and address bus. Parity is calculated from all command and address signals (CKE, ODT, and S# are not included in parity). The last bit of the sum is compared to the parity signal provided by the system at the Par_In pin. Parity errors are flagged on the Err_Out# pin. Parity is also checked during control-word programming.

Serial Presence-Detect EEPROM with Temperature Sensor

Serial Presence-Detect EEPROM Operation

DDR3 SDRAM modules incorporate serial presence-detect. The SPD data is stored in a 256-byte EEPROM. The first 128 bytes are programmed by Micron to comply with JEDEC standard JC-45, "Appendix X: Serial Presence Detect (SPD) for DDR3 SDRAM Modules." These bytes identify module-specific timing parameters, configuration information, and physical attributes. User-specific information can be written into the remaining 128 bytes of storage. READ/WRITE operations between the system (master) and the EEPROM (slave) device occur via the SMBus. Write-protect (WP) is connected to V_{SS}, permanently disabling hardware write-protect. For further information please refer to Micron technical note TN-04-42, "Memory Module Serial Presence-Detect."

Temperature Sensor

A class-B temperature sensor is integrated with the SPD EEPROM component on the module. The sensor temperature is monitored and converted into a digital word via the SMBus. System designers can use the user-programmable registers to create a custom temperature-sensing solution based on system requirements. Programming and configuration details comply with JEDEC standard No. 21-C page 4.7-1, "Definition of the TSE2002av, Serial Presence Detect with Temperature Sensor."

Electrical Specifications

Stresses greater than those listed may cause permanent damage to the module. This is a stress rating only, and functional operation of the module at these or any other conditions outside those indicated in each device's data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 8: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
V_{DD}	V_{DD} supply voltage relative to V_{SS}	–0.4	1.975	V
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	–0.4	1.975	V

Table 9: Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units	Notes
V_{DD}	V_{DD} supply voltage		1.425	1.5	1.575	V	
$V_{REFCA(DC)}$	Input reference voltage command/address bus		0.49 × V_{DD}	0.5 × V_{DD}	0.51 × V_{DD}	V	
$V_{REFDQ(DC)}$	I/O reference voltage DQ bus		0.49 × V_{DD}	0.5 × V_{DD}	0.51 × V_{DD}	V	
I_{VTT}	Termination reference current from V_{TT}		–600	–	600	mA	
V_{TT}	Termination reference voltage (DC) – command/address bus		0.49 × V_{DD} - 20mV	0.5 × V_{DD}	0.51 × V_{DD} + 20mV	V	1
T_A	Module ambient operating temperature	Commercial	0	–	70	°C	2, 3
T_C	DDR3 SDRAM component case operating temperature	Commercial	0	–	95	°C	2, 3, 4

Notes:
1. V_{TT} termination voltage in excess of the stated limit will adversely affect the command and address signals' voltage margin and will reduce timing margins.
2. T_A and T_C are simultaneous requirements.
3. For further information, refer to technical note TN-00-08: "Thermal Applications," available on Micron's Web site.
4. The refresh rate is required to double when 85°C < T_C ≤ 95°C.

DRAM Operating Conditions

Recommended AC operating conditions are given in the DDR3 component data sheets. Component specifications are available at micron.com. Module speed grades correlate with component speed grades, as shown below.

Table 10: Module and Component Speed Grades

DDR3 components may exceed the listed module speed grades; module may not be available in all listed speed grades

Module Speed Grade	Component Speed Grade
-2G1	-093
-1G9	-107
-1G6	-125
-1G4	-15E
-1G1	-187E
-1G0	-187
-80C	-25E
-80B	-25

Design Considerations

Simulations

Micron memory modules are designed to optimize signal integrity through carefully designed terminations, controlled board impedances, routing topologies, trace length matching, and decoupling. However, good signal integrity starts at the system level. Micron encourages designers to simulate the signal characteristics of the system's memory bus to ensure adequate signal integrity of the entire memory system.

Power

Operating voltages are specified at the DRAM, not at the edge connector of the module. Designers must account for any system voltage drops at anticipated power levels to ensure the required supply voltage is maintained.

I_{DD} Specifications

Table 11: DDR3 I_{CDD} Specifications and Conditions – 32GB (Die Revision E)

Values are for the MT41J2G4 DDR3 SDRAM only and are computed from values specified in the 8Gb TwinDie (2 Gig x 4) component data sheet

Parameter	Combined Symbol	1866	Units
Operating current 0: One bank ACTIVATE-to-PRECHARGE	I_{CDD0}	2484	mA
Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE	I_{CDD1}	2538	mA
Precharge power-down current: Slow exit	I_{CDD2P0}	1296	mA
Precharge power-down current: Fast exit	I_{CDD2P1}	1638	mA
Precharge quiet standby current	I_{CDD2Q}	1908	mA
Precharge standby current	I_{CDD2N}	1908	mA
Precharge standby ODT current	I_{CDD2NT}	2034	mA
Active power-down current	I_{CDD3P}	1710	mA
Active standby current	I_{CDD3N}	2016	mA
Burst read operating current	I_{CDD4R}	4320	mA
Burst write operating current	I_{CDD4W}	3762	mA
Refresh current	I_{CDD5B}	5634	mA
Self refresh temperature current: MAX T_C = 85°C	I_{CDD6}	1440	mA
Self refresh temperature current (SRT-enabled): MAX T_C = 95°C	I_{CDD6ET}	1800	mA
All banks interleaved read current	I_{CDD7}	5886	mA
Reset current	I_{CDD8}	1440	mA

Table 12: DDR3 I_{CDD} Specifications and Conditions – 32GB (Die Revision N)

Values are for the MT41K2G4 DDR3 SDRAM only and are computed from values specified in the 8Gb TwinDie 1.35V (2 Gig x 4) component data sheet

Parameter	Combined Symbol	1866	Units
Operating current 0: One bank ACTIVATE-to-PRECHARGE	I_{CDD0}	1728	mA
Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE	I_{CDD1}	1908	mA
Precharge power-down current: Slow exit	I_{CDD2P0}	576	mA
Precharge power-down current: Fast exit	I_{CDD2P1}	720	mA
Precharge quiet standby current	I_{CDD2Q}	1224	mA
Precharge standby current	I_{CDD2N}	1224	mA
Precharge standby ODT current	I_{CDD2NT}	1368	mA
Active power-down current	I_{CDD3P}	936	mA
Active standby current	I_{CDD3N}	1440	mA
Burst read operating current	I_{CDD4R}	2556	mA
Burst write operating current	I_{CDD4W}	2556	mA
Refresh current	I_{CDD5B}	3996	mA
Self refresh temperature current: MAX T_C = 85°C	I_{CDD6}	864	mA
Self refresh temperature current (SRT-enabled): MAX T_C = 95°C	I_{CDD6ET}	1152	mA
All banks interleaved read current	I_{CDD7}	3366	mA
Reset current	I_{CDD8}	720	mA

Temperature Sensor with Serial Presence-Detect EEPROM

The temperature sensor continuously monitors the module's temperature and can be read back at any time over the SMBus bus shared with the SPD EEPROM and memory buffer.

Serial Presence-Detect

For the latest SPD data, refer to Micron's SPD page: www.micron.com/SPD.

Table 13: Temperature Sensor with SPD EEPROM Operating Conditions

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage	V_{DDSPD}	3.0	3.6	V
Supply current: V_{DD} = 3.3V	I_{DD}	–	2.0	mA
Input high voltage: Logic 1; SCL, SDA	V_{IH}	V_{DDSPD} x 0.7	V_{DDSPD} + 1	V
Input low voltage: Logic 0; SCL, SDA	V_{IL}	–0.5	V_{DDSPD} x 0.3	V
Output low voltage: I_{OUT} = 2.1mA	V_{OL}	–	0.4	V
Input current	I_{IN}	–5.0	5.0	µA
Temperature sensing range	–	–40	125	°C
Temperature sensor accuracy (class B)	–	–1.0	1.0	°C

Table 14: Temperature Sensor and SPD EEPROM Serial Interface Timing

Parameter/Condition	Symbol	Min	Max	Units
Time bus must be free before a new transition can start	^{t}BUF	4.7	–	µs
SDA fall time	^{t}F	20	300	ns
SDA rise time	^{t}R	–	1000	ns
Data hold time	^{t}HD:DAT	200	900	ns
Start condition hold time	^{t}H:STA	4.0	–	µs
Clock HIGH period	^{t}HIGH	4.0	50	µs
Clock LOW period	^{t}LOW	4.7	–	µs
SCL clock frequency	^{t}SCL	10	100	kHz
Data setup time	^{t}SU:DAT	250	–	ns
Start condition setup time	^{t}SU:STA	4.7	–	µs
Stop condition setup time	^{t}SU:STO	4.0	–	µs

EVENT# Pin

The temperature sensor also adds the EVENT# pin (open-drain). Although not used by the SPD EEPROM, EVENT# is a temperature sensor output used to flag critical events that can be set up in the sensor's configuration register.

EVENT# has three defined modes of operation: interrupt mode, compare mode, and critical temperature mode. The open-drain output of EVENT# under the three separate operating modes is illustrated below. Event thresholds are programmed in the 0x01 reg-

ister using a hysteresis. The alarm window provides a comparison window, with upper and lower limits set in the alarm upper boundary register and the alarm lower boundary register, respectively. When the alarm window is enabled, EVENT# will trigger whenever the temperature is outside the MIN or MAX values set by the user.

The interrupt mode enables software to reset EVENT# after a critical temperature threshold has been detected. Threshold points are set in the configuration register by the user. This mode triggers the critical temperature limit and both the MIN and MAX of the temperature window.

The compare mode is similar to the interrupt mode, except EVENT# cannot be reset by the user and returns to the logic HIGH state only when the temperature falls below the programmed thresholds.

Critical temperature mode triggers EVENT# only when the temperature has exceeded the programmed critical trip point. When the critical trip point has been reached, the temperature sensor goes into comparator mode, and the critical EVENT# cannot be cleared through software.

SMBus Slave Subaddress Decoding

The temperature sensor's physical address differs from the SPD EEPROM's physical address: binary 0011 for A0, A1, A2, and RW#, where A2, A1, and A0 are the three slave subaddress pins and the RW# bit is the READ/WRITE flag.

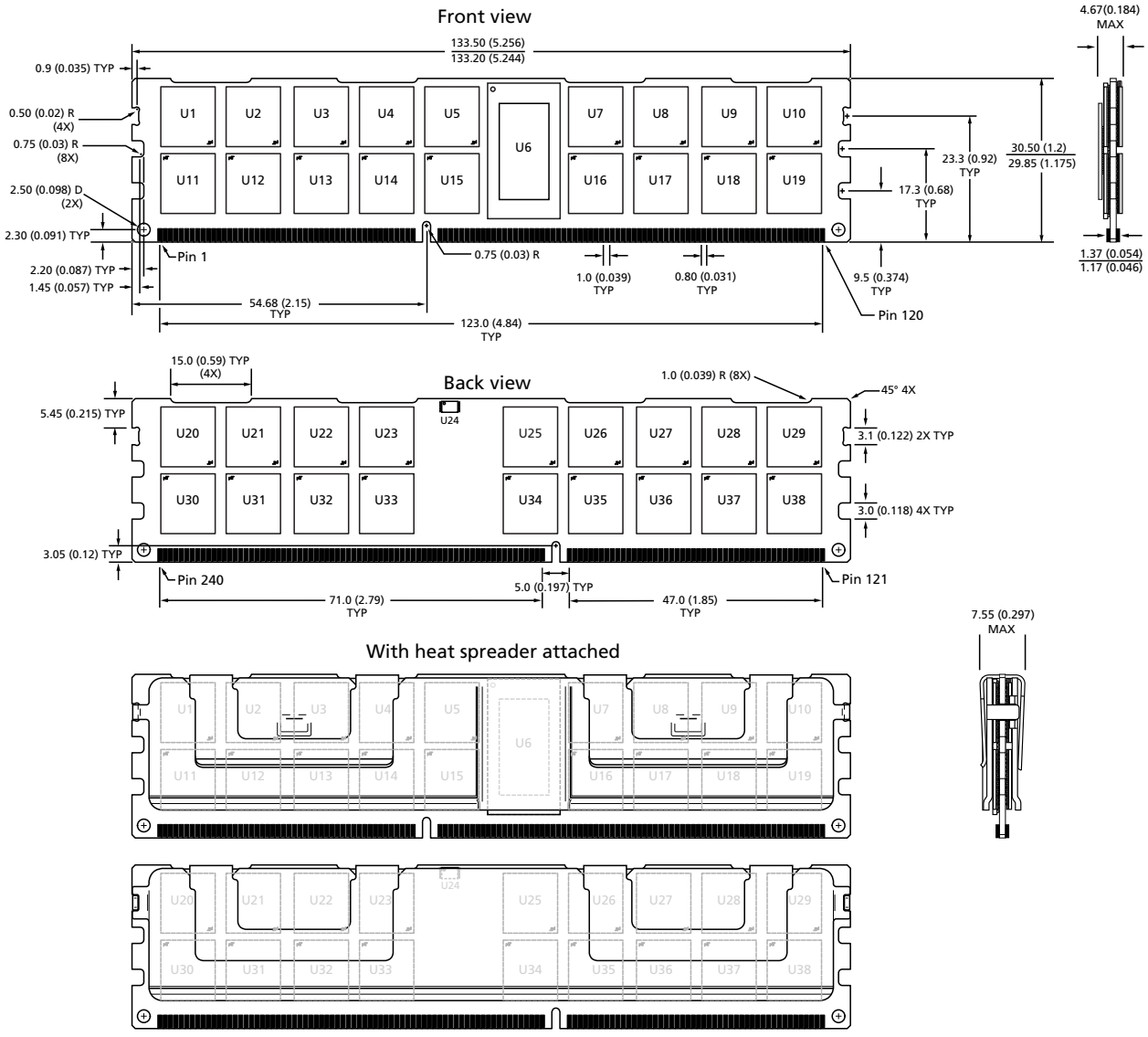
If the slave base address is fixed for the SPD EEPROM/temperature sensor, then the pins set the subaddress bits of the slave address, enabling the devices to be located anywhere within the eight slave address locations. For example, they could be set from 30h to 3Eh.

Serial Presence-Detect Data

For the latest serial presence-detect data, refer to Micron's SPD page: www.micron.com/SPD.

Module Dimensions

Figure 3: 240-Pin DDR3 LRDIMM



Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only.

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