UM2340
User manual

STNRG011 NVM parameters description

Introduction

This user manual provides information for developing applications with the STNRG011 digital combo multi-mode PFC and time-shift LLC resonant controller.

The STNRG011 is a STMicroelectronics® digital device tailored for SMPS applications. It embodies a multi-mode (transition-mode and DCM) PFC controller, a high voltage double-ended controller for the LLC resonant half-bridge, an 800 V-rated startup generator and a sophisticated digital engine, that manages optimal operation of the three blocks.

All the key application parameter of the device are stored into an internal NVM (non-volatile memory), allowing wide configurability and calibration.

This user manual goes in detail through all the NVM parameters and explains how to set them in a real application. For any other information about STNRG011 product, please refer to the STNRG011 datasheet.

Contents

1 Notes

1.1 Parameters packing

The parameters in the NVM are packed starting from the first one at the address 0x00, going through the boundaries between bytes if required.

1.2 NVM configuration

The NVM is divided into 4 parts called bank0, bank1, bank2 and bank3.

Each bank size is 8 bytes.

Bank0 contains mainly trimming and traceability information. For this reason, users cannot modify it.

Bank1, 2 and 3 contain the parameters described in this document. The user can modify them to adapt the STNRG011 algorithms to his application.

1.3 GUI application

In order to easily program the NVM during the development of a new application, a graphical user interface (GUI) has been developed. The GUI strictly works with a communication interface board and allows real time monitoring of the device, NVM and EEPROM contents checking and programming. For more information about the GUI and the interface board, please refer to the UM2342 - user manual: Getting started with the STEVAL-PCC020V1: USB to I²C UART interface board and associated GUI for STNRG products.

2 Equations to set the parameters

2.1 PFC

2.1.1 PFC power calculation

The device uses an internal numerical representation of the power delivered. The relationship between the internal value and the true power is as follows

Equation 1

$$pinn = P\frac{L}{128 \cdot LSBVin^2 \cdot Tck}$$

Where:

- *pinn* is the internal numerical power estimation
- *P* is the real power level
- *L* is the PFC choke inductance value
- *LSBVin* = 1.89 V
- *Tck* = 16.66 ns

Note that this relation is a loose approximation due to the PFC parasitics, which offset the true power level.

2.1.2 PFC compensation parameters

The PFC compensation is calculated at each line valley (i.e. input mains zero crossing).

The device uses the following formula to calculate the power

Equation 2

$$pinn = \left(2 \cdot Kp + Ki\frac{1}{1 - z^{-1}}\right)err$$

where *err* is equal to the voltage error (target output voltage - real output voltage) divided by $Verr_{LSB}$ = 0.473 V.

2.2 LLC

The LLC compensation is based on an analog circuitry at the secondary side.

The time shift value applied by the controller is calculated using the sampled value on the LLC_FB pin.

Equation 3

$$TS = K \cdot \left(\frac{V_{FB}}{LSBV_{FB}} - FBos \right)$$

where:

- *TS* = time shift value applied to LLC SMEDs (in 60 MHz clock ticks)
- *K* is a coefficient that changes accordingly to the LLC switching frequency range used (see *Section 3.4.1: LLC low frequency range on page 29*)
  - *K* = 0.5 for standard range
  - *K* = 1 for low frequency range
- V_{FB} = Voltage on the LLC_FB pin
- $LSBV_{FB}$ = 2.44 mV (used to convert the LLC_FB voltage value in the internal numerical format)
- *FBos* = fixed offset (68)

3 Parameters description

3.1 General system configuration

3.1.1 Shutdown feature

Size: 1 bit

Enables / disables the shutdown comparator connected to the LLC_FB pin.

Available values are

- Disabled
- Enabled

The shutdown comparator is connected to the LLC_FB pin. Its threshold is 125 mV. If the pin is brought below this threshold, and the comparator is enabled, the system will shut down as long as the pin's voltage remains below the threshold.

This feature can be used to realize extra protections (e.g. OTP protection for power stage)

Use

It is suggested to disable the shutdown comparator if it is not used.

3.1.2 Patch upload from EEPROM

Size: 1 bit

Enables / disables the patching feature.

Available values are

- Disabled
- Enabled

If patching is disabled the STNRG011 will not upload the patch from the external EEPROM.

Use

The default value is enabled (i.e. patching enabled). The user has to disable the patching feature if no EEPROM is installed on the application.

3.1.3 ATE mode

Size: 1 bit

Enables / disables the ATE mode.

Available values are

- Enabled
- Disabled

Use

The ATE mode is required to read/write the NVM. Therefore, this parameter should be set to “Enabled”.

In case, after the correct programming of all NVM parameters, the user wants to keep such information protected, he can disable the ATE mode.

Warning: Once the bit will be set to disabled, it will be impossible to access the NVM.

3.1.4 System monitoring

Size: 1 bit

Enables / disables the system monitoring.

Available values are

- Enabled
- Disabled

Monitoring is the periodic unidirectional communication through the UART interface used by the STNRG011 to send out information (including the power estimation, PFC operating mode, etc.). If this feature is not requested, the user can disable it and stop the activity on the UART interface.

3.1.5 VAC reading improvement

Size: 1 bit

Enables / disables the VAC reading improvement feature.

Available values are

- Disabled
- Enabled

If the feature is enabled, the IC will sink from the VAC pin $I_{VAC\_HV\_SINK}$ current during line synchronization at the start-up and I_{XCD} current for about 5 ms in case of the brown-out event, to avoid false brown-in. This allows having a voltage on the VAC pin that has a good shape and compensate the effect of an unbalanced Y-cap in the AC input (such unbalance generates a charge pump effect that increases the VAC voltage).

Use

It is suggested to keep the feature enabled.

3.1.6 Early warning feature

Size: 1 bit

Enables / disables the early warning (EW) pulse generation. This pulse is used to manage the “Power OK” signal.

Available values are

- Enabled
- Disabled

The EW pulse is generated on the PFC_FB pin. This pin, normally the input for sensing the PFC output voltage, in case of device shutdown becomes an output and goes to 5 V.

The duration of the pulse depends on the shut-down cause.

For the normal shutdown (i.e. mains removal, brown-out event, OLP and PFC UVP faults) the pulse is 5 ms long (normal pulse). During this time, the PFC is stopped while the LLC is still working keeping the output voltage regulated.

In case of a dangerous fault, both PFC and LLC stages are immediately stopped and the EW pulse is about 270 µs long (quick pulse).

3.1.7 EW signal in burst mode

Size: 1 bit

Selects the duration of the early warning pulse in the burst mode.

Available values are

- Quick
- Normal

Use

The selection will force the system to use the quick pulse without any LLC activity in the burst mode also during the normal shutdown. This is useful in case the LLC tank is not designed to keep the output voltage regulated at no-load, avoiding the overshoot of the output.

3.1.8 Non latched faults timer

Size: 2 bits

Sets the time between retries in the non-latched (auto restart) mode.

Available values are

- 546 ms
- 1.09 s
- 2.18 s
- 4.37 s

3.2 Faults parameters

3.2.1 Surge detection

Size: 1 bit

Enable / disable the surge comparator.

Available values are

- Disabled
- Enabled

The surge comparator is connected to the VAC pin and its threshold is 430 V.

3.2.2 PFC OC2 detection

Size: 1 bit

Enables / disables the PFC OC2 comparator.

Available values are

- Disabled
- Enabled

The PFC OC2 comparator is connected to the PFC_CS pin and its threshold is 900 mV.

3.2.3 Max number of PFC OC2

Size: 2 bits

Sets the number of consecutive PFC OC2 events before shutting down.

Available values are

- 1
- 2
- 3
- 4

Use

The suggested value is “2”, since it is a good compromise between the noise rejection and protection reactiveness.

The value “1” can be used if minimum intervention time is required: in this case, pay attention because some noise could trigger the protection.

Higher values can be used in case of noisy boards (in this case, the reaction to real OCP2 events will be slower).

3.2.4 PFC HW OVP detection

Size: 1 bit

Enable / disable the hardware PFC OVP comparator.

Available values are

- Disabled
- Enabled

The PFC OVP comparator is the hardware protection against the bulk overvoltage. It is connected to the PFC_FB pin and its threshold is set at 2.3 V.

The fault is always immediate and shuts down the system.

Use

It is suggested to leave the PFC OVP comparator enabled.

3.2.5 LLC OC2 detection

Size: 1 bit

Enables / disables the LLC OC2 comparator.

Available values are

- Disabled
- Enabled

The LLC OC2 comparator is connected to the LLC_CS pin and its threshold is 700 mV.

3.2.6 Max number of LLC OC2

Size: 2 bits

Sets the number of consecutive LLC OC2 events before shutting down.

Available values are

- 1
- 2
- 3
- 4

Use

The suggested value is “2”, since it is a good compromise between the noise rejection and protection reactiveness.

The value “1” can be used if minimum intervention time is required: in this case, pay attention because some noise could trigger the protection.

3.2.7 LLC OVP detection

Size: 1 bit

Enables / disables the LLC OVP comparator.

Available values are

- Disabled
- Enabled

The LLC OVP comparator is connected to the LLC_AUX pin and its threshold is 2.5 V.

3.2.8 Disconnection faults detection

Size: 1 bit

Enables / disables the feedback disconnections faults detection.

Available values are

- Disabled
- Enabled

Use

It is suggested to enable the feedback disconnection faults detection.

Note: Disconnection faults have always “latched” behavior.

3.2.9 PFC OC2 behavior

Size: 1 bit

Sets the behavior of PFC OC2 protection.

Available values are

- Not latched
- Latched

If the fault is set as “Not latched” the system will try to restart after the time defined by the “Non latched faults timer” parameter.

If the fault is set as “Latched” the switching activity will remain off and the V_{CC} will remain between 15 V and 17 V using the HV start-up generator (as long as there is the mains connected).

3.2.10 PFC HW OVP behavior

Size: 1 bit

Sets the behavior of the PFC OVP.

Available values are

- Not latched
- Latched

If the fault is set as “Not latched” the system will try to restart after the time defined by the “Non latched faults timer” parameter.

If the fault is set as “Latched” the switching activity will remain off and the V_{CC} will remain between 15 V and 17 V using the HV start-up generator (as long as there is the mains connected).

3.2.11 PFC UVP behavior

Size: 1 bit

Sets the behavior of the PFC UVP.

Available values are

- Slow
- Adaptive

When the UVP threshold is detected, if this parameter is set “Slow”, the device will shut down the power supply if the PFC UVP is still present for at least 100 ms.

If the behavior is set to “Adaptive”, the device will shut down the power supply if the PFC UVP is triggered and the mains voltage is detected below the brown-out threshold. If both conditions are not true, the system will manage the fault as if the selection is set “Slow”. This selection enables large capacitive loads to be connected through the OR-Ing FET.

The “Slow” timing could be helpful in some case, when the designer would like to let the system work with a low bulk voltage.

Please remember that, because of the LLC OC2 protection and the ACP feature, the system is still protected against overstresses.

3.2.12 LLC SS timeout behavior

Size: 1 bit

Sets the behavior of the LLC soft-start timeout protection.

Available values are

- Not latched
- Latched

If the fault is set as “Not latched” the system will try to restart after the time defined by the “Non latched faults timer” parameter.

If the fault is set as “Latched” the switching activity will remain off and the V_{CC} will remain between 15 V and 17 V using the HV start-up generator (as long as there is the mains connected).

3.2.13 LLC ACP behavior

Size: 1 bit

Sets the behavior of the LLC ACP (both “Soft” and “Hard”).

Available values are

- Not latched
- Latched

If the fault is set as “Not latched” the system will try to restart after the time defined by the “Non latched faults timer” parameter.

If the fault is set as “Latched” the switching activity will remain off and the V_{CC} will remain between 15 V and 17 V using the HV start-up generator (as long as there is the mains connected).

3.2.14 LLC OC2 behavior

Size: 1 bit

Sets the behavior of the LLC OC2 protection.

Available values are

- Not latched
- Latched

If the fault is set as “Not latched” the system will try to restart after the time defined by the “Non latched faults timer” parameter.

If the fault is set as “Latched” the switching activity will remain off and the V_{CC} will remain between 15 V and 17 V using the HV start-up generator (as long as there is the mains connected).

3.2.15 LLC OLP behavior

Size: 1 bit

Sets the behavior of the LLC overload protection (OLP).

Available values are

- Not latched
- Latched

If the fault is set as “Not latched” the system will try to restart after the time defined by the “Non latched faults timer”.

If the fault is set as “Latched” the switching activity will remain off and the V_{CC} will remain between 15 V and 17 V using the HV start-up generator (as long as there is the mains connected).

3.2.16 LLC OVP behavior

Size: 1 bit

Sets the behavior of the LLC OVP.

Available values are

- Not latched
- Latched

If the fault is set as “Not latched” the system will try to restart after the time defined by the “Non latched faults timer” parameter.

If the fault is set as “Latched” the switching activity will remain off and the V_{CC} will remain between 15 V and 17 V using the HV start-up generator (as long as there is the mains connected).

3.3 PFC parameters

3.3.1 PFC Ki

Size: 3 bits

Sets the integral constant of the PFC compensation filter.

Available values are:

- 4
- 6
- 8
- 12
- 16
- 24
- 32
- 48

3.3.2 PFC Kp

Size: 3 bits

Sets the proportional constant of the PFC compensation filter.

- 8
- 12
- 16
- 24
- 32
- 48
- 64
- 96

*Note: The device uses 2 * Kp for calculations (see Section 2.1.2: PFC compensation parameters on page 6).*

3.3.3 PFC boost exiting burst

Size: 1 bit

Enables / disables the PFC improved dynamic response exiting burst mode.

Available values are

- Disabled
- Enabled

Use

This feature prevents bulk voltage undershoot in the case of a high load transient from the burst mode.

It is suggested to enable the PFC SW OVP in case the feature is enabled (see *Section 3.3.20: PFC SW OVP threshold (delta) on page 29* for details).

3.3.4 PFC MOSFET LEB

Size: 3 bits

Sets the PFC MOSFET minimum on-time (also called LEB, i.e. “Leading Edge Blanking”).

Available values are

- 133 ns
- 167 ns
- 200 ns
- 233 ns
- 267 ns
- 333 ns
- 400 ns
- 467 ns

This time is used to filter the spike on the PFC_CS pin at the PFC MOSFET turn-on. During this time the PFC_CS comparator output (THD improver) is ignored.

Use

Adjust the blanking time according to design requirements.

The middle value 267 ns can be used as a starting point and then, after looking at the PFC_CS waveform during the PFC operation it can be adjusted.

3.3.5 PFC THD improver base

Size: 3 bits

Sets the base value for the ReCOT functionality (THD improver).

Available values are

- 0 mV
- 2 mV
- 4 mV
- 6 mV
- 8 mV
- 10 mV
- 12 mV
- 14 mV

The parameter sets the PFC_CS comparator threshold.

Use

This parameter can be tuned to improve the THD of the system. Together with the “PFC THD improver gain”, this parameter can be used to improve the distortion and power factor of the PFC observing the current waveform and THD/PF measurements.

3.3.6 PFC THD improver gain

Size: 3 bits

Sets the slope of the ReCOT functionality (THD improver) to compensate for the current in the input capacitors.

Available values are

- 0 - gain disabled
- 1
- 2
- 3
- 4
- 5
- 6
- 7

The threshold level difference between the beginning and the end of the line cycle is

Equation 4

$$Vramp = \frac{igain \cdot \sqrt{2}Vin \cdot 3.9mV}{256 \cdot 484.5V/256}$$

i.e.

Equation 5

$$Vramp = igain \cdot Vin \cdot 11.38 \cdot 10^{-6}$$

Which will act as a negative capacitance of the value

Equation 6

$$Cneg = 2 \cdot 10^{-6} \frac{gain}{\pi f_{line} R_{sense}}$$

Use

Together with the “PFC THD improver base”, this parameter can be used to improve the distortion and power factor of the PFC.

The value can be initially calculated with *Equation 6* to compensate for the capacitance at the PFC input and EMI filter and then tune it by observing the current waveform at the converter input and THD/PF measurements to find the optimum point.

3.3.7 PFC maximum power

Size: 4 bits

Sets the upper clamp of the PI filter, i.e. the maximum power that the PFC can provide.

Available values are

- 4096
- 4608
- 5120
- 5632
- 6144
- 6656
- 7168
- 7680
- 8192
- 9216
- 10240
- 11264
- 12288
- 13312
- 14336
- 15360

Use

Select a value higher than the nominal power in order to be able to respond to transients.

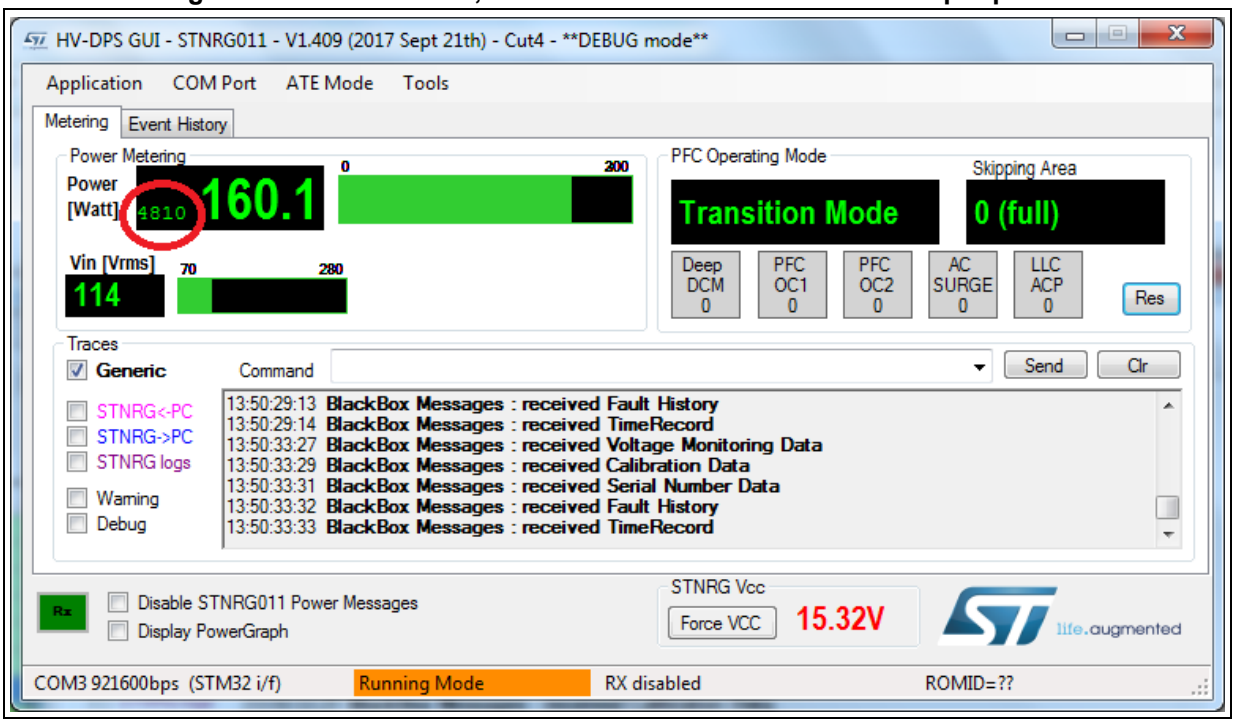
To initially setup this value, set it to twice the maximum power estimation using *Equation 1* in *Section 2.1.1: PFC power calculation on page 6*.

Then fine-tune it by

- Turning on the board with the maximum load
- Reading the input power raw value using the GUI (see *Figure 1* for details)
- Setting the parameter to input power raw value + 30%

The value can be further adjusted by looking at the PFC stage transient response.

Figure 1. STNRG011 GUI; circled in red the raw value of the input power



3.3.8 PFC pss

Size: 3 bits

Sets the PFC power during the soft-start.

Available values are

- 640
- 1280
- 1920
- 2560
- 3200
- 3840
- 4480
- 5120

The higher the value, the higher the on-time of the PFC MOSFET during the soft-start phase.

Use

Choose the value that allows reaching the required PFC soft-start time.

The faster the soft-start time required the higher the PFC current will be.

Using a high value can lead to overshoots (the bulk voltage increases at every line cycle increase).

3.3.9 PFC pcc

Size: 2 bits

Sets the PFC reference the power during burst mode operation.

Available values are

- 3218
- 5558
- 7898
- 10238

The higher the value, the higher the maximum on-time of the PFC MOSFET during the burst mode operation. This means that the transferred power will be also higher.

The algorithm will adjust the on-time of the PFC MOSFET according to the required power, in order to reduce the acoustic noise.

Use

Select the lowest value that allows correct bulk voltage regulation at the no-load and minimum AC voltage condition.

3.3.10 PFC Min Pin Vskip

Size: 5 bits

Sets the internal power threshold at which the mode is changed towards DCM (i.e. one more valley is skipped).

Available values are

- 1280
- 1344
- 1408
- 1472
- 1536
- 1600
- 1664
- 1728
- 1792
- 1856
- 1920
- 1984
- 2048
- 2112
- 2176
- 2240
- 2304
- 2368
- 2432
- 2496
- 2560
- 2624
- 2688
- 2752
- 2816
- 2880
- 2944
- 3008
- 3072
- 3136
- 3200
- 3264

Use

This parameter is mainly used to guarantee a fast reaction to transients, forcing the PFC to increase the number of valleys or switch to DCM when the internal power value plus nValleys * “PFC Delta Pin Vskip” is lower than this parameter.

The frequency based mode change measures the frequency at each half line cycle, then if the frequency is out of the “PFC Min Tsw Vskip” or “PFC Max Tsw Vskip” values it increments or decrements the number of valleys by one. By only relying on the frequency it would require 4 half-line cycles to change from TM to DCM, potentially causing an overshoot on the Vbus.

The threshold should be kept low enough so that in steady state the frequency dominates the mode change.

3.3.11 PFC Max Pin Vskip (delta)

Size: 5 bits

Sets the internal power threshold at which the mode is changed toward TM (i.e. one less valley is skipped).

Available values are

- 1280
- 1408
- 1536
- 1664
- 1792
- 1920
- 2048
- 2176
- 2304
- 2432
- 2560
- 2688
- 2816
- 2944
- 3072
- 3200
- 3328
- 3456
- 3584
- 3712
- 3840
- 3968
- 4096
- 4224
- 4352
- 4480
- 4608
- 4736
- 4864
- 4992
- 5120
- 5248

The parameter in the NVM is a positive delta with respect to the “PFC Min Tsw Vskip”.

The real value used during the code execution is therefore

Equation 7

$$\text{"PFC Max Pin Vskip"} = \text{"PFC Min Pin Vskip"} + \text{"PFC Max Pin Vskip(delta)"}$$

Use

This parameter is mainly used to guarantee a fast reaction to transients, forcing the PFC to reduce the number of valleys or to switch to the transition mode when the internal power value plus nValleys * “PFC Delta Pin Vskip” is greater than this parameter.

The frequency based mode change measures the frequency at each half line cycle, then if the frequency is out of the “PFC Min Tsw Vskip” or “PFC Max Tsw Vskip” values it increments or decrements the number of valleys by one. By only relying on the frequency it would require 4 half-line cycles to change from DCM to TM, potentially causing a dip on the Vbus.

The threshold should be kept high enough so that in the steady state the frequency dominates the mode change.

3.3.12 PFC Delta Pin Vskip

Size: 5 bits

Sets a correction factor used when switching between valley-skipping modes.

Available values are

- 160
- 176
- 192
- 208
- 224
- 240
- 252
- 272
- 288
- 304
- 320
- 336
- 352
- 368
- 384
- 400
- 416
- 432
- 448
- 464
- 480
- 496
- 512
- 528
- 544
- 560
- 576
- 592
- 608
- 624
- 640
- 656

Use

This parameter should be approximately set to the reduction of output power determined by the addition of one valley.

The device uses this parameter to reduce the discontinuity on the output power when changing the number of valleys skipped.

3.3.13 PFC maximum DCM power

Size: 4 bits

Sets the power threshold to switch from the DCM to the valley-skipping mode. Sets also the on-time duration of the PFC gate drive while in the DCM mode.

Available values are

- 1024
- 1152
- 1280
- 1408
- 1536
- 1664
- 1792
- 1920
- 2048
- 2304
- 2560
- 2816
- 3072
- 3328
- 3584
- 3840

In the DCM mode, the MOSFET on-time is calculated with the following formula

Equation 8

$$Ton = \frac{"PFC\ \ Maximum\ \ DCM\ \ power" \cdot 2}{Vin^2}$$

3.3.14 PFC Min Tsw Vskip

Size: 5 bits

Sets the minimum switching period (i.e. the maximum switching frequency) for the valley-skipping mode.

Available values are

- 234 kHz
- 221 kHz
- 208 kHz
- 197 kHz
- 188 kHz
- 179 kHz
- 170 kHz
- 163 kHz
- 117 kHz
- 110 kHz
- 104 kHz
- 99 kHz
- 94 kHz
- 89 kHz
- 85 kHz
- 82 kHz

- 156 kHz
- 150 kHz
- 144 kHz
- 139 kHz
- 134 kHz
- 129 kHz
- 125 kHz
- 121 kHz
- 78 kHz
- 75 kHz
- 72 kHz
- 69 kHz
- 67 kHz
- 65 kHz
- 63 kHz
- 60 kHz

The period is measured at the peak of the mains sinusoidal voltage. If the measured period is lower than this value, the system increases the number of valleys, towards DCM.

The corresponding frequency values are shown above.

Use

This value, together with the “PFC Max Tsw Vskip”, is used to set the range of PFC switching frequency; therefore, it is important to optimize the efficiency of the PFC.

The max. value should be at least 1.5 times the min. value to avoid the system continuously switching between different modes.

3.3.15 PFC Max Tsw Vskip

Size: 5 bits

Sets the maximum switching period (i.e. the minimum switching frequency) for the valley-skipping mode.

Available values are

- 101 kHz
- 96 kHz
- 91 kHz
- 87 kHz
- 83 kHz
- 80 kHz
- 77 kHz
- 74 kHz
- 71 kHz
- 68 kHz
- 66 kHz
- 64 kHz
- 61 kHz
- 60 kHz
- 54 kHz
- 51 kHz
- 49 kHz
- 46 kHz
- 44 kHz
- 42 kHz
- 40 kHz
- 39 kHz
- 37 kHz
- 36 kHz
- 34 kHz
- 33 kHz
- 32 kHz
- 31 kHz

- 58 kHz
- 56 kHz
- 30 kHz
- 29 kHz

The period is measured at the peak of the mains sinusoidal voltage. If the measured period is higher than this value, the system decreases the number of valleys, towards TM.

The corresponding frequency values are shown above.

Use

This value, together with the “PFC Min Tsw Vskip”, is used to set the range of PFC switching frequency; therefore, it is important to optimize the efficiency of the PFC.

The max. value should be at least 1.5 times the min. value to avoid the system continuously switching between different modes.

3.3.16 Skipping area threshold

Size: 4 bits

Sets the power level at which the PFC will start reducing the conduction phase to a part of the AC line half-cycle (skipping area feature).

Available values are

- 0
- 320
- 384
- 448
- 512
- 640
- 768
- 896
- 1024
- 1280
- 1536
- 1792
- 2048
- 2560
- 3072
- 3584

Use

This parameter can be used to improve efficiency at the power levels at which harmonic contents are not subject to regulation (e.g. below 75 W).

To tune the parameter, run the system at the desired threshold level and Vac value, read the input power raw value from the GUI and use it as the threshold (see *Figure 1 on page 20* for details).

It is suggested to keep a 20% margin to take into account variations from unit to unit (e.g. set the threshold to 60 W to assure it is out of this mode at 75 W).

Test the exit point from the skipping area mode at the nominal mains voltages to check that the system returns in the continuous switching mode below 75 W.

Setting this parameter to “0” disables the skipping area feature, in case good THD and PF are required even at very low loads.

3.3.17 PFC Vout target

Size: 3 bits

Sets the nominal PFC output voltage.

Available values are

- 1.946 V - 377 V
- 1.965 V - 381 V
- 1.985 V - 385 V
- 2.004 V - 388 V
- 2.024 V - 392 V
- 2.063 V - 400 V
- 2.102 V - 407 V
- 2.141 V - 415 V

This is the voltage level at which the PFC stage regulates its output, in all operating conditions.

Use

Set the PFC output voltage according to the application specs.

The values on the left are referred to the PFC_FB pin, that corresponds to values on the right if the bulk voltage divider is designed with the standard ratio $k = 5.16 \cdot 10^{-3}$ (i.e. 484.5 V on the bulk voltage correspond to 2.5 V on the PFC_FB pin).

If other bulk voltage dividers are used, the values on the left can be used to set the output voltage. In this case, consider that the PFC HW OVP comparator has a fixed threshold of 2.3 V.

3.3.18 PFC Vout SS end (delta)

Size: 2 bits

Sets the voltage at which the PFC terminates the soft-start and the system begins the LLC soft-start.

Available values are

- 19.5 mV - 3.8 V
- 29.3 mV - 5.7 V
- 39.1 mV - 7.6 V
- 58.6 mV - 11.4 V

Use

The above values are intended as a negative delta with respect to the “PFC Vout target” parameter.

The PFC soft-start end voltage will be therefore:

Equation 9

$$\text{"PFC Vout SS end"} = \text{"PFC Vout target"} - \text{"PFC Vout SS end (delta)"}$$

The values on the left are referred to the PFC_FB pin, that corresponds to values on the right if the bulk voltage divider is designed with the standard ratio k = $5.16 \cdot 10^{-3}$ (i.e. 484.5 V on the bulk voltage correspond to 2.5 V on the PFC_FB pin).

If other bulk voltage dividers are used, the values on the left can be used to set the output voltage.

3.3.19 PFC UVP threshold (delta)

Bits: 3

Sets the UVP level for PFC output voltage.

Available values are

- 0.156 V - 30 V
- 0.234 V - 45 V
- 0.313 V - 61 V
- 0.391 V - 76 V
- 0.469 V - 91 V
- 0.547 V - 106 V
- 0.625 V - 121 V
- 0.703 V - 136 V

Use

The above values are intended as a negative delta with respect to the “PFC Vout target” parameter.

In fact, the UVP threshold is defined as

Equation 10

$$\text{"PFC UVP threshold"} = \text{"PFC Vout target"} - \text{"PFC UVP threshold (delta)"}$$

The values on the left are referred to the PFC_FB pin, that corresponds to values on the right if the bulk voltage divider is designed with the standard ratio k = $5.16 \cdot 10^{-3}$ (i.e. 484.5 V on the bulk voltage correspond to 2.5 V on the PFC_FB pin).

If other bulk voltage dividers are used, the values on the left can be used to set the output voltage.

3.3.20 PFC SW OVP threshold (delta)

Size: 2 bits

Sets the PFC SW OVP level.

Available values are

- 51.3 mV - 10 V
- 78.1 mV - 15 V
- 105 mV - 20 V
- SW OVP disabled

Use

The above values are intended as a positive delta with respect to the “PFC Vout target” parameter.

In fact, the SW OVP threshold is defined as:

Equation 11

$$\text{"PFC SW OVP threshold"} = \text{"PFC Vout target"} - \text{"PFC SW OVP threshold (delta)"}$$

The values on the left are referred to the PFC_FB pin, that corresponds to values on the right if the bulk voltage divider is designed with the standard ratio $k = 5.16 \cdot 10^{-3}$ (i.e. 484.5 V on the bulk voltage correspond to 2.5 V on the PFC_FB pin).

If other bulk voltage dividers are used, the values on the left can be used to set the output voltage.

It is suggested to keep the SW OVP enabled with the maximum value 105 mV - 20 V, especially if the “PFC boost exiting burst” feature is enabled.

3.4 LLC parameters

3.4.1 LLC low frequency range

Size: 1 bit

Enables / disables the low LLC switching frequency range selection.

Available values are

- Enabled
- Disabled

This parameter is used to select the operating frequency range for the LLC. More in detail, if it is set as disabled the frequency range is the standard one.

In case an application is designed for a low operating switching frequency range, setting this parameter to “Enable” allows using an appropriate range for some of the timing parameters.

Use

As a rule of thumb, considering a system designed to work near resonance in nominal condition, if the resonance frequency is greater than 70 kHz the standard range can be used.

In case the resonance frequency is lower than 60 kHz, the low frequency range is suggested.

3.4.2 LLC HVG first Ton

Size: 4 bits

Sets the total on-time of the first LLC HVG.

Available values are

- 133.3 ns
- 200 ns
- 266.7 ns
- 333.3 ns
- 400 ns
- 466.7 ns
- 533.3 ns
- 600 ns
- 666.7 ns
- 800 ns
- 933.3 ns
- 1067 ns
- 1200 ns
- 1333 ns
- 1467 ns
- 1600 ns

At the LLC turn-on, during the safe-start phase, this is the total on-time of the first pulse of the high-side gate drive. Typically, higher values have to be used with high L_{lk} resonant tanks.

3.4.3 LLC LVG first TS

Size: 4 bits

Sets the time shift value of the first LLC LVG.

Available values are

“LLC low frequency range” = disabled

- 166.7 ns
- 200 ns
- 233.3 ns
- 266.7 ns
- 300 ns
- 333.3 ns
- 366.7 ns

“LLC low frequency range” = enabled

- 333.3 ns
- 366.7 ns
- 400 ns
- 433.3 ns
- 466.7 ns
- 500 ns
- 533.3 ns

- 400 ns
- 433.3 ns
- 500 ns
- 566.7 ns
- 633.3 ns
- 700 ns
- 766.7 ns
- 833.3 ns
- 900 ns
- 566.7 ns
- 600 ns
- 666.7 ns
- 733.3 ns
- 800 ns
- 866.7 ns
- 933.3 ns
- 1000 ns
- 1067 ns

This parameter defines the time shift for the first low side gate drive pulse, during the safe start.

Such time shift value is then used as the first one for the LLC soft-start.

The available values depend on the LLC switching frequency range selected with the “LLC low frequency range” parameter.

3.4.4 LLC dead time

Size: 2 bits

Sets the LLC half-bridge dead time.

Available values are

- 266.7 ns
- 333.3 ns
- 400 ns
- 466.7 ns

Use this parameter to select the dead time duration (for both transitions) according to resonant tank needs.

3.4.5 LLC soft-start speed

Size: 3 bits

Sets the speed of the LLC soft-start.

Available values are

“LLC low frequency range” = disabled

- 8.3 ns
- 16.7 ns
- 25 ns
- 33.3 ns
- 41.7 ns
- 50 ns

“LLC low frequency range” = enabled

- 16.7 ns
- 33.3 ns
- 50 ns
- 66.7 ns
- 83.3 ns
- 100 ns

- 58.3 ns
- 66.7 ns
- 117 ns
- 133 ns

This parameter is the time shift increment applied every 30 µs during the LLC soft-start.

The smaller the value the slower will be the output voltage rise and the LLC tank current.

The suggestion is to start with the minimum value (usually OK for most applications) and increase it in case a faster Vout rise time is required.

The available values depend on the LLC switching frequency range selected with the “LLC low frequency range” parameter.

3.4.6 Minimum time shift

Size: 4 bits

Sets the minimum value for the time shift during the normal operation.

Available values are

“LLC low frequency range” = disabled

- 125 ns
- 158.3 ns
- 191.7 ns
- 225 ns
- 258.3 ns
- 291.7 ns
- 325 ns
- 358.3 ns
- 391.7 ns
- 425 ns
- 458.3 ns
- 491.7 ns
- 525 ns
- 558.3 ns
- 591.7 ns
- 625 ns

“LLC low frequency range” = enabled

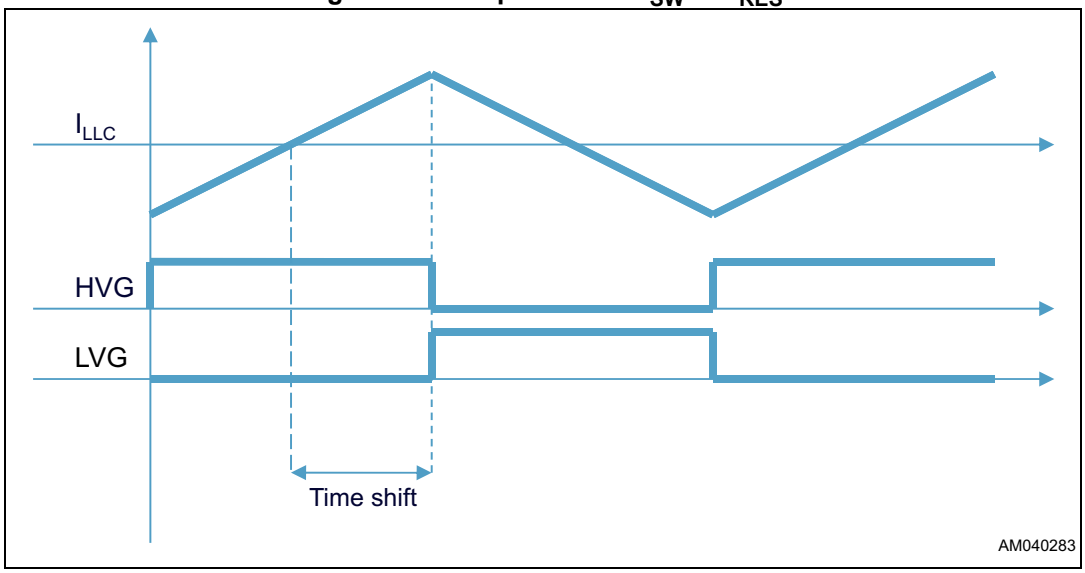
- 250 ns
- 316.7 ns
- 383.3 ns
- 450 ns
- 516.7 ns
- 583.3 ns
- 650 ns
- 716.7 ns
- 783.3 ns
- 850 ns
- 916.7 ns
- 983.3 ns
- 1050 ns
- 1117 ns
- 1183 ns
- 1250 ns

The available values depends on the LLC switching frequency range selected with the “LLC low frequency range” parameter.

Use

The minimum time shift value is used to set the maximum LLC switching frequency. The relationship between the time shift and switching period is complex. Anyway, for this limit condition, a good approximation can be found (see *Figure 2*).

Figure 2. LLC operation at f_{SW} >> f_{RES}



When the operating frequency is much higher than the resonance frequency, the resonant tank current I_{LLC} becomes a triangular waveform, because the current provided to the secondary side becomes negligible with respect to the magnetizing current.

Approximating the current triangular and neglecting the dead times, the time shift value (i.e. the time between zero crossing and MOS turn-off) becomes half of each MOSFET on-time.

Therefore:

Equation 12

$$f_{SWmax} = \frac{1}{4 \cdot (TS_{min} + ZCD_{delay})}$$

where TS_{min} is the minimum time shift value and ZCD_{delay} is the delay given by the ZCD comparator and digital filtering:

Equation 13

$$ZCD_{delay} = ZCD\_comp_{del} + "LLC\ \ ZCD\ \ comp\ \ digital\ \ fitering"$$

ZCD_comp_{del} is the comparator delay, estimated in 150 ns. *"LLC ZCD comp digital filtering"* is the digital filtering of the ZCD comparator.

Even if the dead times are not negligible (since we are working at high frequency) the above relationship is still valid if the system is well designed and guarantees the ZVS operation.

3.4.7 Maximum time shift

Size: 4 bits

Sets the maximum value for the time shift during the normal operation.

Available values are

“LLC low frequency range” = disabled

- 3.96 µs
- 4.22 µs
- 4.49 µs
- 4.76 µs
- 5.02 µs
- 5.29 µs
- 5.56 µs
- 5.82 µs
- 6.09 µs
- 6.36 µs
- 6.62 µs
- 6.89 µs
- 7.16 µs
- 7.42 µs
- 7.69 µs
- 7.96 µs

“LLC low frequency range” = enabled

- 7.92 µs
- 8.45 µs
- 8.98 µs
- 9.52 µs
- 10.05 µs
- 10.58 µs
- 11.12 µs
- 11.65 µs
- 12.18 µs
- 12.72 µs
- 13.25 µs
- 13.78 µs
- 14.32 µs
- 14.85 µs
- 15.38 µs
- 15.92 µs

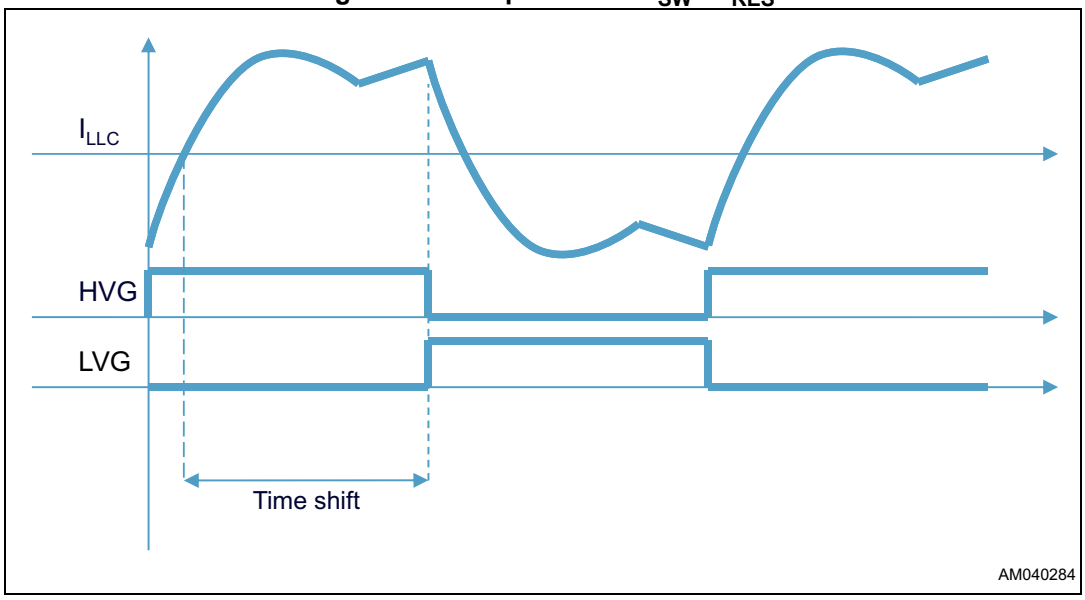
The available values depend on the LLC switching frequency range selected with the “LLC low frequency range” parameter.

Use

The maximum time shift value is used to set the minimum LLC switching frequency. The relationship is not as easy as for the maximum frequency but it is possible to find a simple relationship to set the parameter.

Talking about minimum frequency means typically working in the below resonance region. The key waveform is shown in *Figure 3*.

Figure 3. LLC operation at $f_{SW} < f_{RES}$



Looking at *Figure 2* is it possible to see that, when working below resonance, the time shift duration and the half period become quite similar. As a limit case, when working on the boundary between inductive and capacitive regions, the time shift is exactly half of the switching cycle.

The above information can be used to estimate a first value for the maximum time shift

Equation 14

$$f_{SWmin} \cong \frac{1}{2 \cdot (TS_{max} + ZCD_{delay})}$$

Where TS_{max} is the maximum time shift value and ZCD_{delay} is the delay given by the ZCD comparator and digital filtering

Equation 15

$$ZCD_{delay} = ZCD\_comp_{del} + "LLC\ ZCD\ comp\ digital\ fitering"$$

ZCD_comp_{del} is the comparator delay, estimated in 150 ns. *"LLC ZCD comp digital filtering"* is the digital filtering of the ZCD comparator.

This formula can be used to start the design and the value can be fine-tuned at the bench, running the real application prototype.

Remember that the STNRG011 provides anti capacitive protection (ACP), so, even if the user puts a large value there is no risk of damaging the board components.

3.4.8 LLC OLP threshold

Size: 4 bits

Sets the threshold of the LLC OC1 comparator on LLC_CS pin for OLP functionality.

Available values are

- 23.87 mV
- 55.61 mV
- 87.35 mV
- 119.1 mV
- 150.84 mV
- 182.58 mV
- 214.32 mV
- 246.06 mV
- 277.81 mV
- 309.55 mV
- 341.29 mV
- 373.03 mV
- 404.77 mV
- 436.52 mV
- 468.26 mV
- 500 mV

Use

The LLC OC1 comparator is used to manage overloads conditions (OLP). This parameter defines the threshold of the current sense level of the application at which the system has to enter the OLP fault, after a timeout defined by the “LLC OLP timeout”.

3.4.9 LLC OLP timeout

Size: 2 bits

Sets the duration of the OLP management.

Available values are

- 10 ms
- 200 ms
- 400 ms
- 1 s

Use

The LLC OC1 comparator is used to manage overloads conditions (OLP). This parameter defines how long overload condition can be sustained.

If the load is high enough to continuously trigger the LLC OC1 comparator, set with the “LLC OLP threshold” parameter, the system will shut down after the timeout defined by this parameter.

3.4.10 ACP sensitivity

Size: 1 bit

Sets the sensitivity on detection ACP condition.

Available values are

- Low
- High

The ACP sensitivity applies either for hard and soft ACP features.

3.4.11 Hard ACP detection

Size: 1 bit

Enables / disables the hard ACP detection.

Available values are

- Disabled
- Enabled

Hard ACP is the protection that is triggered when the system reaches the capacitive mode (i.e. the time between the MOSFET turn-on and tank current zero crossing becomes zero or negative). The system immediately shutdowns both sections if the fault is triggered.

The fault can be latched or not latched depending on the “LLC ACP behavior”.

Note: In case the hard ACP detection is disabled, the system will not shutdown if ACP is sensed during dead time, but it will wait for the correct ZCD sign in order to turn on the next gate-drive.

3.4.12 Soft ACP feature

Size: 1 bit

Enables / disables the soft ACP management.

Available values are

- Enabled
- Disabled

Soft ACP is the protection that is triggered when the system is approaching the capacitive mode (i.e. the time between the MOSFET turn-on and tank current zero crossing becomes smaller than the value programmed with the parameter “Soft ACP entering threshold”).

The feature will try to recover the capacitive mode, reducing the LLC time shift value of a quantity defined by the “Soft ACP TS decrement”, every time the protection is triggered, for a maximum number of occurrences of “Maximum soft ACP occurrences”.

Every time the system triggers the soft ACP feature, the STNRG011 will move to the soft-start state, to smoothly recover the regulation.

The system will shut down for the soft ACP fault if the minimum time shift or the maximum number of soft ACP occurrences is reached. The fault can be latched or not latched depending on the “LLC ACP behavior”.

3.4.13 Soft ACP entering threshold

Size: 3 bits

Sets the time threshold for entering the soft ACP management.

Available values are

“LLC low frequency range” = disabled

- 100 ns
- 167 ns
- 233 ns
- 300 ns
- 367 ns
- 433 ns
- 500 ns
- 567 ns

“LLC low frequency range” = enabled

- 200 ns
- 333 ns
- 467 ns
- 600 ns
- 733 ns
- 867 ns
- 1000 ns
- 1133 ns

Use

If the time between the MOSFET turn-on and LLC ZCD signal becomes lower than the threshold defined by this parameter (i.e. the system is approaching the capacitive mode), the IC enters the soft ACP management.

The available values depend on the LLC switching frequency range selected with the “LLC low frequency range” parameter.

3.4.14 Soft ACP TS decrement

Size: 3 bits

Sets the immediate time shift decrease during the soft ACP management.

Available values are:

“LLC low frequency range” = disabled

- 66.7 ns
- 100 ns
- 133 ns
- 200 ns
- 267 ns
- 400 ns
- 533 ns
- 800 ns

“LLC low frequency range” = enabled

- 133 ns
- 200 ns
- 267 ns
- 400 ns
- 533 ns
- 800 ns
- 1067 ns
- 1600 ns

Use

During the Soft ACP management, the time shift value is decreased by the amount defined by this parameter. This delta is applied immediately, every time the system triggers the soft ACP. The higher the value the faster the shift towards higher switching frequencies.

The system will shut down for the soft ACP fault if the minimum time shift is reached. The fault can be latched or not latched depending on the “LLC ACP behavior”.

The time shift decrement depends on the “LLC low frequency range” parameter.

3.4.15 Maximum soft ACP occurrences

Size: 1 bit

Sets the maximum number of consecutive soft ACP occurrences before the shutdown.

Available values are

- 8
- 16

Use

This parameter defines the maximum consecutive number of times the soft ACP is managed.

Every time the system triggers the soft ACP feature, the STNRG011 will move to the soft-start state, to recover smoothly the regulation. The counter of the soft ACP managed is not cleared if the system cannot move to the normal running state.

The system will shut down for the soft ACP fault if the maximum number of soft ACP occurrences is reached. The fault can be latched or not latched depending on the “LLC ACP behavior” parameter.

3.5 Burst mode parameters

3.5.1 External burst mode

Size: 1 bit

Enables / disables the external burst mode feature.

Available values are

- Disabled
- Enabled

Use

The external burst mode feature is used to drive the burst mode through an external signal. The feature enables / disables the external BM comparator active on the LLC_AUX pin with a threshold of 0.9 V.

Two types of the external burst mode can be defined

- Pure external burst mode: only the external BM comparator manages the burst mode entering / exiting
- Hybrid external burst mode: if the external BM comparator is high, the system stays out of the burst mode while if the external BM comparator is low, the burst mode entering / exiting is managed by the LLC_FB pin parameters.

The selection between the pure and hybrid is done with the “LLC_FB burst entering thr” parameter.

In both external burst mode cases, the burst switching activity is managed by the LLC_FB pin and the burst comparator.

3.5.2 BM enter for minimum TS

Size: 1 bit

Enables / disables the burst mode entering request if the minimum time shift is reached.

Available values are

- Disabled
- Enabled

Use

This feature can be useful in case the resonant tank is not able to regulate the output at light/no loads even at the minimum time shift value. If the time shift has reached its minimum value, the feature allows entering the burst mode if the condition is asserted for at least 480 µs, in addition to the “Burst entering digital filtering”. This will prevent output overshoot. For this reason, the feature will not wait for the “No-burst window width” time before entering burst mode.

3.5.3 Burst entering digital filtering

Size: 2 bits

Sets the digital filtering to enter the burst mode.

Available values are

- 270 µs
- 510 µs
- 750 µs
- 990 µs

To enter burst mode, the burst request (external or LLC_FB pin driven) must be asserted for the time defined by this parameter.

This allows reject noise on LLC_FB and LLC_AUX pins.

3.5.4 LLC_FB burst entering thr

Size: 6 bits

Sets the voltage threshold to enter the burst mode.

Available values are

Voltage on LLC_FB pin	“LLC low frequency range” = disabled	“LLC low frequency range” = enabled
• 268.6 mV	• 350 ns	• 700 ns
• 278.3 mV	• 383.3 ns	• 766.7 ns
• 288.1 mV	• 416.7 ns	• 833.3 ns
• 297.9 mV	• 450 ns	• 900 ns
• 307.6 mV	• 483.3 ns	• 966.7 ns

- 317.4 mV
- 327.1 mV
- 336.9 mV
- 346.7 mV
- 356.4 mV
- 366.2 mV
- 376.0 mV
- 385.7 mV
- 395.5 mV
- 405.3 mV
- 415.0 mV
- 424.8 mV
- 434.6 mV
- 444.3 mV
- 454.1 mV
- 463.9 mV
- 473.6 mV
- 483.4 mV
- 493.2 mV
- 502.9 mV
- 512.7 mV
- 522.5 mV
- 532.2 mV
- 542.0 mV
- 551.8 mV
- 561.5 mV
- 571.3 mV
- 581.1 mV
- 590.8 mV
- 600.6 mV
- 610.4 mV
- 620.1 mV
- 629.9 mV
- 639.6 mV
- 649.4 mV
- 516.7 ns
- 550 ns
- 583.3 ns
- 616.7 ns
- 650 ns
- 683.3 ns
- 716.7 ns
- 750 ns
- 783.3 ns
- 816.7 ns
- 850 ns
- 883.3 ns
- 916.7 ns
- 950 ns
- 983.3 ns
- 1017 ns
- 1050 ns
- 1083 ns
- 1117 ns
- 1150 ns
- 1183 ns
- 1217 ns
- 1250 ns
- 1283 ns
- 1317 ns
- 1350 ns
- 1383 ns
- 1417 ns
- 1450 ns
- 1483 ns
- 1517 ns
- 1550 ns
- 1583 ns
- 1617 ns
- 1650 ns
- 1033 ns
- 1100 ns
- 1167 ns
- 1233 ns
- 1300 ns
- 1367 ns
- 1433 ns
- 1500 ns
- 1567 ns
- 1633 ns
- 1700 ns
- 1767 ns
- 1833 ns
- 1900 ns
- 1967 ns
- 2033 ns
- 2100 ns
- 2167 ns
- 2233 ns
- 2300 ns
- 2367 ns
- 2433 ns
- 2500 ns
- 2567 ns
- 2633 ns
- 2700 ns
- 2767 ns
- 2833 ns
- 2900 ns
- 2967 ns
- 3033 ns
- 3100 ns
- 3167 ns
- 3233 ns
- 3300 ns

- 659.2 mV
- 668.9 mV
- 678.7 mV
- 688.5 mV
- 698.2 mV
- 708.0 mV
- 717.8 mV
- 727.5 mV
- 737.3 mV
- 747.1 mV
- 756.8 mV
- 766.6 mV
- 776.4 mV
- 786.1 mV
- 795.9 mV
- 805.7 mV
- 815.4 mV
- 825.2 mV
- 835.0 mV
- 844.7 mV
- 854.5 mV
- 864.3 mV
- 874.0 mV
- 883.8 mV
- 1683 ns
- 1717 ns
- 1750 ns
- 1783 ns
- 1817 ns
- 1850 ns
- 1883 ns
- 1917 ns
- 1950 ns
- 1983 ns
- 2017 ns
- 2050 ns
- 2083 ns
- 2117 ns
- 2150 ns
- 2183 ns
- 2217 ns
- 2250 ns
- 2283 ns
- 2317 ns
- 2350 ns
- 2383 ns
- 2417 ns
- 2450 ns
- 3367 ns
- 3433 ns
- 3500 ns
- 3567 ns
- 3633 ns
- 3700 ns
- 3767 ns
- 3833 ns
- 3900 ns
- 3967 ns
- 4033 ns
- 4100 ns
- 4167 ns
- 4233 ns
- 4300 ns
- 4367 ns
- 4433 ns
- 4500 ns
- 4567 ns
- 4633 ns
- 4700 ns
- 4767 ns
- 4833 ns
- 4900 ns

Use

When the external burst mode is disabled, the parameter sets the voltage threshold at the LLC_FB pin to enter the burst mode. In order to correctly select this parameter, set it first to the minimum level, then adjust the board to work at the required load to enter burst mode. Measure the voltage at the LLC_FB pin and select the closer “LLC_FB burst entering thr” value, from the values on the left.

If the external burst mode is enabled and the minimum value (268.6 mV) is selected, the pure external burst mode is activated: only the LLC_AUX Ext. The BM comparator manages the burst mode entering / exiting.

If the external burst mode is enabled and the minimum value (268.6 mV) is NOT selected, the hybrid external burst mode is activated: when the LLC_AUX Ext. BM comparator is high, the system stays out of burst mode; when the LLC_AUX Ext. BM comparator is low, burst mode entering / exiting is managed by the voltage at the “LLC_FB burst entering thr”, as the standard burst mode.

Note: In order to enter the burst mode driven by LLC_FB pin voltage, the equivalent time shift (on the right of the voltage threshold and depending on "LLC low frequency range") must be higher than the "Minimum time shift", otherwise the system will not enter the burst mode for LLC_FB.

3.5.5 LLC_FB burst wake-up thr

Size: 2 bits

Sets the threshold for the burst wake-up comparator (connected to the LLC_FB pin).

Available values are

Voltage on LLC_FB pin	"LLC low frequency range" = disabled	"LLC low frequency range" = enabled
• 0.75 V	• 2 µs	• 4 µs
• 1 V	• 2.85 µs	• 5.7 µs
• 1.25 V	• 3.7 µs	• 7.4 µs

During the burst mode, the STNRG011 restarts switching and performs one burst when the LLC_FB pin goes over this threshold.

Use

The wake-up threshold on the left has to be set higher than the "LLC_FB burst entering thr".

After wake-up, the time shift follows the LLC_FB if it is higher than the "Min TS in burst mode". On the right of the voltage threshold the equivalent time shift of that voltage is shown and it depends on the "LLC low frequency range" parameter.

The most suitable values are usually 0.75 V or 1 V.

3.5.6 LLC_FB burst wake-up hyst

Size: 1 bit

Sets the hysteresis for the burst wake-up comparator (connected to LLC_FB).

Available values are

- 5 mV
- 10 mV

Use

The best choice is usually 5 mV.

3.5.7 Min TS in burst mode

Size: 5 bits

Sets the minimum time shift value during the burst mode.

Available values are:

“LLC low frequency range” = disabled

- 1 µs
- 1.13 µs
- 1.27 µs
- 1.4 µs
- 1.53 µs
- 1.67 µs
- 1.8 µs
- 1.93 µs
- 2.07 µs
- 2.2 µs
- 2.33 µs
- 2.47 µs
- 2.6 µs
- 2.73 µs
- 2.87 µs
- 3 µs
- 3.13 µs
- 3.27 µs
- 3.4 µs
- 3.53 µs
- 3.67 µs
- 3.8 µs
- 3.93 µs
- 4.07 µs
- 4.2 µs
- 4.33 µs
- 4.47 µs
- 4.6 µs
- 4.73 µs
- 4.87 µs
- 5 µs
- 5.13 µs

“LLC low frequency range” = enabled

- 4.2 µs
- 4.33 µs
- 4.47 µs
- 4.6 µs
- 4.73 µs
- 4.87 µs
- 5 µs
- 5.13 µs
- 5.27 µs
- 5.4 µs
- 5.53 µs
- 5.67 µs
- 5.8 µs
- 5.93 µs
- 6.07 µs
- 6.2 µs
- 6.33 µs
- 6.47 µs
- 6.6 µs
- 6.73 µs
- 6.87 µs
- 7 µs
- 7.13 µs
- 7.27 µs
- 7.4 µs
- 7.53 µs
- 7.67 µs
- 7.8 µs
- 7.93 µs
- 8.07 µs
- 8.2 µs
- 8.33 µs

Setting the time shift value (and therefore the switching frequency), is it possible to fix how much energy is transferred to the output by one burst sequence.

The parameter sets the time shift of the first low-side and high-side gate drives of the burst sequence. Please note that the time shift value also works as a low limit: if the feedback should ask for an in increased time shift, the system will follow the feedback request. This is very useful during load transient, in order to have a prompt response in case of large load increases. Consider also the equivalent time shift of the “LLC_FB burst wake-up thr”: if this is higher, the time shift will increase after the first pulses.

The time shift value depends on the “LLC low frequency range” parameter.

Use

The suggestion is to use a value that provides good energy transfer, in order to have efficient operation.

For example, in systems designed to work at resonance, the time-shift during the burst mode can be selected to work at resonance or a little below it.

3.5.8 Min number of burst pulses

Size: 4 bits

Sets the minimum number of switching cycles inside one burst sequence.

Available values are

- 2
- 3
- 4
- 5
- 6
- 7
- 8
- 9
- 10
- 11
- 12
- 13
- 14
- 15
- 16
- 17

This parameter defines the minimum number of switching cycles composing a single burst. This condition is reached at light loads.

Use

The minimum number of switching cycles is usually selected in order not to have a long distance between two bursts at the no-load and therefore to avoid the saturation of the optocoupler output transistor.

3.5.9 Max number of burst pulses (delta)

Size: 4 bits

Sets the maximum number of switching cycles inside one burst sequence.

Available values are

- 0
- 1
- 2
- 3
- 4
- 5
- 6
- 7
- 8
- 9
- 10
- 11
- 12
- 13
- 14
- 15

This parameter defines the maximum number of switching cycles composing a single burst. This condition is reached at medium/high loads (in the burst mode).

Please note that this parameter is defined as a positive delta with respect to the “Min number of burst pulses” parameter, so the total maximum number of burst pulses is

Equation 16

$$\text{"Max number of burst pulses"} = \text{"Min number of burst pulses"} + \text{"Max number of burst pulses (delta)"}$$

Use

The maximum number of switching cycles is usually selected in order to stay within the maximum output voltage ripple allowed.

If the designer wants a fixed number of switching cycles, it could be done by setting the parameter to 0.

3.5.10 Min time between burst seq

Size: 2 bits

Sets the minimum time between two burst sequences to increase the number of switching cycles.

Available values are

- 5.93 ms
- 10.2 ms

- 14.47 ms
- 18.73 ms

During the burst mode, if the load is increased and the distance between two bursts reaches the value defined by this parameter, the system increases the number of switching cycles by one.

The upper limit for the switching cycles is defined by the “Max number of burst pulses (delta)” parameter.

3.5.11 Max time between burst seq (delta)

Size: 2 bits

Sets the maximum time between two burst sequences to decrease the number of switching cycles.

Available values are

- 2.83 ms
- 4.97 ms
- 7.1 ms
- 9.23 ms

During the burst mode, if the load is decreased and the distance between two bursts reaches the value defined by this parameter, the system decreases the number of switching cycles by one. The lower limit for the switching cycles is defined by the “Min number of burst pulses” parameter.

Please note that this parameter is defined as a positive delta with respect to the “Min time between burst seq” parameter, so the total maximum time between burst sequences is

Equation 17

$$\text{"Max time between burst seq"} = \text{"Min time between burst seq"} + \text{"Max time between burst seq (delta)"}$$

3.5.12 Minimum period to exit burst

Size: 4 bits

Sets the minimum time between two consecutive burst sequences to exit the burst mode.

Available values are

- 66.7 µs
- 100 µs
- 133 µs
- 167 µs
- 200 µs
- 233 µs
- 267 µs
- 300 µs
- 333 µs
- 367 µs

- 400 µs
- 433 µs
- 467 µs
- 500 µs
- 533 µs
- 567 µs

When the system is in the burst mode and the load increases, the time between two burst sequences is reduced. If the time distance between two consecutive burst sequences reaches the time threshold set by this parameter, the system will exit the burst mode.

Therefore, the lower the value for this parameter the higher the load for exiting the burst mode.

Please note that this mechanism is not used with the pure external burst mode.

Use

To tune this parameter, initially set it to a very low value. Bring the system in the burst mode and then increase the load to the desired burst exit point. Measure the distance between two consecutive burst sequences and program that value in the parameter.

3.5.13 No-burst window width

Size: 1 bit

Sets the minimum time that avoids burst re-entering.

Available values are

- 90 µs
- 7.5 ms

If the system exits the burst mode, the burst mode re-entering is forbidden for a minimum time defined to this parameter.

Use

The suggested value is 7.5 ms to avoid burst mode re-entering at low load in case the feedback voltage undershoot at the burst mode exit.

Please note that the no-burst window does not apply for the “BM enter for minimum TS”.

3.6 Comparators setting

3.6.1 Surge comp digital filtering

Size: 1 bit

Sets the digital filtering for the line surge comparator.

Available values are

- 100 ns
- 500 ns

3.6.2 PFC CS comp digital filtering

Size: 2 bits

Sets the digital filtering for the PFC CS comparator for the ReCOT functionality (THD improver).

Available values are

- No filtering
- 16.7 ns
- 33.3 ns
- 50 ns

3.6.3 PFC CS comp digital hysteresis

Size: 1 bit

Sets the PFC CS comparator hysteresis for the ReCOT functionality (THD improver).

Available values are

- 5 mV
- 10 mV

Use

For better operation of the comparator (that has to work with small input signals), it is suggested to use 5 mV.

3.6.4 PFC OC2 comp digital filtering

Size: 2 bits

Sets the digital filtering for the PFC OC2 comparator.

Available values are

- No filtering
- 133.3 ns
- 266.7 ns
- 400 ns

3.6.5 PFC OC1 comp digital filtering (delta)

Size: 1 bit

Sets the digital filtering for the PFC OC1 comparator.

Available values are

- 33.3 ns
- 166.7 ns

Use

The digital filter for the PFC OCP1 comparator is defined as a positive delta with respect to the “PFC OC2 comp digital filtering” parameter:

Equation 18

$$\text{"PFC OC1 comp digital fitering"} = \text{"PFC OC2 comp digital fitering"} + \text{"PFC OC1 comp digital fitering (delta)"}$$

The digital filter in the OC1 comparator has to be longer than the one in the OCP2 because otherwise OC1 detection and management could mask the OC2 events.

3.6.6 PFC ZCD comp digital filtering

Size: 1 bit

Sets the digital filtering for the PFC ZCD comparator.

Available values are

- 33.3 ns
- 66.7 ns

3.6.7 PFC ZCD comp falling thr

Size: 2 bits

Sets the falling threshold for the PFC ZCD comparator (TH_F).

Available values are

- 0 mV
- 50 mV
- 100 mV
- 200 mV

3.6.8 PFC ZCD comp rising thr

Size: 2 bits

Sets the rising threshold for the PFC ZCD comparator (TH_R).

Available values are

- 210 mV
- 110 mV (N/A with TH_F = 200 mV)
- 310 mV
- TH_F + 10 mV

Use

The rising threshold of the PFC ZCD comparator must be higher than the falling one. For this reason, the selection TH_F = 200 mV and TH_R = 110 mV is not allowed.

The last selection sets the rising threshold 10 mV higher with respect to any selection of the falling threshold.

3.6.9 PFC HW OVP comp digital filtering

Size: 2 bits

Sets the digital filtering for the PFC HW OVP comparator.

Available values are

- 4.25 µs
- 2.12 µs
- 1.05 µs
- 516.7 µs

3.6.10 LLC OLP comp digital filtering

Size: 2 bits

Sets the digital filtering for the LLC OC1 comparator, for the OLP functionality.

Available values are

- No filtering
- 16.7 ns
- 33.3 ns
- 50 ns

Use

The value 16.7 ns can be used as the starting value.

In noisy applications, it could be needed to increase the filtering.

3.6.11 LLC OC2 digital filtering

Size: 2 bits

Sets the digital filtering for the LLC OC2 comparator.

Available values are

- 133.3 ns
- 166.7 ns
- 200 ns
- 233.3 ns

3.6.12 LLC ZCD comp digital filtering

Size: 3 bits

Sets the digital filtering for the LLC ZCD comparator.

Available values are

- 50 ns
- 116.7 ns
- 183.3 ns
- 250 ns

- 316.7 ns
- 383.3 ns
- 450 ns
- 516.7 ns

Use

The filtering has to be chosen considering the trade-off between the noise rejection and maximum operating frequency.

3.6.13 LLC ZCD comp hysteresis

Size: 1 bit

Sets the LLC ZCD comparator hysteresis.

Available values are

- 5 mV
- 10 mV

Use

The comparator's hysteresis has to be chosen considering the trade-off between the noise rejection and LLC_CS signal at the minimum time shift.

3.6.14 LLC OVP comp digital filtering

Size: 2 bits

Sets the digital filtering for the LLC OVP comparator.

Available values are

- 4.25 µs
- 2.12 µs
- 1.05 µs
- 516.7 ns

4 Revision history

Table 1. Document revision history

Date	Revision	Changes
20-Feb-2018	1	Initial release.

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