Evaluation Board User Guide
UG-189

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Evaluation Board for the 2 A/3 A, 20 V, Nonsynchronous Step-Down Regulators

FEATURES

Wide input voltage range: 3.0 V to 20 V
Maximum load current
- **2 A for ADP2302**
- **3 A for ADP2303**

±1.5% output accuracy over temperature
Output voltage down to 0.8 V
700 kHz switching frequency
Current-mode control architecture
Automatic PFM/PWM mode
Precision enable pin with hysteresis
Integrated high-side MOSFET
Integrated bootstrap diode
Internal compensation and soft start
Power-good output
Undervoltage lockout (UVLO)
Overcurrent protection (OCP)
Thermal shutdown (TSD)
8-lead SOIC package with exposed paddle

GENERAL DESCRIPTION

The ADP2302/ADP2303 are 2 A/3 A, 20 V, nonsynchronous step-down, dc-to-dc regulators with an integrated power MOSFET in a SOIC package with an exposed paddle. The ADP2302/ ADP2303 evaluation boards are complete buck regulator solutions that allow users to evaluate the performance of the regulators.

The ADP2302/ADP2303 integrated soft-start circuitry prevents inrush current at power-up. The power-good output indicates that the output voltage is regulated within tolerance, and it can be used to sequence devices that have an enable input. The precision enable feature allows the part to be easily sequenced from external supplies. Other key features include undervoltage lockout (UVLO), output overvoltage protection (OVP), thermal shutdown (TSD), and overcurrent protection (OCP). Full details on the ADP2302/ADP2303 are provided in the ADP2302/ADP2303 data sheet available from Analog Devices, Inc., which should be consulted in conjunction with this user guide.

ADP2302/ADP2303 EVALUATION BOARD

09315-001

Figure 1. ADP2302/ADP2303 Evaluation Board

TABLE OF CONTENTS

REVISION HISTORY

8/10—Revision 0: Initial Version

USING THE EVALUATION BOARD

The ADP2302/ADP2303 evaluation boards are fully assembled and tested. Before applying power to the evaluation board, follow the procedures in this section.

JUMPER J5 (ENABLE)

Jumper J5 enables/disables the ADP2302/ADP2303. Set J5 to EN HIGH to enable the device, and set J5 to EN LOW to disable the device.

JUMPER J8 (PGOOD)

Jumper J8 connects/disconnects the power-good signal to VIN. To pull the power good (PGOOD) pin up, connect J8 to the input voltage through a 100 kΩ resistor. Disconnect J8 to leave PGOOD open.

INPUT POWER SOURCE

If the input power source includes a current meter, use that meter to monitor the input current. Connect the positive terminal of the power source to J2 (VIN) on the evaluation board and the negative terminal of the power source to J4 (GND) of the evaluation board.

If the power source does not include a current meter, connect a current meter in series with the input source voltage. Connect the positive lead (+) of the power source to the positive (+) ammeter terminal, the negative lead (−) of the power source to J4 (GND), and the negative lead (−) of the ammeter to J2 (VIN).

OUTPUT LOAD

Make sure that the board is turned off before connecting the load. Connect an electronic load or resistor to set the load current. If the load includes an ammeter, or if the current is not measured, connect the load directly to the evaluation board, with the positive (+) load connection to J1 (VOUT) and the negative (−) load connection to J3 (GND).

If an ammeter is used, connect it in series with the load. Connect the positive (+) ammeter terminal to J1 (VOUT), the negative (−) ammeter terminal to the positive (+) load terminal, and the negative (−) load terminal to J3 (GND).

INPUT AND OUTPUT VOLTMETER

Measure the input and output voltages with voltmeters. Make sure that the voltmeters are connected to the appropriate evaluation board terminals and not to the load or power source. If the voltmeters are not connected directly to the evaluation board, the measured voltages are incorrect due to the voltage drop across the leads and/or connections between the evaluation board, the power source, and/or the load.

To measure the input voltage, connect the positive terminal of the voltmeter to J2 (VIN) and the negative terminal to J4 (GND). Likewise, to measure the output voltage, connect the positive terminal of the voltmeter to J1 (VOUT) and the negative terminal to J3 (GND).

TURNING ON THE EVALUATION BOARD

Once the power source and load are connected to the evaluation board, it can be powered for operation.

Perform the following steps:

1. Ensure that the power source voltage is >V_{OUT} + 2.1 V and <20 V.
2. Ensure that J5 (EN) is high and monitor the output voltage.

If the load is not already enabled, enable the load, check that the load is drawing the proper current, and verify that the output voltage maintains voltage regulation.

MEASURING EVALUATION BOARD PERFORMANCE

Measuring the Switching Waveform

To observe the switching waveform with an oscilloscope, place the oscilloscope probe tip at Test Point J7 (SW) with the probe ground at GND. Set the scope to dc with the appropriate voltage and time divisions. The switching waveform should alternate between 0 V and approximate the input voltage.

Measuring Load Regulation

Load regulation should be tested by increasing the load at the output and by observing the change in output voltage. To minimize voltage drop, it is recommended to use short low resistance wires.

Measuring Line Regulation

Vary the input voltage and examine the change in the output voltage at a fixed output current.

Measuring Efficiency

The efficiency, η, is measured by comparing the input power with the output power.

$$\eta = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}}$$

Measure the input and output voltages as close as possible to the input and output capacitors to reduce the effect of voltage drop.

Measuring Inductor Current

The inductor current can be measured by removing one end of the inductor from its pad and connecting a current loop in series. A current probe can be connected to this wire.

Measuring Output Voltage Ripple

To observe the output voltage ripple, place an oscilloscope probe across the output capacitor (C3) with the probe ground lead placed at the negative (–) capacitor terminal and the probe tip placed at the positive (+) capacitor terminal. Set the oscilloscope to ac, 10 mV/division, 2 μs/division time base, and 20 MHz bandwidth.

A standard oscilloscope probe has a long wire ground clip. For high frequency measurements, this ground clip picks up high frequency noise and injects it into the measured output ripple. Figure 2 shows an easy way to measure the output ripple properly. It requires removing the oscilloscope probe sheath and wrapping a nonshielded wire around the oscilloscope probe. By keeping the ground length of the oscilloscope probe as short as possible, true ripple can be measured.

Output Voltage Change

The ADP2302/ADP2303 evaluation board output is preset to 3.3 V; however, the output voltage can be adjusted using the following equation:

$$V_{OUT} = 0.8\ V \times \left(\frac{R5 + R3}{R5}\right)$$

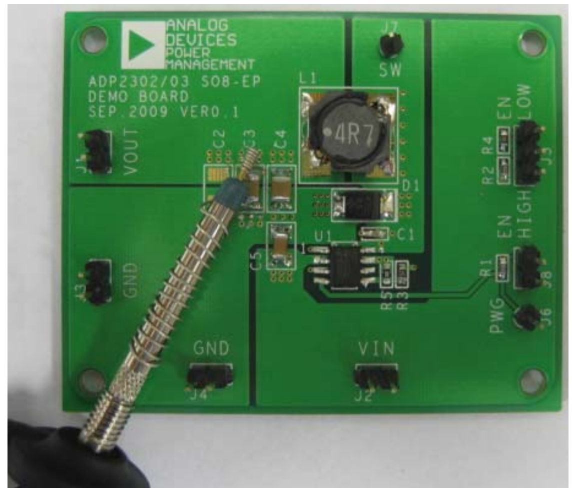

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Figure 2. Measuring Output Voltage Ripple

TYPICAL PERFORMANCE CHARACTERISTICS

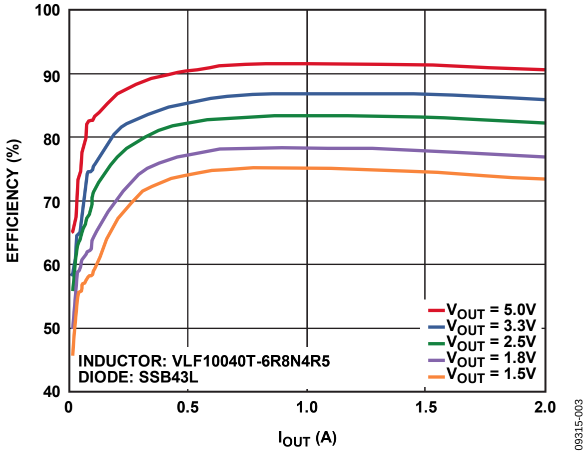

Figure 3. ADP2302 Efficiency, V_{IN} = 12 V

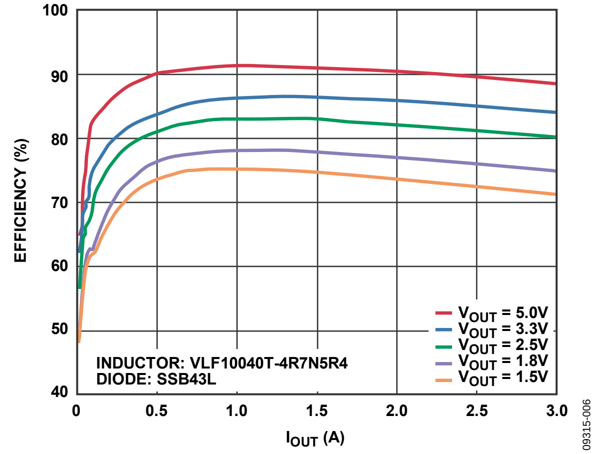

Figure 6. ADP2303 Efficiency, V_{IN} = 12 V

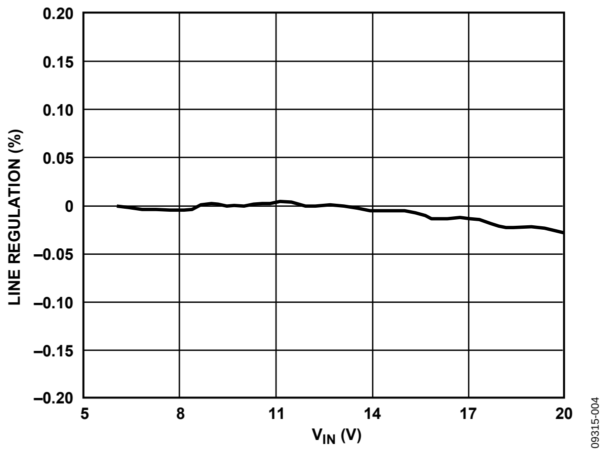

Figure 4. ADP2302 Line Regulation, V_{OUT} = 3.3 V, I_{OUT} = 2 A

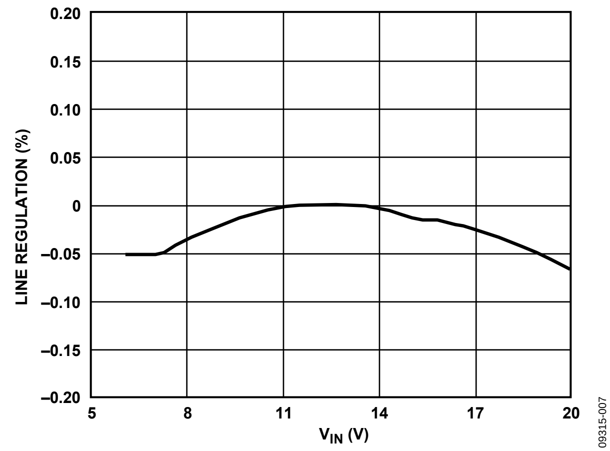

Figure 7. ADP2303 Line Regulation, V_{OUT} = 3.3 V, I_{OUT} = 3 A

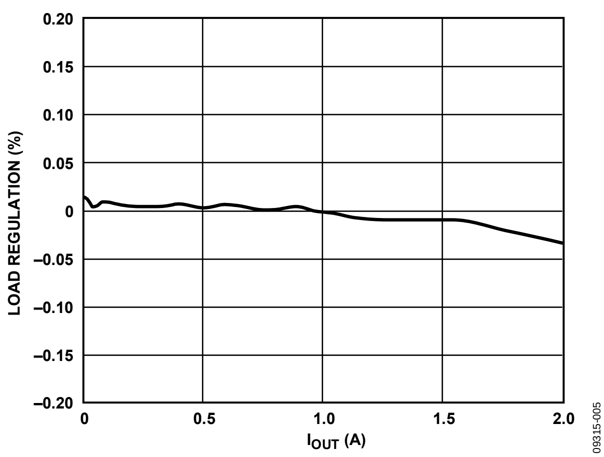

Figure 5. ADP2302 Load Regulation, V_{OUT} = 3.3 V, V_{IN} = 12 V

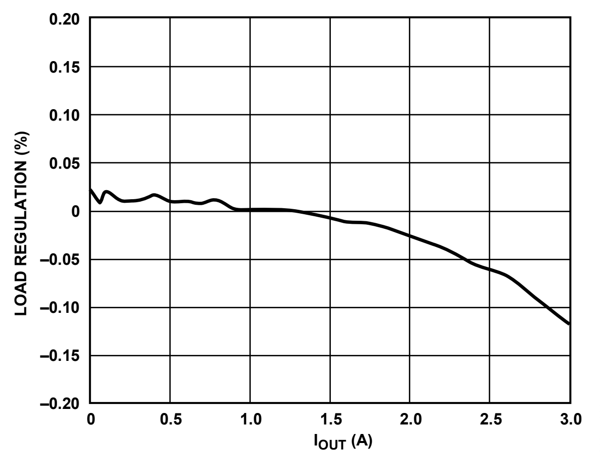

Figure 8. ADP2303 Load Regulation, V_{OUT} = 3.3 V, V_{IN} = 12 V

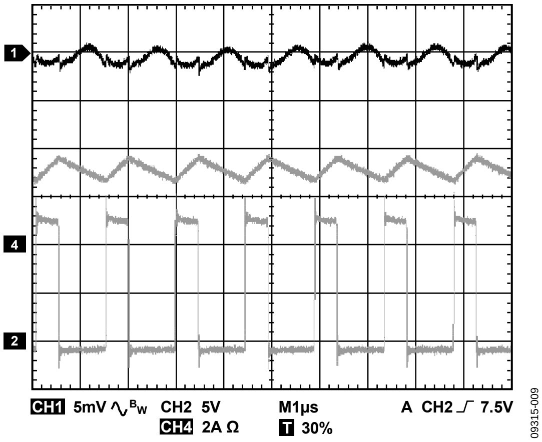

Figure 9. Continuous Conduction Mode (CCM)

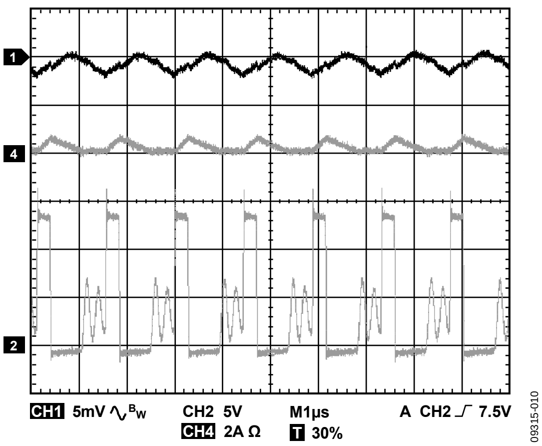

Figure 10. Discontinuous Conduction Mode (DCM)

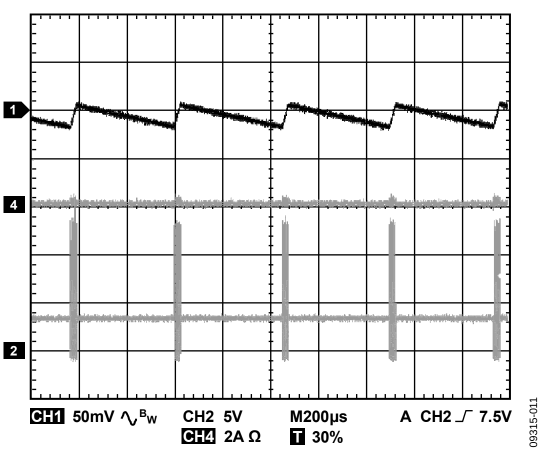

Figure 11. Power Saving Mode

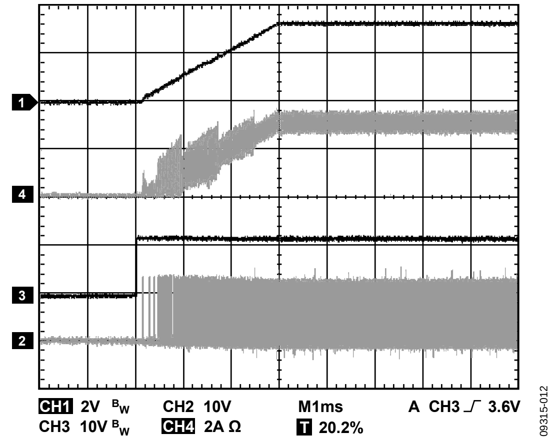

Figure 12. Soft Start with Full Load

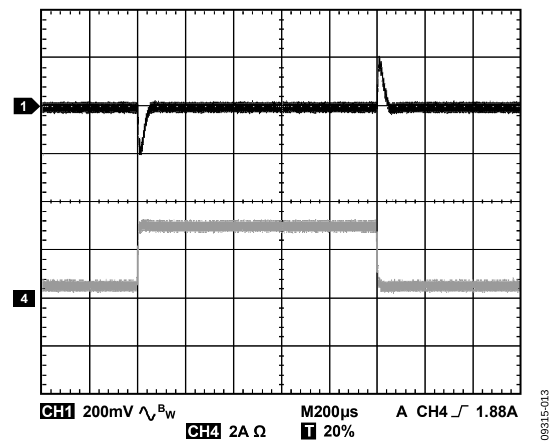

Figure 13. ADP2303 Load Transient, 0.5 A to 3.0 A, V_{OUT} = 3.3 V, V_{IN} = 12 V, L = 4.7 µH, C_{OUT} = 2 × 47 µF

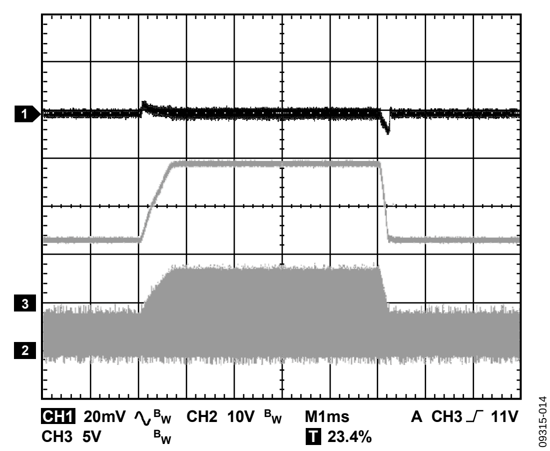

Figure 14. ADP2303 Line Transient, 7 V to 15 V, V_{OUT} = 3.3 V, I_{OUT} = 3 A, L = 4.7 µH, C_{OUT} = 2 × 47 µF

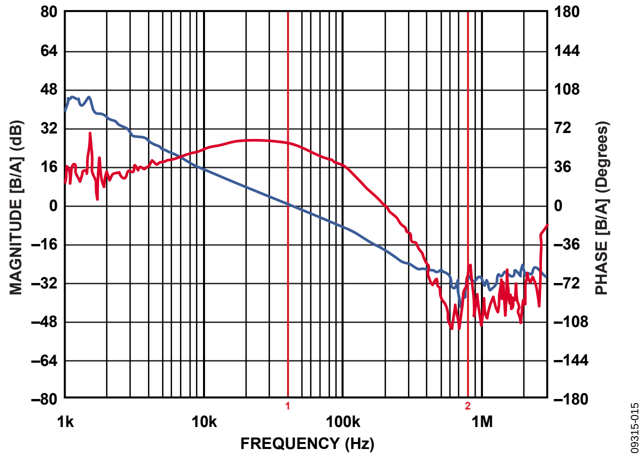

Figure 15. ADP2302 Bode Plot, V_{OUT} = 3.3 V, V_{IN} = 12 V, L = 6.8 μH, C_{OUT} = 2 × 22 μF

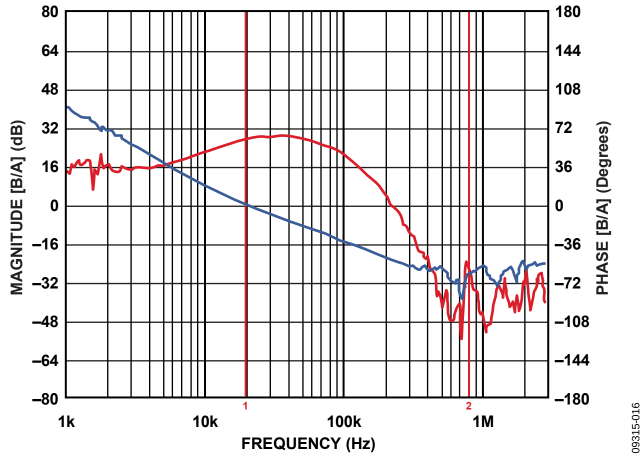

Figure 16. ADP2303 Bode Plot, V_{OUT} = 3.3 V, V_{IN} = 12 V L = 4.7 μH, C_{OUT} = 2 × 47 μF

DEMONSTRATION BOARD SCHEMATICS AND BILL OF MATERIALS

ADP2302 SCHEMATIC AND BILL OF MATERIALS

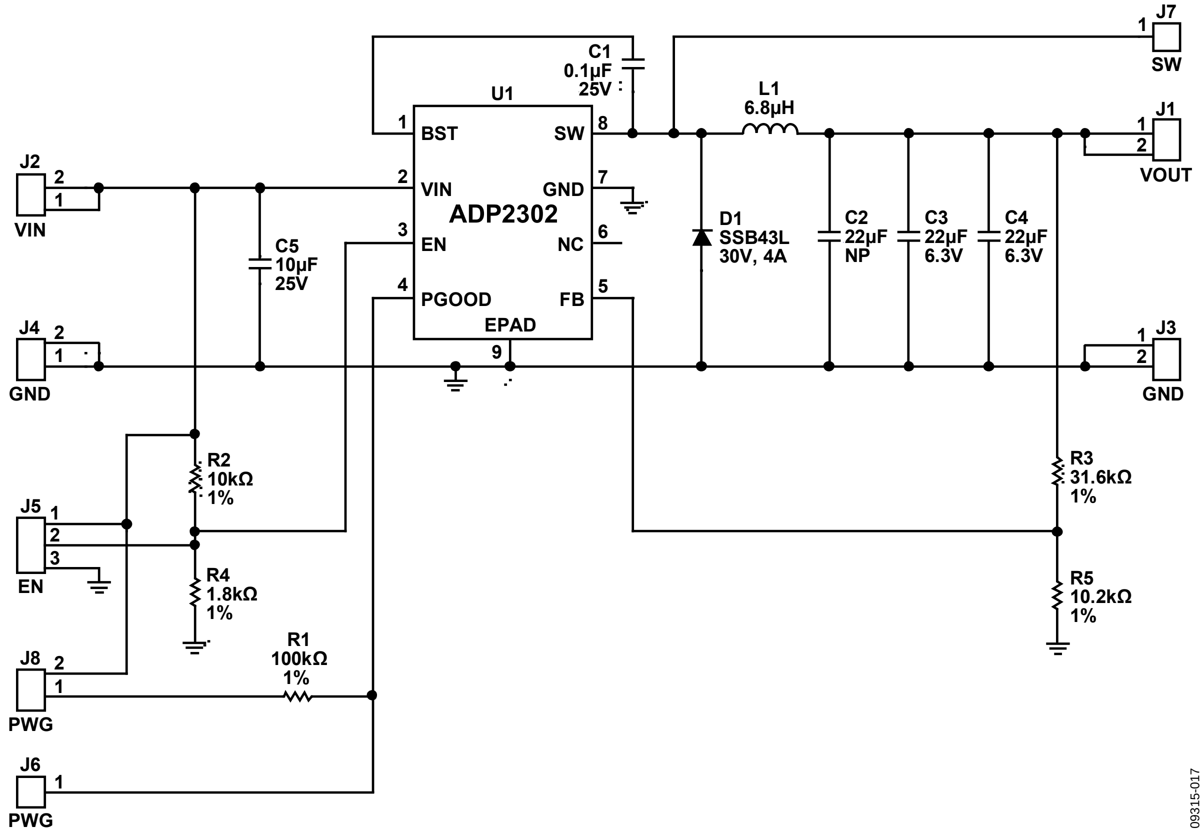

Figure 17. Evaluation Board Schematic for ADP2302

Table 1. Bill of Materials for ADP2302 Evaluation Board

Qty	Reference Designator	Part Number	Type	Description	PCB Footprint	Vendor
1	C1	GRM188R71E104KA01	Capacitor	0.1 µF, 25 V	C0603	Murata
1	C2	Optional	Capacitor	Optional	C1206	Murata
1	C3	GRM31CR60J226KE19	Capacitor	22 µF, 6.3 V	C1206	Murata
1	C4	GRM31CR60J226KE19	Capacitor	22 µF, 6.3 V	C1206	Murata
1	C5	GRM31CR61E106KA12	Capacitor	10 µF, 25 V	C1206	Murata
1	D1	SSB43L	Diode	30 V, 4 A	SMB_SD	Vishay Dale
1	L1	VLF10040-6R8N5R4	Inductor	L = 6.8 µH, I_{RAT} = 4.6 A, DCR = 19.8 mΩ	DS104LC	TDK
1	R1	CRCW0603100KFKEA	Resistor	100 kΩ, 1%	R0603	Vishay Dale
1	R2	CRCW060310K0FKEA	Resistor	10 kΩ, 1%	R0603	Vishay Dale
1	R3	CRCW060331K6FKEA	Resistor	31.6 kΩ, 1%	R0603	Vishay Dale
1	R4	CRCW06031K80FKEA	Resistor	1.8 kΩ, 1%	R0603	Vishay Dale
1	R5	CRCW060310K2FKEA	Resistor	10.2 kΩ, 1%	R0603	Vishay Dale
1	U1	ADP2302	IC	2 A, 700 kHz nonsynchronous step-down dc-dc switching regulator	8-lead, SOIC with exposed paddle	Analog Devices
2	J6, J7	M20-9990245	Test point	2.54 mm pitch SIL vertical PC tail pin header, 6.1 mm mating pin height, tin	SIP1	Harwin
5	J1, J2, J3, J4, J8	M20-9990245	Connector	2.54 mm pitch SIL vertical PC tail pin header, 6.1 mm mating pin height, tin, 2-way	SIP2	Harwin
1	J5	M20-9990346	Jumper	0.1-inch header, 3-way	SIP3	Harwin

ADP2303 SCHEMATIC AND BILL OF MATERIALS

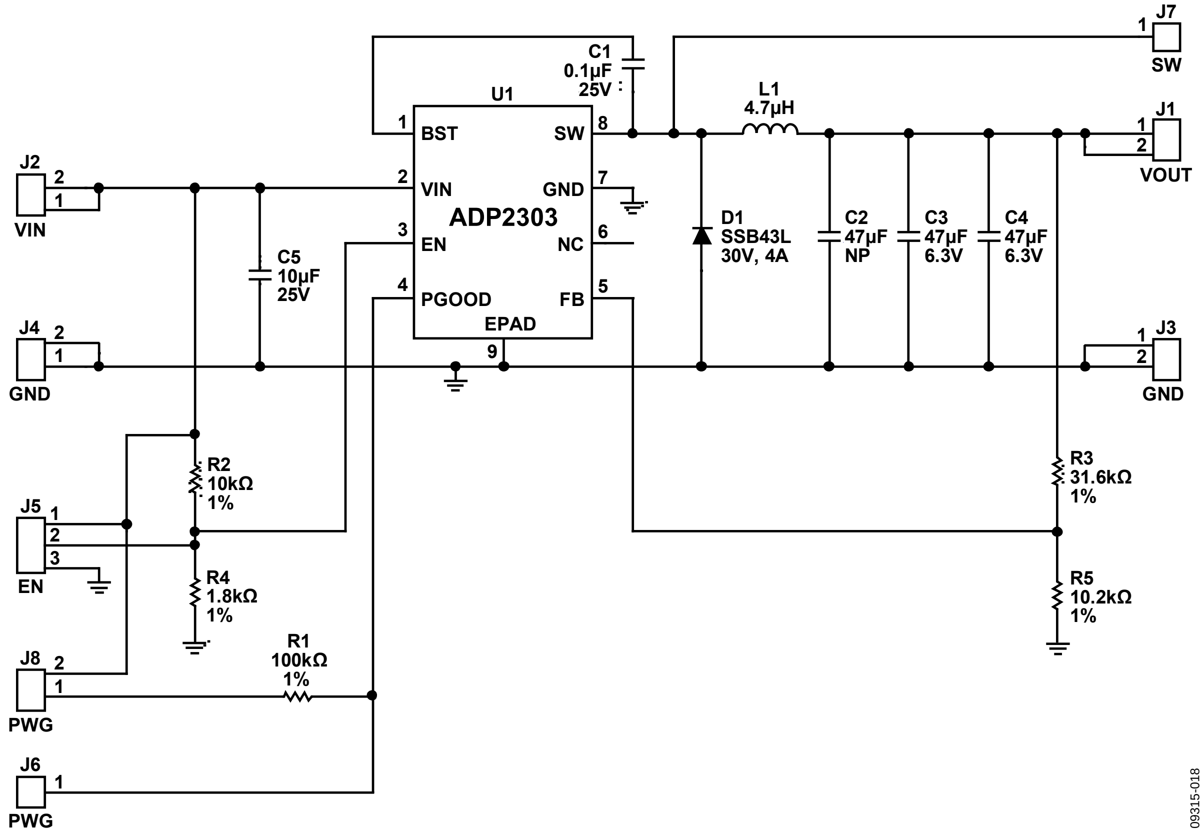

Figure 18. Evaluation Board Schematic for ADP2303

Table 2. Bill of Materials for ADP2303 Evaluation Board

Qty	Reference Designator	Part Number	Type	Description	PCB Footprint	Vendor
1	C1	GRM188R71E104KA01	Capacitor	0.1 µF, 25 V	C0603	Murata
1	C2	Optional	Capacitor	Optional	C1210	Murata
1	C3	GRM32ER60J476ME20	Capacitor	47 µF, 6.3 V	C1210	Murata
1	C4	GRM32ER60J476ME20	Capacitor	47 µF, 6.3 V	C1210	Murata
1	C5	GRM31CR61E106KA12	Capacitor	10 µF, 25 V	C1206	Murata
1	D1	SSB43L	Diode	30 V, 4 A	SMB_SD	Vishay Dale
1	L1	VLF10040-4R7N5R4	Inductor	L = 4.7 µH, I_{RAT} = 5.4 A, DCR = 12.7 mΩ	DS104LC	TDK
1	R1	CRCW0603100KFKEA	Resistor	100 kΩ, 1%	R0603	Vishay Dale
1	R2	CRCW060310K0FKEA	Resistor	10 kΩ, 1%	R0603	Vishay Dale
1	R3	CRCW060331K6FKEA	Resistor	31.6 kΩ, 1%	R0603	Vishay Dale
1	R4	CRCW06031K80FKEA	Resistor	1.8 kΩ, 1%	R0603	Vishay Dale
1	R5	CRCW060310K2FKEA	Resistor	10.2 kΩ, 1%	R0603	Vishay Dale
1	U1	ADP2303	IC	3 A, 700 kHz nonsynchronous step-down dc-dc switching regulator	8-lead, SOIC with exposed paddle	Analog Devices
2	J6, J7	M20-9990245	Test point	2.54 mm pitch SIL vertical PC tail pin header, 6.1 mm mating pin height, tin	SIP1	Harwin
5	J1, J2, J3, J4, J8	M20-9990245	Connector	2.54 mm pitch SIL vertical PC tail pin header, 6.1 mm mating pin height, tin, 2-way	SIP2	Harwin
1	J5	M20-9990346	Jumper	0.1-inch header, 3-way	SIP3	Harwin

DEMONSTRATION BOARD LAYOUT

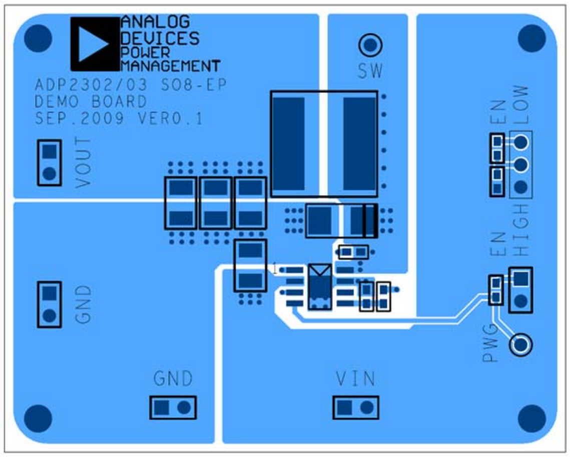

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Figure 19. Demonstration Board Layer1, Component Side

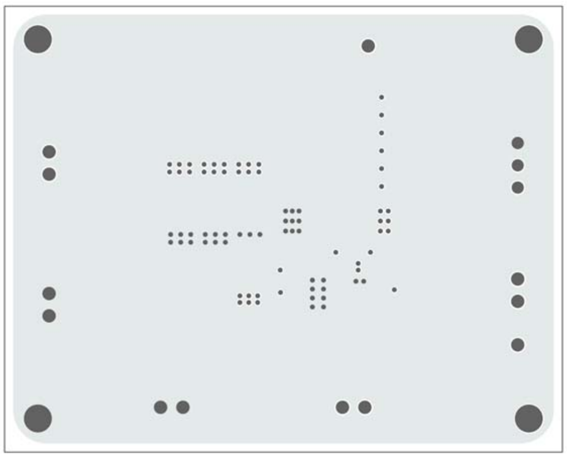

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Figure 20. Demonstration Board Layer 2, Ground Plane

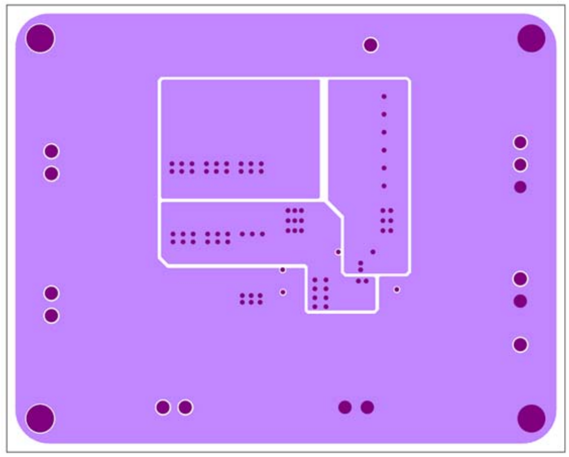

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Figure 21. Demonstration Board Layer3, Power Plane

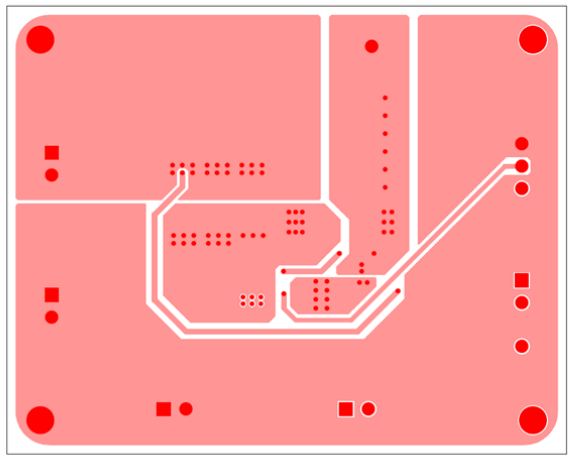

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Figure 22. Demonstration Board Layer 4, Bottom Side

NOTES

NOTES

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Legal Terms and Conditions

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