Ordering number: ENA1963

LV4904V

Monolithic IC

Digital Input Class-D Power Amplifier

ON Semiconductor®

http://onsemi.com

Overview

The LV4904V is a 2-channel class-D amplifier IC that supports digital input. With this single chip and with a minimal number of external components, it is possible to effectively implement class-D amplifiers. The LV4904V incorporates a soft mute function and a gain controller without pop noise, and can be used as a master volume control of the set. Its function settings can be established through an I^2C bus interface, but it is also possible to establish these settings simply by pin settings without using the I^2C bus. The LV4904V is ideally suited as the power amplifiers in mini components, flat-panel TVs, game machines, electronic musical instruments and other such products.

Features

- I^2S input, 2-channel class-D power amplifier
- On-chip variable over-sampler
- Gain controller (+12dB to -81dB, in 1.5 dB increments)
- Soft mute function
- Controllable via I^2C bus or pin settings
- Under voltage protection circuit, overcurrent protection circuit, thermal protection circuit integrated

Functions

- Input PCM (Fs): 32 kHz/44.1 kHz/48 kHz/88.1 kHz/96 kHz/176.2 kHz/192 kHz
- Master clock input: 256 fs/384 fs/512 fs/768 fs (when Fs=32/44.1/48 kHz)
- Input format: I^2S/24 bits left justified MSB-first / 24 bits right justified LSB-first / 16/18/20/24 bits right justified MSB-first
- Output (THD + N=10%) : 10W × 2 channels (PVD = 15V, RL = 8Ω), 15W × 2 channels (PVD = 18V, RL = 8Ω)
- Efficiency : 85% (PVD = 15V, RL = 8Ω, fin = 1 kHz, Po = 10W)
- THD + N : 0.1% or less (PVD = 15V, RL = 8Ω, fin = 1 kHz, Po = 1W, filter: AES17)
- Power supply voltages : PVD = 8 to 20V, VDD = 3.3V

Semiconductor Components Industries, LLC, 2013

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Power cell power supply	PVD	Externally applied power supply	-0.3 to 24	V
Logic power supply	V_{DD}	Externally applied power supply	-0.3 to 4.0	V
Maximum junction temperature	Tj max		125	°C
Operating temperature	Topr		-30 to +70	°C
Storage temperature	Tstg		-50 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Recommended Operating Range at Ta = 25°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Power cell power supply	PVD	Externally applied power supply	8	13	20	V
Logic power supply	V_{DD}	Externally applied power supply	3.0	3.3	3.6	V
Load	R_L	Speaker load	8	-	-	Ω

Electrical Characteristics

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Digital/Ta=25°C, V_{DD}=3.3V, PVD=13V						
Standby current	IPD		-	1	10	μA
Operating current	I_OP		-	12	30	mA
H input voltage	V_{IH}HIS		0.8V_{DD}	-	5.5	V
L input voltage	V_{IL}HIS		-0.3	-	0.2V_{DD}	V
H input current	I_IH	V_{IN}=V_{DD}	-	-	10	μA
L input current	I_IL	V_{IN}=GND	-10	-	-	μA
Output pin current	I_OH	V_{OUT}=V_{DD}-0.4V	-0.8	-	-	mA
	I_OL	V_{OUT}=0.4V	1	-	-	mA
Power/Ta=25°C, V_{DD}=3.3V, PVD=13V, R_L=8Ω, L=22μH(TOKO:A7040HN-220M), C=33μF, Fin=1kHz						
Standby current	I_{ST}	PVD, RSTB=Low	-	1	10	μA
Mute on current	I_{MUTE}	PVD, ENABLE=Low	-	1	10	mA
Quiescent current	I_{CCO}	PVD, 50% duty	-	16	60	mA
Power Tr. ON resistance *1	R_{DS}ON	I_D=1A	-	300	-	mΩ
Output power	Pout1	8Ω, 15V, THD+N=10%, Modulation index 87.5%	9	10	-	W
	Pout2	8Ω, 18V, THD+N=10%, Modulation index 87.5%	12	14	-	W
Output noise	V_N	IHF-A	-	4	10	mV
THD+N	THD	P_O=1W, 1kHz, 8Ω	-	0.1	0.3	%
Channel separation	CHSEP	P_O=1W, 1kHz, 8Ω	40	60	-	dB

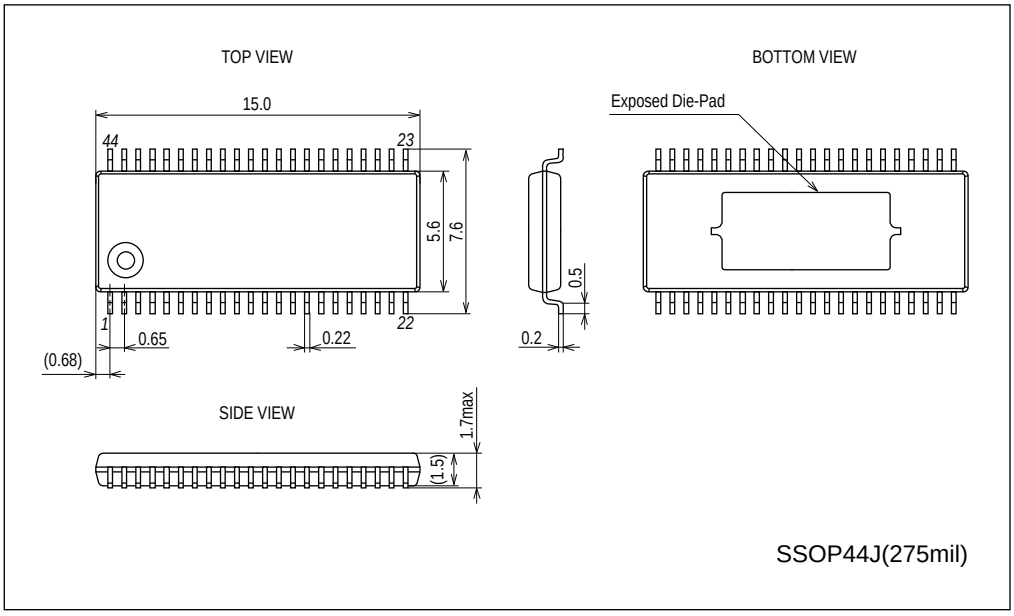
*1 : The maximum power transistor ON resistance(R_{DS}ON) is 360mΩ(design guarantee value).

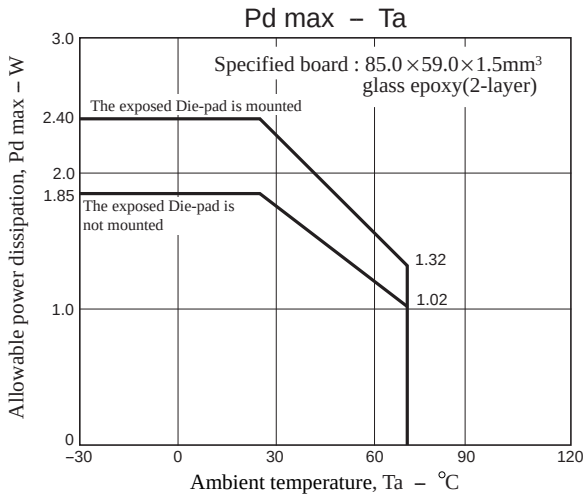
Note : The value of these characteristics were measured in Our test environment. The actual value in an end system will vary depending on the printed circuit board pattern, the components used, and other factors.

Package Dimensions

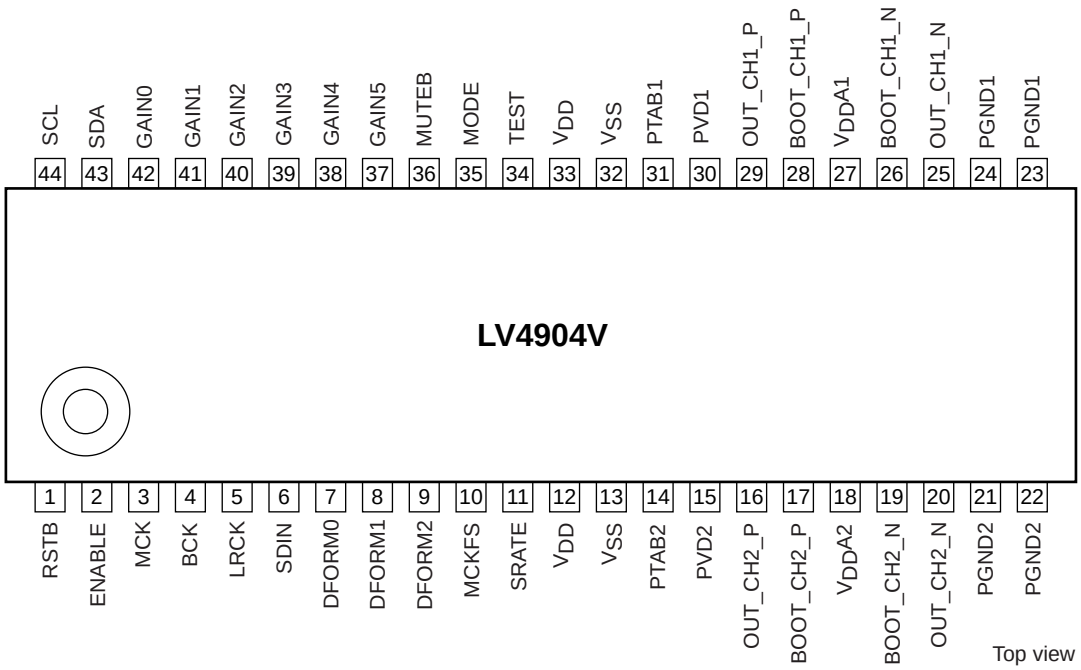
unit : mm (typ)

3285

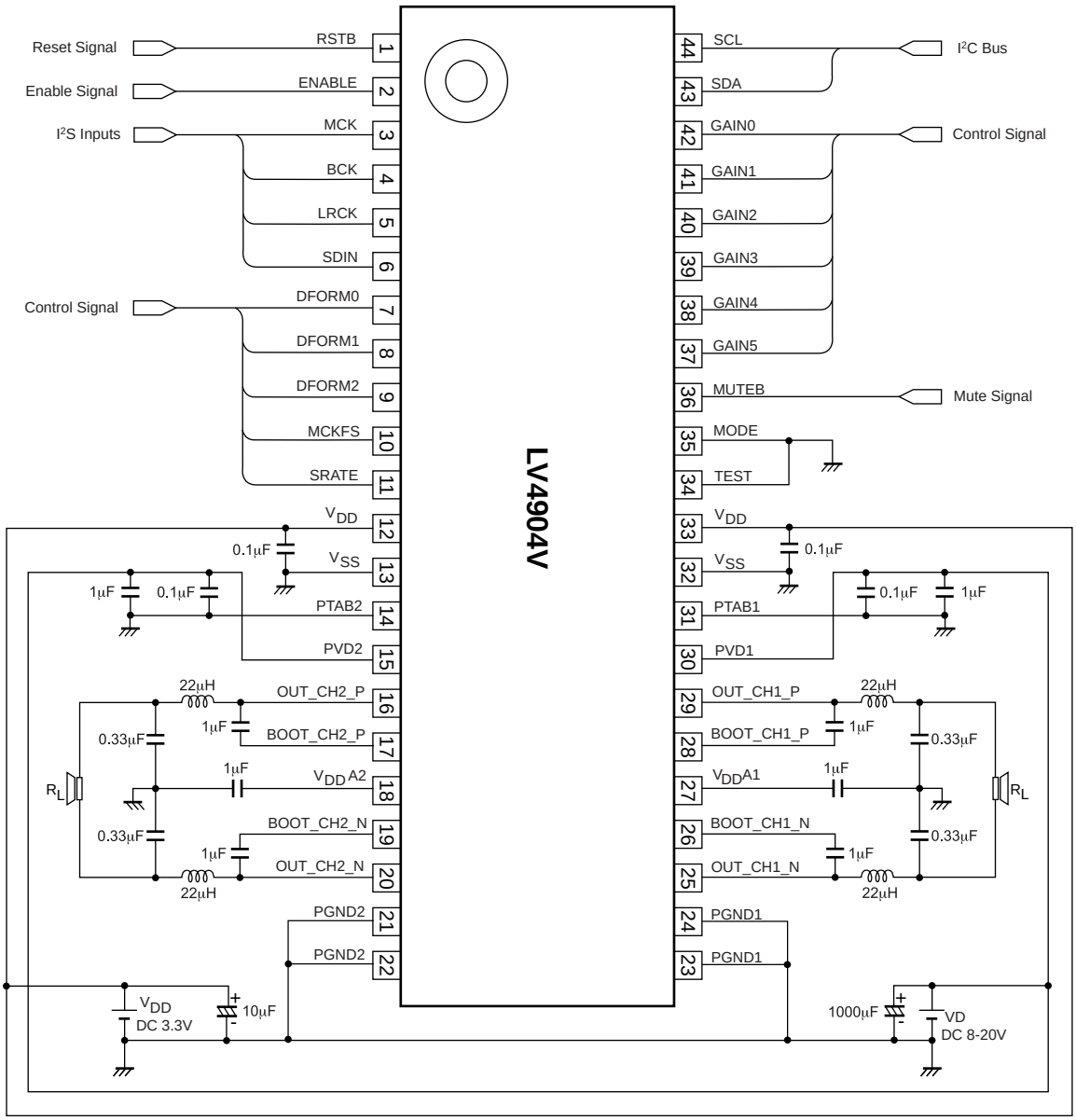




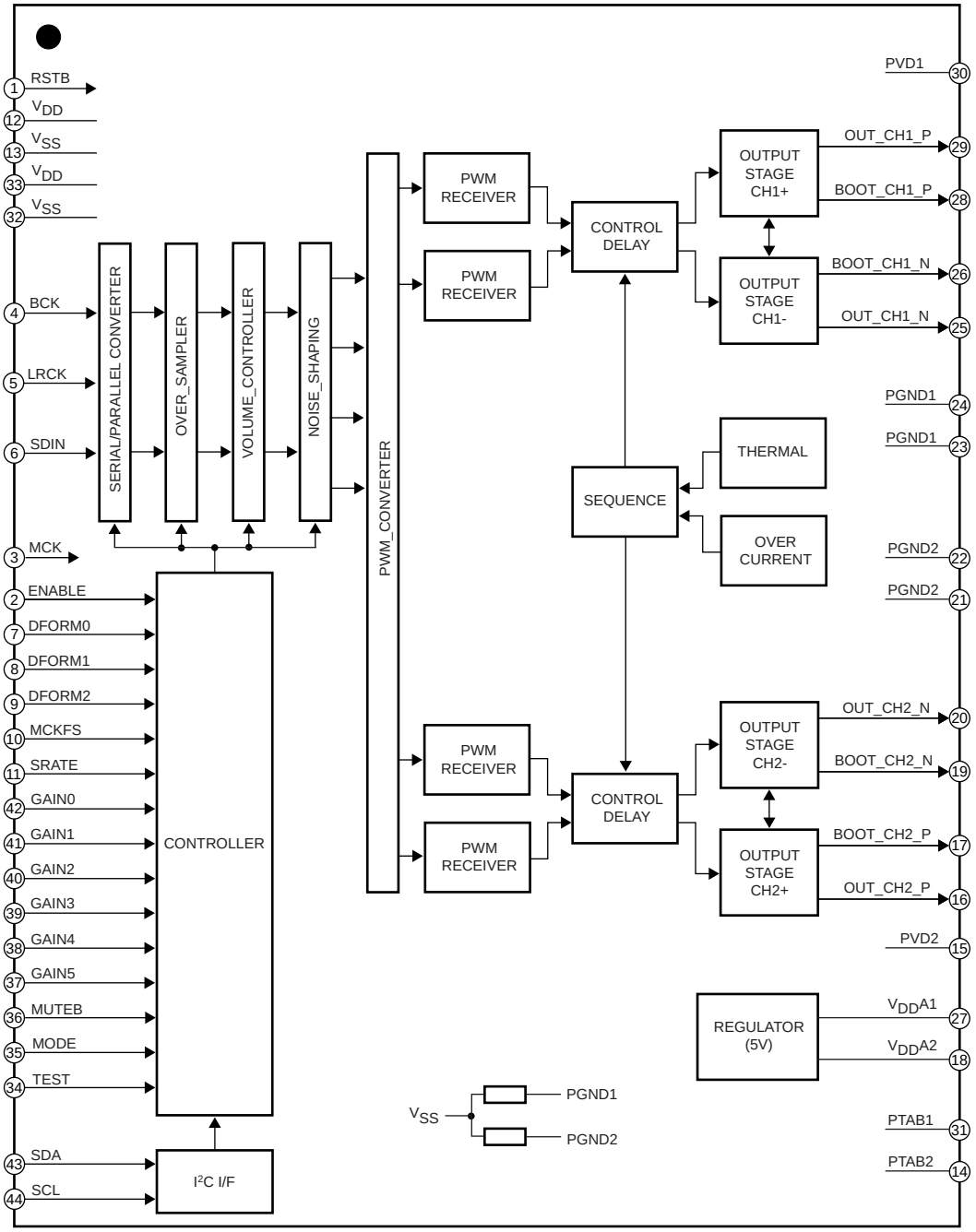
Pin Assignment



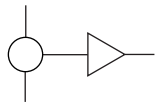
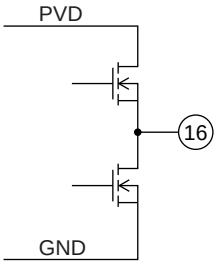
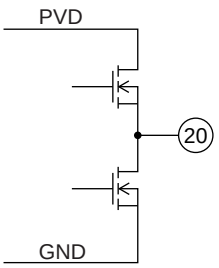
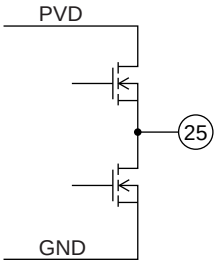
Application Circuit



Block Diagram



Pin Equivalent Circuit

Pin No.	Pin name	I/O	Description	Equivalent Circuit
1	RSTB	DI	Reset input (low active)	
2	ENABLE	DI	System enable input	
3	MCK	DI	Master clock input	
4	BCK	DI	3-wire serial bit clock input	
5	LRCK	DI	3-wire serial LR clock input	
6	SDIN	DI	3-wire serial data input	
7	DFORM0	DI	Input format setting input 0	
8	DFORM1	DI	Input format setting input 1	
9	DFORM2	DI	Input format setting input 2	
10	MCKFS	DI	Master clock (MCK) rate setting pin	
11	SRATE	DI	Input data sampling rate setting pin	
12	V_{DD}	-	Digital power supply (3.3V)	
13	V_{SS}	-	Small-signal ground (GND)	
14	PTAB2	-	Substrate ground	
15	PVD2	-	Power cell power supply	
16	OUT_CH2_P	O	Output pin, channel 2 (Rch) +	
17	BOOT_CH2_P	I/O	Bootstrap I/O pin, channel 2 (Rch) +	
18	$V_{DD}A2$	O	De-coupling capacitor connection pin for internal power supply	
19	BOOT_CH2_N	I/O	Bootstrap I/O pin, channel 2 (Rch) -	
20	OUT_CH2_N	O	Output pin, channel 2 negative	
21	PGND2	-	Channel 2 power ground	
22	PGND2	-	Channel 2 power ground	
23	PGND1	-	Channel 1 power ground	
24	PGND1	-	Channel 1 power ground	
25	OUT_CH1_N	O	Output pin, channel 1 (Lch) -	
26	BOOT_CH1_N	I/O	Bootstrap I/O pin, channel 1 (Lch) -	
27	$V_{DD}A1$	O	De-coupling capacitor connection pin for internal power supply	
28	BOOT_CH1_P	I/O	Bootstrap I/O pin, channel 1 (Lch) +	

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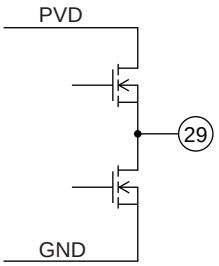
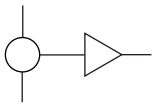
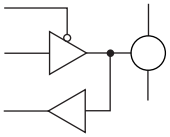
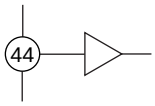
Pin No.	Pin name	I/O	Description	Equivalent Circuit
29	OUT_CH1_P	O	Output pin, channel 1 (Lch) +	
30	PVD1	-	Power cell power supply	
31	PTAB1	-	Substrate ground	
32	V_{SS}	-	Small-signal ground	
33	V_{DD}	-	Digital IO power supply (3.3V)	
34	TEST	DI	Test mode setting pin (fixed at a low level)	
35	MODE	DI	Output mode setting pin	
36	MUTEB	DI	Mute setting input (low active)	
37	GAIN5	DI	Gain setting input 5	
38	GAIN4	DI	Gain setting input 4	
39	GAIN3	DI	Gain setting input 3	
40	GAIN2	DI	Gain setting input 2	
41	GAIN1	DI	Gain setting input 1	
42	GAIN0	DI	Gain setting input 0	
43	SDA	DIO	[I^2C I/F] data	
44	SCL	DI	[I^2C I/F] bit clock	

1. Mode Switching (combined I²C bus and pin setting mode ⇔ pin setting mode)

1.1 Description of modes

Combined I²C bus and pin setting mode

In this mode, the function settings can be established according to both the I²C bus and pins. With some pin settings, the settings established according to the I²C bus registers are enabled; with the other pin settings, the settings established according to the pins are enabled.

Pin setting mode

In this mode, the LV4904V is controlled only by pin settings. This has the advantage of not requiring the I²C bus for control purposes, but the parameters that can be set are limited. Table 1.1 below lists the differences between the items that can be set through the I²C bus and those that can be set using only the pins.

Table 1.1 Differences between combined I²C bus and pin setting mode

Symbol	Description	Settings Using the I²C Bus	Settings Using the Pin
DFORM	Input data format	7 formats available	2 formats available
MCKFS	Master clock (MCK) rate	4 rates available (256fs, 384fs, 512fs, and 768fs)	2 rates available (256fs and 512fs)
SRATE	Input data sampling rate	32 kHz to 192 kHz	44.1 kHz to 96 kHz
GAIN	Gain controller setting	2-channel independently controllable	2-channel common control
MUTE	Muting	2-channel independently controllable	2-channel common control
PSTP	PWM output stop setting	2-channel independently controllable	2-channel common control
IDPEN	50% pulse setting during mute	ON or OFF setting enabled	ON fixed
MDIDX	Modulation index setting	87.5% ⇔ 100% switchable	87.5% fixed
NSORD	Noise shaping orders	Fifth order ⇔ seventh order switchable	Seventh order fixed

1.2 Mode setting methods

Combined I²C bus and pin setting mode

The combined I²C bus and pin setting mode is established when RSTB is set from low to high in a state other than SCL=SDA=low. However, for this to happen, it is necessary that proper clocks have been input from the MCK pin.

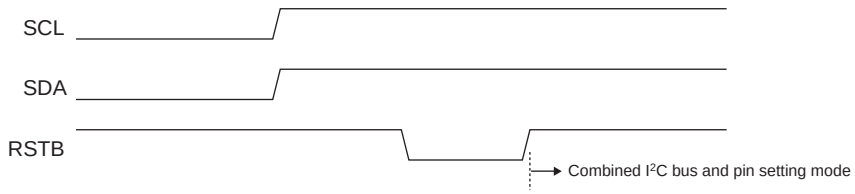


Figure1-1 Placing the IC in combined I²C bus and pin setting mode

Pin setting mode

The pin setting mode is established when RSTB is set from low to high in the SCL=SDA=low state. However, for this to happen, it is necessary that proper clocks have been input from the MCK pin.

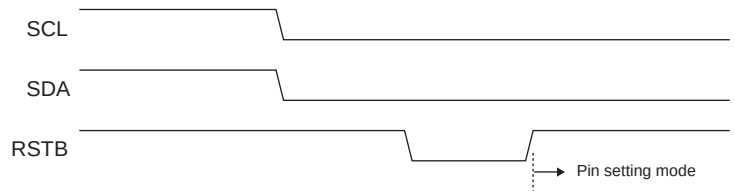


Figure1-2 Placing the IC in pin setting mode

2. Description of Pin Functions

2.1 Hardware reset pin (RSTB)

RSTB is a low active hardware reset pin.
The LV4904V is initialized by setting this pin to low. When the pin is set to low, the internal registers are cleared, and the I^2C bus registers are also reset to the initial values.
Table 2.1 shows the RSTB function settings.

Table 2.1 RSTB pin functions

RSTB	Setting
L	Hardware reset (registers cleared)
H	For normal operation

2.2 System enable pin (ENABLE)

ENABLE is the system enable pin of the LV4904V.
When this pin is set to low, the output is muted regardless of any other settings (mute, gain), and the PWM output is stop(set to high-impedance). ENABLE must be set to high in order to activate the LV4904V.
If the ENABLE function does not need to be set to ON or OFF, the ENABLE pin can be fixed at high.
Table 2.2 shows the ENABLE function settings.

Table 2.2 ENABLE pin function settings

ENABLE	Setting
L	System disabled
H	System enabled

2.3 Master clock input pin (MCK)

The master clock is input from the MCK pin.
For details on this pin, refer to “8.1 Input data settings.”

2.4 3-wire serial data input pins (BCK, LRCK, SDIN)

BCK, LRCK and SDIN are pins used for 3-wire serial data input.
For details on these pins, refer to “8.1 Input data settings.”

2.5 I^2C bus pins (SCL, SDA)

SCL and SDA are the pins used for I^2C bus communication.
The I^2C bus interface of the LV4904V does not function as the master but operates only as a slave.
SCL is the I^2C bus clock pin and operates only as an input pin. This means that the LV4904V never requests wait by pulling the SCL line to low. SDA is the I^2C bus data pin, and since it is an N-channel open drain pin, the data line must be pulled up.
For details on the I^2C bus interface, refer to “5 I^2C Bus Specifications.”

2.6 Input data format setting pins (DFORM0, DFORM1, DFORM2)

The DFORM0, DFORM1 and DFORM2 pins are set to high or low to match the data format that is input.
In the combined I^2C bus and pin setting mode, the data format settings (Table 5.1.1) established according to the I^2C register are valid when DFORM0, DFORM1, and DFORM2 are low. Since the initial setting of the I^2C register is I^2S, I^2S is the setting that is established when DFORM0, DFORM1, and DFORM2 are low in the initial state after reset release.
Table 2.6 shows the format settings established according to the DFORM0, DFORM1, and DFORM2 pins.

Table 2.6 Input data format settings

DFORM2	DFORM1	DFORM0	Setting	
			Combined I^2C Bus and Pin setting Mode	Pin Setting Mode
L	L	L	I^2C register setting	I^2S
L	L	H	Left justified, MSB first	
L	H	L	Right justified, LSB first	
L	H	H	24-bit, right justified, MSB first	
H	L	L	20-bit, right justified, MSB first	
H	L	H	18-bit, right justified, MSB first	
H	H	L	16-bit, right justified, MSB first	

2.7 Master clock setting pin (MCKFS)

The MCKFS pin is set to high or low to match the rate of the master clock that is to be input from the MCK pin.
In the combined I^2C bus and pin setting mode, the master clock settings (Table 8.1.2) established according to the I^2C register are valid when MCKFS is low. Since the initial setting of the I^2C register is 256fs, 256fs is the setting that is established when MCKFS is low in the initial state after reset release.
If the rate of the clock that is input from the MCK pin does not match the MCKFS pin or the setting established according to the I^2C register, an abnormal sound is generated or the output is set to off.
Table 2.7 shows the MCKFS function settings.

Table 2.7 MCKFS pin function settings

MCKFS	Setting	
	Combined I^2C Bus and Pin setting mode	Pin Setting Mode
L	I^2C register setting	256 fs
H	512 fs	

2.8 Sample rate setting pin (SRATE)

The SRATE pin is set to high or low to match the sample rate of the input data.
In the combined I^2C bus and pin setting mode, the sample rate settings (Table 8.1.2) established according to the I^2C register are valid when SRATE is low. Since the initial setting of the I^2C register is 44.1 kHz/48 kHz, 44.1 kHz/48 kHz is the setting that is established when SRATE is low in the initial state after reset release.
Table 2.8 shows the SRATE function settings.

Table 2.8 SRATE pin function settings

SRATE	Setting	
	Combined I^2C Bus and Pin setting mode	Pin Setting Mode
L	I^2C register setting	44.1 kHz/48 kHz
H	88.2 kHz/96 kHz	

2.9 Gain setting pins (GAIN0, GAIN1, GAIN2, GAIN3, GAIN4, GAIN5)

The gain can be set by setting the GAIN0 to GAIN5 pins to high or low.
In the combined I^2C bus and pin setting mode, the gain settings (Table 8.2.1) established according to the I^2C register are valid when all the GAIN0 to GAIN5 pins are low. Since the initial setting of the I^2C register is in mute state, mute is the setting that is established when GAIN0 to GAIN5 are low in the initial state after reset release.
Table 2.9 shows the gain settings established according to the GAIN0 to GAIN5 pins. The gain settings established according to the pin 6 bits and the gain settings established according to the register 6 bits are identical, so refer to Table 8.2.1 for the detailed settings.

Table 2.9 Gain settings

GAIN5	GAIN4	GAIN3	GAIN2	GAIN1	GAIN0	Gain Setting	
						Combined I^2C Bus and Pin setting mode	Pin Setting Mode
H	H	H	H	H	H	+12.0dB	
H	H	H	H	H	L	+10.5dB	
H	H	H	H	L	H	+9.0dB	
…	…	…	…	…	…	(settings in increments of 1.5dB)	
H	H	H	L	L	L	+1.5dB	
H	H	L	H	H	H	0dB	
H	H	L	H	H	L	-1.5dB	
…	…	…	…	…	…	(settings in increments of 1.5dB)	
L	L	L	L	H	L	-79.5dB	
L	L	L	L	L	H	-81.0dB	
L	L	L	L	L	L	I^2C register settings	Mute

2.10 Mute pin (MUTEB)

MUTEB is the low active soft mute pin that controls both the left and right channels.
In the combined I^2C bus and pin setting mode, the mute setting (Table 8.2.2) established according to the I^2C register is valid when MUTEB is low. Since the initial setting of the I^2C register is in mute state, mute is the setting that is established when MUTEB is low in the initial state after reset release.
Table 2.10 shows the MUTEB function settings.

Table 2.10 MUTEB pin function settings

MUTEB	Setting	
	Combined I^2C Bus and Pin setting mode	Pin Setting Mode
L	I^2C register setting	Mute ON
H	Mute OFF	

2.11 Test mode setting pins (TEST, MODE)

TEST and MODE are the test pins. TEST and MODE must be low while using the LV4904V.
Table 2.11 shows the TEST, MODE function settings.

Table 2.11 TEST, MODE pin settings

TEST, MODE	Setting
L	Setting when using the LV4904V
H	Inhibited

3. Start and Stop Sequences

The start and stop sequences given below are recommended in order to reduce pop noise that occurs when LV4909V is turned on or off.

3.1 Start sequence

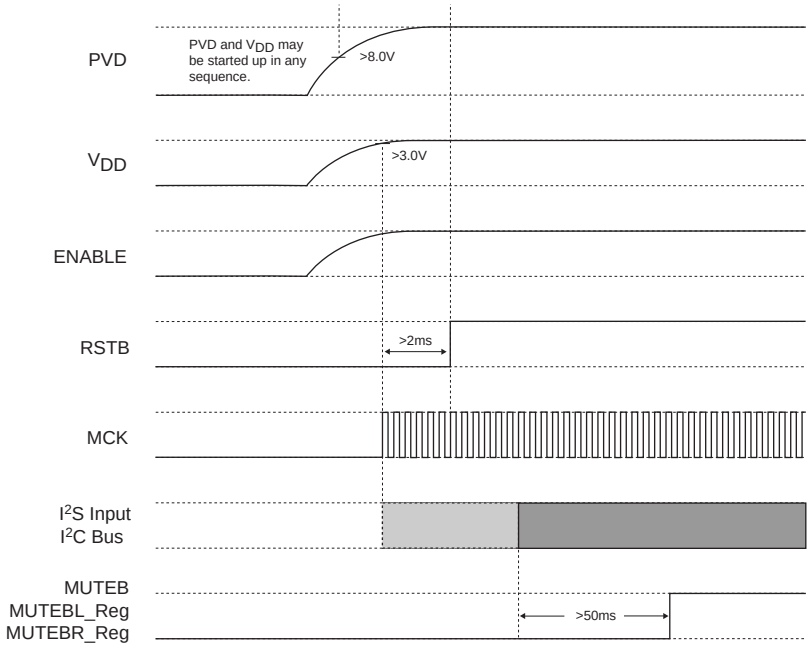


Figure 3.1 Start sequence

3.2 Stop sequence

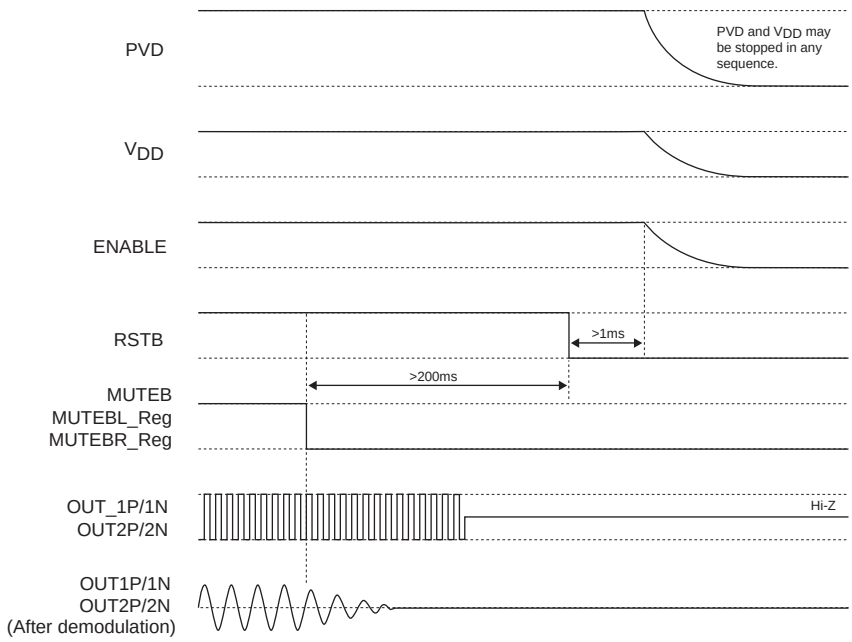


Figure 3.2 Stop sequence

4. Protection Circuits

The LV4904V is provided with under voltage protection circuit, overcurrent protection circuit and thermal protection circuit.

4.1 Under voltage protection circuit

In order to prevent unstable operation at low voltages, the under voltage protection circuit monitors the PVD pin voltage, and once the attack voltage (PVD=7V typ.) has been exceeded, it turns on the amplifier. Furthermore, the recovery voltage (6V typ.) is set so that unstable operation is also prevented when the PVD pin voltage has dropped for some reason during operation. Since hysteresis of 1V or so is provided between the attack voltage and recovery voltage, unstable operation near the threshold voltage where the under voltage protection circuit is continuously set to ON and OFF is prevented. Figure 4.1 shows the operating model of the under voltage protection circuit.

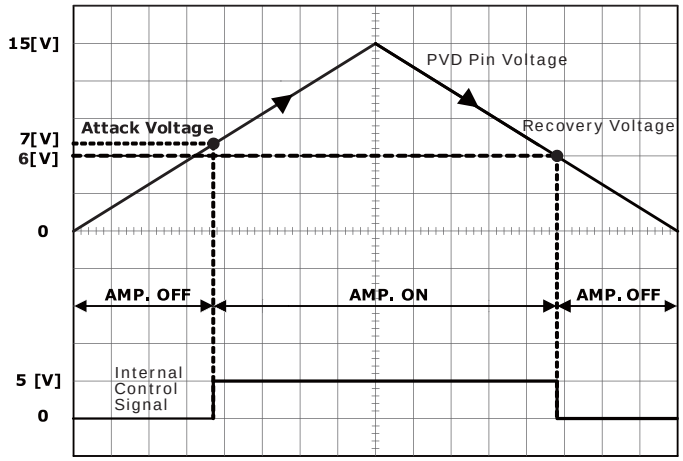


Figure 4.1 Under voltage protection circuit operation

The circuit is designed to turn the amplifier OFF in the same sequence as when Mute is set to ON so that this can be used as a measure to prevent pop noise when the primary power for PVD has been turned off.

Our company's demonstration board is designed so that the above processes are carried out by the charge stored in the power supply capacitor (470 μF) that has been added to the primary power supply line.
However, bear in mind that, in the actual products into which this IC has been incorporated, the primary power supply is connected to other blocks as well, so the time constant for the fall may differ.

4.2 Overcurrent protection circuit

The overcurrent protection circuit is for protecting the output transistors from overcurrent. When it has detected an overcurrent caused by shorting to power, shorting to ground or load shorting and the current level has reached 6A or so, it turns off the output transistors for approximately 20 μsec. About 20 μsec after the output transistors have been turned off, normal operation is recovered automatically, and if another overcurrent is detected, it performs the protection operation again. However, this protection operation is a function that temporarily prevents an overcurrent trouble state and it does not guarantee that the ICs will not be damaged. Figures 4.2.1 and 4.2.2 show the operating models of the overcurrent protection circuit.

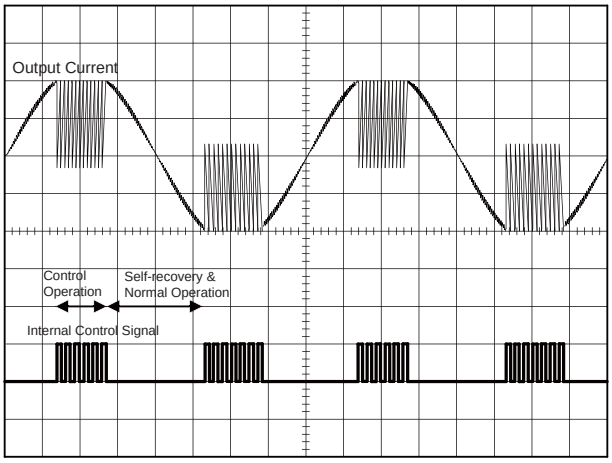


Figure 4.2.1 Graphical representation of overcurrent protection circuit operation

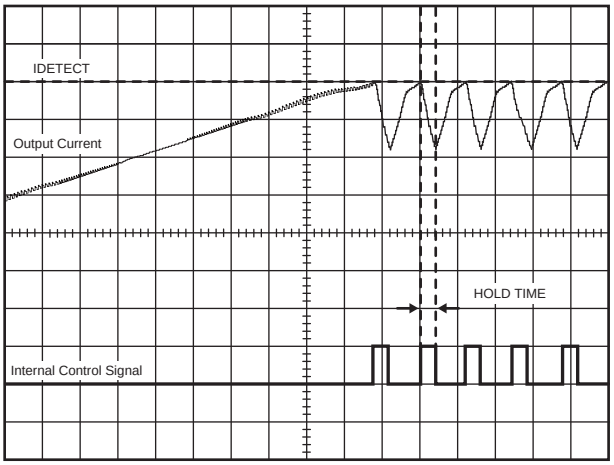


Figure 4.2.2 Graphical representation of overcurrent protection circuit operation (enlarged)

4.3 Thermal protection circuit

The thermal protection circuit is designed to safeguard the ICs from damage or deterioration when the ICs have generated abnormally high levels of heat. When inadequate heat dissipation, a faulty wiring connection or other factor has caused the IC junction temperature (Tj) to rise beyond its rating, the thermal protection circuit sets both the high and low sides of the output transistors to OFF and places the output in the high-impedance state. When, after shutdown, the junction temperature has dropped, the IC is automatically recovered. The attack and recovery temperatures of the circuit are provided with hysteresis to prevent unstable operation near the threshold temperature where the thermal protection circuit is continuously set to ON and OFF.
However, the thermal protection circuit is a function that temporarily prevents abnormal internal heat generation and does not guarantee that the ICs will not be damaged. Similarly, the operating temperature of the thermal protection circuit is not a guaranteed value. Figure 4.3 is a graphical representation of the thermal protection circuit.

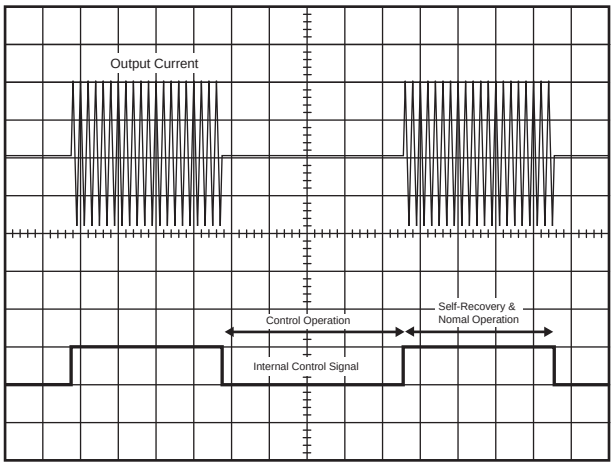


Figure 4.3 Thermal protection circuit operation

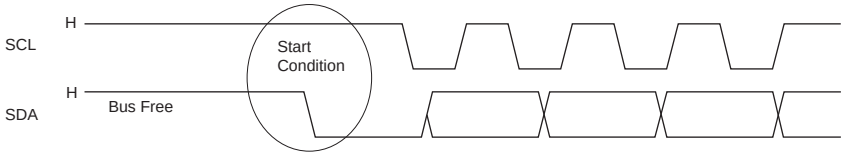
5. I²C Bus Specifications

5.1 Overview of I²C bus interface

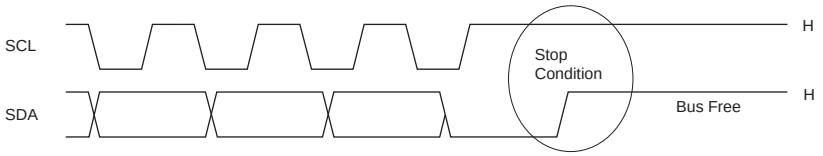
The LV4904V supports the standard I²C bus interface (max. 100 kHz). The device ID of the LV4904V is 11011000 (read) and 11011001 (write). Its I²C bus interface does not function as the master but operates only as a slave.

5.2 I²C bus transfer rules

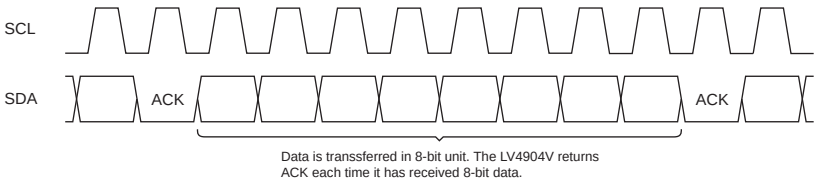
In the bus-free state where there is no I²C transmission or reception, both the SCL and SDA pins must be high. From the state in which both pins are high, by holding the SCL pin state to high and setting the SDA to low, communication is started. This is referred to as the start condition.



To end I²C transmission or reception, change the SDA pin state from low to high with the SCL still high. This is referred to as the stop condition.

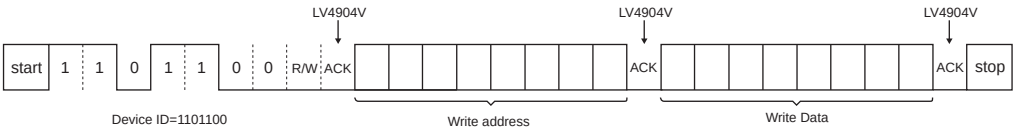


Data transfer is started after the start condition has been transmitted. The data is transferred in 8-bit units from the master to the LV4904V at the slave, and the LV4904V responds every time 8 bits are received by setting the SDA pin to low. This is referred to as acknowledge (ACK). The master sets the bus free and waits for ACK.



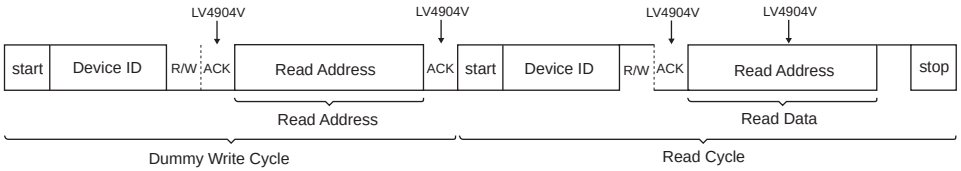
5.3 Data write

To write data in the LV4904V, the device ID, write address and data are sent in this sequence after the start condition has been sent, and lastly the stop condition is sent. The read/write flag bit is added to the 7-bit device ID, and the write mode is established according to setting this bit too low.



5.4 Data read

By sending the data read command, the data held in the registers of the LV4904V can be read. To read the data, first the address is sent using a dummy write cycle, and then operation is restarted. Next, after the device ID and read flag has been sent in the read cycle, the LV4904V outputs the data of the address sent in the dummy write cycle to the SDA line. The transmission side establishes the I^2C bus-free state to prepare for data reception. After the data has been received, ACK is not returned, and the stop condition is sent to end communication.



5.5 Internal register initialization

The internal registers accessed at address FFh through the I^2C bus are write-only registers. By writing the value of FFh into these registers, the internal registers are reset to the initial values.

6. I^2C Register Map

Register	Address	D7	D6	D5	D4	D3	D2	D1	D0
STAT	00h	Last accessed address (read-only)							
DATA	10h	0	MCKFS_I^2C [1:0]		SRATE_I^2C [1:0]		DFORM [2:0]		
GAINL	20h	PSTPL	MUTEBL	GAINL [5:0]					
GAINR	21h	PSTPR	MUTEBR	GAINR [5:0]					
MISC	30h	Reserved				NSORD	MDIDX	IDPEN	1
RST	FFh	SOFTR [7: 0] (for initializing registers)							

7. I^2C Command List

Register	Address	Bit	Signal Name	Pin Description	Initial Value
DATA	10h	[2:0]	DFORM	3-wire serial PCM input, format setting	000
		[4:3]	SRATE_I^2C	3-wire serial PCM input, sampling rate setting	01
		[6:5]	MCKFS_I^2C	Master clock rate setting	00
		[7]		0 (Fixed)	0
GAINL	20h	[5:0]	GAINL	Channel 1 (L channel), gain setting	00000
		[6]	MUTEBL	Channel 1 (L channel), mute setting	0
		[7]	PSTPL	Channel 1 (L channel), output disable setting	0
GAINR	21h	[5:0]	GAINR	Channel 2 (R channel), gain setting	00000
		[6]	MUTEBR	Channel 2 (R channel), mute setting	0
		[7]	PSTPR	Channel 2 (R channel), output disable setting	0
MISC	30h	[0]		1 (Fixed)	1
		[1]	IDPEN	Pulse operation control when muted	1
		[2]	MDIDX	PWM modulation index setting	0
		[3]	NSORD	Noise shaper order setting	0

8. Description of I²C Bus Registers

8.1 Input data settings

Register	Address	D7	D6	D5	D4	D3	D2	D1	D0
DATA	10h	0	MCKFS_I²C [1: 0]		SRATE_I²C [1: 0]		DFORM _I²C [2: 0]		

DFORM_I²C is set to match the format of the 3-wire serial input that is to be input.
The setting established according to DFORM_I²C is valid only when the DFORM0, DFORM1, and DFORM2 pins are low in the combined I²C bus and pin setting mode. With any other pin settings or when the pin setting mode is established, the settings established according to the pins described in section 2.6 are valid, therefore DFORM_I²C setting described here is ignored. Table 16.1.1 and Figure 16.1.1 to Figure 16.1.4 show the formats that are set by DFORM_I²C.
Table 8.1.1 Data format settings (initial setting in **bold**)

DFORM_I²C	Data Format
000	**I²S**
001	Left justified, MSB first
010	Right justified, LSB first
011	24 bits, right justified, MSB first
100	20 bits, right justified, MSB first
101	18 bits, right justified, MSB first
110	16 bits, right justified, MSB first

Figure 16.1.1 [DFORM_I²C = 0000] BCK=64 fs, I²S (24 bits)

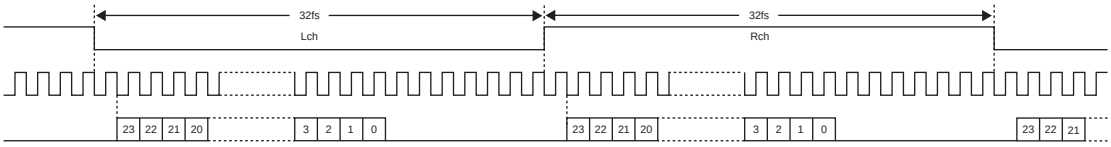


Figure 16.1.2 [DFORM _I²C = 0001] BCK=64 fs, left justified, MSB first (24 bits)

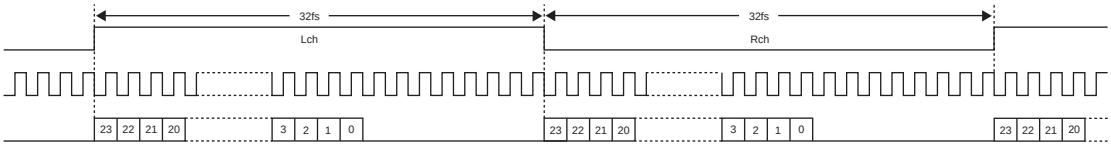


Figure 16.1.3 [DFORM _I²C = 0010] BCK=64 fs, right justified, LSB first (24 bits)

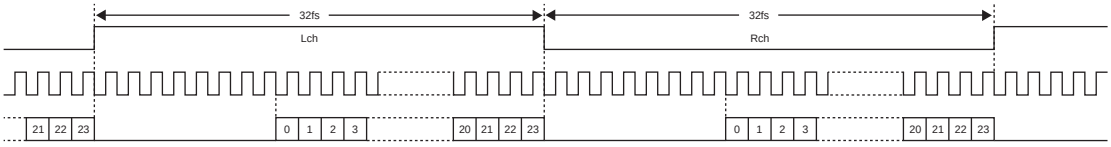
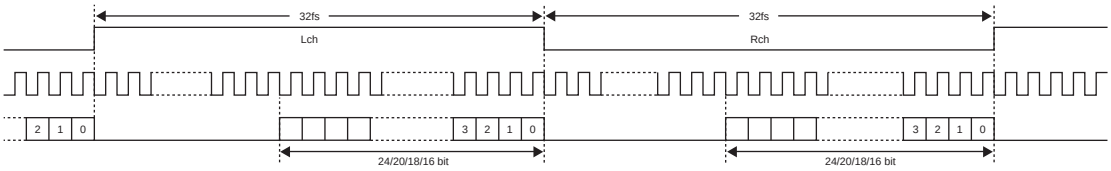


Figure 8.1.4 [DFORM_I²C = 011/100/101/110] BCK=64 fs, 24/20/18/16 bits, right justified, MSB first



Master clock rate MCKFS_I²C and sample rate SRATE_I²C are set in accordance with the master clock and input sample rate. The settings established according to MCKFS_I²C are valid only when the MCKFS pin is set to low in the combined I²C bus and pin setting mode. When MCKFS is high or when the pin setting mode is established, the settings established according to the pins described in section 2.7 are valid, therefore MCKFS_I²C setting described here is ignored. The settings established according to SRATE_I²C are valid only when the SRATE pin is low in the combined I²C bus and pin setting mode. When SRATE is high or when the pin setting mode is established, the settings established according to the pins described in section 2.8 are valid, therefore SRATE_I²C setting described here is ignored.
If these settings are illegal and they do not match the input signals, an abnormal sound is generated or the output is set to off. Noise is generated when switching the settings, so mute the output before changing any settings.
Table 8.1.2 shows the settings of the master clock that is set by SRATE and MCKFS.

Table 8.1.2 Master clock settings (initial values in **bold**)

SRATE_I²C		Sampling Rate	MCKFS_I²C Setting and MCK Rate			
[1]	[0]		**[00]**	[01]	[10]	[11]
0	0	32 kHz	256 fs	384 fs	512 fs	768 fs
0	**1**	**44.1/48 kHz**	**256 fs**	384 fs	512 fs	768 fs
1	0	88.2/96 kHz	128 fs	192 fs	256 fs	384 fs
1	1	176.4/192 kHz	64 fs	96 fs	128 fs	192 fs

8.2 Gain and mute settings

Register	Address	D7	D6	D5	D4	D3	D2	D1	D0
GAINL	20h	PSTPL	MUTEBL	GAINL [5:0]					
GAINR	21h	PSTPR	MUTEBR	GAINR [5:0]					

The left-channel volume and right-channel volume are each set with 6 bits and in 64 steps using the GAINL and GAINR registers, respectively. The volume setting ranges from +12 dB to -81 dB in 1.5 dB increments.
The settings established according to GAINL and GAINR are valid only when all the GAIN0 to GAIN5 pins are low in the combined I²C bus and pin setting mode. With any other pin settings or when the pin setting mode is established, the settings established according to the pins described in section 2.9 are valid, therefore GAINL and GAINR setting described here is ignored.
Table 8.2.1 shows the volume settings established according to GAINL and GAINR.

Table 8.2.1 Gain settings (initial value in **bold**)

No.	GAINL GAINR	Gain (dB)
63	111111	+12.0
62	111110	+10.5
61	111101	+9.0
60	111100	+7.5
59	111011	+6.0
58	111010	+4.5
57	111001	+3.0
56	111000	+1.5
55	110111	0.0
54	110110	-1.5
53	110101	-3.0
52	110100	-4.5
51	110011	-6.0
50	110010	-7.5
49	110001	-9.0
48	110000	-10.5
47	101111	-12.0
46	101110	-13.5
45	101101	-15.0
44	101100	-16.5
43	101011	-18.0
42	101010	-19.5

No.	GAINL GAINR	Gain (dB)
41	101001	-21.0
40	101000	-22.5
39	100111	-24.0
38	100110	-25.5
37	100101	-27.0
36	100100	-28.5
35	100011	-30.0
34	100010	-31.5
33	100001	-33.0
32	100000	-34.5
31	011111	-36.0
30	011110	-37.5
29	011101	-39.0
28	011100	-40.5
27	011011	-42.0
26	011010	-43.5
25	011001	-45.0
24	011000	-46.5
23	010111	-48.0
22	010110	-49.5
21	010101	-51.0
20	010100	-52.5

No.	GAINL GAINR	Gain (dB)
19	010011	-54.0
18	010010	-55.5
17	010001	-57.0
16	010000	-58.5
15	001111	-60.0
14	001110	-61.5
13	001101	-63.0
12	001100	-64.5
11	001011	-66.0
10	001010	-67.5
9	001001	-69.0
8	001000	-70.5
7	000111	-72.0
6	000110	-73.5
5	000101	-75.0
4	000100	-76.5
3	000011	-78.0
2	000010	-79.5
1	000001	-81.0
0	**000000**	**MUTE**

Left channel mute is set using MUTEBL and right channel mute is set using MUTEBR. Both MUTEBL and MUTEBR are low active.
The settings established according to MUTEBL and MUTEBR are valid only when the MUTEB pin is low in the combined I^2C bus and pin setting mode. With any other pin settings or when the pin setting mode is established, the settings established according to the pins described in section 2.10 are valid, therefore MUTEBL and MUTEBR setting described here is ignored.
Table 8.2.2 shows the mute settings established according to MUTEBL and MUTEBR.

Table 8.2.2 Mute settings (initial value in **bold**)

MUTEBL/MUTEBR	Setting
0	**Mute**
1	Audio output ON

The left channel PWM output can be stopped by PSTPL and the right channel PWM output can be stopped by PSTPR.
Table 8.2.3 shows the PWM output stop settings established according to PSTPL and PSTPR.

Table 8.2.3 PWM output stop settings (initial value in **bold**)

PSTPL/PSTPR	Setting
0	**Normal output operation mode**
1	PWM output stopped

8.3 Other settings

Register	Address	D7	D6	D5	D4	D3	D2	D1	D0
PWM1	41h	Reserved				NSORD	MDIDX	IDPEN	1

By setting IDPEN, the PWM output can be fixed to the 50% duty cycle pulse or idled during mute or under no-signal conditions.
Table 8.3.1 shows the IDPEN function settings.

Table 8.3.1 IDPEN function settings (initial value in **bold**).

IDPEN	Setting
0	Idle operation mode
1	**50% duty pulse**

The modulation index of the PWM modulator can be switched by setting MDIDX.
Table 8.3.2 shows the MDIDX function settings.

Table 8.3.2 MDIDX function settings (initial value in **bold**).

MDIDX	Setting
0	**87.5%**
1	100%

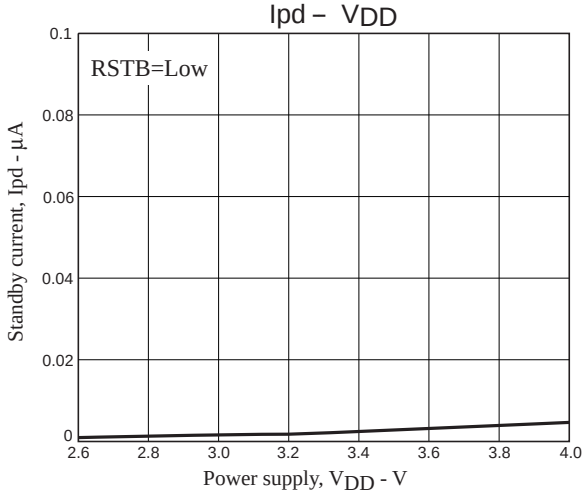
The noise shaper order can be switched by setting NSORD.
Table 8.3.3 shows the NSORD function settings.

Table 8.3.3 NSORD function settings (initial value in **bold**)

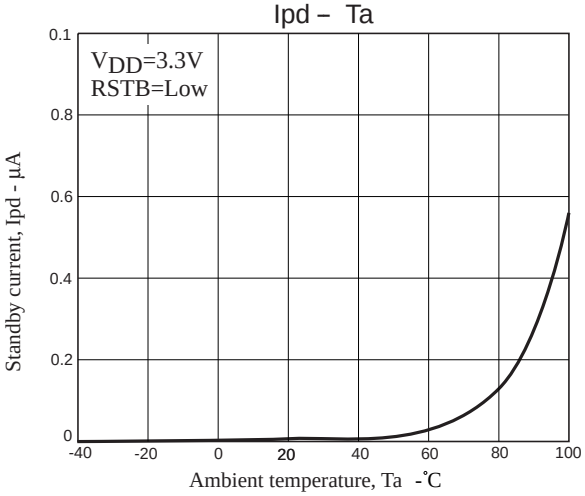
NSORD	Setting
0	**Seventh order**
1	Fifth order

8. Characteristics Data: Ta=27°C, Fs=48 kHz, Master Clock=256 fs

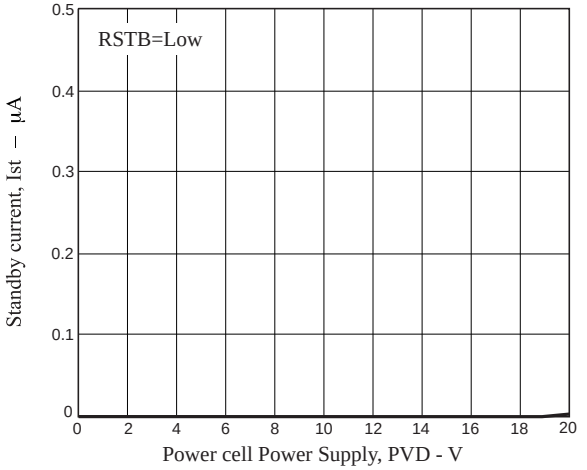
Ipd – V_{DD}



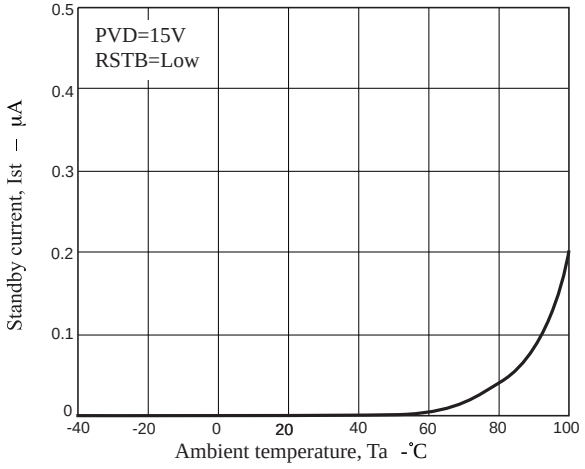
Ipd – Ta



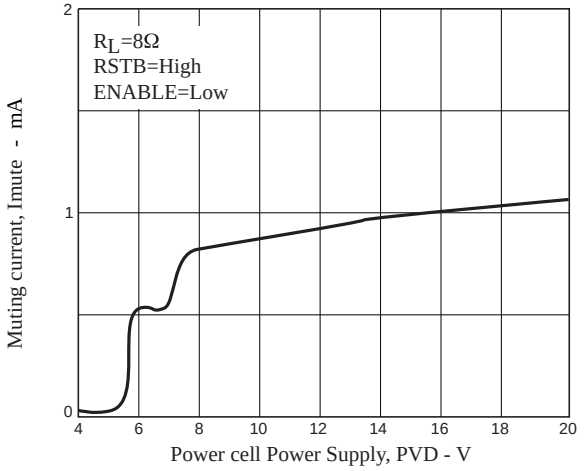
Ist – PVD



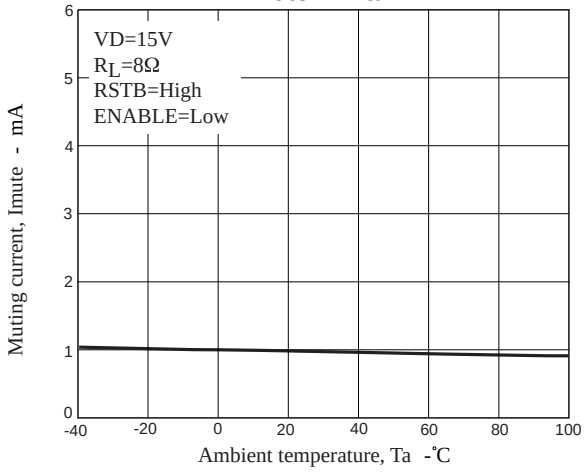
Ist – Ta



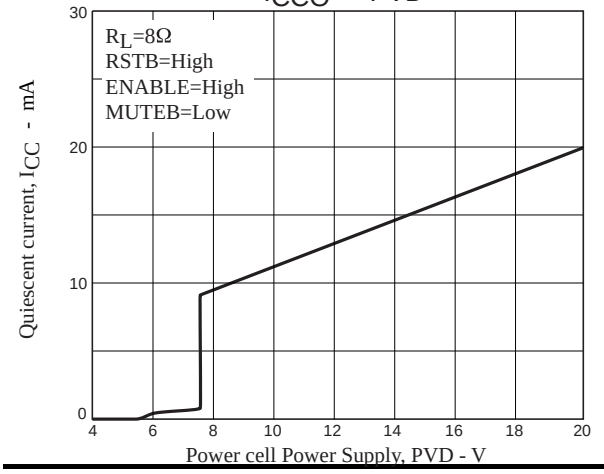
Imute – PVD



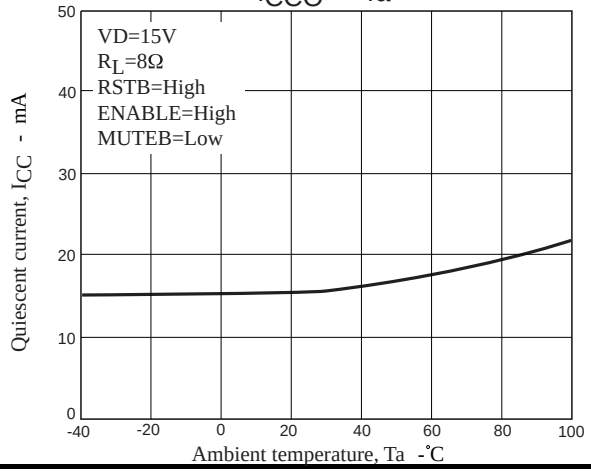
Imute – Ta



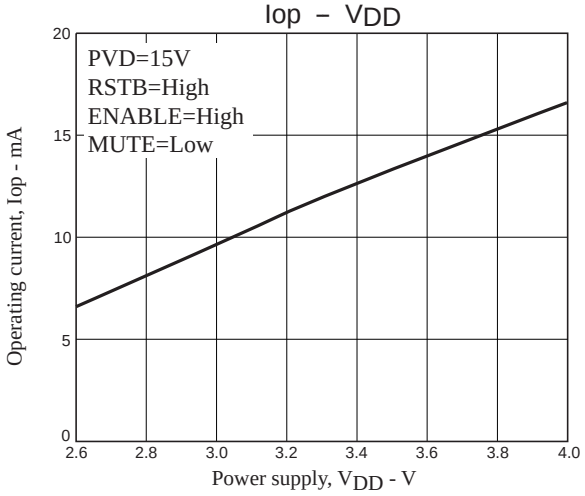
I_{CCO} – PVD



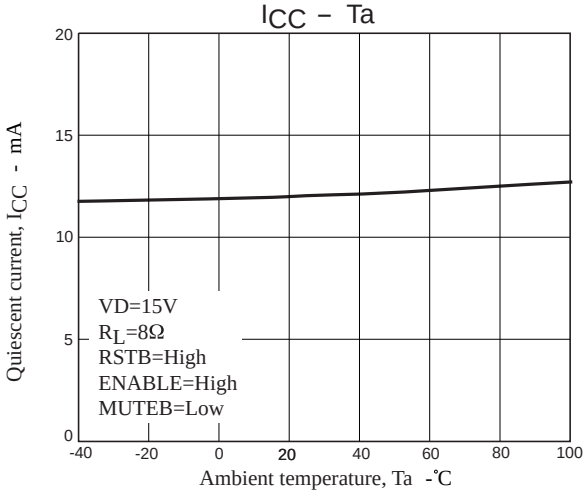
I_{CCO} – Ta



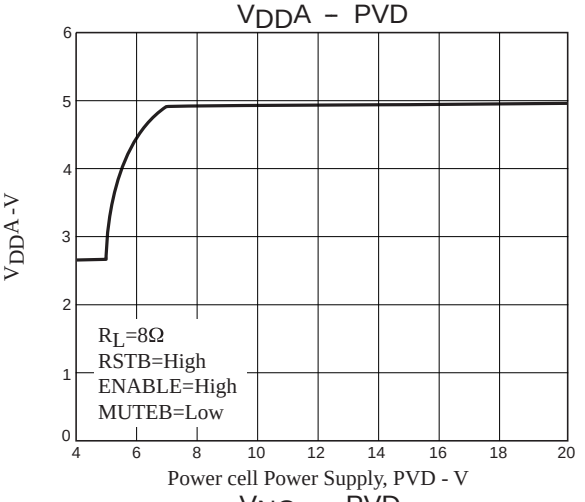
Iop – V_{DD}



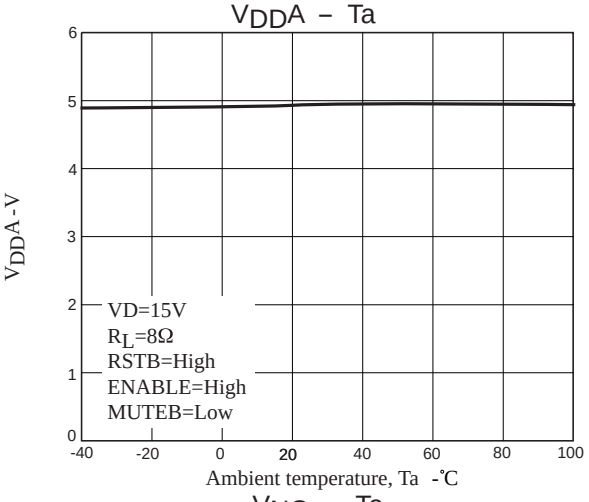
I_{CC} – Ta



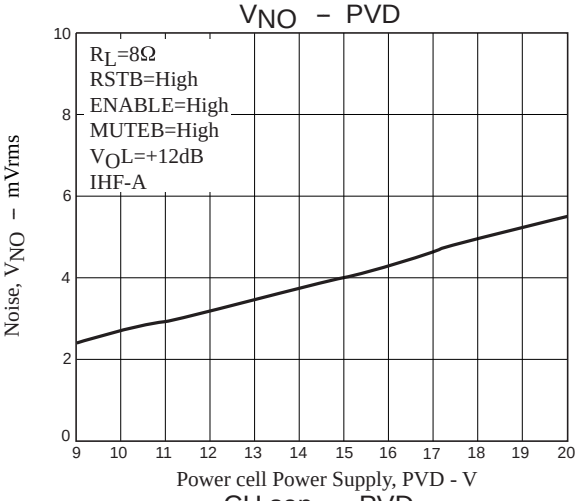
V_{DD}A – PVD



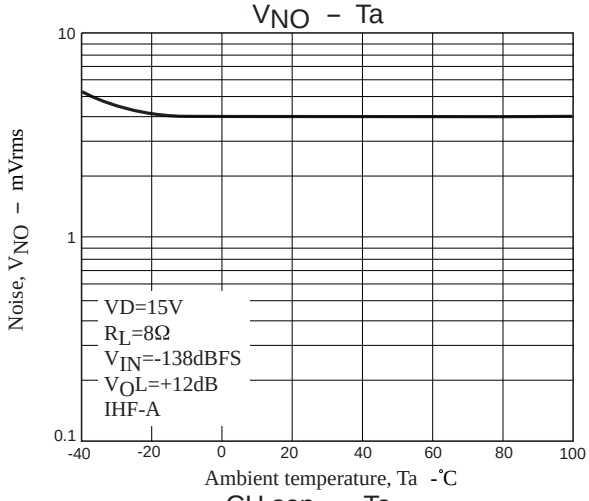
V_{DD}A – Ta



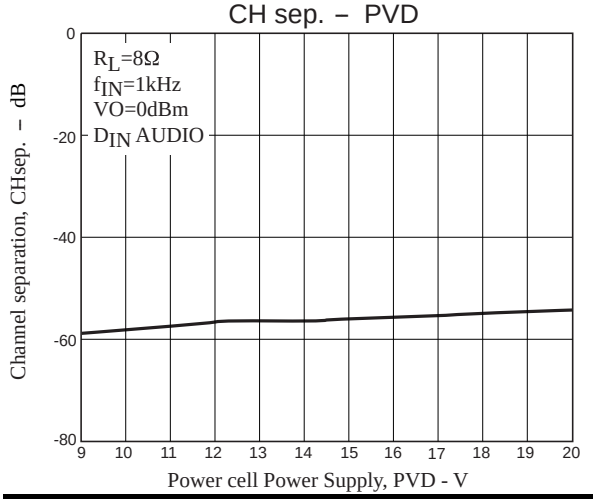
V_{NO} – PVD



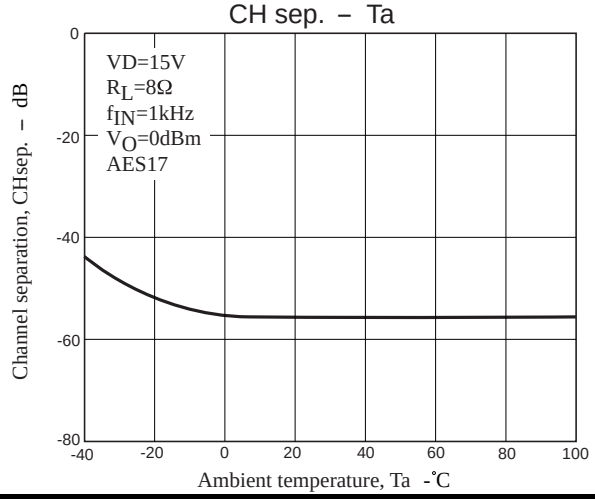
V_{NO} – Ta



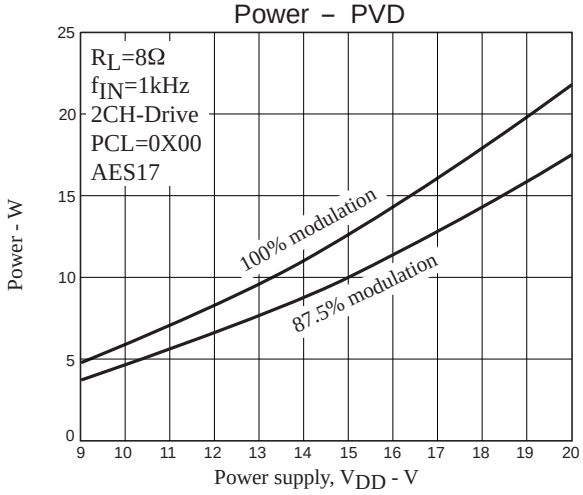
CH sep. – PVD



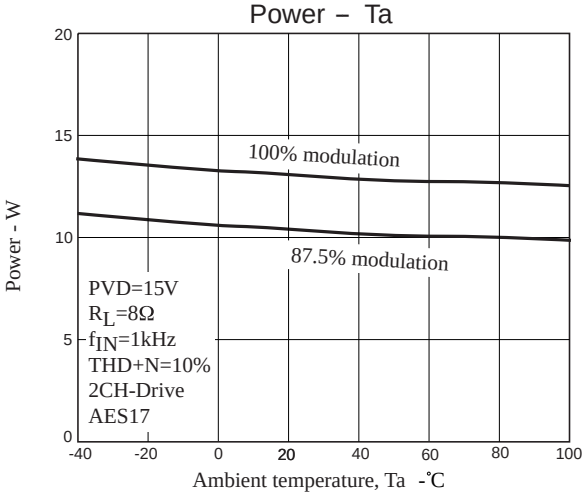
CH sep. – Ta



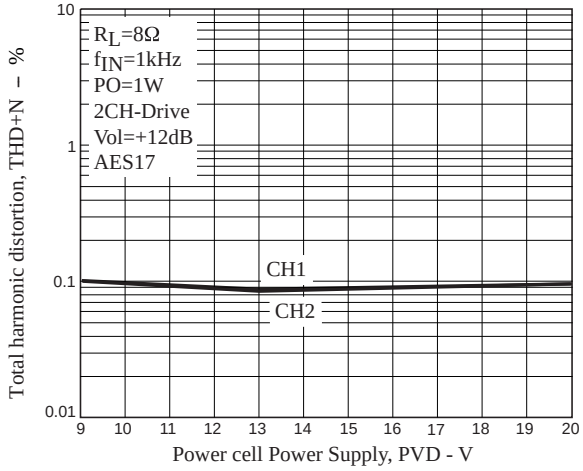
Power – PVD



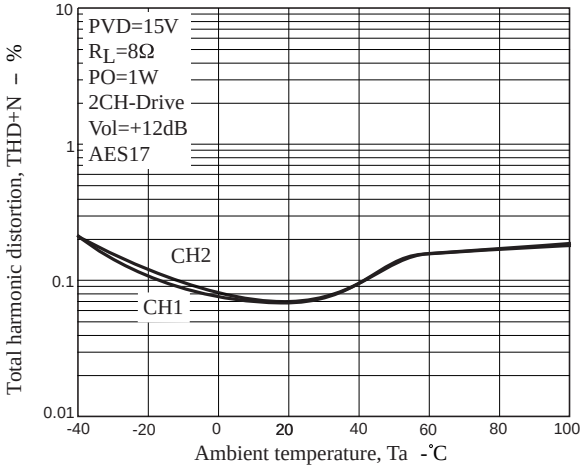
Power – Ta



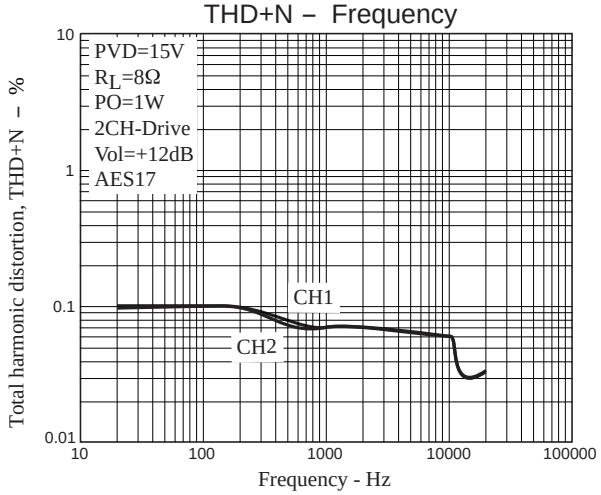
THD+N – PVD



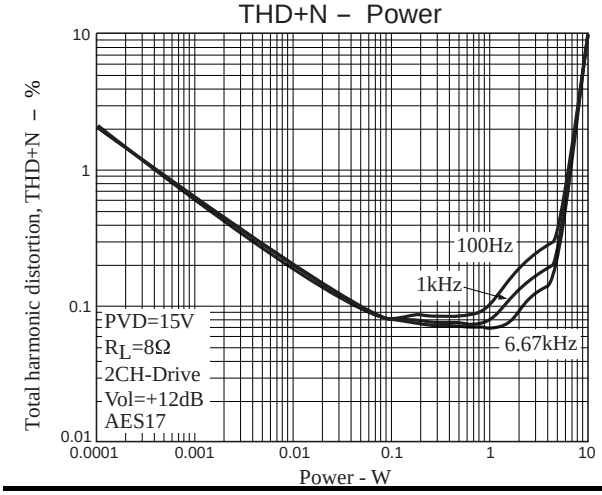
THD+N – Ta



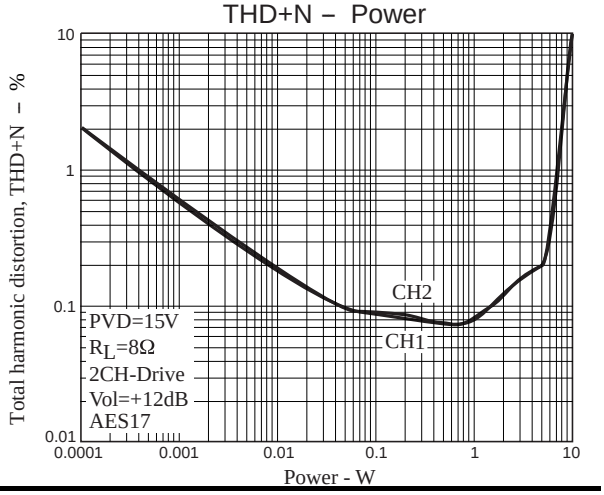
THD+N – Frequency



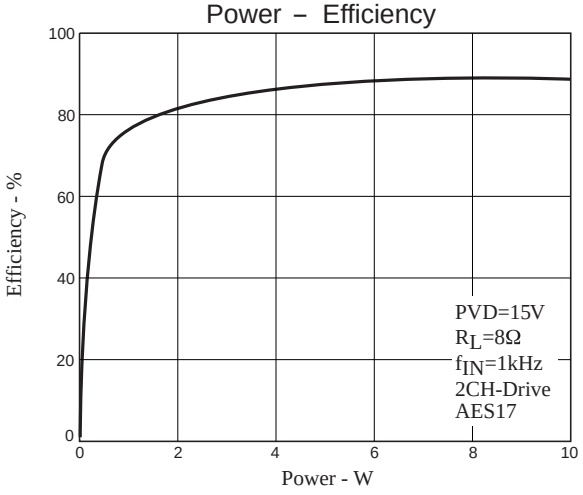
THD+N – Power



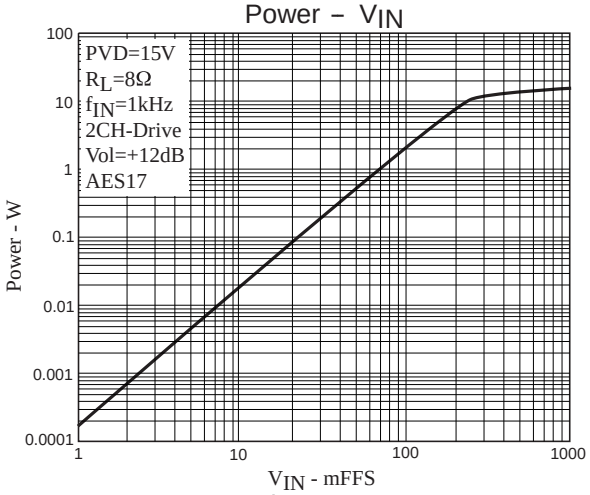
THD+N – Power



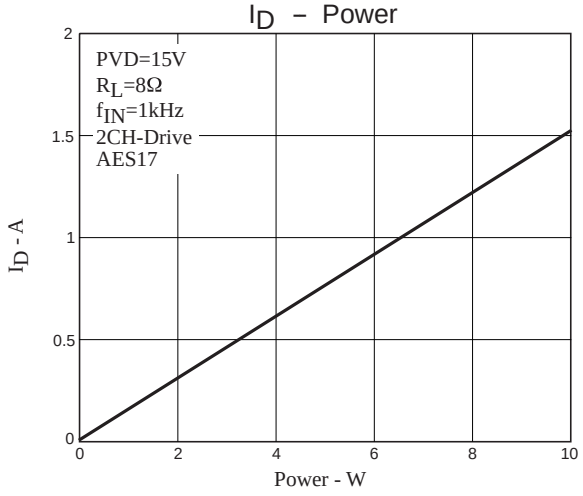
Power – Efficiency



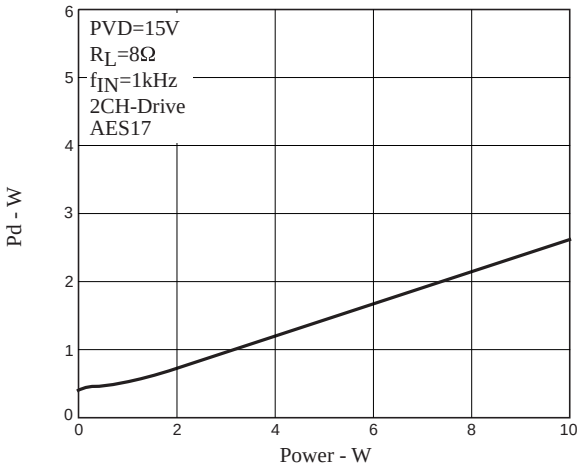
Power – V_{IN}



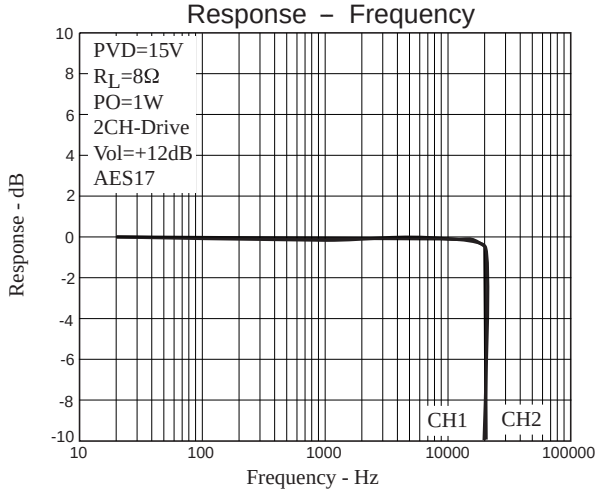
I_D – Power



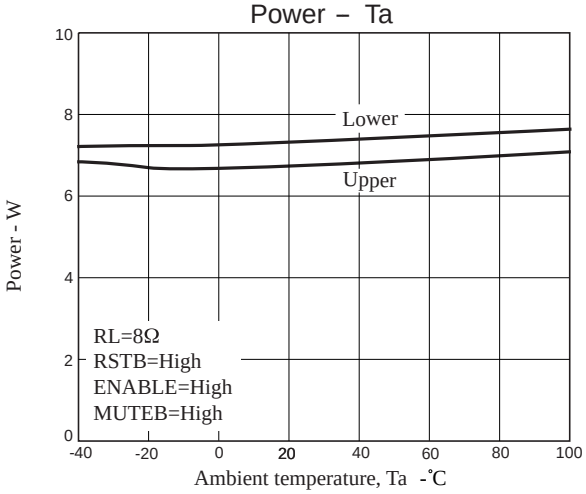
Pd – Power



Response – Frequency



Power – Ta



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