ABRACON CORPORATION
The Power of Linking Together

30332 Esperanza
Rancho Santa Margarita, CA-92688
Tel: (949) 546-8000 Fax: (949) 546-8001
Tech-Support@abracon.com

Application Manual

AB-RTCMC-32.768kHz-B5GA-S3

Real Time Clock/Calendar Module with I^2C Interface

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Rancho Santa Margarita, CA-92688
Tel: (949) 546-8000 Fax: (949) 546-8001
Tech-Support@abracon.com

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Tel: (949) 546-8000 Fax: (949) 546-8001
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AB-RTCMC-32.768kHz-B5GA-S3

I²C-Bus Interface Real Time Clock / Calendar Module

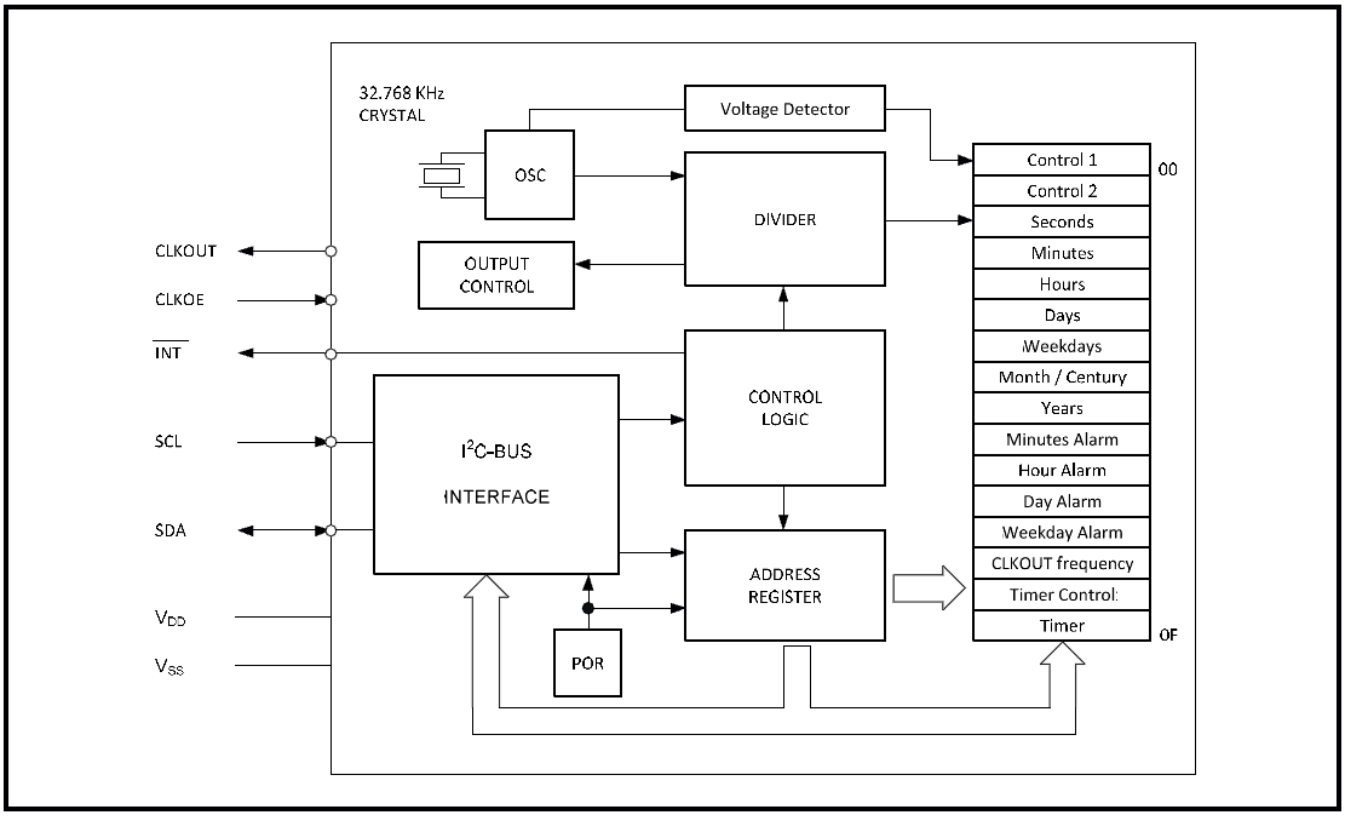
1.0 OVERVIEW

- RTC module with built-in crystal oscillating at 32.768 kHz
- 400kHz two-wire I²C interface
- Wide Interface operating voltage: 1.8 – 5.5 V
- Wide clock operating voltage: 1.2 – 5.5 V
- Low power consumption: 250 nA typ @ 3.0V / 25°C
- Provides year, month, day, weekday, hours, minutes, seconds
- Alarm and Timer functions
- Century flag
- Low voltage detector, internal power on reset
- Programmable clock output for peripheral devices (32.768 kHz, 1024 Hz, 32 Hz, 1 Hz)
- I2C slave address: read A3h, write A2h
- Small and compact package size: 3.7 x 2.5 x 0.9 mm. RoHS-compliant and 100% leadfree

2.0 GENERAL DESCRIPTION

The AB-RTCMC-32.768kHz-B5GA-S3 is a CMOS real time clock / calendar optimized for low power consumption. A programmable clock output, interrupt output and voltage low detector are also provided. All address and data are transferred serially via a two-line bi-directional I²C bus. Maximum bus speed is 400kbit/sec. The built-in word address register is incremented automatically after each written or read data byte.

3.0 BLOCK DIAGRAM



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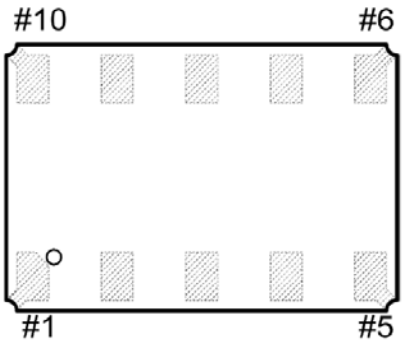
4.0 PINOUT



Pin #	Function	Pin #	Function
1	CLKOE	6	$\overline{INT}$
2	V_{DD}	7	V_{SS}
3	CLKOUT	8	N.C
4	SCL	9	N.C.
5	SDA	10	N.C.

5.0 PIN DESCRIPTION

Pin No.	Pin Name	Function
1	CLKOE	CLKOUT enable/disable pin; enable is active HIGH; tie to GND when not using CLKOUT
2	V_{DD}	Positive supply voltage
3	CLKOUT	Clock Output pin; push-pull
4	SCL	Serial Clock Input pin; requires pull-up resistor
5	SDA	Serial Data Input-Output pin; open-drain; requires pull-up resistor
6	$\overline{INT}$	Interrupt Output pin; open-drain; active LOW
7	V_{SS}	Ground
8	N.C.	Not Connected
9	N.C.	Not Connected
10	N.C.	Not Connected

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6.0 FUNCTIONAL DESCRIPTION

The AB-RTCMC-32.768kHz-B5GA-S3 RTC module combines a RTC IC with on chip oscillator together with a 32.768 kHz quartz crystal in a miniature ceramic package.

The AB-RTCMC-32.768kHz-B5GA-S3 contains sixteen 8-bit registers with an auto-incrementing address register, a frequency divider which provides the source clock for the Real Time Clock (RTC), a programmable clock output, a timer, a voltage low detector and a 400 kHz I^2C bus interface.

All 16 registers are designed as addressable 8-bit parallel registers although not all bits are implemented. The first two registers (memory address 00h and 01h) are used as control and/or status registers. The memory addresses 02h through 08h are used as counters for the clock function (seconds up to year counters). Address locations 09h through 0Ch contain alarm registers which define the conditions for an alarm. Address 0Dh controls the CLKOUT output frequency. 0Eh and 0Fh are the timer control and timer registers, respectively.

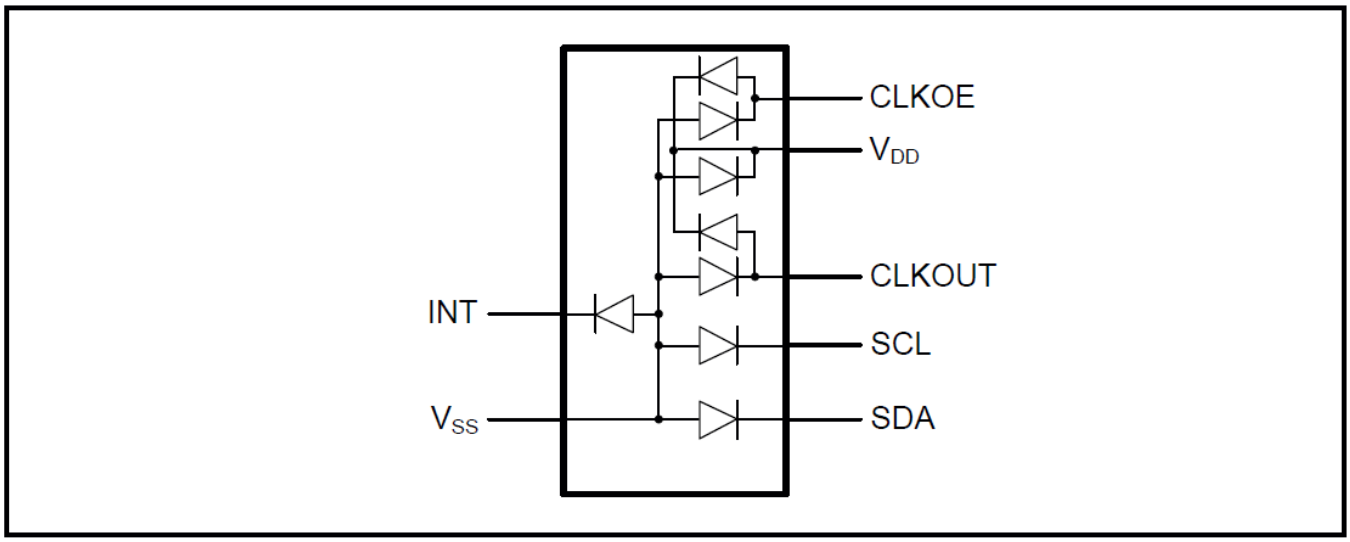
The seconds, minutes, hours, days, weekdays, months, years as well as the minute alarm, hour alarm, day alarm and weekday alarm registers are all coded in BCD format.

When one of the RTC counters is read (memory locations 02h through 08h), the contents of all counters are frozen at the beginning of a read cycle. Therefore, faulty reading of the clock / calendar during a carry condition is prevented.

6.1 CLKOUT OUTPUT

A programmable square wave is available at the CLKOUT pin. Frequencies of 32.768 kHz, 1024 Hz, 32 Hz and 1 Hz can be generated for use as system clock, microcontroller clock or input to a charge pump. CLKOUT is a CMOS push-pull output, and if disabled it becomes logic 0.

7.0 DEVICE PROTECTION DIAGRAM



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8.0 REGISTER ORGANIZATION

8.1 REGISTER OVERVIEW

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h	Control/Status 1	TEST1	N	STOP	N	TESTC	N	N	N
01h	Control/Status 2	N	N	N	TI/TP	AF	TF	AIE	TIE
02h	Seconds	VL	40	20	10	8	4	2	1
03h	Minutes	X	40	20	10	8	4	2	1
04h	Hours	X	X	20	10	8	4	2	1
05h	Days	X	X	20	10	8	4	2	1
06h	Weekdays	X	X	X	X	X	4	2	1
07h	Months/Century	C	X	X	10	8	4	2	1
08h	Years	80	40	20	10	8	4	2	1
09h	Minute Alarm	AE_M	40	20	10	8	4	2	1
0Ah	Hour Alarm	AE_H	X	20	10	8	4	2	1
0Bh	Day Alarm	AE_D	X	20	10	8	4	2	1
0Ch	Weekday Alarm	AE_W	X	X	X	X	4	2	1
0Dh	CLKOUT Frequency	FE	X	X	X	X	X	FD1	FD0
0Eh	Timer Control	TE	X	X	X	X	X	TD1	TD0
0Fh	Timer	128	64	32	16	8	4	2	1

Bit positions labeled as "X" are not implemented.
Bit positions labeled as "N" should always be written with logic 0.

8.2 CONTROL REGISTERS

8.2.1 CONTROL / STATUS 1 (address 00h…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h	Control/Status 1	TEST1	N	STOP	N	TESTC	N	N	N

Bit	Symbol	Value	Description	Reference
7	TEST1	0 [1)]	Must be set to logic 0 for normal operations	
		1	Test mode	
6	N	0 [2)]	Default value	
5	STOP	0 [1)]	RTC source clock runs	See section 9.5
		1	RTC divider chain flip-flops are asynchronously set to logic 0 The RTC clock is stopped (CLKOUT at 32.768kHz is still available)	
4	N	0 [2)]	Default value	
3	TESTC	0	Must be set to logic 0 for normal operations	
		1 [1)]	Test mode	
2 to 0	N	000 [2)]	Default value	

1) Default value.
2) Bits labeled as "N" should always be written with logic 0.

Note:
The two bits: TEST1 and TESTC are for device testing. Make sure TEST1 and TESTC are set to 0 during normal operation. If accidentally set to 1, they may modify the clock data or result in abnormal time.

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8.2.2 CONTROL / STATUS 2 (address 01h…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
01h	Control/Status 2	N	N	N	TI/TP	AF	TF	AIE	TIE

Bit	Symbol	Value	Description	Reference
7 to 5	N	000 [2)]	Default value	
4	TI/TP	0 [1)]	$\overline{INT}$ is active when TF is active (subject to the status of TIE)	See section 8.6 and 9.1
		1	$\overline{INT}$ pulses active according to 9.1.3 (subject to the status of TIE) Remark: if AF and AIE are active then $\overline{INT}$ will be permanently active	
3	AF	0 [1)]	Alarm flag inactive	See section 9.1
		1	Alarm flag active	
2	TF	0 [1)]	Timer flag inactive	See section 9.1
		1	Timer flag active	
1	AIE	0 [1)]	Alarm interrupt disabled	See section 9.1
		1	Alarm interrupt enabled	
0	TIE	0 [1)]	Timer interrupt disabled	See section 9.1
		1	Timer interrupt enabled	

1) Default value.
2) Bits labeled as "N" should always be written with logic 0.

8.3 TIME AND DATE REGISTERS

8.3.1 SECONDS (address 02h…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
02h	Seconds	VL	40	20	10	8	4	2	1

Bit	Symbol	Value	Description
7	VL	0	Clock integrity is guaranteed
		1 [1)]	Integrity of clock information is not guaranteed
6 to 0	Seconds	0 to 59	These registers hold the current seconds coded in BCD format

1) Startup value.

8.3.2 MINUTES (address 03h…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
03h	Minutes	X	40	20	10	8	4	2	1

Bit	Symbol	Value	Description
7	X	-	Unused
6 to 0	Minutes	0 to 59	These registers hold the current minutes coded in BCD format

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8.3.3 HOURS (address 04h…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
04h	Hours	X	X	20	10	8	4	2	1

Bit	Symbol	Value	Description
7 to 6	X	-	Unused
5 to 0	Hours	0 to 23	These registers hold the current hours coded in BCD format

8.3.4 DAYS (address 05h…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
05h	Days	X	X	20	10	8	4	2	1

Bit	Symbol	Value	Description
7 to 6	X	-	Unused
5 to 0	Days	1 to 31	These registers hold the current day coded in BCD format

8.3.5 WEEKDAYS (address 06h…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
06h	Weekdays	X	X	X	X	X	4	2	1

Bit	Symbol	Value	Description
7 to 3	X	-	Unused
2 to 0	Weekdays	0 to 6	These registers hold the current weekday coded in BCD format

Weekday [1)]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Sunday	X	X	X	X	X	0	0	0
Monday	X	X	X	X	X	0	0	1
Tuesday	X	X	X	X	X	0	1	0
Wednesday	X	X	X	X	X	0	1	1
Thursday	X	X	X	X	X	1	0	0
Friday	X	X	X	X	X	1	0	1
Saturday	X	X	X	X	X	1	1	0

1) Definition may be re-assigned by the user.

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8.3.6 MONTHS/CENTURY (address 07h…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
07h	Months	C	X	X	10	8	4	2	1

Bit	Symbol	Value	Description
7	C [1)]	0 [2)]	Indicates the century is x
		1	Indicates the century is x+1
6 to 5	X	-	unused
4 to 0	Months	1 to 12	These registers hold the current month coded in BCD format

Month	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
January	X	X	X	0	0	0	0	1
February	X	X	X	0	0	0	1	0
March	X	X	X	0	0	0	1	1
April	X	X	X	0	0	1	0	0
May	X	X	X	0	0	1	0	1
June	X	X	X	0	0	1	1	0
July	X	X	X	0	0	1	1	1
August	X	X	X	0	1	0	0	0
September	X	X	X	0	1	0	0	1
October	X	X	X	1	0	0	0	0
November	X	X	X	1	0	0	0	1
December	X	X	X	1	0	0	1	0

1) This bit may be re-assigned by the user.
2) This bit is toggled when the register Years overflows from 99 to 00.

8.3.7 YEARS (address 08h…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
08h	Years	80	40	20	10	8	4	2	1

Bit	Symbol	Value	Description
7 to 0	Years	00 to 99	These registers hold the current year coded in BCD format [1)]

1) When the register Years overflows from 99 to 00, the century bit C in the register Months is toggled.

Note:
The AB-RTCMC-32.768kHz-B5GA-S3 compensates for leap years by adding a 29th day to February if the year counter contains a value which is divisible by 4, including 00.

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Tech-Support@abracon.com

8.4 ALARM REGISTERS

8.4.1 MINUTE ALARM (address 09h…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
09h	Minute Alarm	AE_M	40	20	10	8	4	2	1

Bit	Symbol	Value	Description
7	AE_M	0	Minute alarm is enabled
		1 [1)]	Minute alarm is disabled
6 to 0	Minute Alarm	0 to 59	Minute Alarm information coded in BCD format

1) Default value.

8.4.2 HOUR ALARM (address 0Ah…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Ah	Hour Alarm	AE_H	X	20	10	8	4	2	1

Bit	Symbol	Value	Description
7	AE_H	0	Hour alarm is enabled
		1 [1)]	Hour alarm is disabled
6	X	-	unused
5 to 0	Hour Alarm	0 to 23	Hour Alarm information coded in BCD format

1) Default value.

8.4.3 DAY ALARM (address 0Bh…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Bh	Day Alarm	AE_D	X	20	10	8	4	2	1

Bit	Symbol	Value	Description
7	AE_D	0	Day alarm is enabled
		1 [1)]	Day alarm is disabled
6	X	-	unused
5 to 0	Day Alarm	1 to 31	Day Alarm information coded in BCD format

1) Default value.

8.4.4 WEEKDAY ALARM (address 0Ch…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Ch	Weekday Alarm	AE_W	X	X	X	X	4	2	1

Bit	Symbol	Value	Description
7	AE_W	0	Weekday alarm is enabled
		1 [1)]	Weekday alarm is disabled
6 to 3	X	-	unused
2 to 0	Weekday Alarm	0 to 6	Weekday Alarm information coded in BCD format

1) Default value.

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8.5 CLKOUT REGISTER

A programmable square wave output is available at CLKOUT pin. Operation is controlled by the FE bit in register CLKOUT Frequency and Clock Output Enable pin (CLKOE). To enable CLKOUT, CLKOE pin must be set HIGH.

Frequencies of 32.768 kHz (default), 1024 Hz, 32 Hz and 1 Hz can be generated for use as a system clock, microcontroller clock, input to a charge pump, or for calibration of the oscillator.

8.5.1 CLKOUT FREQUENCY (address 0Dh…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Dh	CLKOUT Frequency	FE	X	X	X	X	X	FD1	FD0

Bit	Symbol	Value	Description
7	FE	0	The CLKOUT output is inhibited and set to logic 0
		1 [1)]	The CLKOUT output is activated
6 to 2	X	-	unused
1 to 0	FD [1:0]	00 [1)] to 11	CLKOUT Frequency selection

CLKOUT Frequency	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
32.768kHz	X	X	X	X	X	X	0	0
1024Hz	X	X	X	X	X	X	0	1
32Hz	X	X	X	X	X	X	1	0
1Hz	X	X	X	X	X	X	1	1

1) Default value.

8.6 TIMER REGISTER

The 8-bit countdown timer register at address 0Fh is controlled by the timer control register at address 0Eh. The Timer Control register determines one of 4 source clock frequencies for the timer (4096 Hz, 64 Hz, 1 sec, or 1/60 Hz) and enables / disables the timer. The timer counts down from a software loaded 8-bit binary value. At the end of every countdown, the timer sets the Timer Flag TF to logic 1. The TF may only be cleared using the interface.

The generation of interrupts from the timer function is controlled via bit TIE (Control / Status 2 register). If bit TIE is enabled, the $\overline{\text{INT}}$ pin follows the condition of bit TF. The interrupt may be generated as a pulsed signal every countdown period or as a permanent active signal which follows the condition of the Timer Flag TF. TI/TP (Control / Status 2 register) is used for this mode control. When reading the timer, the current countdown value is returned.

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8.6.1 TIMER CONTROL (address 0Eh…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Eh	Timer Control	TE	X	X	X	X	X	TD1	TD0

Bit	Symbol	Value	Description
7	TE	0 [1)]	Timer is disabled
		1	Timer is enabled
6 to 2	X	-	unused
1 to 0	TD [1:0]	00 to 11 [1)]	Timer source clock frequency selection [2)]

Timer Frequency	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
4096Hz	X	X	X	X	X	X	0	0
64Hz	X	X	X	X	X	X	0	1
1Hz	X	X	X	X	X	X	1	0
$\frac{1}{60}$ Hz	X	X	X	X	X	X	1	1

1) Default value.
2) These bits determine the source clock frequency for the countdown timer. when not in use, TD1/TD0 should be set to 1/60Hz for power saving.

8.6.2 TIMER (address 0Fh…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Fh	Timer	128	64	32	16	8	4	2	1

Bit	Symbol	Value	Description
7 to 0	Timer	00h to FFh	Countdown value = n $\text{Countdown period} = \frac{n}{\text{Source Clock Frequency}}$

Note:
For accurate read back of the countdown value, the I^2C bus clock (SDA) must be operating at a frequency of at least twice the selected timer clock. Since it is not possible to freeze the countdown timer counter during read back, it is recommended to read the register twice and check for consistent results.

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8.7 REGISTER RESET VALUES

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h	Control/Status 1	0	0	0	0	1	0	0	0
01h	Control/Status 2	0	0	0	0	0	0	0	0
02h	Seconds	1	X	X	X	X	X	X	X
03h	Minutes	X	X	X	X	X	X	X	X
04h	Hours	X	X	X	X	X	X	X	X
05h	Days	X	X	X	X	X	X	X	X
06h	Weekdays	X	X	X	X	X	X	X	X
07h	Months/Century	X	X	X	X	X	X	X	X
08h	Years	X	X	X	X	X	X	X	X
09h	Minute Alarm	1	X	X	X	X	X	X	X
0Ah	Hour Alarm	1	X	X	X	X	X	X	X
0Bh	Day Alarm	1	X	X	X	X	X	X	X
0Ch	Weekday Alarm	1	X	X	X	X	X	X	X
0Dh	CLKOUT Frequency	1	X	X	X	X	X	0	0
0Eh	Timer Control	0	X	X	X	X	X	1	1
0Fh	Timer	X	X	X	X	X	X	X	X

Bit positions labeled as “X” are undefined at power-on and unchanged by subsequent resets.

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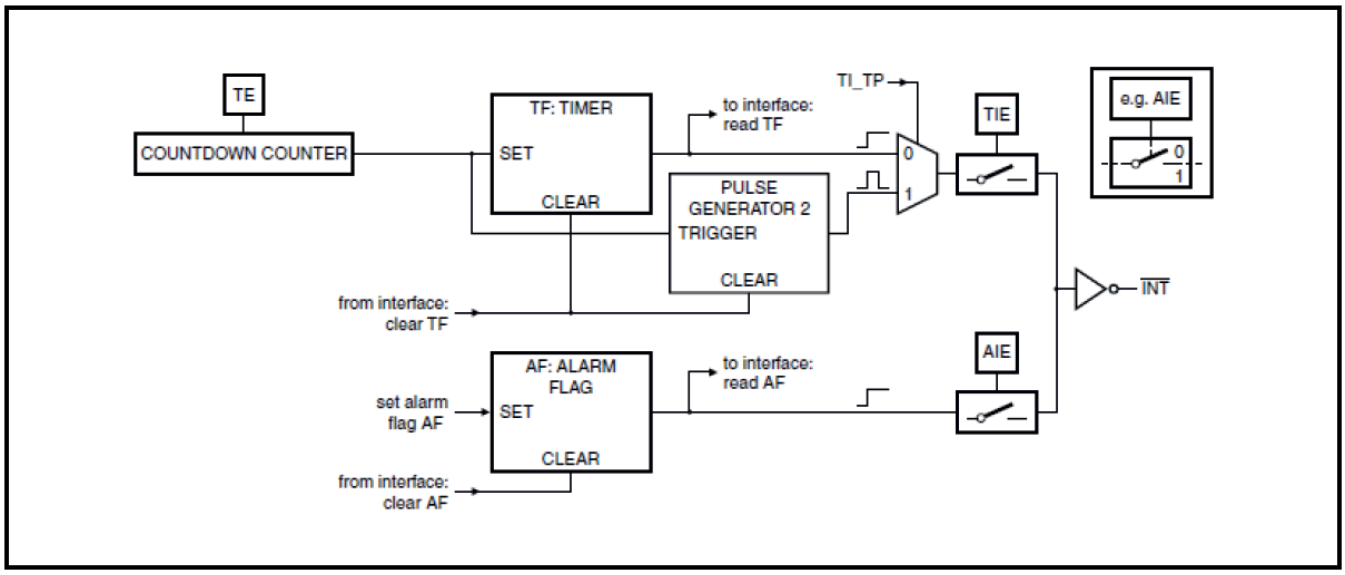
9.0 DETAILED FUNCTIONAL DESCRIPTION

9.1 INTERRUPT OUTPUT

9.1.1 BITS TF AND AF

When an alarm occurs, AF is set to 1. Similarly, at the end of a timer countdown, TF is set to 1. These bits maintain their value unit overwritten using the interface. If both timer and alarm are required in the application, the source of the interrupt can be determined by reading these bits. To prevent one flag being overwritten while clearing another, a logic AND in performed during a write access.



Note:
When bits TIE and AIE are disabled, pin $\overline{INT}$ will remain high-impedance.

9.1.2 BITS TIE AND AIE

These bits activate or deactivate the generation of an interrupt when TF or AF is asserted respectively. The interrupt is the logical OR of these two conditions when both AIE and TIE are set.

9.1.3 COUNTDOWN TIMER INTERRUPT

The pulse generator for the countdown timer interrupt uses an internal clock and is dependent on the selected source clock for the countdown timer and on the countdown value “n”. As a consequence, the width of the interrupt pulse varies.

$\overline{INT}$ operation (bit TI/TP = 1)[1)]

Source Clock	$\overline{INT}$ period [s]	
	n=1 [2)]	n>1
4096Hz	$1/8192$ s	$1/4096$ s
64Hz	$1/128$ s	$1/64$ s
1Hz	$1/64$ s	$1/64$ s
$1/60$ Hz	$1/64$ s	$1/64$ s

1) TF and $\overline{INT}$ become active simultaneously.
2) n = loaded countdown value. Timer is stopped when n = 0.

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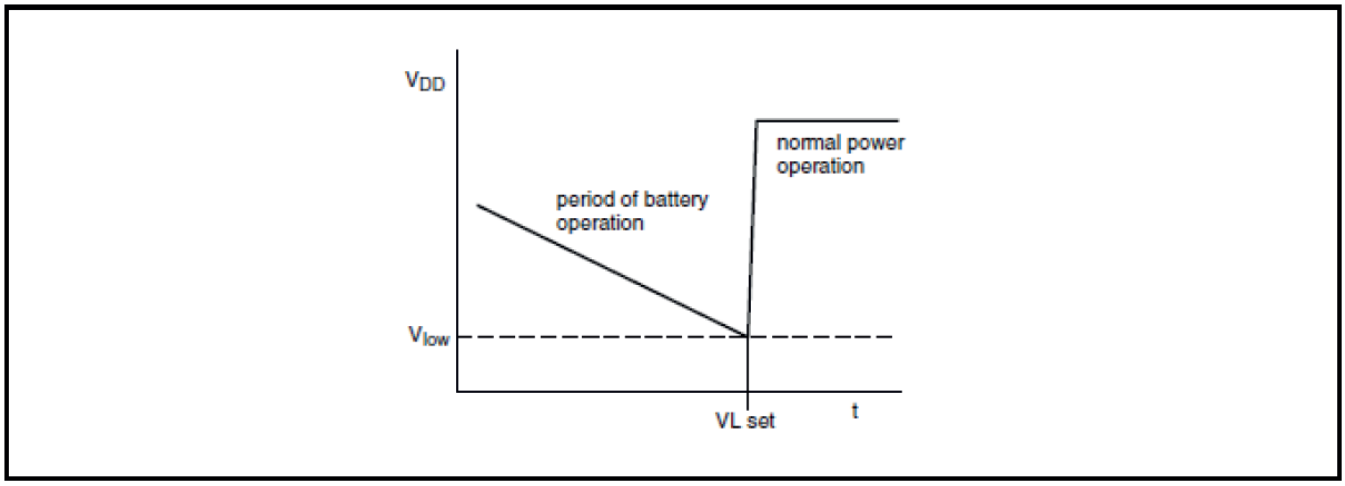
Tech-Support@abracon.com

9.2 VOLTAGE LOW DETECTOR AND CLOCK MONITOR

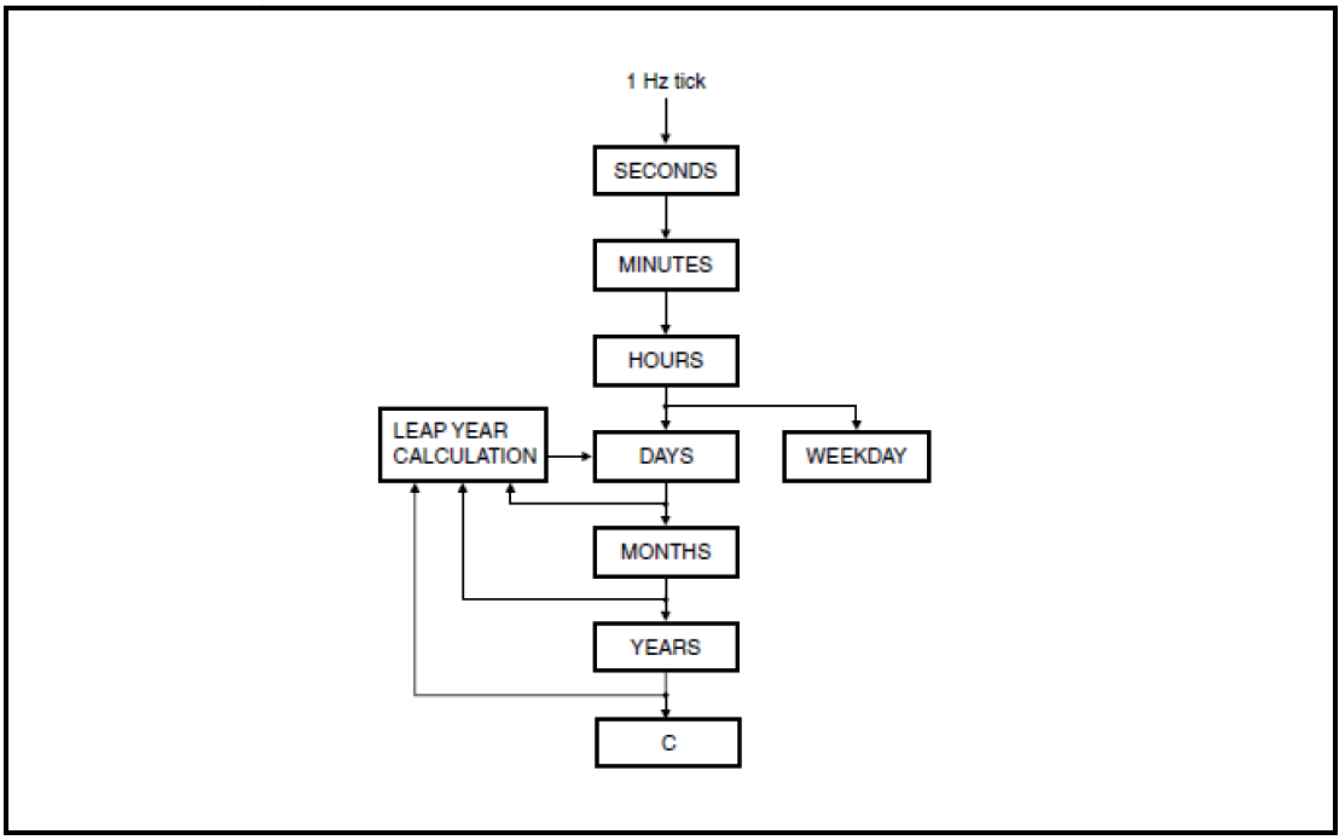
The AB-RTCMC-32.768kHz-B5GA-S3 has an on-chip voltage low detector. When V_{DD} drops below V_{LOW}, the VL (Voltage Low) flag is set to indicate that the integrity of the clock information is no longer guaranteed. The VL flag can only be cleared by using the interface.



The VL flag is intended to detect the situation when V_{DD} is decreasing slowly; for example under battery operation. Should the oscillator stop or V_{DD} reach V_{LOW} before power is reasserted, then the VL flag will be set. This indicates that the time is possibly corrupted.

9.3 SETTING AND READING THE TIME

Data flow and data dependencies starting from 1 Hz clock tick



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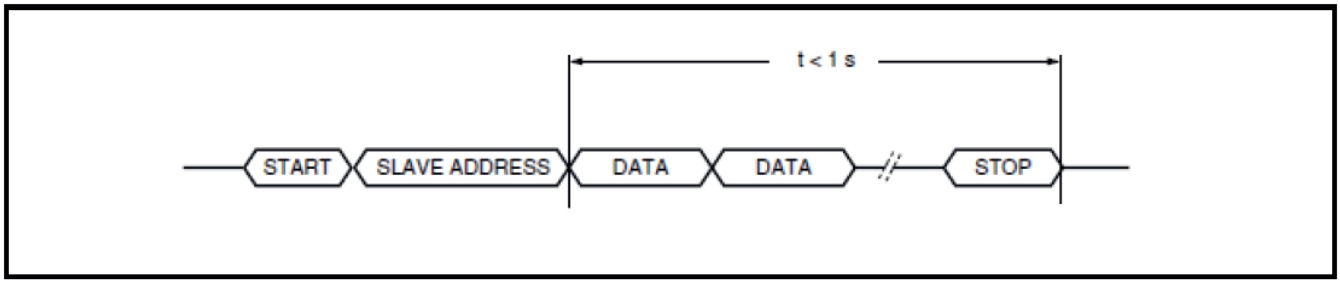
During read / write operations, the time counting circuits (memory locations 02h through 08h) are blocked, in order to prevent the following:

- Faulty writing or reading of the clock and calendar during a carry condition
- Incrementing the time registers during the read cycle

After this read / write access is completed, the time circuit is released again and any pending request to increment the time counters that occurred during the read access is serviced. A maximum of 1 request can be stored; therefore, all accesses must be completed within 1 second.



As a consequence of this method, it is very important to make a read or write access in one go. This means, setting or reading seconds through years should be made in one single access. Failing to comply with this method, could result in the time becoming corrupted.

As an example, if the time (seconds through hours) is set in one access, and then, in a second access the date is set, it is possible that the time may be incremented between the two accesses. A similar problem exists when reading. A roll over may occur between reads thus giving the minutes from one moment and the hours from the next.

Recommended method for reading the time:

1. Send a START condition and the slave address for write (A2h)
2. Set the address pointer to 2 (seconds) by sending 02h
3. Send a RE-START condition or STOP followed by START
4. Send the slave address for read (A3h)
5. Read the seconds
6. Read the minutes
7. Read the hours
8. Read the days
9. Read the weekdays
10. Read the century and months
11. Read the years
12. Send a STOP condition

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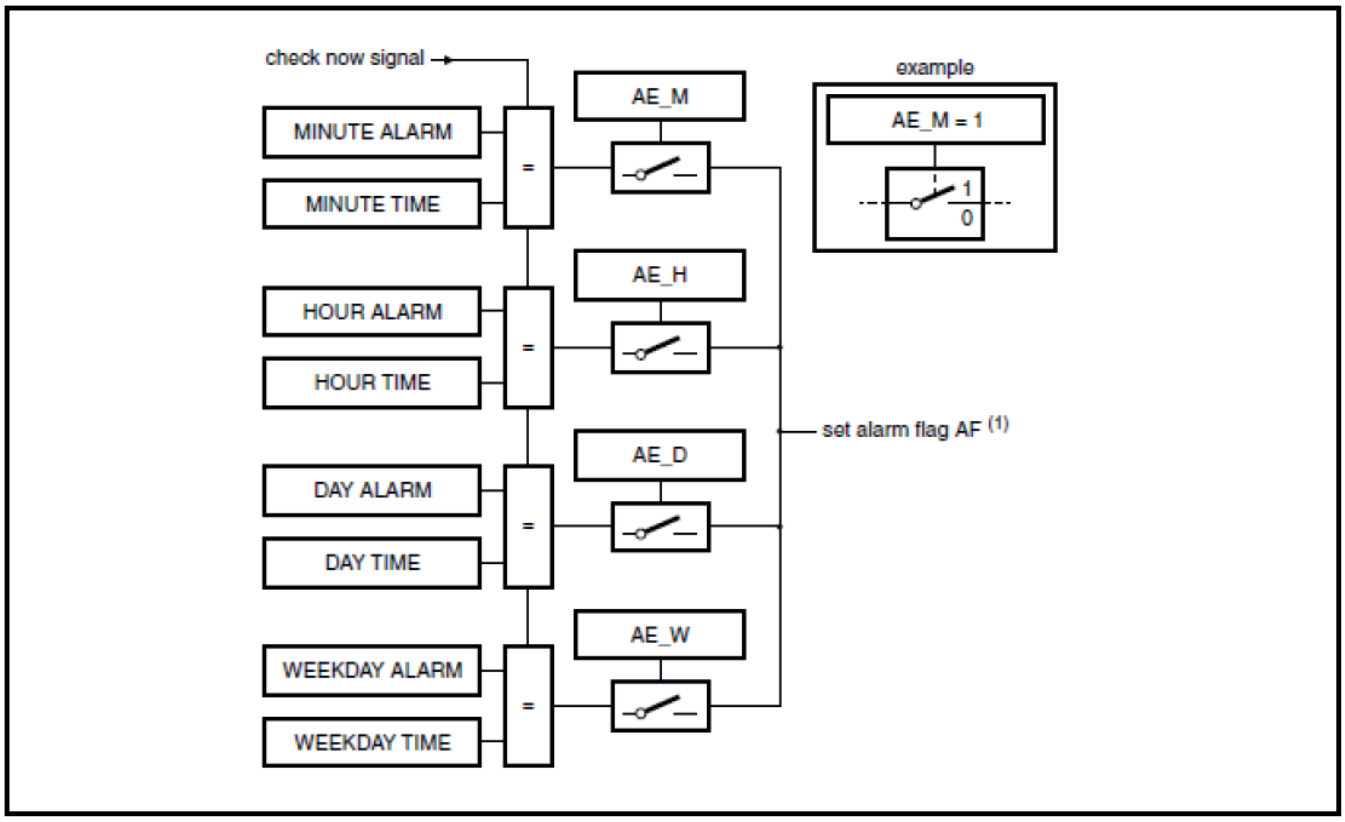
9.4 ALARM FLAG

By clearing the MSB of one or more of the alarm registers AE_x (Alarm Enable), the corresponding alarm condition(s) are active. When an alarm occurs, AF is set to logic 1. The asserted AF can be used to generate an interrupt ($\overline{INT}$). The AF is cleared using the interface.

The registers at addresses 09h through 0Ch contain alarm information. When one or more of these registers is loaded with a valid minute, hour, day or weekday and its corresponding Alarm Enable bit (AE_x) is logic 0, then that information is compared with the current minute, hour, day and weekday. When all enabled comparisons first match, the Alarm Flag (AF in register Control / Status 2) is set to logic 1.

The generation of interrupts from the alarm function is controlled via bit AIE. If bit AIE is enabled, the $\overline{INT}$ pin follows the condition of bit AF. AF will remain set until cleared by the interface. Once AF has been cleared it will only be set again when the time increments to match the alarm condition once more. Alarm registers which have their AE_x bit at logic 1 are ignored.



1) Only when all enabled alarm settings are matching. It's only on increment to a matched case that the alarm flag is set.

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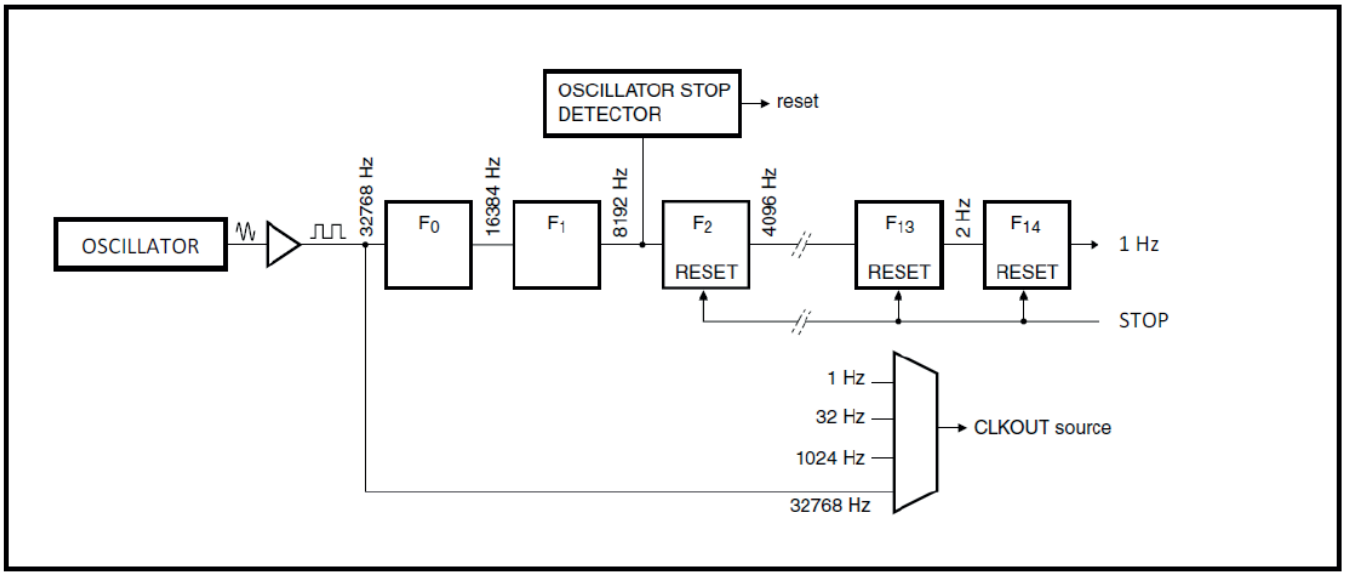
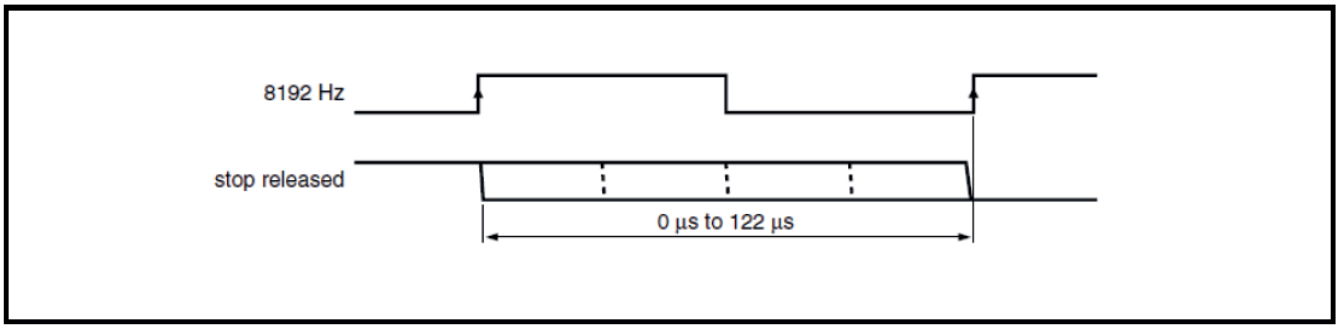
9.5 STOP BIT FUNCTION

The function of the STOP bit is to allow an accurate starting of the time circuits. The STOP bit function will cause the upper part of the prescaler to (F_2 to F_{14}) to be held in reset and thus no 1 Hz ticks will be generated. The time circuits can then be set and will not increment until the STOP bit is released.



The STOP bit function will not affect the 32.768 kHz output on CLKOUT, but will stop the generation of 1024 Hz, 32 Hz and 1 Hz.

The lower two stages of the prescaler (F_0 and F_1) are not reset and as the I^2C bus is asynchronous to the crystal oscillator, the accuracy of re-starting the time circuits will be between zero and one 8192 Hz cycle.



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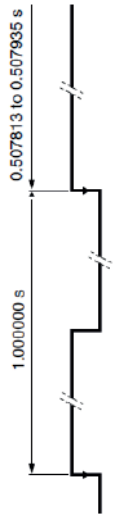
9.5.1 FIRST INCREMENT OF TIME CIRCUITS AFTER STOP BIT RELEASE

Bit	Prescaler Bits [1)]	1Hz Tick	Time	Comment
STOP	$F_0F_1 – F_2$ to F_{14}		hh:mm:ss	
Clock is running normally				
0	01-0 0001 1101 0100		12:45:12	Prescaler counting normally
STOP bit is activated by user. F_0 and F_1 are not reset and values cannot be predicted externally				
1	XX-0 0000 0000 0000		12:45:12	Prescaler is reset; time circuits are frozen
New time is set by user				
1	XX-0 0000 0000 0000		08:00:00	Prescaler is reset; time circuits are frozen
STOP bit is released by user				
0	XX-0 0000 0000 0000		08:00:00	Prescaler is now running
	XX-1 0000 0000 0000		08:00:00	-
	XX-0 1000 0000 0000		08:00:00	-
	XX-1 1000 0000 0000		08:00:00	-
	:		:	:
	11-1 1111 1111 1110		08:00:00	-
	00-0 0000 0000 0001		08:00:01	0 to 1 transition of F_{14} increments the time circuits
	10-0 0000 0000 0001		08:00:01	-
	:		:	:
	11-1 1111 1111 1111		08:00:01	-
	00-0 0000 0000 0000		08:00:01	-
	10-0 0000 0000 0000		08:00:01	-
	:		:	:
	11-1 1111 1111 1110		08:00:01	-
	00-0 0000 0000 0001		08:00:02	0 to 1 transition for F_{14} increments the time circuits

1) F0 is clocked at 32.768 kHz.

The first increment of the time circuits is between 0.507813 s and 0.507935 s after STOP bit is released. The uncertainty is caused by the prescaler bits F_0 and F_1 not being reset and the unknown state of the 32.768 kHz clock.

9.6 RESET

The AB-RTCMC-32.768kHz-B5GA-S3 includes an internal reset circuit which is active whenever the oscillator is stopped. In the reset state, the I^2C bus logic is initialized including the address pointer and all registers are set according to 8.7. I^2C bus communication is not possible during reset.

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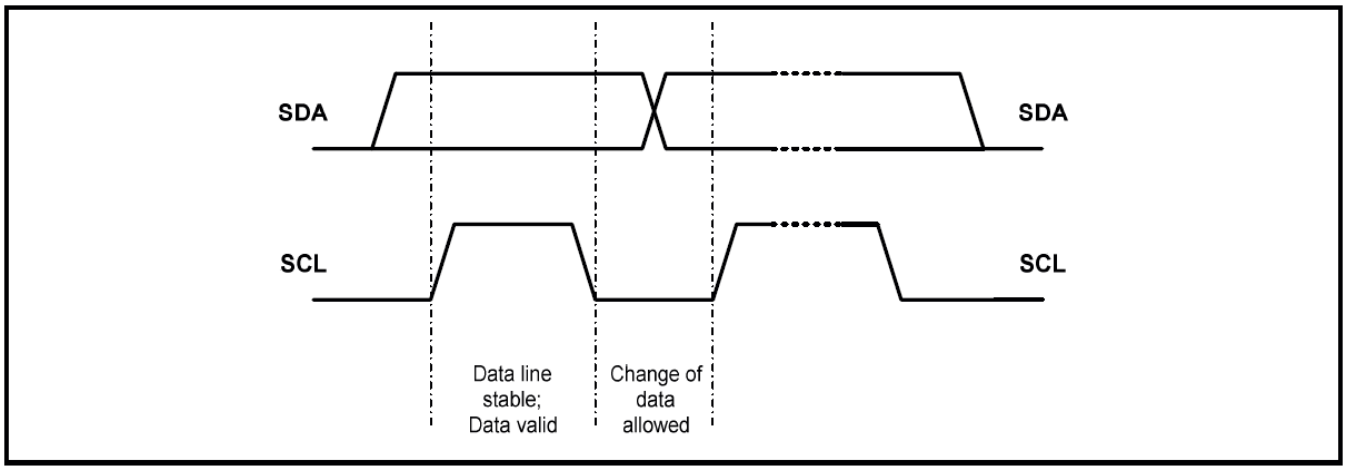
10.0 CHARACTERISTICS OF THE I²C BUS

The I²C bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a Serial Data Line (SDA) and a Serial Clock Line (SCL). Both lines must be connected to a positive supply via pull-up resistors. Data transfer may be initiated only when the bus is not busy.

10.1 BIT TRANSFER

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse, as changes in the data line at this time will be interpreted as a control signal. Data changes should be executed during the LOW period of the clock pulse.

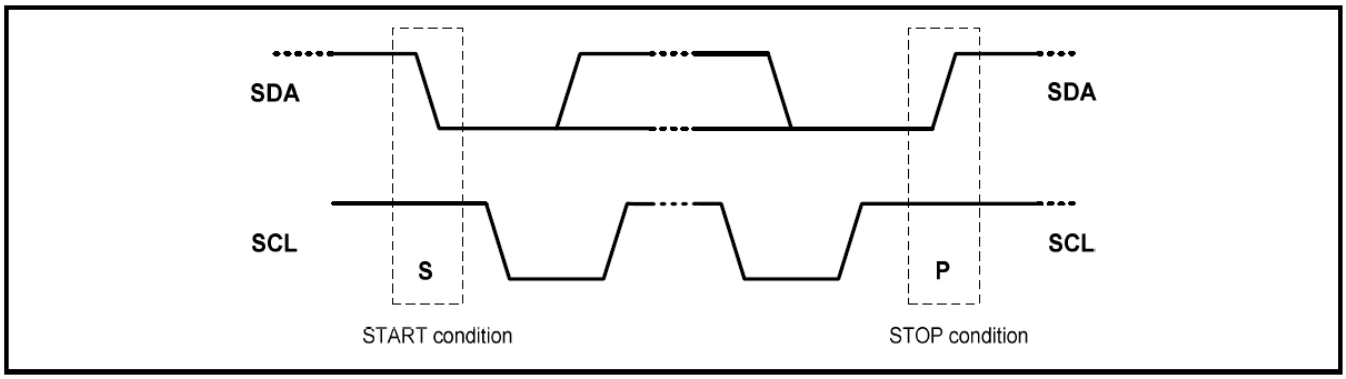


10.2 START AND STOP CONDITIONS

Both SDA data and SCL clock lines remain HIGH when the bus is not busy.

A **HIGH-to-LOW** transition of the data line, while the clock is HIGH, is defined as the START condition (**S**).

A **LOW-to-HIGH** transition of the data line, while the clock is HIGH, is defined as the STOP condition (**P**).



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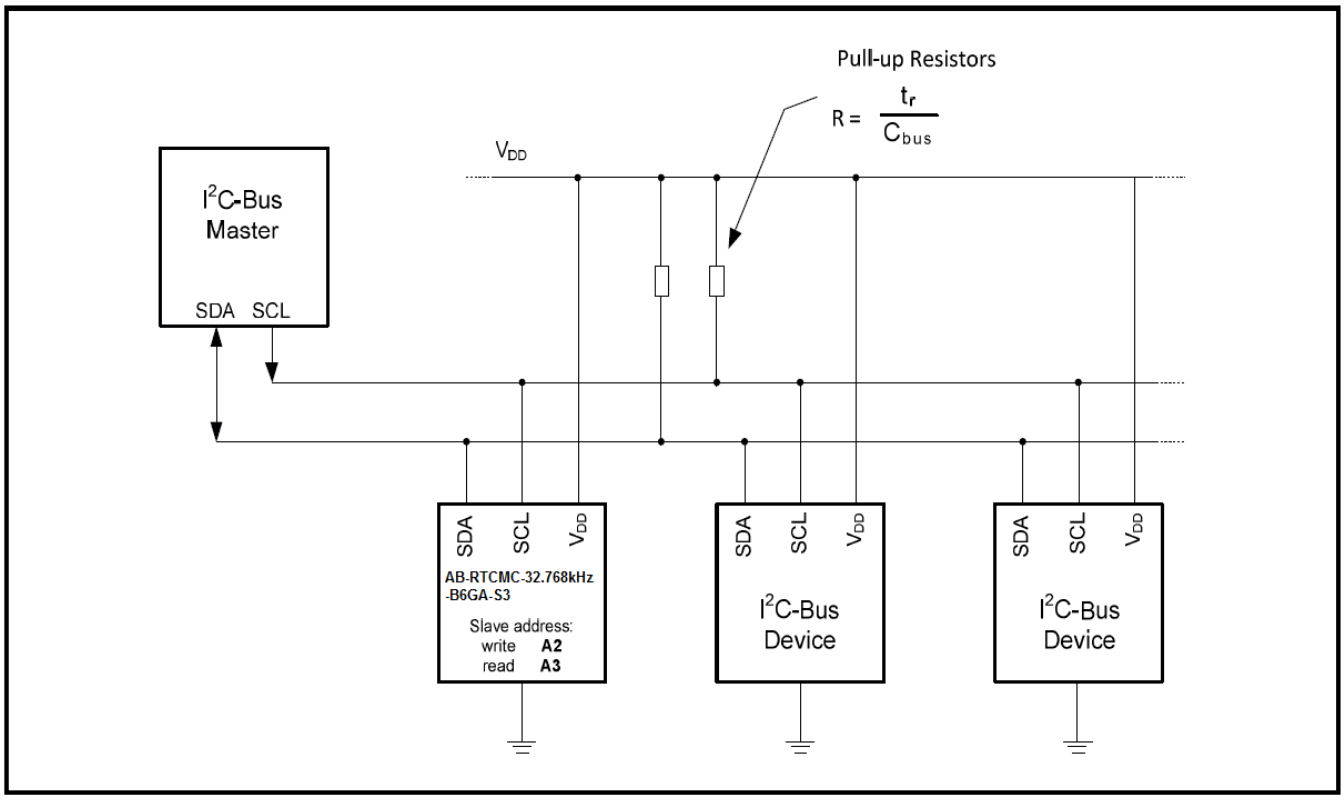
10.3 SYSTEM CONFIGURATION

Since multiple devices can be connected with the I^2C bus, all I^2C bus devices have a fixed and unique device number built-in to allow individual addressing of each device.

The device that controls the I^2C bus is the Master; the devices which are controlled by the Master are the Slaves. A device generating a message is a Transmitter; a device receiving a message is the Receiver. The AB-RTCMC-32.768kHz-B5GA-S3 acts as a Slave-Receiver or Slave-Transmitter.

Before any data is transmitted on the I^2C bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the start procedure. The clock signal SCL is only an input signal, but the data signal SDA is a bidirectional line.



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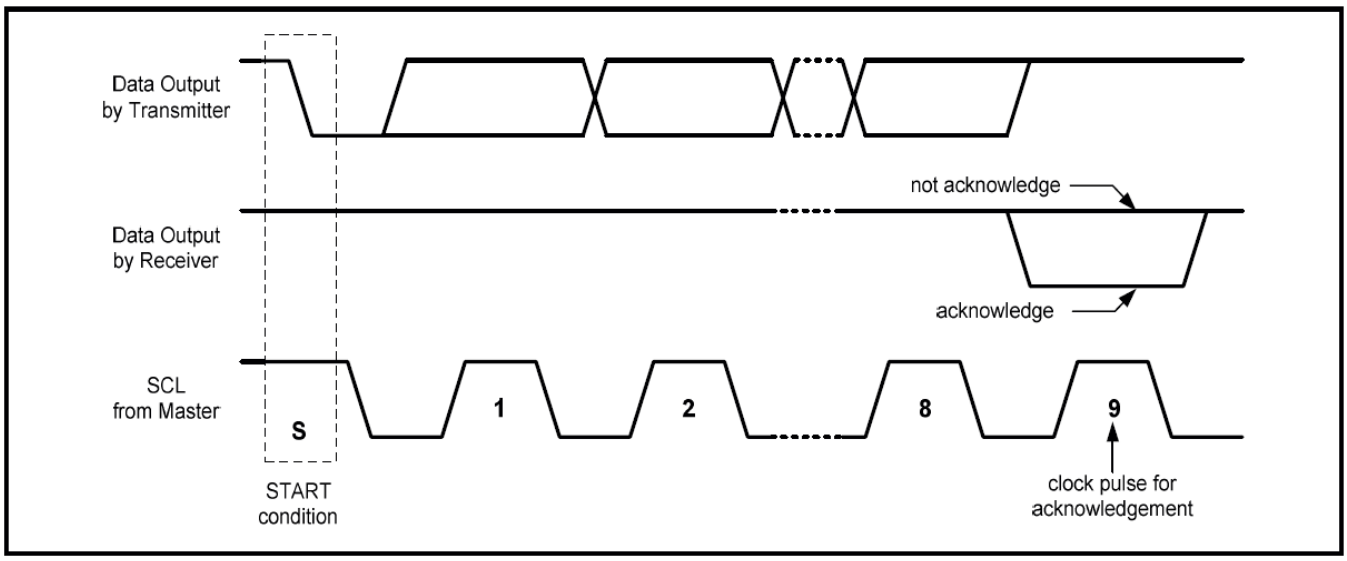
10.4 ACKNOWLEDGE

There is no limit to the numbers of data bytes transmitted between the START and STOP conditions. Each byte (of 8 bits) is followed by an acknowledge cycle. Therefore, the Master generates an extra acknowledge clock pulse.

The acknowledge bit is a HIGH level signal put on the SDA line by the Transmitter-Device, the Receiver-Device must pull down the SDA line during the acknowledge clock pulse to confirm the correct reception of the last byte.

Either a Master-Receiver or a Slave-Receiver which is addressed must generate an acknowledge after the correct reception of each byte. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (setup and hold times must be taken into consideration).

If the Master is addressed as Receiver, it can stop data transmission by not generating an acknowledge on the last byte that has been sent from the Slave-Transmitter. In this event, the Slave-Transmitter must leave the data line HIGH to enable the Master to generate a STOP condition.



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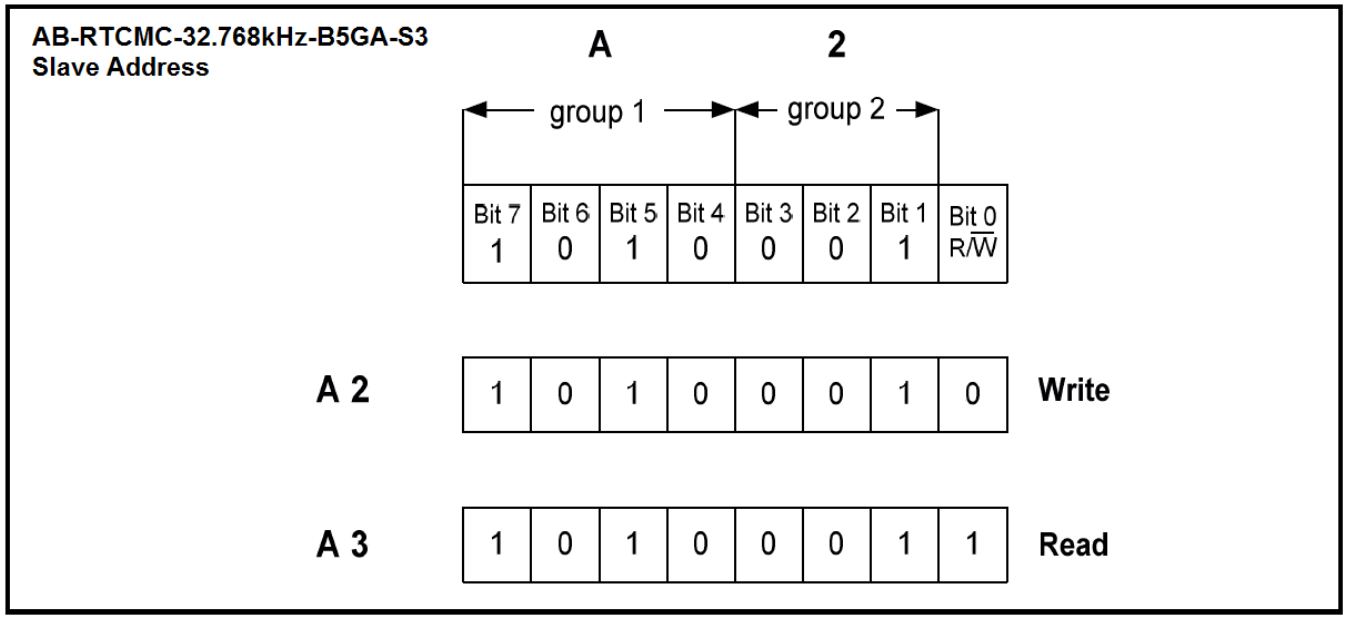
11.0 I²C BUS PROTOCOL

11.1 ADDRESSING

Before any data is transmitted on the I²C bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the start procedure.

The AB-RTCMC-32.768kHz-B5GA-S3 acts as a Slave-Receiver or Slave-Transmitter. Therefore, the clock signal SCL is only an input signal, but the data signal SDA is a bidirectional line.

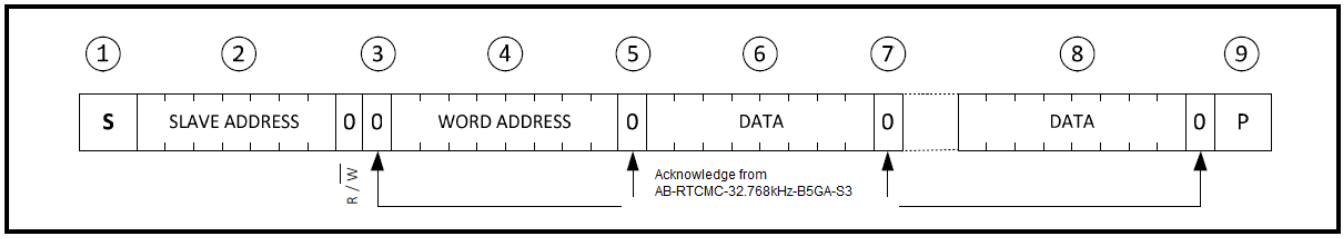


11.2 CLOCK AND CALENDAR READ AND WRITE CYCLES

11.2.1 WRITE MODE

Master transmits to Slave-Receiver at specified address. The Word Address is 4-bit value that defines which register is to be accessed next. The upper four bits of the Word Address are not used. After reading or writing one byte, the Word Address is automatically incremented by 1.

1) Master sends out the "Start Condition".
2) Master sends out the "Slave Address", A2h for the AB-RTCMC-32.768kHz-B5GA-S3; the R/$\overline{W}$ bit in write mode.
3) Acknowledgement from the AB-RTCMC-32.768kHz-B5GA-S3.
4) Master sends out the "Word Address" to the AB-RTCMC-32.768kHz-B5GA-S3.
5) Acknowledgement from the AB-RTCMC-32.768kHz-B5GA-S3.
6) Master sends out the "data" to write to the specified address in step 4).
7) Acknowledgement from the AB-RTCMC-32.768kHz-B5GA-S3.
8) Steps 6) and 7) can be repeated if necessary. The address will be incremented automatically in the AB-RTCMC-32.768kHz-B5GA-S3.
9) Master sends out the "Stop Condition".



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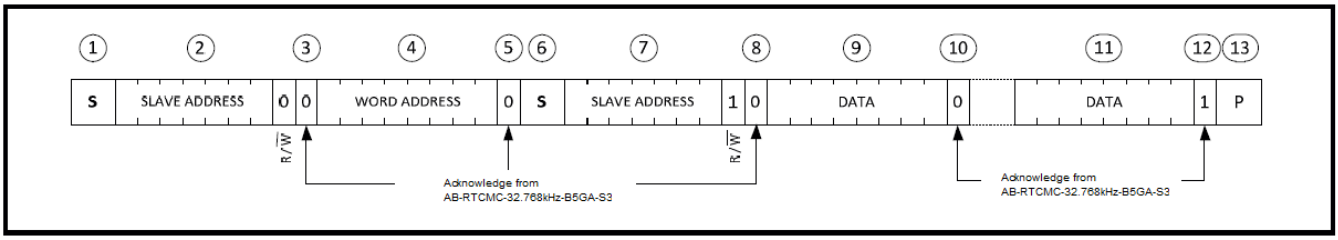
11.2.2 READ MODE AT SPECIFIC ADDRESS

Master reads data after setting Word Address

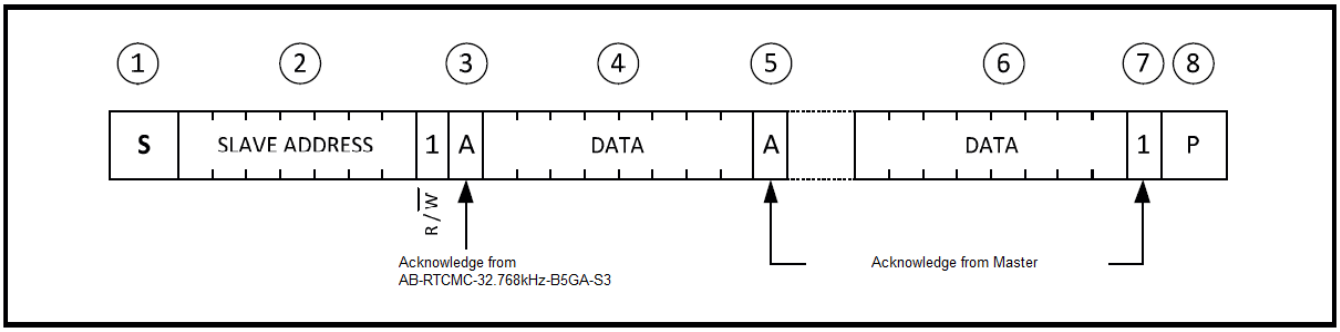
1) Master sends out the "Start Condition".
2) Master sends out the "Slave Address", A2h for the AB-RTCMC-32.768kHz-B5GA-S3; the R/$\overline{W}$ bit in write mode.
3) Acknowledgement from the AB-RTCMC-32.768kHz-B5GA-S3.
4) Master sends out the "Word Address" to the AB-RTCMC-32.768kHz-B5GA-S3.
5) Acknowledgement from the AB-RTCMC-32.768kHz-B5GA-S3.
6) Master sends out the "Start Condition". "Stop Condition" has not been sent.
7) Master sends out the "Slave Address", A3h for the AB-RTCMC-32.768kHz-B5GA-S3; the R/$\overline{W}$ bit in read mode.
8) Acknowledgement from the AB-RTCMC-32.768kHz-B5GA-S3. At this point, the Master becomes a Receiver, the Slave becomes the Transmitter.
9) The Slave sends out the "data" from the Word Address specified in step 4).
10) Acknowledgement from the Master.
11) Steps 9) and 10) can be repeated if necessary. The address will be incremented automatically in the AB-RTCMC-32.768kHz-B5GA-S3.
12) The Master, addressed as Receiver, can stop data transmission by not generating an acknowledge on the last byte that has been sent from the Slave-Transmitter. In this event, the Slave-Transmitter must leave the data line HIGH to enable the Master to generate a stop condition.
13) Master sends out the "Stop Condition".



11.2.3 READ MODE

Master reads Slave-Transmitter immediately after first byte

1) Master sends out the "Start Condition".
2) Master sends out the "Slave Address", A3h for the AB-RTCMC-32.768kHz-B5GA-S3; the R/$\overline{W}$ bit in read mode.
3) Acknowledgement from the AB-RTCMC-32.768kHz-B5GA-S3. At this point, the Master becomes a Receiver, the Slave becomes the Transmitter
4) The AB-RTCMC-32.768kHz-B5GA-S3sends out the "data" from the last accessed Word Address incremented by 1.
5) Acknowledgement from the Master.
6) Steps 4) and 5) can be repeated if necessary. The address will be incremented automatically in the AB-RTCMC-32.768kHz-B5GA-S3.
7) The Master, addressed as Receiver, can stop data transmission by not generating an acknowledge on the last byte that has been sent from the Slave-Transmitter. In this event, the Slave-Transmitter must leave the data line HIGH to enable the Master to generate a stop condition.
8) Master sends out the "Stop Condition".



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11.3 INTERFACE WATCHDOG TIMER

During read/write operations, the time counting circuits are frozen. To prevent a situation where the accessing device becomes locked and does not clear the interface, the AB-RTCMC-32.768kHz-B5GA-S3 has a built in watchdog timer. Should the interface be active for more than 1 s from the time a valid slave address is transmitted, then the AB-RTCMC-32.768kHz-B5GA-S3will automatically clear the interface and allow the time counting circuits to continue counting.

The watchdog is implemented to prevent the excessive loss of time due to interface access failure e. g. if main power is removed from a battery backup system during an interface access.

Each time the watchdog period is exceeded, 1 s will be lost from the time counters. The watchdog will trigger between 1 s and 2 s after receiving a valid slave address.

12.0 ABSOLUTE MAXIMUM RATING

Parameters	Symbol	Conditions	Min.	Max.	Units
Supply Voltage	V_{DD}	>GND / <V_{DD}	-0.5	+6.5	V
Input Voltage	V_I	Input Pin	V_{SS}-0.5	V_{DD} +0.5	V
Output Voltage	V_O	$\overline{INT}$ pin	V_{SS} -0.5	V_{DD} +0.5	V
Supply Current	I_{DD}; I_{SS}	V_{DD} Pin	-50	+50	mA
DC Input Current	I_I		-10	+10	mA
DC Output Current	I_O		-10	+10	mA
Electro Static Discharge Voltage	V_{ESD}	HBM [1)] MM [2)]		±3500 ±250	V
Latch-up Current	I_{LU}	All pins [3)]		100	mA
Operating Ambient Temperature Range	T_{OPR}		-40	+85	ºC
Storage Temperature Range	T_{STO}	Stored as bard product	-55	+125	ºC

1) Pass level; Human Body Model (HBM), according to JESD22-A114.
2) Pass level; Machine Model (MM), according to JESD22-A115.
3) Pass level; latch-up testing, according to JESD78 at maximum ambient temperature (Tamb(max) = +85°C).

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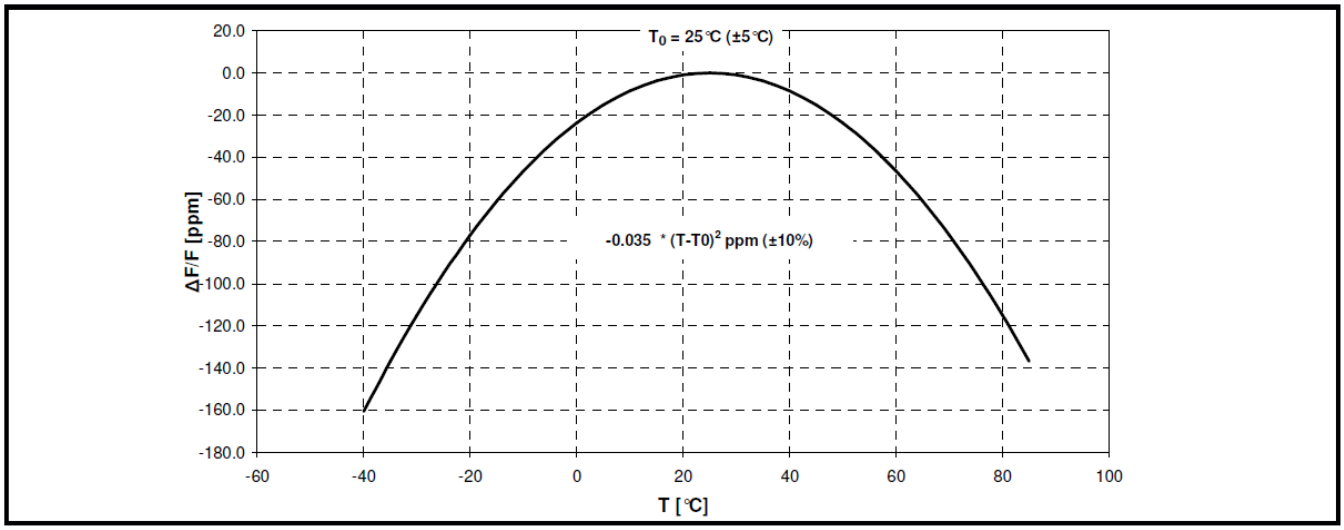
13.0 FREQUENCY CHARACTERISTICS

Parameters	Symbol	Conditions	Typ.	Max.	Units
Frequency Precision	ΔF/F	T_{AMB}=+25°C; V_{DD}=3.0V	±10	±20	ppm
Frequency vs Voltage Characteristics	ΔF/V	T_{AMB}=+25°C; V_{DD}=1.8~5.5V	±0.8	±1.5	ppm/V
Frequency vs Temp. Characteristics	$\Delta F/F_{OPR}$	T_{ref}=+25°C; V_{DD}=3.0V	-0.035ppm/°C^2 (T_{OPR}-T_O)^2 ±10%		ppm
Turnover Temperature	T_O		+25	±5	°C
Aging first year	ΔF/F	At +25°C		±3	ppm
Oscillation Start-up Time	T_{START}	At +25°C	350	500	ms
CLKOUT duty cycle	δ_{CLKOUT}	At +25°C	50	40/60	%

13.1 FREQUENCY VS. TEMPERATURE CHARACTERISTICS



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14.0 DC CHARACTERISTICS

Parameters	Symbol	Conditions	Min.	Typ.	Max.	Units
Supplies						
Supply Voltage	V_{DD}	I^2C bus inactive T_{AMB}=+25°C	1.2		5.5	V
		I^2C bus active f_{SCL}=400kHz	1.8		5.5	
		For clock data integrity T_{AMB}=+25°C	V_{LOW}		5.5	
Current Consumption I^2C bus active	I_{DDO}	f_{SCL}=400kHz			800	µA
		f_{SCL}=100kHz			200	µA
Current Consumption 1) 2) 3) I^2C bus inactive (f_{SCL}=0Hz) CLKOUT disabled T_{amb}= +25°C	I_{DD}	V_{DD} = 5.0V 2)		275	550	nA
		V_{DD} = 3.0V 2)		250	500	nA
		V_{DD} = 2.0V 2)		225	450	nA
Current Consumption 1) 2) 3) I^2C bus inactive (f_{SCL}=0Hz) CLKOUT disabled T_{OPR}= -40 ~ +85°C	I_{DD}	V_{DD} = 5.0V		500	750	nA
		V_{DD} = 3.0V		400	650	nA
		V_{DD} = 2.0V		400	600	nA
Current Consumption 3) I^2C bus inactive (f_{SCL}=0Hz) CLKOUT enabled (32.768kHz) Load = 7.5pF/T_{amb}= +25°C	I_{DD32k}	V_{DD} = 5.0V		2.5	3.4	µA
		V_{DD} = 3.0V		1.5	2.2	µA
		V_{DD} = 2.0V		1.1	1.6	µA
Inputs						
LOW Level Input Voltage	V_{IL}		V_{SS}-0.5		30%V_{DD}	V
HIGH Level Input Voltage	V_{IH}		70%V_{DD}		V_{DD}+0.5	V
Input Leakage Current	I_L	V_I= V_{DD} or V_{SS}	-1	0	+1	µA
Input Capacitance 4)	C_I				7	pF
Outputs						
LOW Level Output Current V_{OL} = 0.4V; V_{DD} = 5V	I_{OL}	Pin: SDA			-3	mA
		Pin: $\overline{INT}$			-1	mA
		Pin: CLKOUT			-1	mA
HIGH Level Output Current V_{OH} = 4.6V; V_{DD} = 5V	I_{OH}	Pin: CLKOUT			1	mA
Output Leakage Current	I_{LO}	V_O = V_{DD} or V_{SS}	-1	0	+1	µA
Operating Temperature Range						
Operating Temperature Range	T_{OPR}		-40		+85	°C
Voltage Detector						
Low Voltage	V_{LOW}	T_{AMB}=+25°C		0.9	1.0	V

1) Timer source clock = 1/60 Hz.
2) CLKOUT disabled (FE = 0 or CLKOE = 0).
3) V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.
4) Tested on sample basis.

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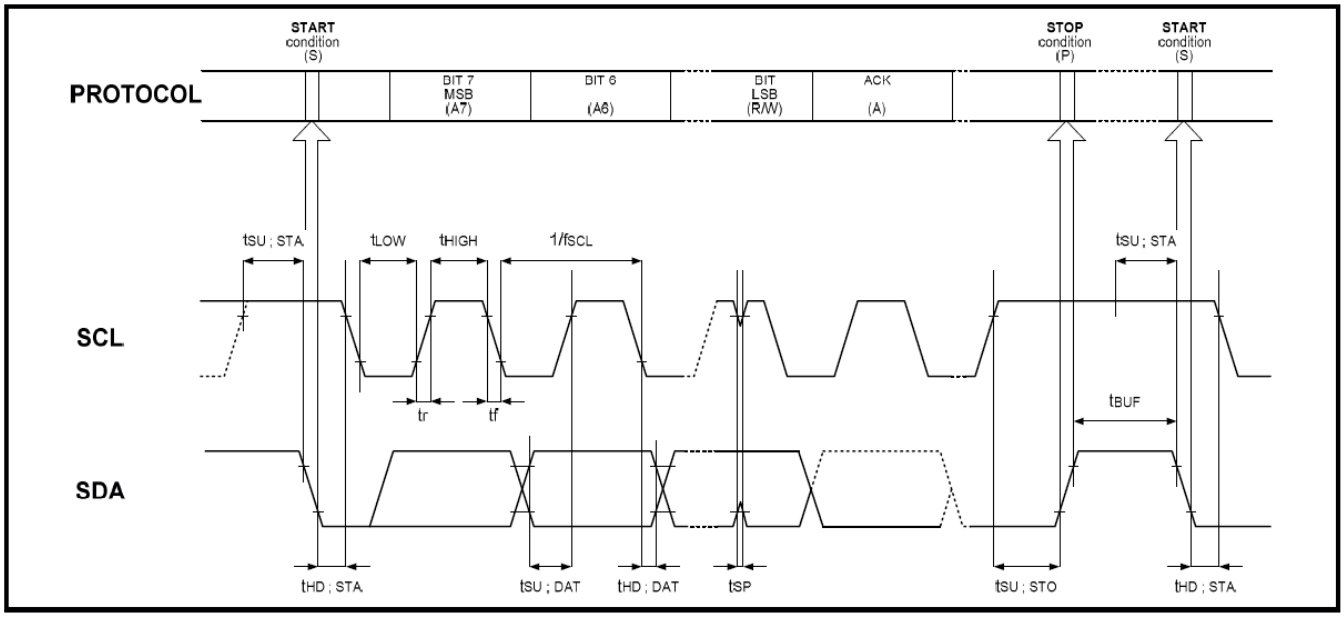
15.0 I²C BUS TIMING CHARACTERISTICS

Parameters [1)]	Symbol	Min.	Typ.	Max.	Units
SCL clock frequency	f_{SCL}			400	kHz
Hold time (repeated) START condition	$t_{HD;STA}$	0.6			µs
Setup time for repeated START condition	$t_{SU;STA}$	0.6			µs
LOW period of SCL clock	t_{LOW}	1.3			µs
HIGH period of SCL clock	t_{HIGH}	0.6			µs
Bus free time between STOP and START condition	t_{BUF}	1.3			µs
Rise time of both SDA and SCL signals	t_r			0.3	µs
Fall time of both SDA and SCL signals	t_f			0.3	µs
Capacitive load for each bus line	C_b			400	pF
Data setup time	$t_{SU;DAT}$	100			ns
Data hold time	$t_{HD;DAT}$	0			ns
Setup time for STOP condition	$t_{SU;STO}$	0.6			µs
Spike pulse width	$t_{w(spike)}$			50	ns

1) All timing values are valid within the operating supply voltage at ambient temperature and referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

15.1 TIMING CHART



Note:
The I²C BUS access time between a START and a START condition or between a START and a STOP condition to this device must be less than one second.

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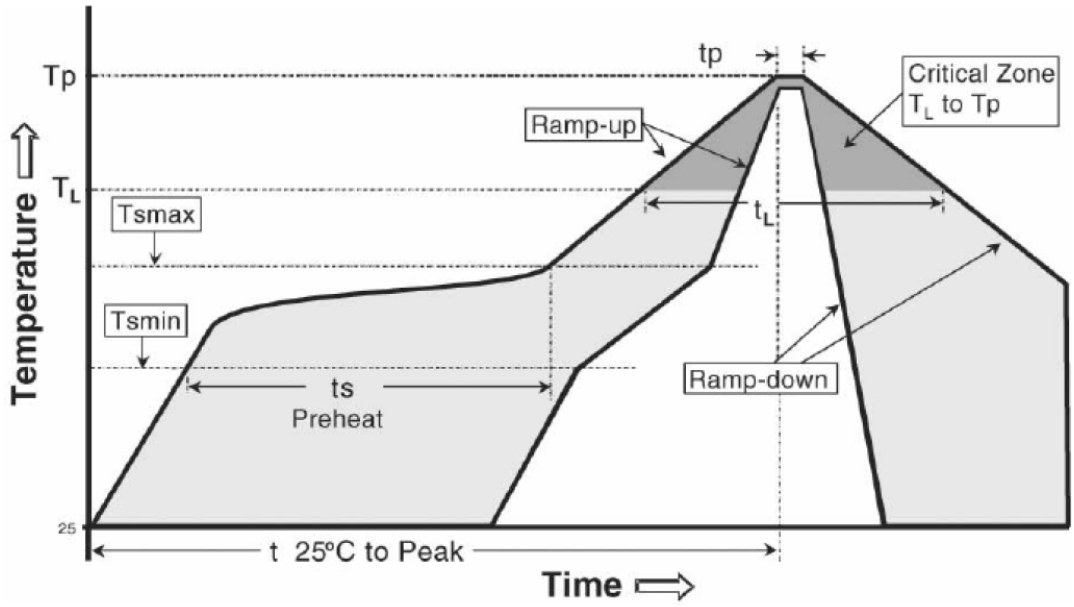
16.0 RECOMMENDED REFLOW TEMPERATURE (LEADFREE SOLDERING)

Maximum Reflow Conditions in accordance with IPC/JEDEC J-STD-020C "Pb-free"



Temperature	Symbol	Conditions	Units
Average Ramp-up Rate	T_{Smax} to T_P	3°C/second max	°C/s
Ramp Down Rate	T_{cool}	6°C/second max	°C/s
Time 25°C to Peak Temperature	$T_{to\text{-}peak}$	8 minutes max	m
Preheat			
Temperature Min	T_{Smin}	150	°C
Temperature Max	T_{Smax}	200	°C
Time Ts_{min} to Ts_{max}	ts	60 ~ 180	sec
Time Above Liquidus			
Temperature Liquidus	T_L	217	°C
Time above Liquidus	t_L	60 ~150	sec
Peak Temperature			
Peak Temperature	T_P	260	°C
Time within 5°C of Peak Temperature	t_P	20 ~ 40	sec

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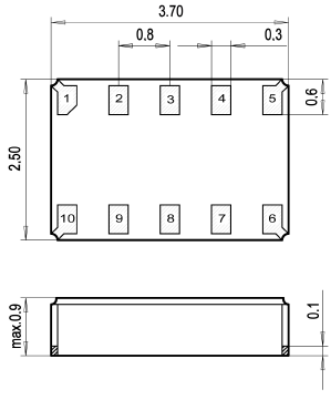
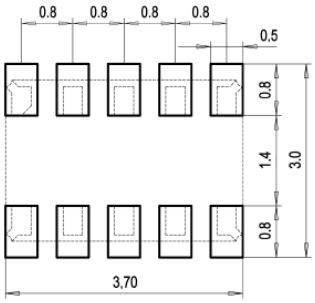
17.0 PACKAGES

17.1 DIMENSIONS AND SOLDERPADS LAYOUT

Package dimensions (bottom view):

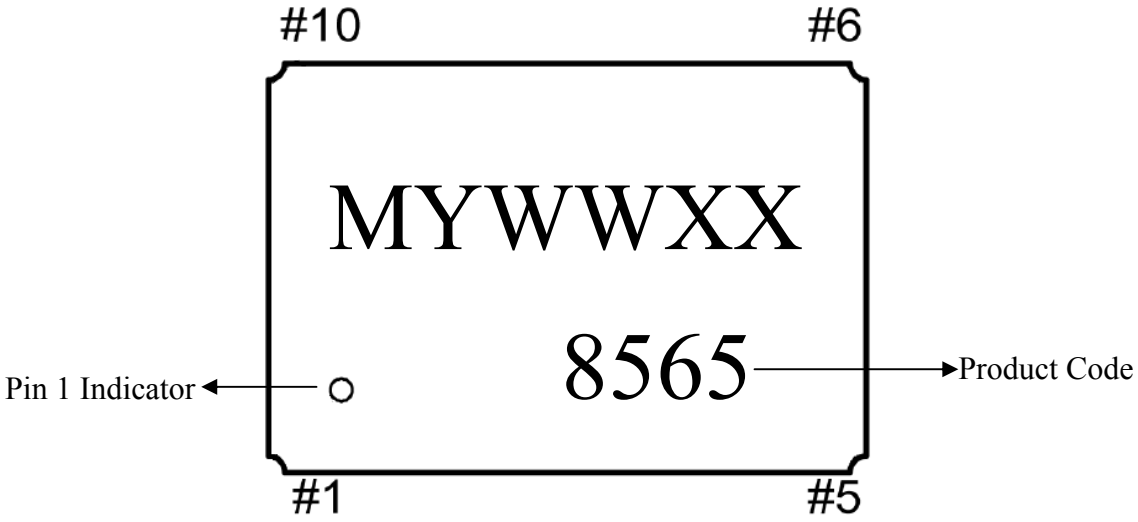


Recommended solderpad layout:



All dimensions are in mm.

17.2 MARKING AND PIN #1 INDEX



M: Internal Code
Y: Year. e.g. 3 for 2013
WW: Week. e.g 08 for the 8th week of the year
XX: Lot Code

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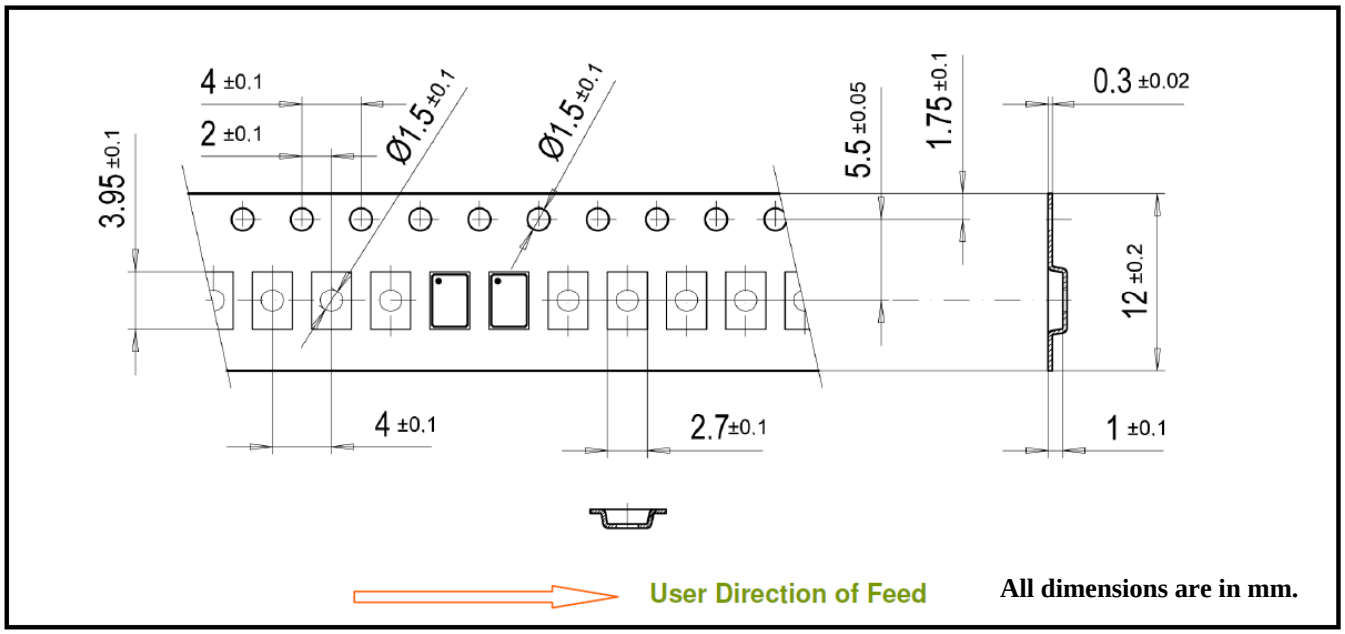
18.0 PACKING INFO

18.1 CARRIER TAPE

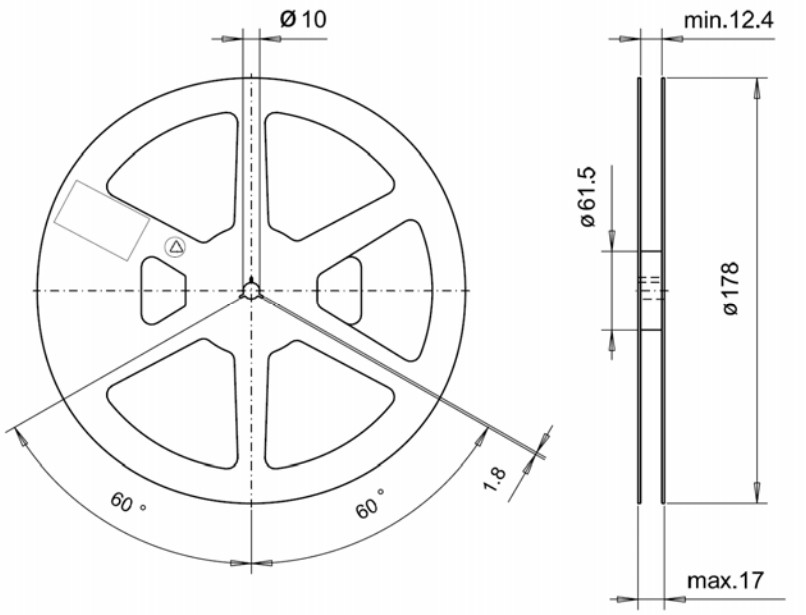
12 mm Carrier-Tape:	Material:	Polystyrene / Butadine or Polystyrol black, conductive
Cover Tape:	Base Material:	Polyester, conductive 0.061 mm
	Adhesive Material:	Pressure-sensitive Synthetic Polymer



Tape Leader and Trailer: 300 mm minimum.

18.2 REEL 7 INCH FOR 12MM TAPE

7" Reel:	Material:	Plastic, Polystyrol
	Qty/Reel:	1000pcs



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19.0 HANDLING PRECAUTIONS FOR CRYSTALS OR MODULES WITH EMBEDDED CRYSTALS

The built-in tuning-fork crystal consists of pure Silicon Dioxide in crystalline form. The cavity inside the package is evacuated and hermetically sealed in order for the crystal blank to function undisturbed from air molecules, humidity and other influences.

Shock and vibration

Keep the crystal from being exposed to **excessive mechanical shock and vibration**. Abracon guarantees that the crystal will bear a mechanical shock of 5000g / 0.3 ms.
The following special situations may generate either shock or vibration:

Multiple PCB panels - Usually at the end of the pick & place process the single PCBs are cut out with a router. These machines sometimes generate vibrations on the PCB that have a fundamental or harmonic frequency close to 32.768 kHz. This might cause breakage of crystal blanks due to resonance. Router speed should be adjusted to avoid resonant vibration.

Ultrasonic Cleaning - Avoid cleaning processes using ultrasonic energy. These processes can damages crystals due to mechanical resonance of the crystal blank.

Overheating, rework high-temperature-exposure

Avoid overheating the package. The package is sealed with a sealring consisting of 80% Gold and 20% Tin. The eutectic melting temperature of this alloy is at 280°C. Heating the sealring up to >280°C will cause melting of the metal seal which then, due to the vacuum, is sucked into the cavity forming an air duct. This happens when using hot-air-gun set at temperatures >300°C.

Use the following methods for re-work:

- Use a hot-air- gun set at 270°C
- Use 2 temperature-controlled soldering irons, set at 270°C, with special-tips to contact all solder-joints from both sides of the package at the same time, remove part with tweezers when pad solder is liquid.