STQ1NK80ZR-AP - STN1NK80Z
STD1NK80Z - STD1NK80Z-1

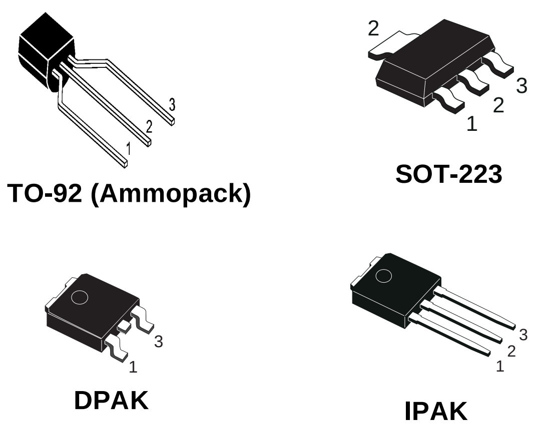
N-CHANNEL 800V - 13 Ω - 1 A TO-92 /SOT-223/DPAK/IPAK
Zener - Protected SuperMESH™ MOSFET

Table 1: General Features

TYPE	V_{DSS}	$R_{DS(on)}$	I_D	Pw
STQ1NK80ZR-AP	800 V	< 16 Ω	0.3 A	3 W
STN1NK80Z	800 V	< 16 Ω	0.25A	2.5 W
STD1NK80Z	800 V	< 16 Ω	1.0 A	45 W
STD1NK80Z-1	800 V	< 16 Ω	1.0 A	45 W

- TYPICAL R_{DS}(on) = 13Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- ESD IMPROVED CAPABILITY
- 100% AVALANCHE TESTED
- NEW HIGH VOLTAGE BENCHMARK
- GATE CHARGE MINIMIZED

Figure 1: Package



DESCRIPTION

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOS-FETs including revolutionary MDmesh™ products.

APPLICATIONS

- AC ADAPTORS AND BATTERY CHARGERS
- SWITH MODE POWER SUPPLIES (SMPS)

Figure 2: Internal Schematic Diagram

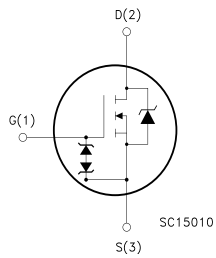


Table 2: Order Codes

SALES TYPE	MARKING	PACKAGE	PACKAGING
STQ1NK80ZR-AP	Q1NK80ZR	TO-92	AMMOPAK
STN1NK80Z	N1NK80Z	SOT-223	TAPE & REEL
STD1NK80ZT4	D1NK80Z	DPAK	TAPE & REEL
STD1NK80Z-1	D1NK80Z	IPAK	TUBE

Rev. 3

Table 3: Absolute Maximum ratings

Symbol	Parameter	Value			Unit
		TO-92	SOT-223	DPAK/IPAK	
V_{DS}	Drain-source Voltage (V_{GS} = 0)	800			V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	800			V
V_{GS}	Gate- source Voltage	± 30			V
I_D	Drain Current (continuous) at T_C = 25°C	0.3	0.25	1.0	A
I_D	Drain Current (continuous) at T_C = 100°C	0.19	0.16	0.63	A
I_{DM} (•)	Drain Current (pulsed)	5			A
P_{TOT}	Total Dissipation at T_C = 25°C	3	2.5	45	W
	Derating Factor	0.025	0.02	0.36	W /°C
$V_{ESD(G-S)}$	Gate source ESD (HBM-C= 100pF, R= 1.5KΩ)	1000			V
dv/dt (1)	Peak Diode Recovery voltage slope	4.5			V/ns
T_j T_{stg}	Operating Junction Temperature Storage Temperature	-55 to 150			°C

(●) Pulse width limited by safe operating area
(1) $I_{SD} \leq 1$ A, di/dt ≤ 200 A/µs, $V_{DD} \leq 640$

Table 4: Thermal Data

		TO-92	SOT-223	DPAK/IPAK	Unit
Rthj-case	Thermal Resistance Junction-case Max	--	--	2.78	°C/W
Rthj-amb(#)	Thermal Resistance Junction-ambient Max	120	50	100	°C/W
Rthj-lead	Thermal Resistance Junction-lead Max	40	--	--	°C/W
T_l	Maximum Lead Temperature For Soldering Purpose	260	--	300	°C

(#) When mounted on 1inch² FR-4 BOARD, 2 oz Cu

Table 5: Avalanche Characteristics

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	1	A
E_{AS}	Single Pulse Avalanche Energy (starting T_j = 25 °C, $I_D = I_{AR}$, V_{DD} = 50 V)	50	mJ

Table 6: GATE-SOURCE ZENER DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate-Source Breakdown Voltage	Igs=± 1mA (Open Drain)	30			V

PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device’s ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device’s integrity. These integrated Zener diodes thus avoid the usage of external components.

ELECTRICAL CHARACTERISTICS (T_{CASE} =25°C UNLESS OTHERWISE SPECIFIED)

Table 7: On/Off

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 1 mA, V_{GS} = 0	800			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating, T_C = 125 °C			1 50	µA µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 20V			±10	µA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 50 µA	3	3.75	4.5	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10V, I_D = 0.5 A		13	16	Ω

Table 8: Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward Transconductance	V_{DS} = 15 V, I_D = 0.5 A		0.8		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0		160 26 6.7		pF pF pF
$C_{oss\ eq.}$ (3)	Equivalent Output Capacitance	V_{GS} = 0V, V_{DS} = 0V to 640V		9.5		pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on Delay Time Rise Time Turn-off Delay Time Fall Time	V_{DD} = 400 V, I_D = 0.5 A R_G = 4.7Ω V_{GS} = 10 V (see Figure 21)		8 30 22 55		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD} = 640V, I_D = 1.0 A, V_{GS} = 10V (see Figure 24)		7.7 1.4 4.5		nC nC nC

Table 9: Source Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (2)	Source-drain Current Source-drain Current (pulsed)				1.0 5	A A
V_{SD} (1)	Forward On Voltage	I_{SD} = 1.0 A, V_{GS} = 0			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 1.0 A, di/dt = 100 A/µs V_{DD} = 50 V, T_j = 25°C (see Figure 22)		365 802 4.4		ns nC A
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 1.0 A, di/dt = 100 A/µs V_{DD} = 50 V, T_j = 150°C (see Figure 22)		388 802.7 4.6		ns nC A

Note: 1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
2. Pulse width limited by safe operating area.
3. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Figure 3: Safe Operating Area for SOT-223

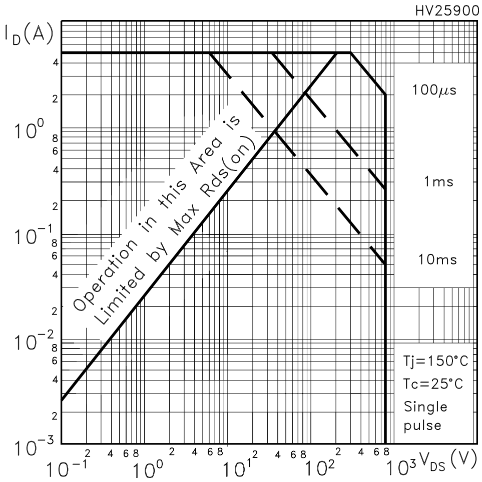


Figure 6: Thermal Impedance for SOT-223

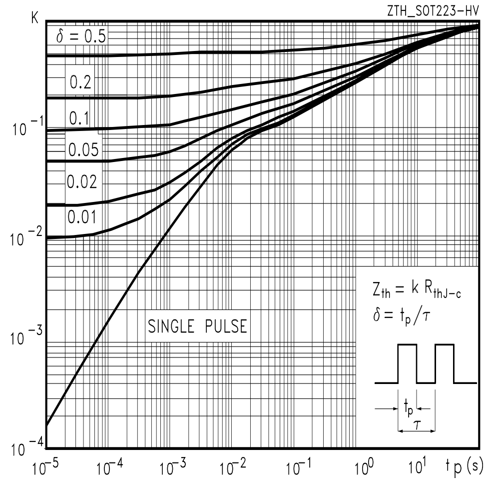


Figure 4: Safe Operating Area for TO-92

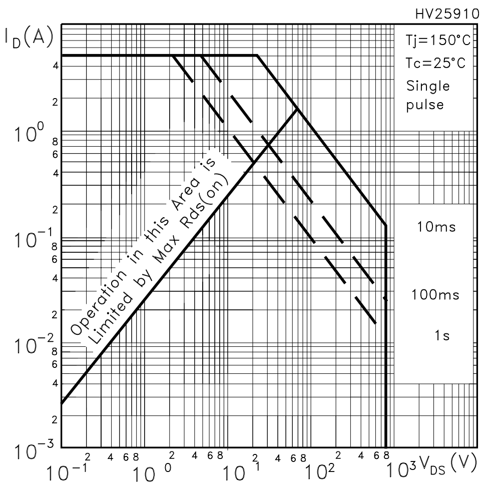


Figure 7: Thermal Impedance for TO-92

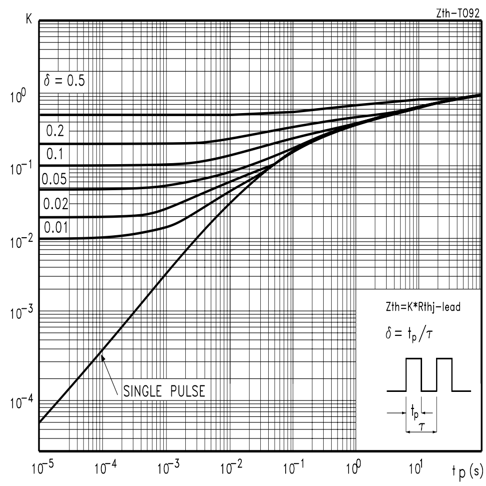


Figure 5: Safe Operating Area for IPAK-DPAK

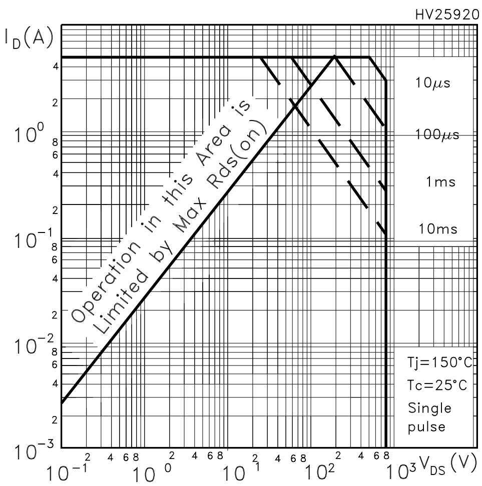


Figure 8: Thermal Impedance for DPAK-IPAK

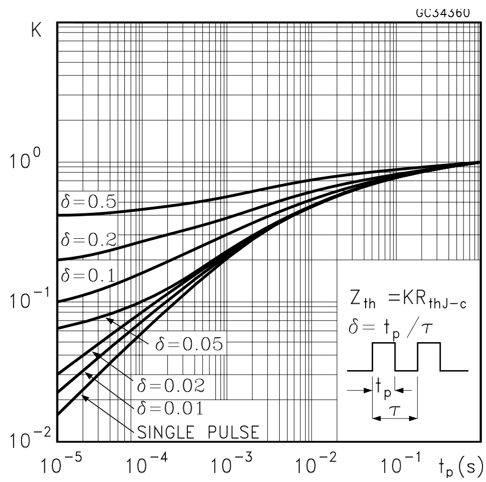


Figure 9: Output Characteristics

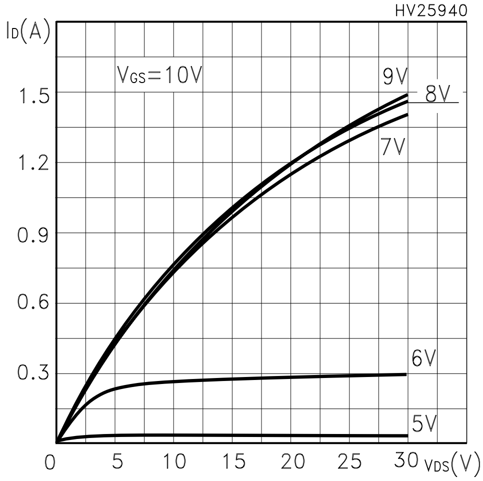


Figure 12: Transfer Characteristics

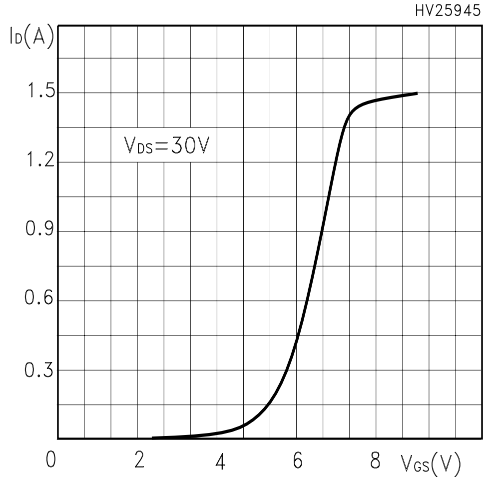


Figure 10: Transconductance

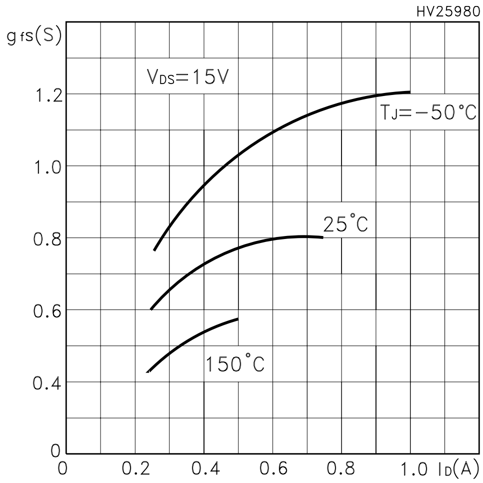


Figure 13: Static Drain-source On Resistance

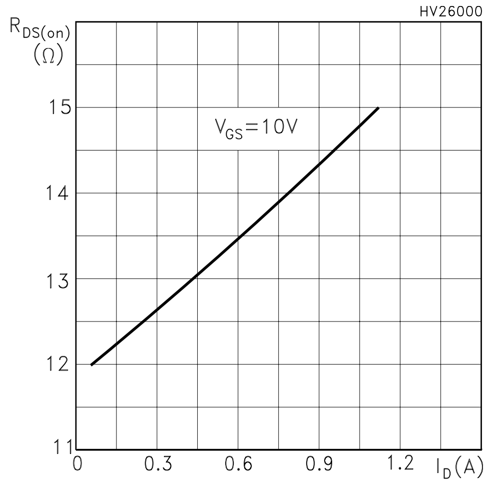


Figure 11: Gate Charge vs Gate-source Voltage

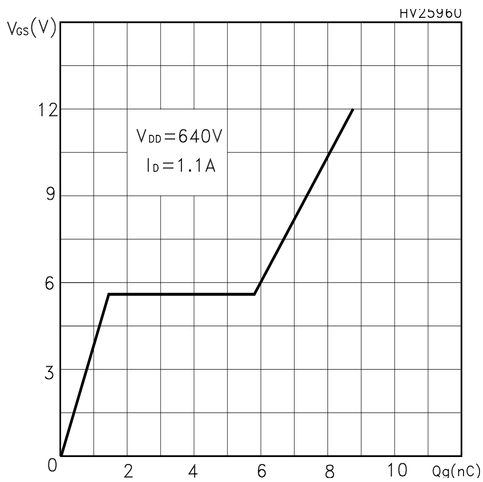


Figure 14: Capacitance Variations

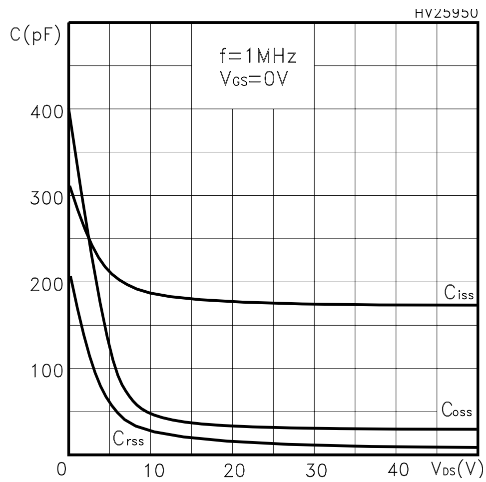


Figure 15: Normalized Gate Thereshold Voltage vs Temperature

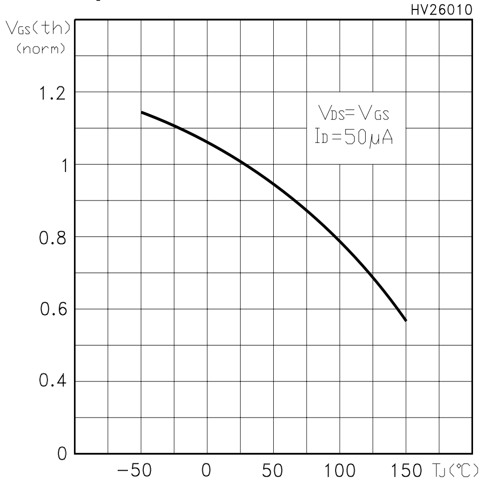


Figure 16: Source-Drain Diode Forward Characteristics

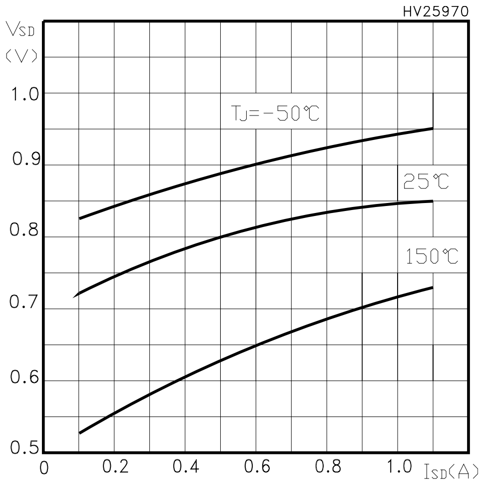


Figure 17: Avalanche Energy vs Starting Tj

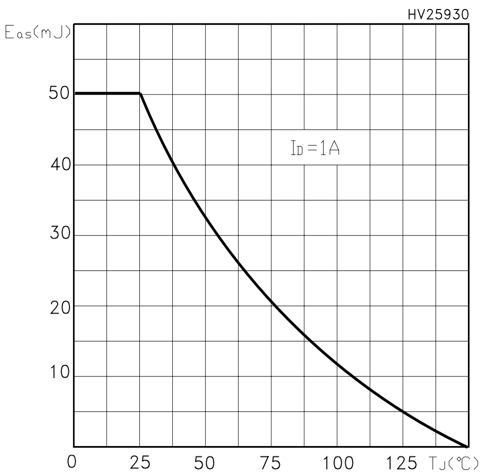


Figure 18: Normalized On Resistance vs Temperature

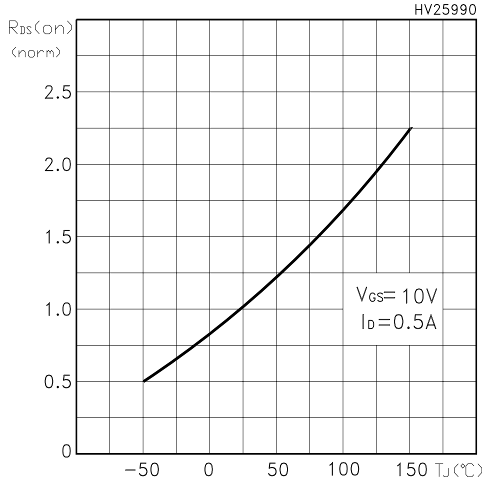


Figure 19: Normalized BVdss vs Temperature

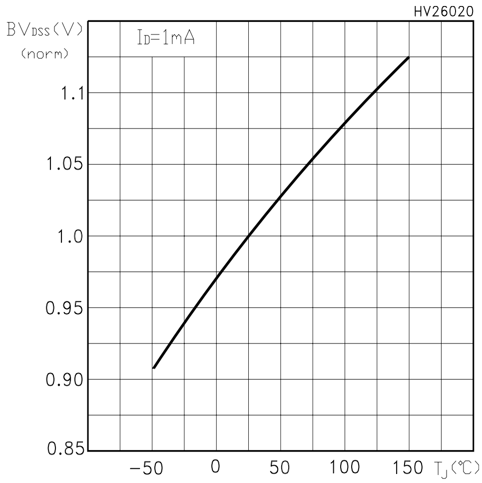


Figure 20: Unclamped Inductive Load Test Circuit

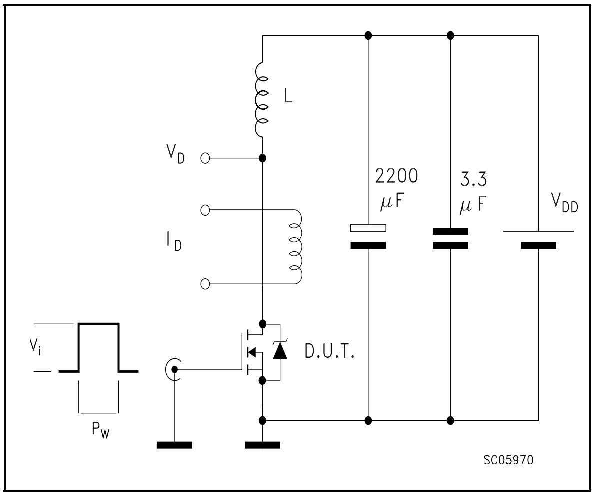


Figure 21: Switching Times Test Circuit For Resistive Load

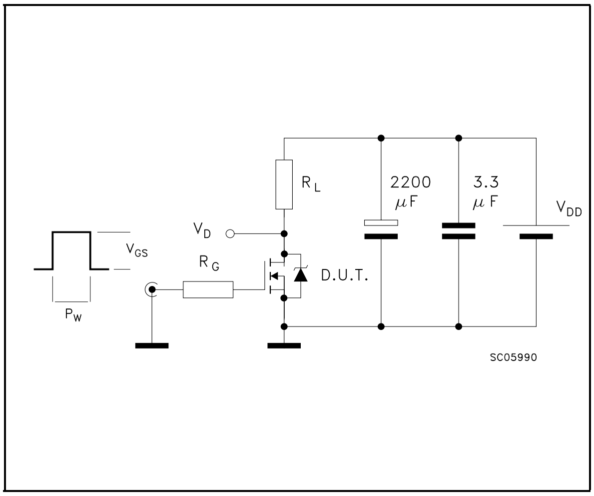


Figure 22: Test Circuit For Inductive Load Switching and Diode Recovery Times

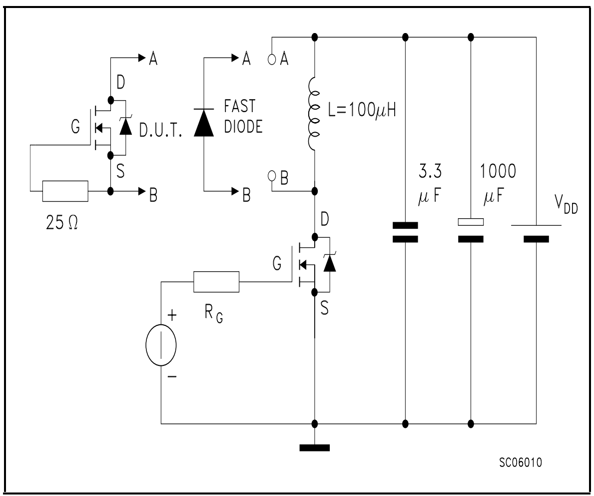


Figure 23: Unclamped Inductive Wafeform

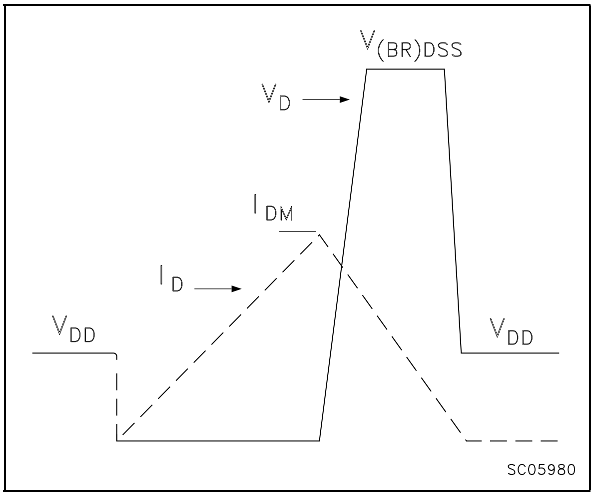
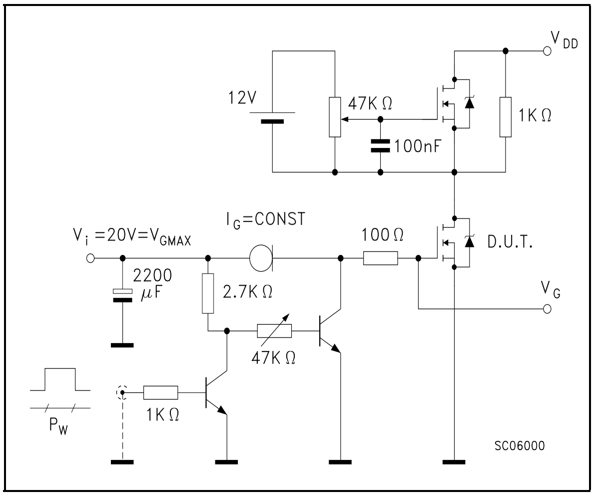
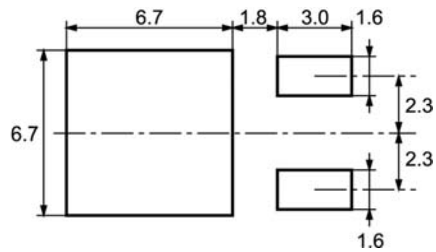


Figure 24: Gate Charge Test Circuit



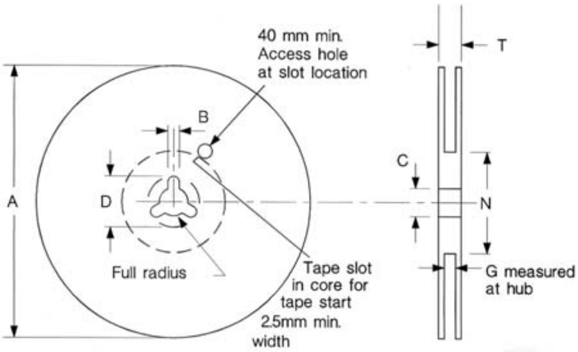
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

DPAK FOOTPRINT



All dimensions are in millimeters

TAPE AND REEL SHIPMENT



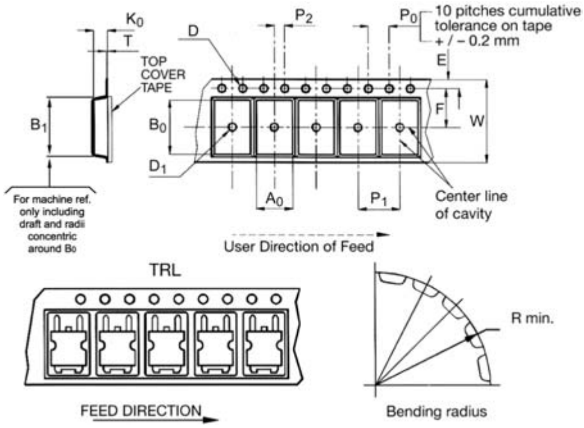
REEL MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	16.4	18.4	0.645	0.724
N	50		1.968	
T		22.4		0.881

BASE QTY	BULK QTY
2500	2500

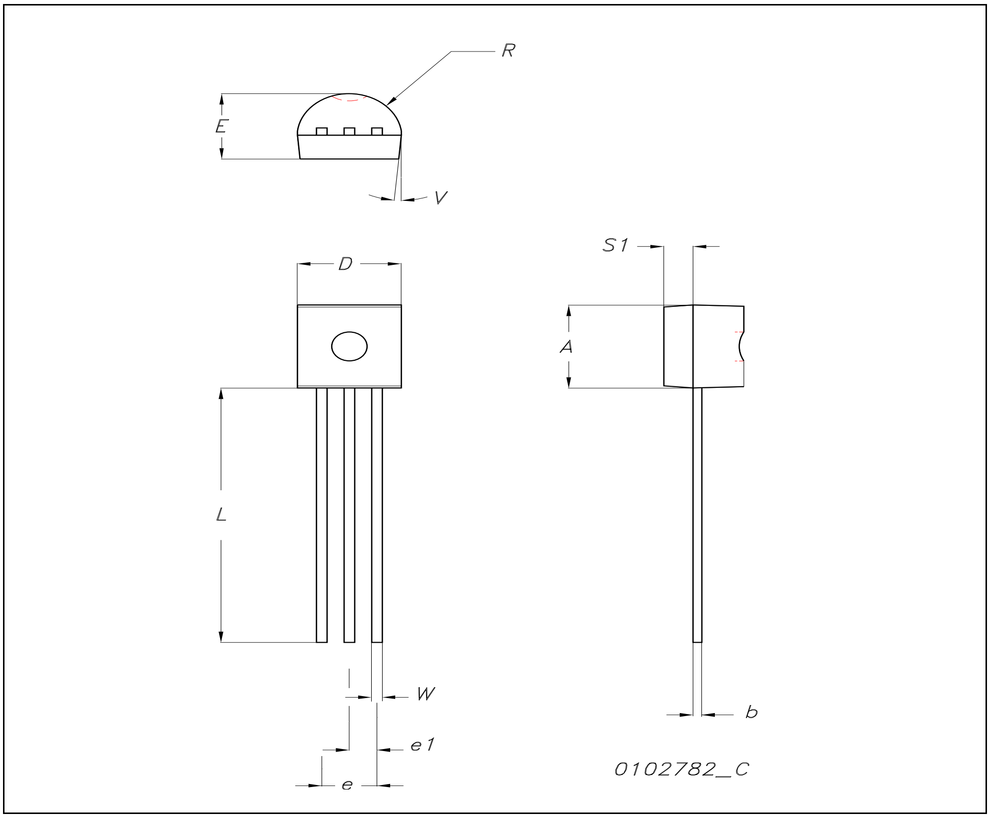
TAPE MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	6.8	7	0.267	0.275
B0	10.4	10.6	0.409	0.417
B1		12.1		0.476
D	1.5	1.6	0.059	0.063
D1	1.5		0.059	
E	1.65	1.85	0.065	0.073
F	7.4	7.6	0.291	0.299
K0	2.55	2.75	0.100	0.108
P0	3.9	4.1	0.153	0.161
P1	7.9	8.1	0.311	0.319
P2	1.9	2.1	0.075	0.082
R	40		1.574	
W	15.7	16.3	0.618	0.641



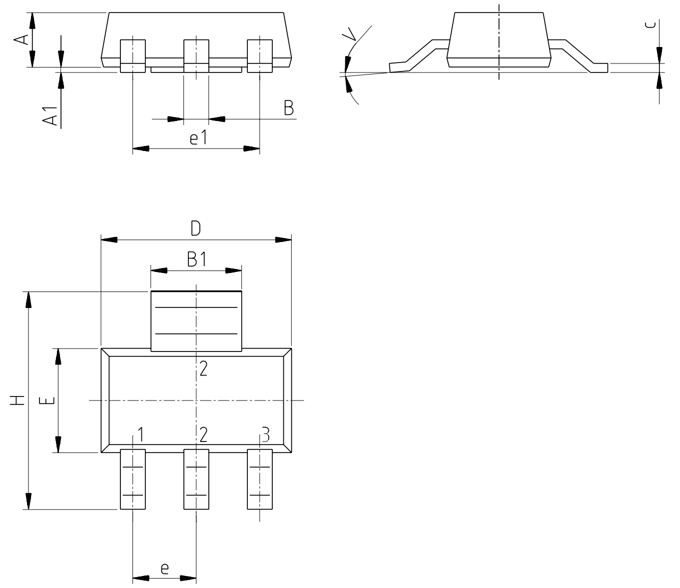
TO-92 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.32		4.95	0.170		0.194
b	0.36		0.51	0.014		0.020
D	4.45		4.95	0.175		0.194
E	3.30		3.94	0.130		0.155
e	2.41		2.67	0.094		0.105
e1	1.14		1.40	0.044		0.055
L	12.70		15.49	0.50		0.610
R	2.16		2.41	0.085		0.094
S1	0.92		1.52	0.036		0.060
W	0.41		0.56	0.016		0.022
V		5°			5°	



SOT-223 MECHANICAL DATA

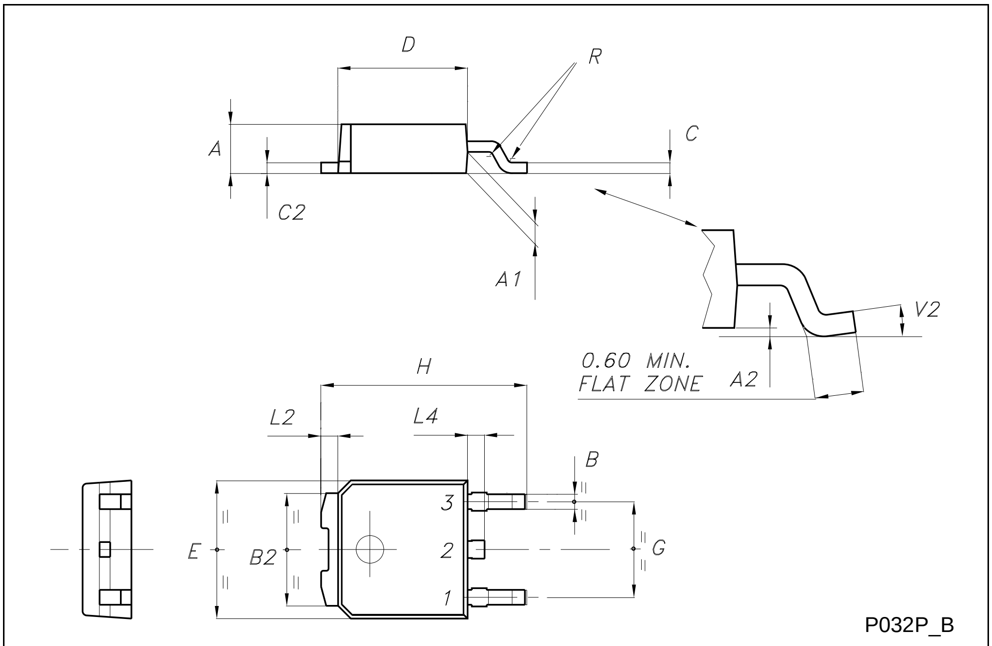
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.80			0.071
B	0.60	0.70	0.80	0.024	0.027	0.031
B1	2.90	3.00	3.10	0.114	0.118	0.122
c	0.24	0.26	0.32	0.009	0.010	0.013
D	6.30	6.50	6.70	0.248	0.256	0.264
e		2.30			0.090	
e1		4.60			0.181	
E	3.30	3.50	3.70	0.130	0.138	0.146
H	6.70	7.00	7.30	0.264	0.276	0.287
V			10^o			10^o
A1		0.02				



P008B

TO-252 (DPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.20		2.40	0.087		0.094
A1	0.90		1.10	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.90	0.025		0.035
B2	5.20		5.40	0.204		0.213
C	0.45		0.60	0.018		0.024
C2	0.48		0.60	0.019		0.024
D	6.00		6.20	0.236		0.244
E	6.40		6.60	0.252		0.260
G	4.40		4.60	0.173		0.181
H	9.35		10.10	0.368		0.398
L2		0.8			0.031	
L4	0.60		1.00	0.024		0.039
V2	0^{o}		8^{o}	0^{o}		0^{o}



TO-251 (IPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
B	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039

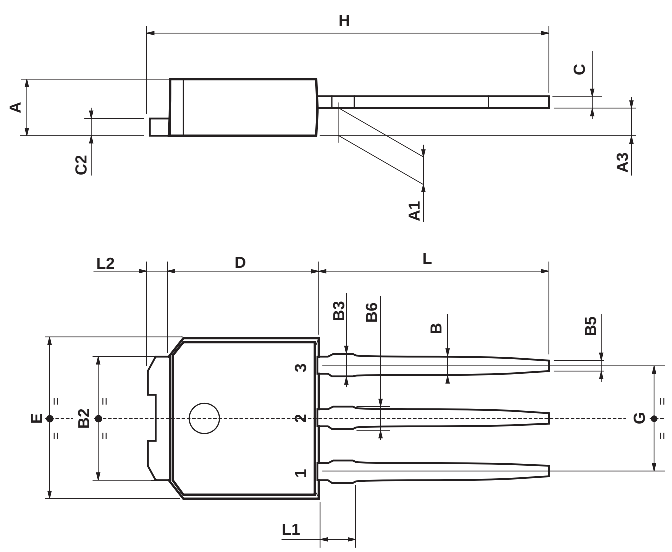


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Table 10: Revision History

Date	Revision	Description of Changes
08-Jun-2005	1	First Release
06-Sep-2005	2	Inserted Ecopack indication
16-Jan-2006	3	Corrected value on Table 3