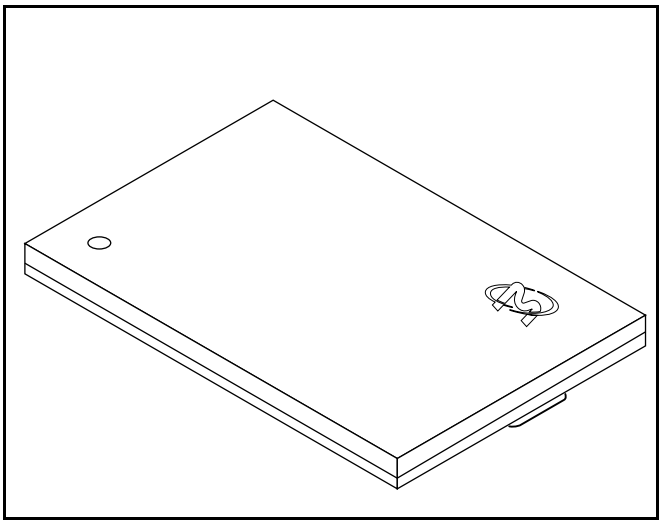
DDR2 SDRAM

MT47H128M4–32 MEG X 4 X 4 BANKS
MT47H64M8–16 MEG X 8 X 4 BANKS
MT47H32M16–8 MEG X 16 X 4 BANKS

For the latest data sheet, please refer to the Micron Web site: http://www.micron.com/datasheets

Features

- VDD = +1.8V ±0.1V, VDDQ = +1.8V ±0.1V
- JEDEC standard 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS, DQS#) option
- Four-bit prefetch architecture
- Duplicate output strobe (RDQS) option for x8 configuration
- DLL to align DQ and DQS transitions with CK
- Four internal banks for concurrent operation
- Programmable CAS Latency (CL): 3 and 4
- Posted CAS additive latency (AL): 0, 1, 2, 3, and 4
- WRITE latency = READ latency - 1 tCK
- Programmable burst lengths: 4 or 8
- Adjustable data-output drive strength
- 64ms, 8,192-cycle refresh
- On-die termination (ODT)



Options	Designation
• Configuration	
128 Meg x 4 (32 Meg x 4 x 4 banks)	128M4
64 Meg x 8 (16 Meg x 8 x 4 banks)	64M8
32 Meg x 16 (8 Meg x 16 x 4 banks)	32M16
• FBGA Package Lead-Free	
92-ball FBGA (11mm x 19mm)	BT
• Timing – Cycle Time	
5.0ns @ CL = 3 (DDR2-400)	-5E
3.75ns @ CL = 4 (DDR2-533)	-37E

ARCHITECTURE	128 MEG X 4	64 MEG X 8	32 MEG X 16
Configuration	32 Meg x 4 x 4 banks	16 Meg x 8 x 4 banks	8 Meg x 16 x 4 banks
Refresh Count	8K	8K	8K
Row Addressing	16K (A0-A12)	16K (A0-A13)	8K (A0-A12)
Bank Addressing	4 (BA0 - BA1)	4 (BA0 - BA1)	4 (BA0 - BA1)
Column Addressing	2K (A0-A9, A11)	1K (A0-A9)	1K (A0-A9)

Table 1: Key Timing Parameters

SPEED GRADE	DATA RATE (MHz)		tRCD (ns)	tRP (ns)	tRC (ns)
	CL = 3	CL = 4			
-5E	400	400	15	15	55
-37E	400	533	15	15	60

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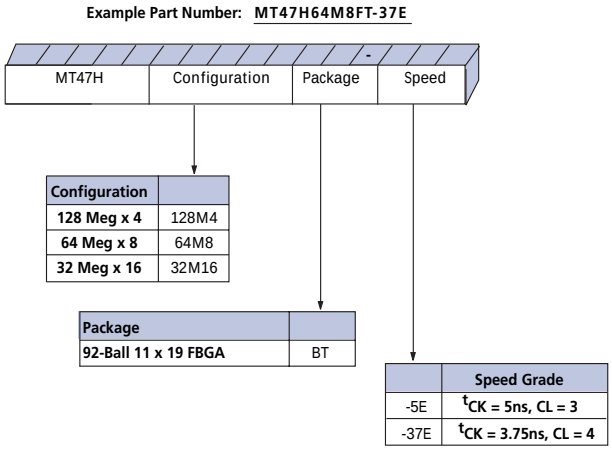
Part Numbers

Figure 1: 512Mb DDR2 Part Numbers



NOTE: Not all speeds and configurations are available.

FBGA Part Marking Decoder

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. Micron's new FBGA Part Marking Decoder makes it easier to understand that part marking. Visit the web site at www.micron.com/decoder.

General Description

The 512Mb DDR2 SDRAM is a high-speed, CMOS dynamic random-access memory containing 5,368,709 bits. It is internally configured as a quad-bank DRAM. The functional block diagrams of the 32 Meg x 16, 64 Meg x 8, and 128 Meg x 4 devices, respectively are shown in the Functional Description section. Ball assignments for the 128 Meg x 4 are shown in Figure 2 and signal descriptions are shown in Table 1. Ball assignments for the 64 Meg x 8 and 128 Meg x 4 are shown in Figure 2 and signal descriptions are shown in Table 2.

The 512Mb DDR2 SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 4*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the 512Mb DDR2 SDRAM effectively consists of a single 4*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and four corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR2 SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs. The x16 offering has two data strobes, one for the lower byte (LDQS, LDQS#) and one for the upper byte (UDQS, UDQS#).

The 512Mb DDR2 SDRAM operates from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Read and write accesses to the DDR2 SDRAM are burst-oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

The DDR2 SDRAM provides for programmable read or write burst lengths of four or eight locations. DDR2 SDRAM supports interrupting a burst read of eight with another read, or a burst write of eight with another write. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard DDR SDRAMs, the pipelined, multibank architecture of DDR2 SDRAMs allows for concurrent operation, thereby providing high, effective bandwidth by hiding row precharge and activation time.

A self refresh mode is provided, along with a power-saving power-down mode.

All inputs are compatible with the JEDEC standard for SSTL_18. All full drive-strength outputs are SSTL_18-compatible.

NOTE: 1. The functionality and the timing specifications discussed in this data sheet are for the DLL-enabled mode of operation.

2. Throughout the data sheet, the various figures and text refer to DQs as “DQ.” The DQ term is to be interpreted as any and all DQ

collectively, unless specifically stated otherwise. Additionally, the x16 is divided into two bytes, the lower byte and upper byte. For the lower byte (DQ0 through DQ7) DM refers to LDM and DQS refers to LDQS. For the upper byte (DQ8 through DQ15) DM refers to UDM and DQS refers to UDQS.

3. Complete functionality is described throughout the document and any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.
4. Any specific requirement takes precedence over a general statement.

Figure 2: 92-ball FBGA Ball Assignment (x16), 11mm x 19mm (Top View)

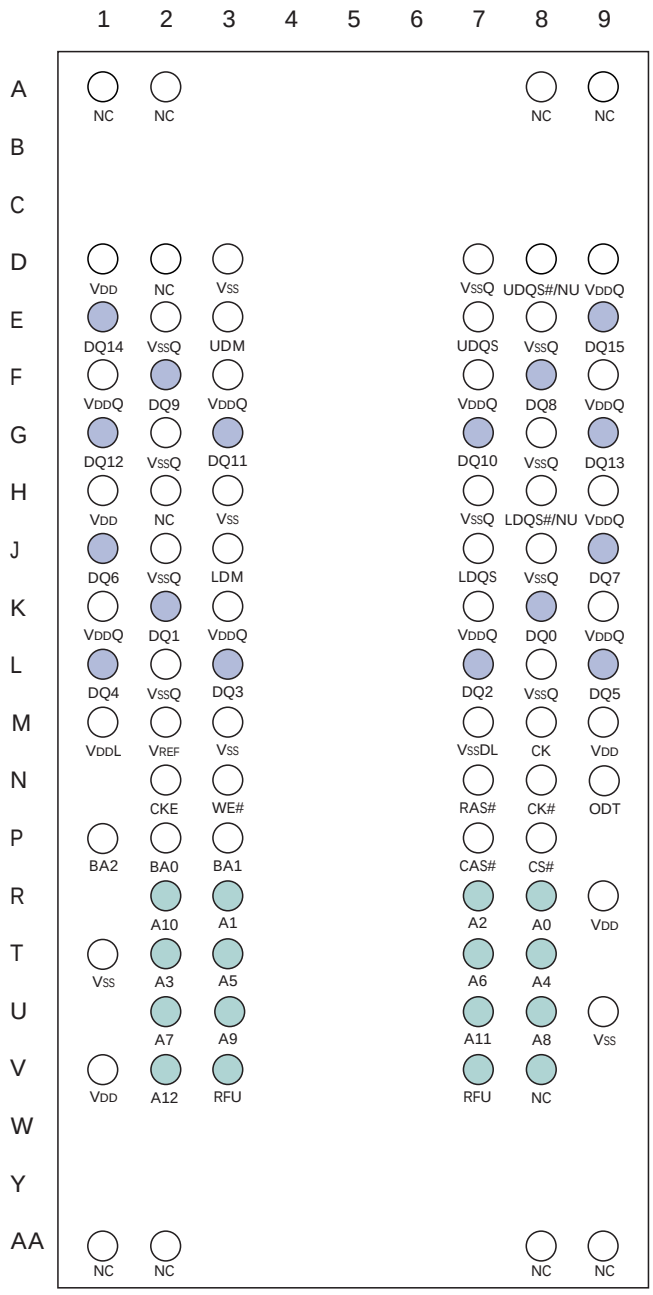


Figure 3: 92-Ball FBGA Ball Assignment (x 4, x 8), 11mm x 19mm (Top View)

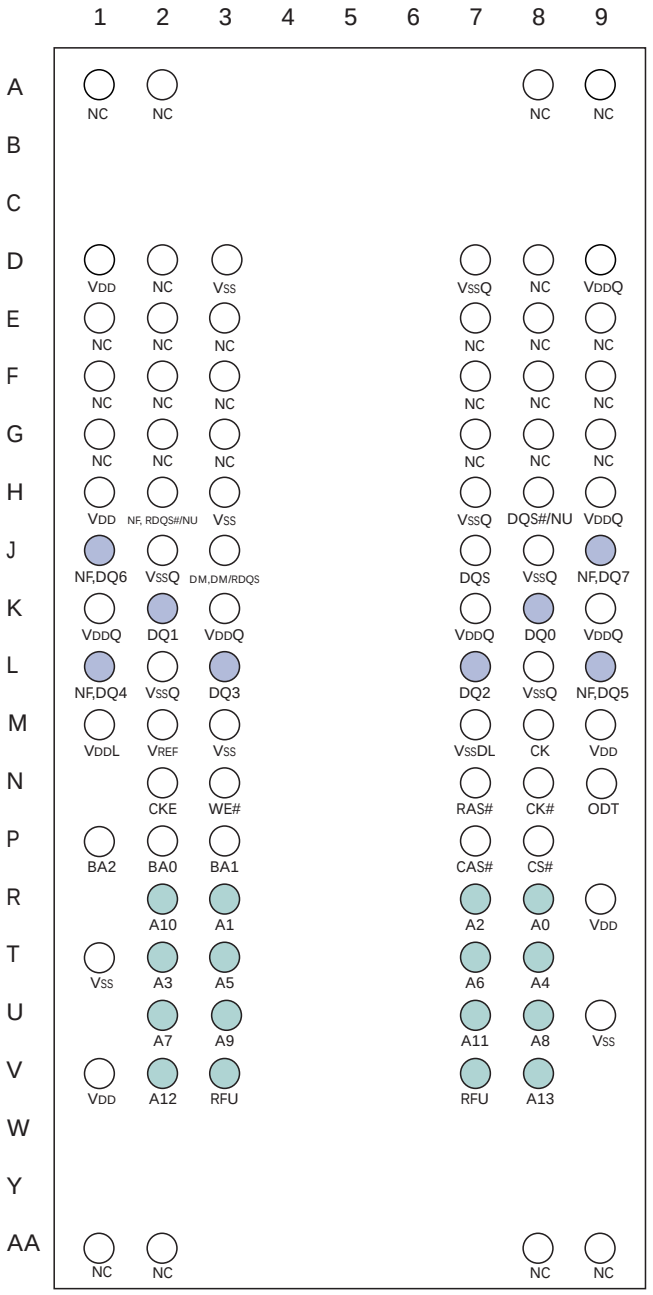


Table 2: FBGA Ball Descriptions 128 Meg x 4, 64 Meg x 8, 32 Meg x 16

x16 FBGA BALL ASSIGNMENT	x4, x8 FBGA BALL ASSIGNMENT	SYMBOL	TYPE	DESCRIPTION
N9	N9	ODT	Input	On-Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each of the following pins: DQ0–DQ15, LDM, UDM, LDQS, LDQS#, UDQS, and UDQS# for the x16; DQ0-DQ7, DQS, DQS#, RDQS, RDQS#, and DM for the x8; DQ0-DQ3, DQS, DQS#, and DM for the x4. The ODT input will be ignored if disabled via the LOAD MODE command.
M8, N8	M8, N8	CK, CK#	Input	Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Output data (DQs and DQS/DQS#) is referenced to the crossings of CK and CK#.
N2	N2	CKE	Input	Clock Enable: CKE (registered HIGH) activates and CKE (registered LOW) deactivates clocking circuitry on the DDR2 SDRAM. The specific circuitry that is enabled/disabled is dependent on the DDR2 SDRAM configuration and operating mode. CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any bank). CKE is synchronous for POWER-DOWN entry, POWER-DOWN exit, output disable, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit. Input buffers (excluding CK, CK#, CKE, and ODT) are disabled during POWER-DOWN. Input buffers (excluding CKE) are disabled during SELF REFRESH. CKE is an SSTL_18 input but will detect a LVCMOS LOW level once V_{DD} is applied during first power-up. After Vref has become stable during the power on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper self-refresh operation V_{REF} must be maintained.
P8	P8	CS#	Input	Chip Select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple ranks. CS# is considered part of the command code.
N7, P7, N3	N7, P7, N3	RAS#, CAS#, WE#	Input	Command Inputs: RAS#, CAS#, and WE# (along with CS#) define the command being entered.
J3, E3	J3	LDM, UDM	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading is designed to match that of DQ and DQS pins. LDM is DM for lower byte DQ0–DQ7 and UDM is DM for upper byte DQ8–DQ15.
P2, P3	P2, P3	BA0-BA1	Input	Bank Address Inputs: BA0-BA2 define to which bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0-BA2 define which mode register including MR, EMR, EMR(2), and EMR(3) is loaded during the LOAD MODE command.

Table 2: FBGA Ball Descriptions 128 Meg x 4, 64 Meg x 8, 32 Meg x 16

x16 FBGA BALL ASSIGNMENT	x4, x8 FBGA BALL ASSIGNMENT	SYMBOL	TYPE	DESCRIPTION
R8,R3,R7,T2, T8,T3,T7,U2, U8,U3,R2,U7, V2	–	A0–A3 A4–A7 A8–A11 A12	Input	Address Inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for Read/ Write commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA1-BA0) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command.
–	R8,R3,R7,T2, T8,T3,T7,U2, U8,U3,R2,U7, V2,V8	A0–A3 A4–A7 A8–A11 A12-A13	Input	Address Inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for Read/ Write commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA1-BA0) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command.
K8,K2,L7,L3, L1,L9,J1,J9, F8,F2,G7,G3, G1,G9,E1,E9	–	DQ0–DQ3 DQ4–DQ7 DQ8–DQ11 DQ12–DQ15	I/O	Data Input/Output: Bidirectional data bus for 32 Meg x 16.
–	K8,K2,L7,L3, L1,L9,J1,J9	DQ0–DQ3 DQ4–DQ7	I/O	Data Input/Output: Bidirectional data bus for 64 Meg x 8.
–	K8,K2,L7,L3	DQ0–DQ3	I/O	Data Input/Output: Bidirectional data bus for 128 Meg x 4.
E7,D8	–	UDQS, UDQS#	I/O	Data Strobe for Upper Byte: Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. UDQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
J7,H8	–	LDQS, LDQS#	I/O	Data Strobe for Lower Byte: Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. LDQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
–	J7,H8	DQS, DQS#	I/O	Data Strobe: Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center aligned with write data. DQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
–	J3,H2	RDQS, RDQS#	Output	Redundant Data Strobe for 64 Meg x 8 only. RDQS is enabled/ disabled via the LOAD MODE command to the Extended Mode Register (EMR). When RDQS is enabled, RDQS is output with read data only and is ignored during write data. When RDQS is disabled, pin J3 becomes Data Mask (see DM pin). RDQS# is only used when RDQS is enabled AND differential data strobe mode is enabled.
D1,H1,M9,R9, V1	D1,H1,M9,R9, V1	V_{DD}	Supply	Power Supply: 1.8V ±0.1V.
M1	M1	V_{DDL}	Supply	DLL Power Supply: 1.8V ±0.1V.

Table 2: FBGA Ball Descriptions 128 Meg x 4, 64 Meg x 8, 32 Meg x 16

x16 FBGA BALL ASSIGNMENT	x4, x8 FBGA BALL ASSIGNMENT	SYMBOL	TYPE	DESCRIPTION
D9,F1,F3,F7, F9,H9,K1,K3, K7,K9	D9,H9,K1, K3,K7,K9	$V_{DD}Q$	Supply	DQ Power Supply: 1.8V ±0.1V. Isolated on the device for improved noise immunity.
M2	M2	V_{REF}	Supply	SSTL_18 reference voltage.
D3,H3,M3,T1, U9	D3,H3,M3,T1, U9	V_{SS}	Supply	Ground.
M7	M7	$V_{SS}DL$	Supply	DLL Ground. Isolated on the device from V_{SS} and $V_{SS}Q$.
D7,E2,E8,G2, G8,H7, J2,J8, L2,L8	D7,H7,J2, J8,L2,L8	$V_{SS}Q$	Supply	DQ Ground. Isolated on the device for improved noise immunity.
A1,A2,A8,A9 D2,H2,V8, AA1,AA2,AA8, AA9	A1,A2,A8,A9, D2,D8,E1-E3, E7-E9,F1-F3, F7-F9, G1-G3, G7-G9, AA1,AA2,AA8, AA9	NC	–	No Connect: These pins should be left unconnected.
–	J1, J9, L1, L9, H2,	NF	–	No Function: These pins are used as DQ4-DQ7 on the 64 Meg x 8, but are NF (No Function) on the 128 Meg x 4 configuration.
D8, H8	-	NU	–	x16 only Not Used: If EMR[E10] = 0, D8 and H8 are UDQS# and LDQS#. If EMR[E10] = 1, then D8 and H8 are Not Used.
-	H2, H8	NU	–	X8 only Not Used: If EMR[E10] = 0, H2 and H8 are RDQS# and DQS#. If EMR[E10] = 1, then H2 and H8 are Not Used.
V3, V7	V3, V7	RFU	–	Reserved for Future Use; Row address bits A14(V3) and A15(V7) are reserved for 2Gb and 4Gb densities.

Figure 4: Functional Description

The 512Mb DDR2 SDRAM is a high-speed, CMOS dynamic random-access memory containing 1,073,741,824 bits. The 512Mb DDR2 SDRAM is internally configured as a four-bank DRAM.

The 512Mb DDR2 SDRAM uses a double data rate architecture to achieve high-speed operation. The DDR2 architecture is essentially a 4*n*-prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the 512Mb DDR2 SDRAM consists of a single 4*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and four corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

Prior to normal operation, the DDR2 SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions, and device operation.

Figure 5: Functional Block Diagram (32 Meg x 16)

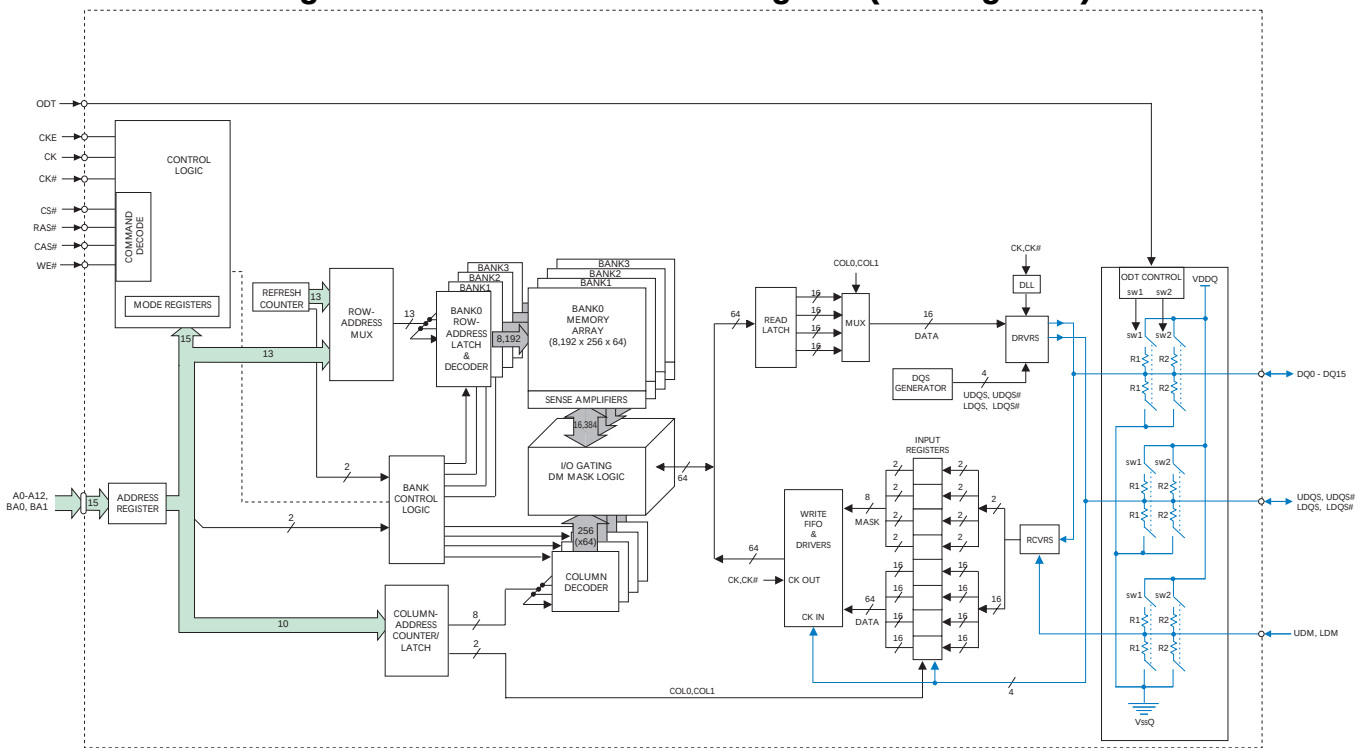


Figure 6: Functional Block Diagram (64 Meg x 8)

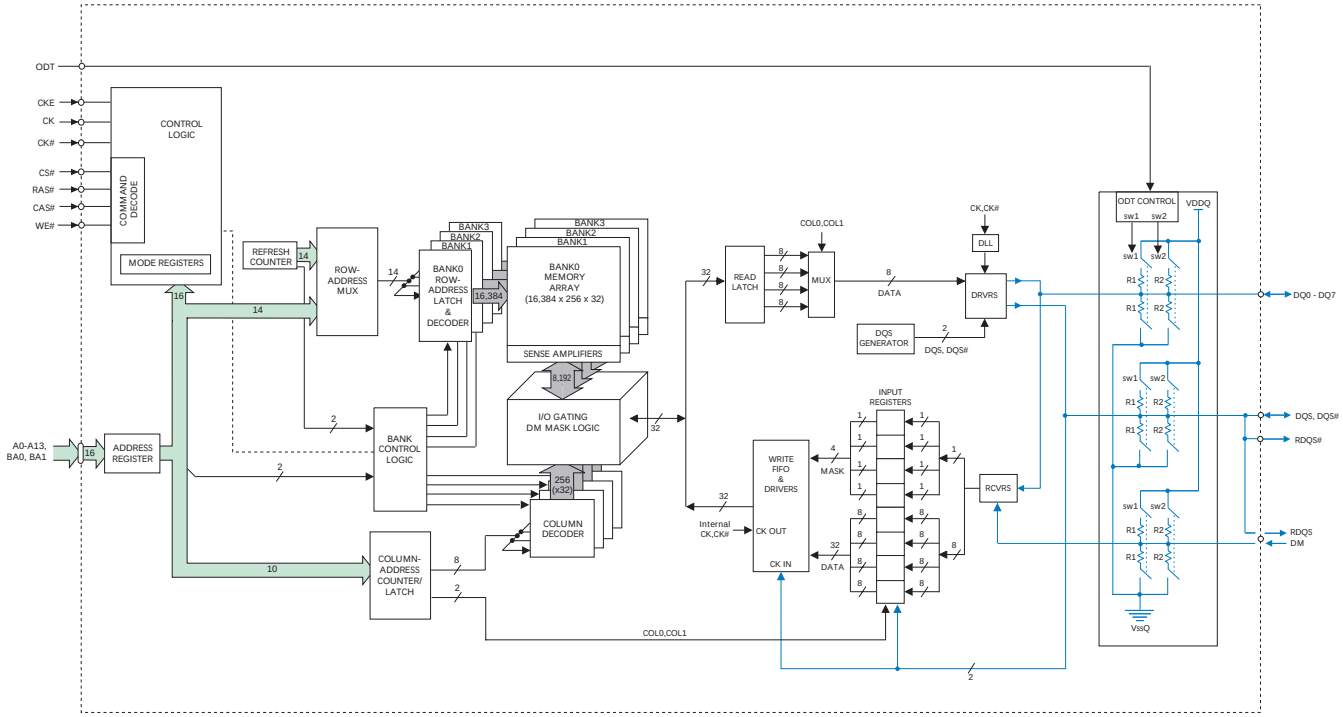
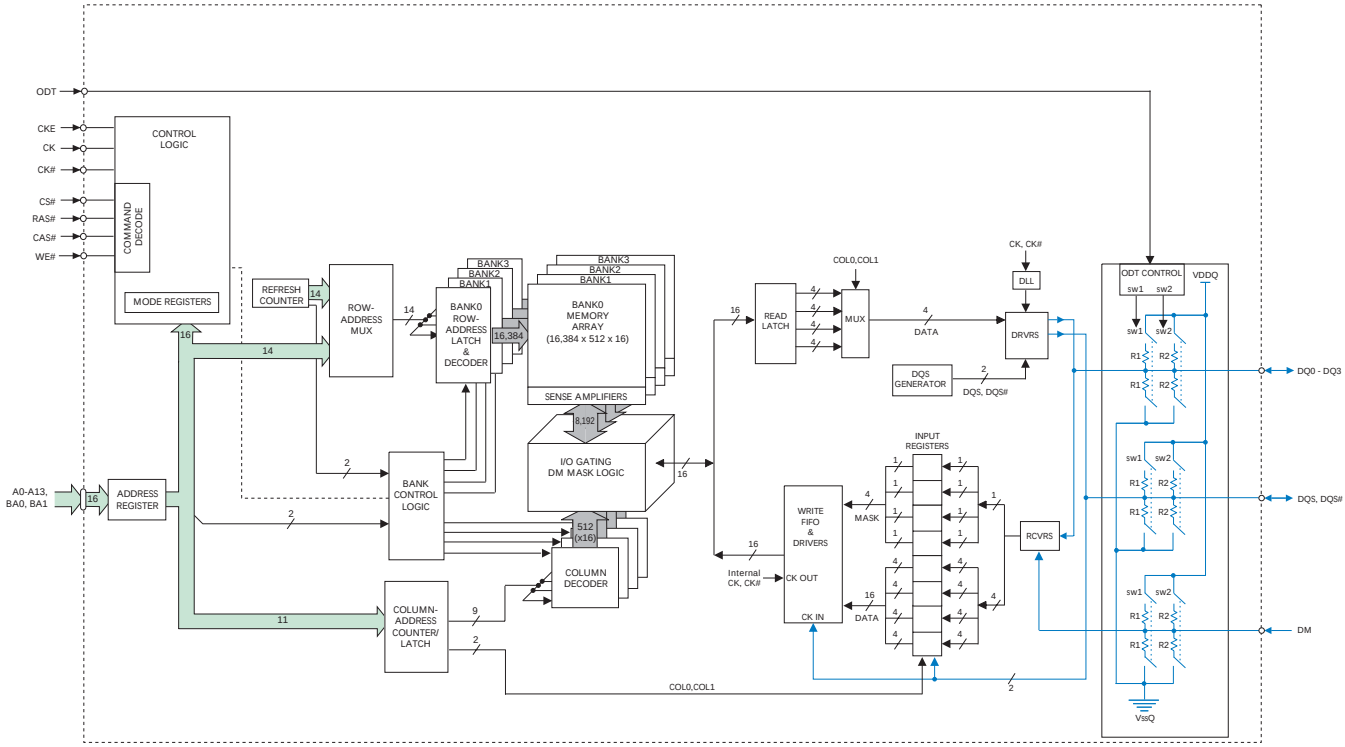


Figure 7: Functional Block Diagram (128 Meg x 4)



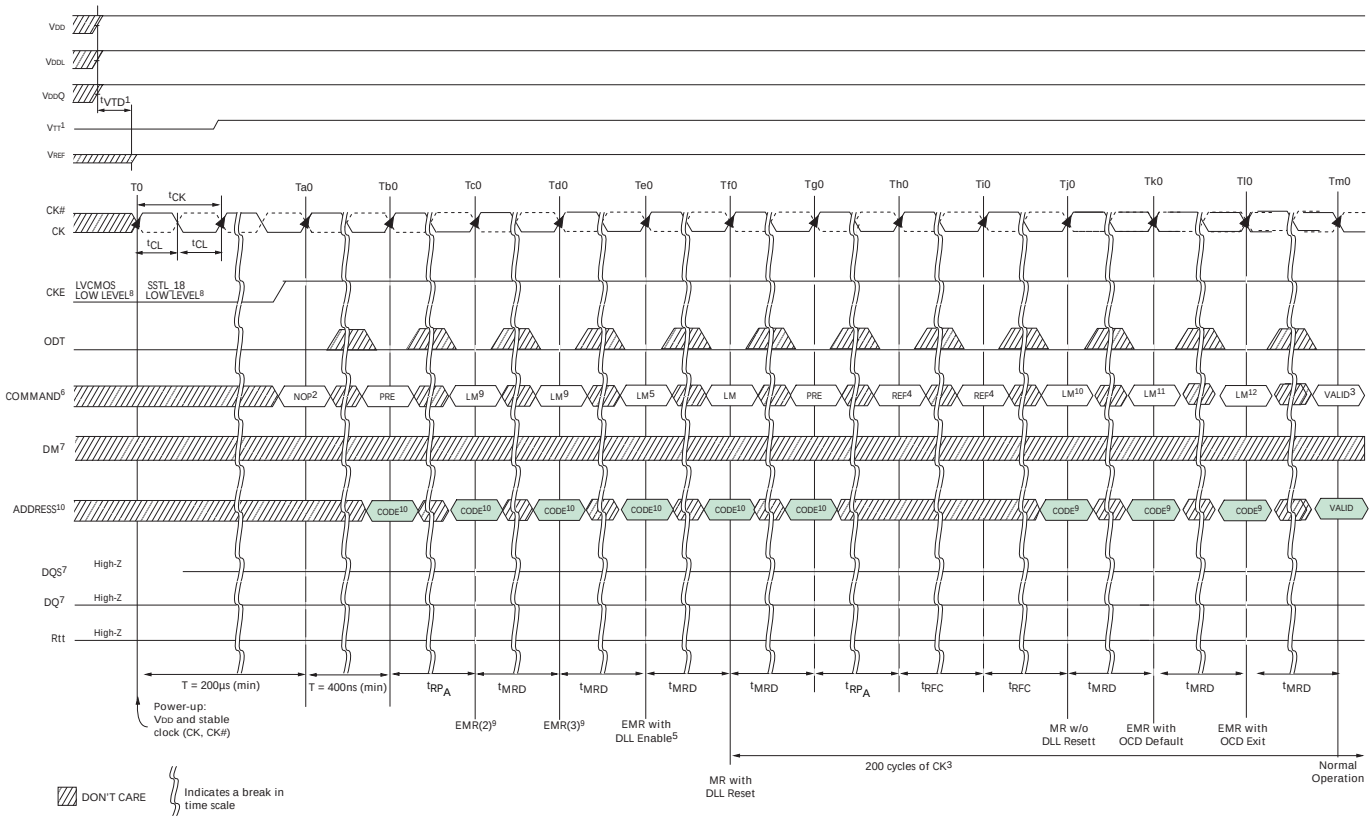
Initialization

The following sequence is required for power-up and initialization and is shown in Figure 8.

1. Apply power; if CKE is maintained below 0.2* VDDQ, outputs remain disabled. To guarantee RTT (ODT Resistance) is off, VREF must be valid and a low level must be applied to the ODT pin (all other inputs may be undefined). The time from when VDD first starts to power-up to the completion of VDDQ must be equal to or less than 10ms. At least one of the following two sets of conditions (A or B) must be met:
   A. CONDITION SET A
   - VDD, VDDL and VDDQ are driven from a single power converter output
   - VTT is limited to 0.95V MAX
   - VREF tracks VDDQ/2.

   B. CONDITION SET B
   - Apply VDD before or at the same time as VDDL.
   - Apply VDDL before or at the same time as VDDQ.
   - Apply VDDQ before or at the same time as VTT and VREF.
   - The voltage difference between any VDD supply can not exceed 0.5V. For a minimum of 200µs after stable power and clock (CK, CK#), apply NOP or DESELECT commands and take CKE HIGH.
2. Wait a minimum of 400ns, then issue a PRECHARGE ALL command.
3. Issue an LOAD MODE command to the EMR(2) register. (To issue an EMR(2) command, provide LOW to BA0, provide HIGH to BA1.)
4. Issue a LOAD MODE command to the EMR(3) register. (To issue an EMR(3) command, provide HIGH to BA0 and BA1.)
5. Issue an LOAD MODE command to the EMR register to enable DLL. To issue a DLL ENABLE command, provide LOW to BA1 and A0, provide HIGH to BA0. Bits E7, E8, and E9 must all be set to 0.
6. Issue a LOAD MODE command for DLL Reset. 200 cycles of clock input is required to lock the DLL. (To issue a DLL Reset, provide HIGH to A8 and provide LOW to BA1 and BA0.) CKE must be HIGH the entire time.
7. Issue PRECHARGE ALL command.
8. Issue two or more REFRESH commands.
9. Issue a LOAD MODE command with LOW to A8 to initialize device operation (i.e., to program operating parameters without resetting the DLL).
10. Issue a LOAD MODE command to the EMR to enable OCD default by setting Bits E7, E8, and E9 to 1 and set all other desired parameters.
11. Issue a LOAD MODE command to the EMR to enable OCD exit by setting Bits E7, E8, and E9 to 0 and set all other desired parameters.
12. The DDR2 SDRAM is now intialized and ready for normal operation 200 clocks after DLL Reset in step 6.

Figure 8: DDR2 Power-Up and Initialization



NOTE:

1. VTT is not applied directly to the device; however, tVTD should be greater than or equal to zero to avoid device latch-up. The time from when VDD first starts to power-up to the completion of VDDQ must be equal to or less than 10ms. One of the following two conditions (a or b) MUST be met:
   a) VDD, VDDL, and VDDQ are driven from a single power converter output.
   VTT may be 0.95V maximum during power up.
   VREF tracks VDDQ/2.
   b) Apply VDD before or at the same time as VDDL.
   Apply VDDL before or at the same time as VDDQ.
   Apply VDDQ before or at the same time as VTT and VREF. The voltage difference between any VDD supply can not exceed 0.5V.
2. Either a NOP or DESELECT command may be applied.
3. 200 cycles of clock (CK, CK#) are required before a READ command can be issued. CKE must be HIGH the entire time.
4. Two or more REFRESH commands are required.
5. Bits E7, E8, and E9 must all be set to 0 with all other operating parameters of EMRS set as required.
6. PRE = PRECHARGE command, LM = LOAD MODE command, REF = REFRESH command, ACT = ACTIVE command, RA = Row Address, BA = Bank Address.
7. DM represents DM for x4, x8 configuration and UDM, LDM for x16 configuration. DQS represents DQS, DQS#, UDQS, UDQS#, LDQS, LDQS#, RDQS, RDQS# for the appropriate configuration (x4, x8, x16). DQ represents DQ0–DQ3 for x4, DQ0–DQ7 for x8, and DQ0–DQ15 for x16.
8. CKE pin uses LVCMOS input levels prior to state T0. After state T0, CKE pin uses SSTL_18 input levels.
9. ADDRESS represents A12-A0 for x4, x8, and A12-A0 for x16, BA0-BA1. A10 should be HIGH at states Tb0 and Tg0 to ensure a PRECHARGE (all banks) command is issued.
10. Bits E7, E8, and E9 must be set to 1 to set OCD default.
11. Bits E7, E8, and E9 must be set to 0 to set OCD exit and all other operating parameters of EMRS set as required.

Mode Register (MR)

The mode register is used to define the specific mode of operation of the DDR2 SDRAM. This definition includes the selection of a burst length, burst type, CAS latency, operating mode, DLL reset, write recovery, and power-down mode as shown in Figure 9. Contents of the mode register can be altered by re-executing the LOAD MODE (LM) command. If the user chooses to modify only a subset of the MR variables, all variables (M0–M14) must be programmed when the LOAD MODE command is issued.

The mode register is programmed via the LM command (bits BA1-BA0 = 0, 0) and other bits (M13 - M0 for x4 and x8, M12 - M0 for x16) will retain the stored information until it is programmed again or the device loses power (except for bit M8, which is self-clearing). Reprogramming the mode register will not alter the contents of the memory array, provided it is performed correctly.

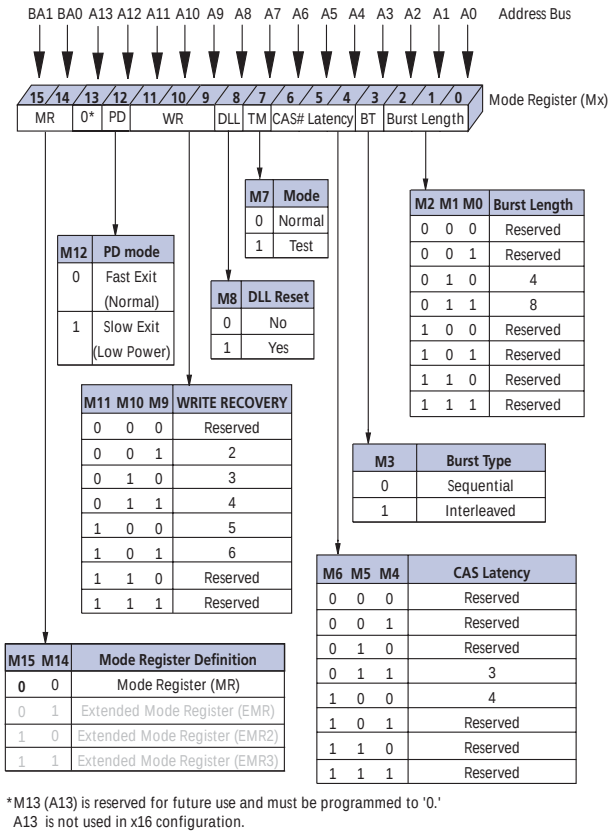
The LOAD MODE command can only be issued (or reissued) when all banks are in the precharged state. The controller must wait the specified time ^{t}MRD before initiating any subsequent operations such as an ACTIVE command. Violating either of these requirements will result in unspecified operation.

Burst Length

Burst length is defined by bits M0–M3 as shown in Figure 9. Read and write accesses to the DDR2 SDRAM are burst-oriented, with the burst length being programmable to either four or eight. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A2–A*i* when the burst length is set to four and by A3–A*i* when the burst length is set to eight (where Ai is the most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both READ and WRITE bursts.

Figure 9: Mode Register (MR) Definition



*M13 (A13) is reserved for future use and must be programmed to '0.'
A13 is not used in x16 configuration.

Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved. The burst type is selected via bit M3 as shown in Figure 9. The ordering of accesses within a burst is determined by the burst length, the burst type, and the starting column address as shown in Table 3. DDR2 SDRAM supports 4-bit burst and 8-bit burst modes only. For 8-bit burst mode, full interleave address ordering is supported; however, sequential address ordering is nibble-based.

Table 3: Burst Definition

BURST LENGTH	STARTING COLUMN ADDRESS (A2, A1, A0)	ORDER OF ACCESSES WITHIN A BURST	
		BURST TYPE = SEQUENTIAL	BURST TYPE = INTERLEAVED
4	0 0 0	0,1,2,3	0,1,2,3
	0 0 1	1,2,3,0	1,0,3,2
	0 1 0	2,3,0,1	2,3,0,1
	0 1 1	3,0,1,2	3,2,1,0
8	0 0 0	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7
	0 0 1	1,2,3,0,5,6,7,4	1,0,3,2,5,4,7,6
	0 1 0	2,3,0,1,6,7,4,5	2,3,0,1,6,7,4,5
	0 1 1	3,0,1,2,7,4,5,6	3,2,1,0,7,6,5,4
	1 0 0	4,5,6,7,0,1,2,3	4,5,6,7,0,1,2,3
	1 0 1	5,6,7,4,1,2,3,0	5,4,7,6,1,0,3,2
	1 1 0	6,7,4,5,2,3,0,1	6,7,4,5,2,3,0,1
	1 1 1	7,4,5,6,3,0,1,2	7,6,5,4,3,2,1,0

Operating Mode

The normal operating mode is selected by issuing a LOAD MODE command with bit M7 set to zero, and all other bits set to the desired values as shown in Figure 9. When bit M7 is '1,' no other bits of the mode register are programmed. Programming bit M7 to '1' places the DDR2 SDRAM into a test mode that is only used by the Manufacturer and should NOT be used. No operation or functionality is guaranteed if M7 bit is '1.'

DLL Reset

DLL reset is defined by bit M8 as shown in Figure 9. Programming bit M8 to '1' will activate the DLL RESET function. Bit M8 is self-clearing, meaning it returns back to a value of '0' after the DLL RESET function has been issued.

Anytime the DLL RESET function is used, 200 clock cycles must occur before a READ command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the ^{t}AC or ^{t}DQSCK parameters.

Write Recovery

Write recovery (WR) time is defined by bits M9–M11 as shown in Figure 9. The WR Register is used by the DDR2 SDRAM during WRITE with AUTO PRECHARGE operation. During WRITE with AUTO PRECHARGE operation, the DDR2 SDRAM delays the internal AUTO PRECHARGE operation by WR clocks (programmed in bits M9–M11) from the last data burst. An example of Write with AUTO PRECHARGE is shown in Figure 26 on page 30.

Write Recovery (WR) values of 2, 3, 4, 5, or 6 clocks may be used for programming bits M9–M11. The user is required to program the value of write recovery, which is calculated by dividing ^{t}WR (in ns) by ^{t}CK (in ns) and rounding up a noninteger value to the next integer; WR [cycles] = ^{t}WR [ns] / ^{t}CK [ns]. Reserved states should not be used as unknown operation or incompatibility with future versions may result.

Power-Down Mode

Active power-down (PD) mode is defined by bit M12 as shown in Figure 9. PD mode allows the user to determine the active power-down mode, which determines performance vs. power savings. PD mode bit M12 does not apply to precharge power-down mode.

When bit M12 = 0, standard Active Power-down mode or 'fast-exit' active power-down mode is enabled. The ^{t}XARD parameter is used for 'fast-exit' active power-down exit timing. The DLL is expected to be enabled and running during this mode.

When bit M12 = 1, a lower power active power-down mode or 'slow-exit' active power-down mode is enabled. The ^{t}XARDS parameter is used for 'slow-exit' active power-down exit timing. The DLL can be enabled, but 'frozen' during active power-down mode since the exit-to-READ command timing is relaxed. The power difference expected between PD 'normal' and PD 'low-power' mode is defined in the IDD table.

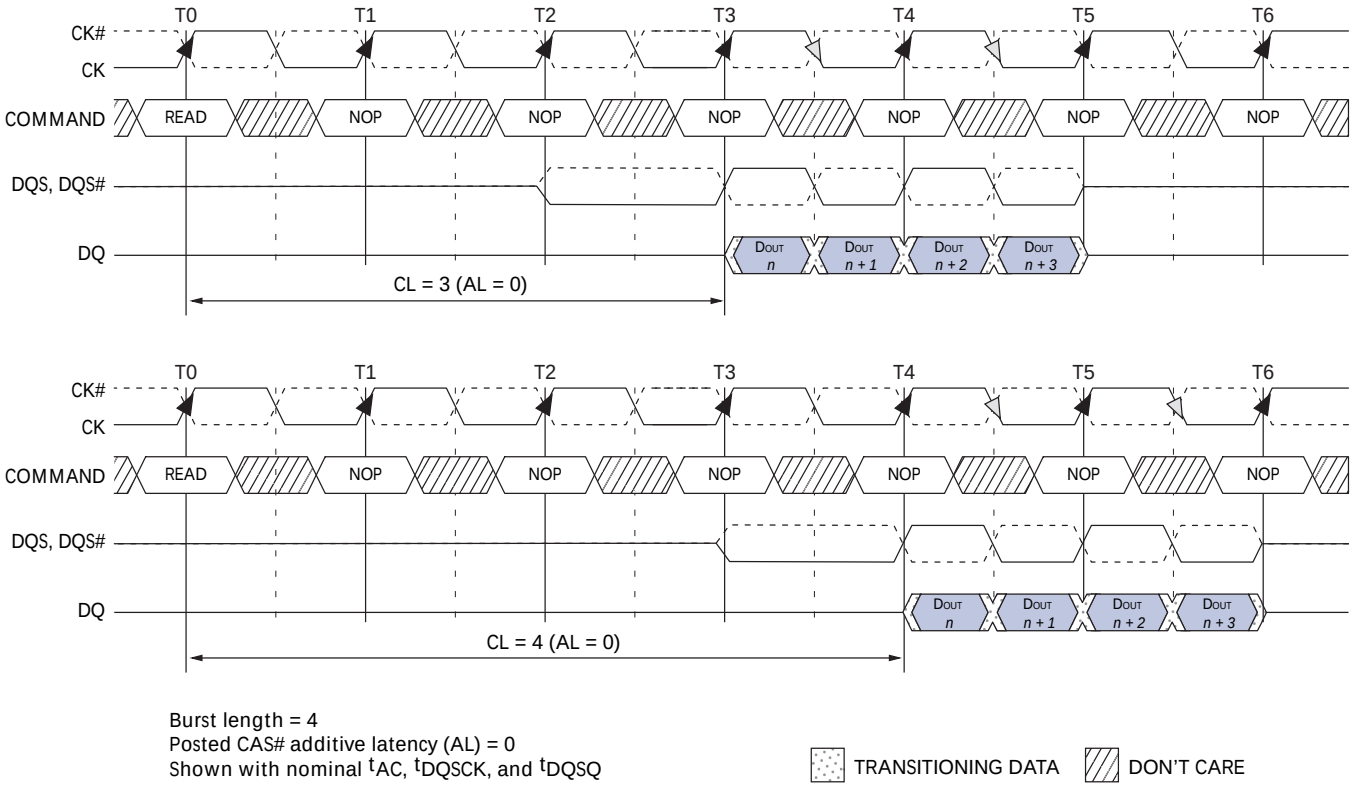
CAS Latency (CL)

The CAS Latency (CL) is defined by bits M4–M6 as shown in Figure 9. CAS Latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first bit of output data. The CAS Latency can be set to 3 or 4 clocks. CAS Latency of 2 or 5 clocks are JEDEC optional features and may be enabled in future speed grades. DDR2 SDRAM does not support any half clock latencies. Reserved states should not be used as unknown operation or incompatibility with future versions may result.

DDR2 SDRAM also supports a feature called Posted CAS additive latency (AL). This feature allows the READ command to be issued prior to ^{t}RCD(MIN) by delaying the internal command to the DDR2 SDRAM by AL clocks. The AL feature is described in more detail in the Extended Mode Register (EMR) and Operational sections.

Examples of CL = 3 and CL = 4 are shown in Figure 10; both assume AL = 0. If a READ command is registered at clock edge *n*, and the CAS Latency is *m* clocks, the data will be available nominally coincident with clock edge *n* + *m* (this assumes AL = 0).

Figure 10: CAS Latency (CL)



Burst length = 4
Posted CAS# additive latency (AL) = 0
Shown with nominal ^{t}AC, $^{t}DQSCK$, and $^{t}DQSQ$

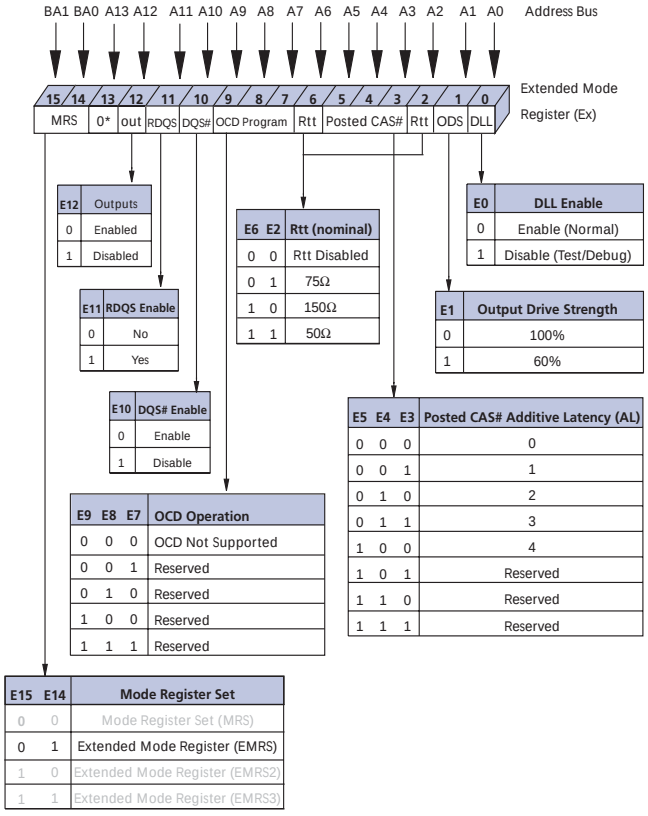
TRANSITIONING DATA DON'T CARE

Extended Mode Register (EMR)

The extended mode register controls functions beyond those controlled by the mode register; these additional functions are DLL enable/disable, output drive strength, ODT (RTT), Posted CAS additive latency (AL), off-chip driver impedance calibration (OCD), DQS# enable/disable, RDQS/RDQS# enable/disable, and OUTPUT disable/enable. These functions are controlled via the bits shown in Figure 11. The extended mode register is programmed via the LOAD MODE (LM) command and will retain the stored information until it is programmed again or the device loses power. Reprogramming the extended mode register will not alter the contents of the memory array, provided it is performed correctly.

The extended mode register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time ^{t}MRD before initiating any subsequent operation. Violating either of these requirements could result in unspecified operation.

Figure 11: Extended Mode Register Definition



*E13 (A13) is not used on the x16 configuration.

DLL Enable/Disable

The DLL may be enabled or disabled by programming bit E0 during the LOAD MODE command as shown in Figure 11. The DLL must be enabled for normal operation. DLL enable is required during power-up initialization and upon returning to normal operation after having disabled the DLL for the purpose of debugging or evaluation. Enabling the DLL should always be followed by resetting the DLL using a LOAD MODE command.

The DLL is automatically disabled when entering self refresh operation and is automatically re-enabled and reset upon exit of self refresh operation.

Any time the DLL is enabled (and subsequently reset), 200 clock cycles must occur before a READ command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the ^{t}AC or ^{t}DQSCK parameters.

Output Drive Strength

The output drive strength is defined by bit E1 as shown in Figure 11. The normal drive strength for all outputs are specified to be SSTL_18. Programming bit E1 = 0 selects normal (100 percent) drive strength for all outputs. Selecting a reduced drive strength option (bit E1 = 1) will reduce all outputs to approximately 60 percent of the SSTL_18 drive strength. This option is intended for the support of the lighter load and/or point-to-point environments.

DQS# Enable/Disable

The DQS# enable function is defined by bit E10. When enabled (bit E10 = 0), DQS# is the complement of the differential data strobe pair DQS/DQS#. When disabled (bit E10 = 1), DQS is used in a single-ended mode and the DQS# pin is disabled. This function is also used to enable/disable RDQS#. If RDQS is enabled (E11 = 1) and DQS# is enabled (E10 = 0), then both DQS# and RDQS# will be enabled.

RDQS Enable/Disable

The RDQS enable function is defined by bit E11 as shown in Figure 11. This feature is only applicable to the x8 configuration. When enabled (E11 = 1), RDQS is identical in function and timing to data strobe DQS during a READ. During a WRITE operation, RDQS is ignored by the DDR2 SDRAM.

Output Enable/Disable

The OUTPUT enable function is defined by bit E12 as shown in Figure 11. When enabled (E12 = 0), all outputs (DQs, DQS, DQS#, RDQS, RDQS#) function normally. When disabled (E12 = 1), all DDR2 SDRAM outputs (DQs, DQS, DQS#, RDQS, RDQS#) are disabled removing output buffer current. The OUTPUT disable feature is intended to be used during IDD characterization of read current.

On Die Termination (ODT)

ODT effective resistance RTT(EFF) is defined by bits E2 and E6 of the EMR as shown in Figure 11. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DDR2 SDRAM controller to independently turn on/off ODT for any or all devices. RTT effective resistance values of 75Ω and 150Ω are selectable and apply to each DQ, DQS/DQS#, RDQS/RDQS#, UDQS/UDQS#, LDQS/LDQS#, DM, and UDM/LDM signals. A functional representation of ODT is shown in block diagrams in "Functional Description" on page 13. Bits (E6, E2) determine what ODT resistance is enabled by turning on/off 'sw1' or 'sw2'. The ODT effective resistance value is selected by enabling switch 'sw1,' which enables all 'R1' values that are 150Ω each, enabling an effective resistance of 75Ω (RTT1(EFF) = 'R1' / 2). Similarly, if 'sw2' is enabled, all 'R2' values that are 300Ω each, enable an effective ODT resistance of 150Ω (RTT2(EFF) = 'R2'/2). Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

The ODT control pin is used to determine when RTT(EFF) is turned on and off, assuming ODT has been enabled via bits E2 and E6 of the EMR. The ODT feature and ODT input pin are only used during active, active power-down (both fast-exit and slow-exit modes), and precharge power-down modes of operation. If SELF REFRESH operation is used, RTT(EFF) should *always* be disabled and the ODT input pin is disabled by the DDR2 SDRAM. During power-up and initialization of the DDR2 SDRAM, ODT should be disabled until the EMR command is issued to enable the ODT feature, at which point the ODT pin will determine the RTT(EFF) value. See "ODT Timing" on page 9 for ODT timing diagrams.

Off-Chip Driver (OCD) Impedance Calibration

The OCD function is no longer supported and must be set to the default state. See "Initialization" on page 15 to properly set OCD defaults.

Posted CAS Additive Latency (AL)

Posted CAS additive latency (AL) is supported to make the command and data bus efficient for sustainable bandwidths in DDR2 SDRAM. Bits E3–E5 define the value of AL as shown in Figure 11. Bits E3–E5 allow the user to program the DDR2 SDRAM with a CAS# Additive latency of 0, 1, 2, 3, or 4 clocks. Reserved states should not be used as unknown operation or incompatibility with future versions may result.

In this operation, the DDR2 SDRAM allows a READ or WRITE command to be issued prior to ^{t}RCD (MIN) with the requirement that AL ≤ ^{t}RCD(MIN). A typical application using this feature would set AL = ^{t}RCD (MIN) - 1 x ^{t}CK. The READ or WRITE command is held for the time of the additive latency (AL) before it is issued internally to the DDR2 SDRAM device. READ Latency (RL) is controlled by the sum of the Posted CAS additive latency (AL) and CAS Latency (CL); RL = AL + CL. Write latency (WL) is equal to READ latency minus one clock; WL = AL + CL - 1 x ^{t}CK. An example of a READ latency is shown in Figure 12. An example of a WRITE latency is shown in Figure 13.

Figure 12: READ Latency

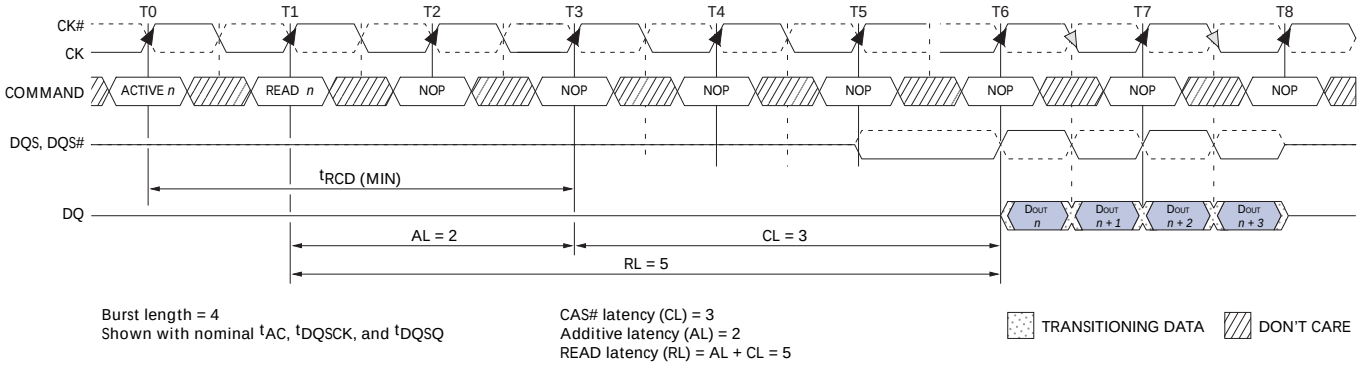
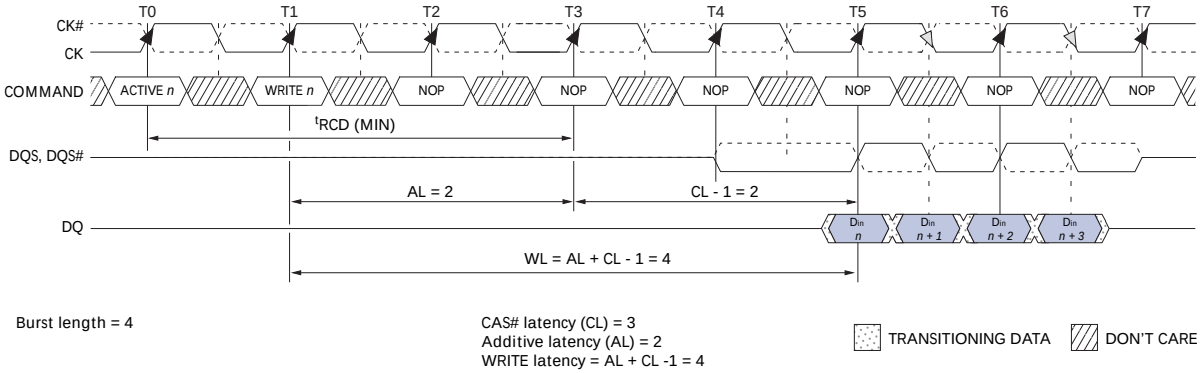


Figure 13: Write Latency

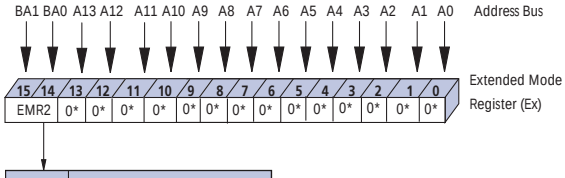


Extended Mode Register 2 (EMR2)

The Extended Mode Register 2 (EMR2) controls functions beyond those controlled by the mode register. Currently all bits in EMR2 are reserved as shown in Figure 14. The EMR2 is programmed via the LOAD MODE command and will retain the stored information until it is programmed again or the device loses power. Reprogramming the extended mode register will not alter the contents of the memory array, provided it is performed correctly.

The extended mode register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time ^{t}MRD before initiating any subsequent operation. Violating either of these requirements could result in unspecified operation.

Figure 14: Extended Mode Register 2 (EMR2) Definition



M15	M14	Mode Register Definition
0	0	Mode Register (MR)
0	1	Extended Mode Register (EMR)
1	0	Extended Mode Register (EMR2)
1	1	Extended Mode Register (EMR3)

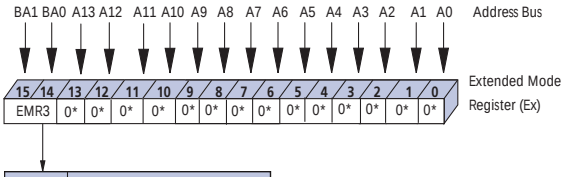
* E13 (A13) - E0 (A0) are reserved for future use and must all be programmed to '0'.
A13 is not used in x16 configuration.

Extended Mode Register 3 (EMR3)

The Extended Mode Register 3 (EMR3) controls functions beyond those controlled by the mode register. Currently all bits in EMR3 are reserved as shown in Figure 15. The EMR3 is programmed via the LOAD MODE command and will retain the stored information until it is programmed again or the device loses power. Reprogramming the extended mode register will not alter the contents of the memory array, provided it is performed correctly.

The extended mode register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time ^{t}MRD before initiating any subsequent operation. Violating either of these requirements could result in unspecified operation.

Figure 15: Extended Mode Register 3 (EMR3) Definition



M15	M14	Mode Register Definition
0	0	Mode Register (MR)
0	1	Extended Mode Register (EMR)
1	0	Extended Mode Register (EMR2)
1	1	Extended Mode Register (EMR3)

* E13 (A13) - E0 (A0) are reserved for future use and must all be programmed to '0'.
A13 is not used in x16 configuration.

Command Truth Tables

The following tables provide a quick reference of DDR2 SDRAM available commands, including CKE power-down modes, and bank-to-bank commands.

Table 4: Truth Table – DDR2 Commands

Notes: 1, 5, and 6 apply to the entire Table.

FUNCTION	CKE		CS#	RAS#	CAS#	WE#	BA1 BA0	A12 A11	A10	A9–A0	NOTES
	PREVIOUS CYCLE	CURRENT CYCLE									
Load Mode	H	H	L	L	L	L	BA	OP Code			2
Refresh	H	H	L	L	L	H	X	X	X	X	
Self Refresh Entry	H	L	L	L	L	H	X	X	X	X	
Self Refresh Exit	L	H	H	X	X	X	X	X	X	X	7
			L	H	H	H					
Single Bank Precharge	H	H	L	L	H	L	BA	X	L	X	2
ALL Banks Precharge	H	H	L	L	H	L	X	X	H	X	
Bank Activate	H	H	L	L	H	H	BA	Row Address			
Write	H	H	L	H	L	L	BA	Column Address	L	Column Address	2, 3
Write with Auto Precharge	H	H	L	H	L	L	BA	Column Address	H	Column Address	2, 3
Read	H	H	L	H	L	H	BA	Column Address	L	Column Address	2, 3
Read with Auto Precharge	H	H	L	H	L	H	BA	Column Address	H	Column Address	2, 3
No Operation	H	X	L	H	H	H	X	X	X	X	
Device Deselect	H	X	H	X	X	X	X	X	X	X	
Power-Down Entry	H	L	H	X	X	X	X	X	X	X	4
			L	H	H	H					
Power-Down Exit	L	H	H	X	X	X	X	X	X	X	4
			L	H	H	H					

NOTE:

1. All DDR2 SDRAM commands are defined by states of CS#, RAS#, CAS#, WE#, and CKE at the rising edge of the clock.
2. Bank addresses (BA) BA1-BA0 determine which bank is to be operated upon. BA during a Load Mode command selects which mode register is programmed.
3. Burst reads or writes at BL = 4 cannot be terminated or interrupted. See sections "Read Interrupted by a Read" and "Write Interrupted by a Write" for other restrictions and details.
4. The Power Down Mode does not perform any refresh operations. The duration of power-down is therefore limited by the refresh requirements outlined in the AC parametric section.
5. The state of ODT does not affect the states described in this table. The ODT function is not available during self refresh. See the ODT section for details.
6. "X" means "H or L" (but a defined logic level).
7. Self refresh exit is asynchronous.

Table 5: Truth Table – Current State Bank *n* - Command to Bank *n*

Notes: 1–6; notes appear below and on next page.

CURRENT STATE	CS#	RAS#	CAS#	WE#	COMMAND/ACTION	NOTES
Any	H	X	X	X	DESELECT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	L	L	H	H	ACTIVE (select and activate row)	
	L	L	L	H	REFRESH	7
	L	L	L	L	LOAD MODE	7
Row Active	L	H	L	H	READ (select column and start READ burst)	9
	L	H	L	L	WRITE (select column and start WRITE burst)	9
	L	L	H	L	PRECHARGE (deactivate row in bank or banks)	8
Read (Auto-Precharge Disabled	L	H	L	H	READ (select column and start new READ burst)	9
	L	H	L	L	WRITE (select column and start WRITE burst)	9, 11
	L	L	H	L	PRECHARGE (start precharge)	8
Write (Auto-Precharge Disabled)	L	H	L	H	READ (select column and start READ burst)	9, 10
	L	H	L	L	WRITE (select column and start new WRITE burst)	9
	L	L	H	L	PRECHARGE (start precharge)	8, 10

NOTE:

1. This table applies when CKE*n* - 1 was HIGH and CKE*n* is HIGH (see Table 5) and after ^{t}XSNR has been met (if the previous state was self refresh).
2. This table is bank-specific, except where noted (i.e., the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state). Exceptions are covered in the notes below.
3. Current state definitions:

   Idle: The bank has been precharged, and ^{t}RP has been met.

   Row Active: A row in the bank has been activated, and ^{t}RCD has been met. No data bursts/accesses and no register accesses are in progress.

   Read: A READ burst has been initiated, with auto precharge disabled, and has not yet terminated.

   Write: A WRITE burst has been initiated, with auto precharge disabled, and has not yet terminated.
4. The following states must not be interrupted by a command issued to the same bank. DESELECT or NOP commands, or allowable commands to the other bank, should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and Table 5, and according to Table 6.

   Precharging: Starts with registration of a PRECHARGE command and ends when ^{t}RP is met. Once ^{t}RP is met, the bank will be in the idle state.

   Row Activating: Starts with registration of an ACTIVE command and ends when ^{t}RCD is met. Once ^{t}RCD is met, the bank will be in the "row active" state.

   Read with Auto Precharge Enabled: Starts with registration of a READ command with auto precharge enabled and ends when ^{t}RP has been met. Once ^{t}RP is met, the bank will be in the idle state.

   Write with Auto Precharge Enabled: Starts with registration of a WRITE command with auto precharge enabled and ends when ^{t}RP has been met. Once ^{t}RP is met, the bank will be in the idle state.
5. The following states must not be interrupted by any executable command; DESELECT or NOP commands must be applied on each positive clock edge during these states.

   Refreshing: Starts with registration of an REFRESH command and ends when ^{t}RFC is met. Once ^{t}RFC is met, the DDR2 SDRAM will be in the all banks idle state.

   Accessing Mode Register: Starts with registration of a LOAD MODE command and ends when ^{t}MRD has been met. Once ^{t}MRD is met, the DDR2 SDRAM will be in the all banks idle state.

   Precharging All: Starts with registration of a PRECHARGE ALL command and ends when ^{t}RP is met. Once ^{t}RP is met, all banks will be in the idle state.
6. All states and sequences not shown are illegal or reserved.

7. Not bank-specific; requires that all banks are idle, and bursts are not in progress.
8. May or may not be bank-specific; if multiple banks are to be precharged, each must be in a valid state for precharging.
9. READs or WRITEs listed in the Command/Action column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
10. Requires appropriate DM masking.
11. A WRITE command may be applied after the completion of the READ burst.

Table 6: Truth Table – Current State Bank *n* - Command to Bank *m*

Notes: 1–6; notes appear below and on next page.

CURRENT STATE	CS#	RAS#	CAS#	WE#	COMMAND/ACTION	NOTES
Any	H	X	X	X	DESELECT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	X	X	X	X	Any Command Otherwise Allowed to Bank m	
Row Activating, Active, or Precharging	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7
	L	H	L	L	WRITE (select column and start WRITE burst)	7
	L	L	H	L	PRECHARGE	
Read (Auto Precharge Disabled	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	7
	L	H	L	L	WRITE (select column and start WRITE burst)	7, 9
	L	L	H	L	PRECHARGE	
Write (Auto Precharge Disabled.)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7, 8
	L	H	L	L	WRITE (select column and start new WRITE burst)	7
	L	L	H	L	PRECHARGE	
Read (with Auto-Precharge)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	7, 3a
	L	H	L	L	WRITE (select column and start WRITE burst)	7, 9, 3a
	L	L	H	L	PRECHARGE	
Write (with Auto-Precharge)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7, 3a
	L	H	L	L	WRITE (select column and start new WRITE burst)	7, 3a
	L	L	H	L	PRECHARGE	

NOTE:

1. This table applies when CKE*n* - 1 was HIGH and CKE*n* is HIGH (see Truth Table 2) and after ^{t}XSNR has been met (if the previous state was self refresh).
2. This table describes alternate bank operation, except where noted (i.e., the current state is for bank *n* and the commands shown are those allowed to be issued to bank *m*, assuming that bank *m* is in such a state that the given command is allowable). Exceptions are covered in the notes below.
3. Current state definitions:

   Idle: The bank has been precharged, and ^{t}RP has been met.

   Row Active: A row in the bank has been activated, and ^{t}RCD has been met. No data bursts/accesses and no register accesses are in progress.
   Read: A READ burst has been initiated, with auto precharge disabled, and has not yet terminated.
   Write: A WRITE burst has been initiated, with auto precharge disabled, and has not yet terminated.
   Read with Auto Precharge Enabled: See following text – 3a
   Write with Auto Precharge Enabled: See following text – 3a
   3a.The read with auto precharge enabled or write with auto precharge enabled states can each be broken into two parts: the access period and the precharge period. For read with auto precharge, the precharge period is defined as if the same burst was executed with auto precharge disabled and then followed with the earliest possible PRECHARGE command that still accesses all of the data in the burst. For write with auto precharge, the precharge period begins when ^{t}WR ends, with ^{t}WR measured as if auto precharge was disabled. The access period starts with registration of the command and ends where the precharge period (or ^{t}RP) begins.
   This device supports concurrent auto precharge such that when a read with auto precharge is enabled or a write with auto precharge is enabled any command to other banks is allowed, as long as that command does not interrupt the read or write data transfer already in process. In either case, all other related limitations apply (e.g., contention between read data and write data must be avoided).

3b.The minimum delay from a read or write command with auto precharge enabled, to a command to a different bank is summarized below.

CL = CAS Latency; BL = bust length; WL = WRITE latency

FROM COMMAND (BANK *n*)	TO COMMAND (BANK *m*)	MINIMUM DELAY (WITH CONCURRENT AUTO PRECHARGE)	UNITS
WRITE with Auto Precharge	READ or READ w/AP	(CL - 1) + (BL / 2) + ^{t}WTR	^{t}CK
	WRITE or WRITE w/AP	(BL / 2)	^{t}CK
	PRECHARGE or ACTIVE	1	^{t}CK
READ with Auto Precharge	READ or READ w/AP	(BL / 2)	^{t}CK
	WRITE or WRITE w/AP	(BL / 2) + 2	^{t}CK
	PRECHARGE or ACTIVE	1	^{t}CK

4. REFRESH and LOAD MODE commands may only be issued when all banks are idle.
5. Not used.
6. All states and sequences not shown are illegal or reserved.
7. READs or WRITEs listed in the Command/Action column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
8. Requires appropriate DM masking.
9. A WRITE command may be applied after the completion of the READ burst.
10. ^{t}WTR is defined as Min (2 or ^{t}WTR/^{t}CK rounded up to the next integer).

DESELECT, NOP, and LOAD MODE Commands

DESELECT

The DESELECT function (CS# HIGH) prevents new commands from being executed by the DDR2 SDRAM. The DDR2 SDRAM is effectively deselected. Operations already in progress are not affected.

NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to instruct the selected DDR2 SDRAM to perform a NOP (CS# is LOW; RAS#, CAS#, and WE are HIGH). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

LOAD MODE (LM)

The mode registers are loaded via inputs BA1-BA0 and A13 – A0 for x4 and x8, and A12 - A0 for x16 configurations. BA1-BA0 determine which mode register will be programmed. See “Mode Register (MR)” on page 11. The LOAD MODE command can only be issued when all banks are idle, and a subsequent executable command cannot be issued until ^{t}MRD is met.

Bank/Row Activation

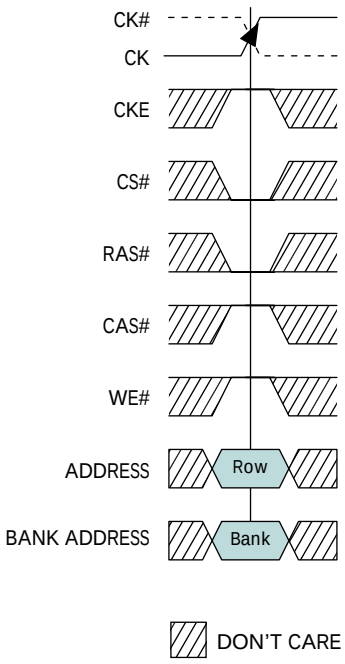
ACTIVE Command

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA1-BA0 inputs selects the bank, and the address provided on inputs A13 – A0 for x4 and x8, and A12 - A0 for x16 selects the row. This row remains active (or open) for accesses until a PRECHARGE command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

ACTIVE Operation

Before any READ or WRITE commands can be issued to a bank within the DDR2 SDRAM, a row in that bank must be "opened" (activated). This is accomplished via the ACTIVE command, which selects both the bank and the row to be activated, as shown in Figure 16.

Figure 16: ACTIVE Command



After a row is opened with an ACTIVE command, a READ or WRITE command may be issued to that row, subject to the ^{t}RCD specification. ^{t}RCD (MIN) should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVE command on which a READ or WRITE command can be entered. The same procedure is used to convert other specification limits from time units to clock cycles. For example, a ^{t}RCD(MIN) specification of 20ns with a 266 MHz clock (^{t}CK = 3.75ns) results in 5.3 clocks rounded up to 6. This is reflected in Figure 18, which covers any case where 5 < ^{t}RCD (MIN) / ^{t}CK ≤ 6. Figure 18 also shows the case for ^{t}RRD where 2 < ^{t}RRD (MIN) / ^{t}CK ≤ 3.

A subsequent ACTIVE command to a different row in the same bank can only be issued after the previous active row has been "closed" (precharged). The minimum time interval between successive ACTIVE commands to the same bank is defined by ^{t}RC.

A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive ACTIVE commands to different banks is defined by ^{t}RRD.

READs

READ Command

The READ command is used to initiate a burst read access to an active row. The value on the BA1-BA0 inputs selects the bank, and the address provided on inputs A0–*i* (where i = A9 for x16, A9 for x8, or A9, A11 for x4) selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the READ burst; if auto precharge is not selected, the row will remain open for subsequent accesses.

READ Operation

READ bursts are initiated with a READ command, as shown in Figure 17. The starting column and bank addresses are provided with the READ command and auto precharge is either enabled or disabled for that burst access. If auto precharge is enabled, the row being accessed is automatically precharged at the completion of the burst. If auto precharge is disabled, the row will be left open after the completion of the burst.

During READ bursts, the valid data-out element from the starting column address will be available READ latency (RL) clocks later. READ latency (RL) is defined as the sum of Posted CAS additive latency (AL) and CAS Latency (CL); RL = AL + CL. The value for AL and CL are programmable via the MR and EMR commands, respectively. Each subsequent data-out element will be valid nominally at the next positive or negative clock edge (i.e., at the next crossing of CK and CK#). Figure 19 shows examples of READ latency based on different AL and CL settings.

Figure 17: READ Command

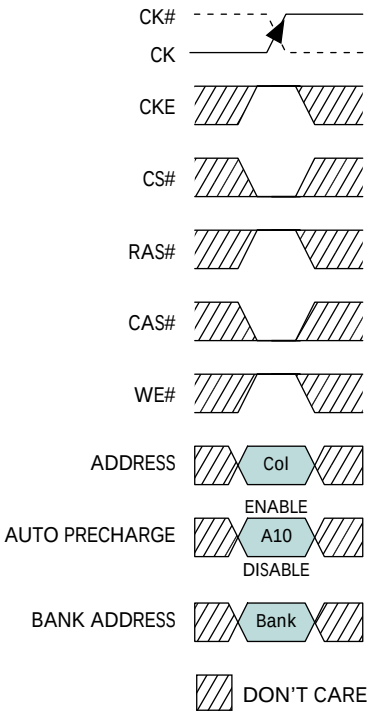


Figure 18: Example: Meeting ^{t}RRD (MIN) and ^{t}RCD (MIN)

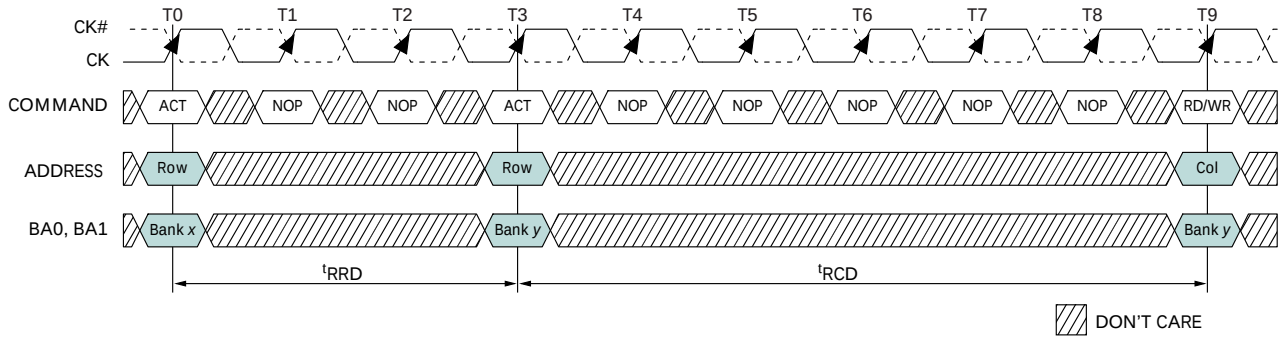
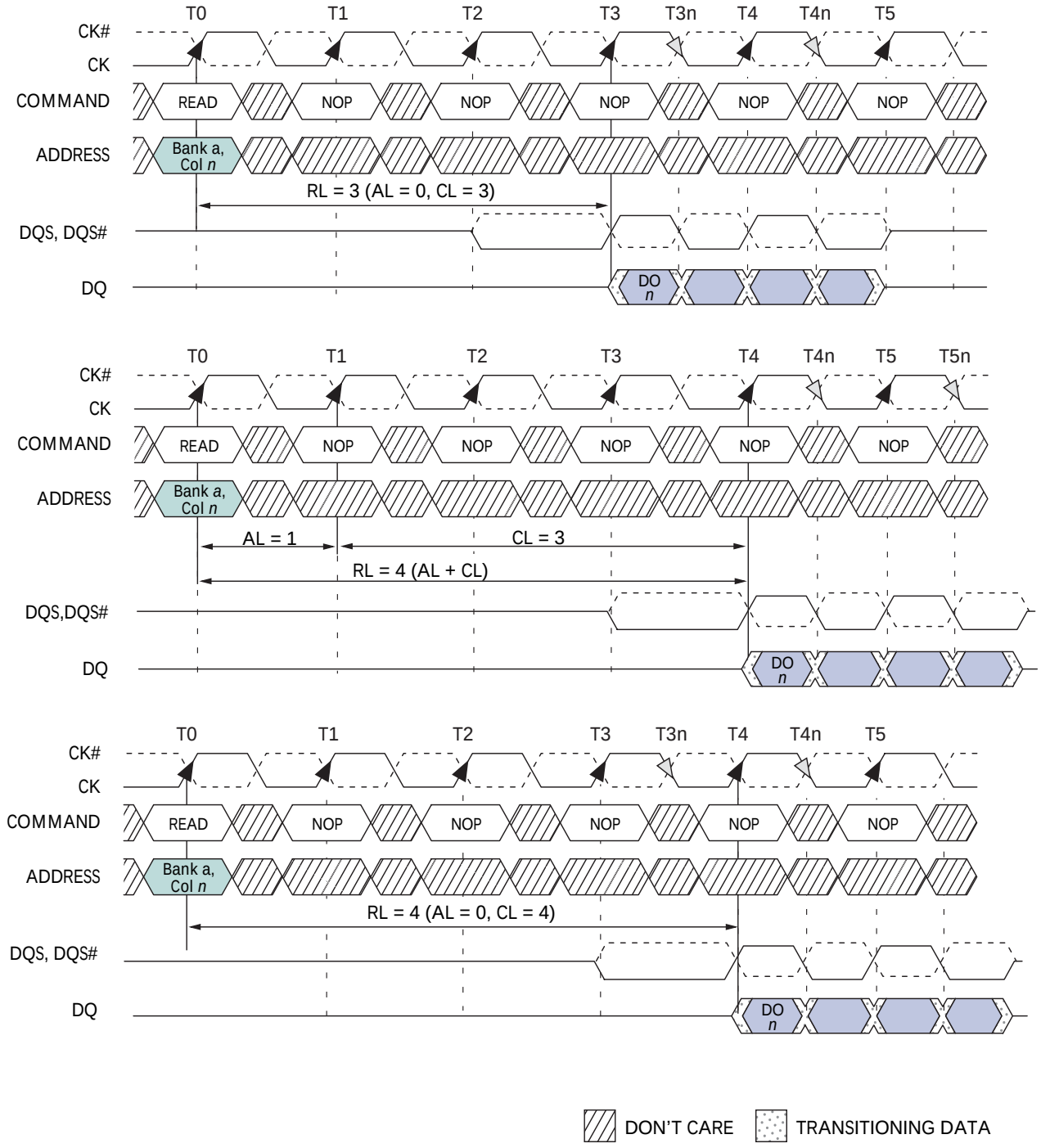


Figure 19: READ Latency



NOTE:

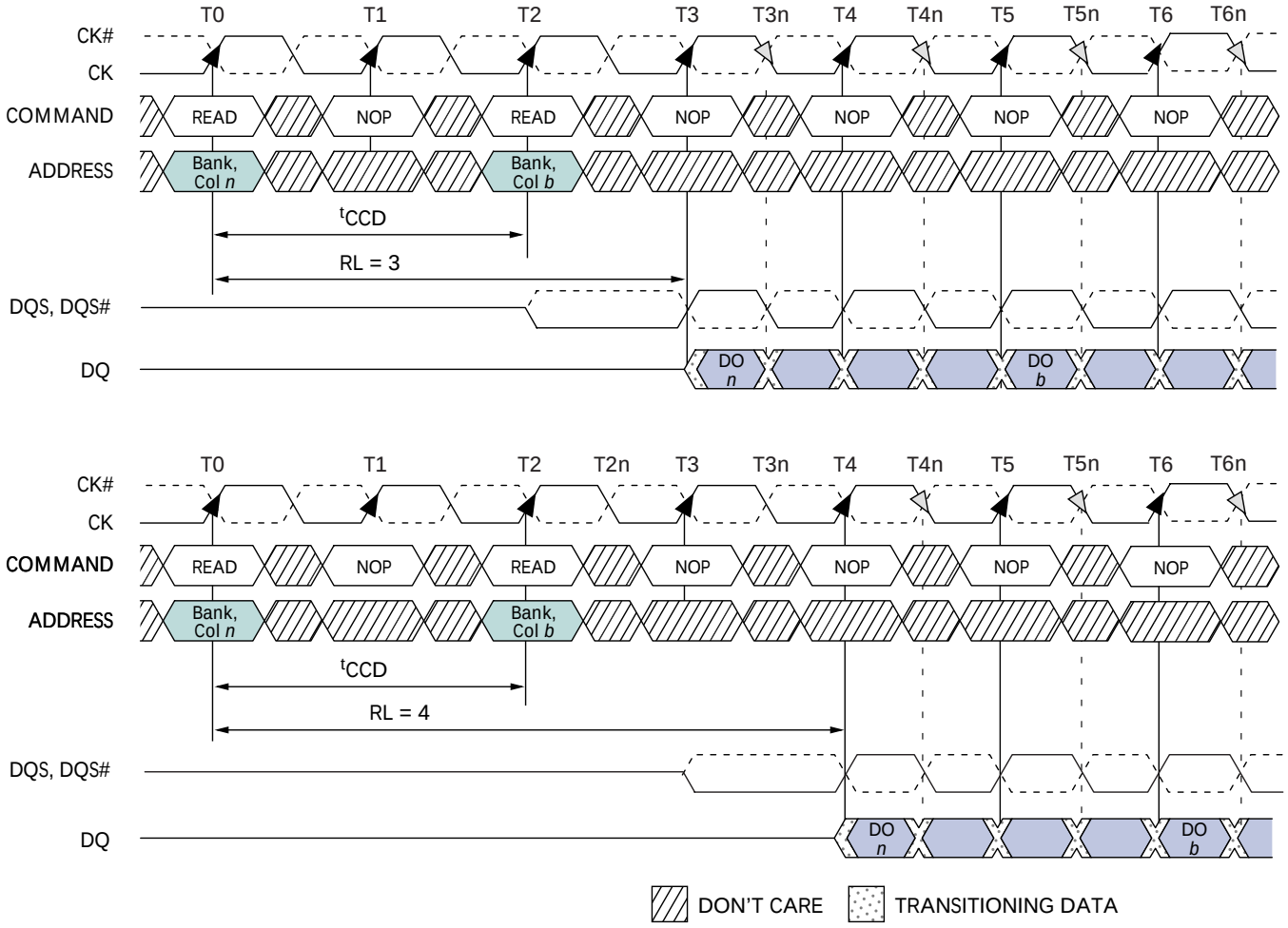
1. DO *n* = data-out from column *n*.
2. Burst length = 4.
3. Three subsequent elements of data-out appear in the programmed order following DO *n*.
4. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.

DQS/DQS# is driven by the DDR2 SDRAM along with output data. The initial LOW state on DQS and HIGH state on DQS# is known as the READ preamble (^{t}RPRE). The LOW state on DQS and HIGH state on DQS# coincident with the last data-out element is known as the read postamble (^{t}RPST).

Upon completion of a burst, assuming no other commands have been initiated, the DQs will go High-Z. A detailed explanation of ^{t}DQSQ (valid data-out skew), ^{t}QH (data-out window hold), the valid data window are depicted in Figure 28 on page 40 and Figure 29 on page 41. A detailed explanation of ^{t}DQSCK (DQS transition skew to CK) and ^{t}AC (data-out transition skew to CK) is shown in Figure 30 on page 42.

Data from any READ burst may be concatenated with data from a subsequent READ command to provide a continuous flow of data. The first data element from the new burst follows the last element of a completed burst. The new READ command should be issued *x* cycles after the first READ command, where *x* equals BL / 2 cycles. This is shown in Figure 20.

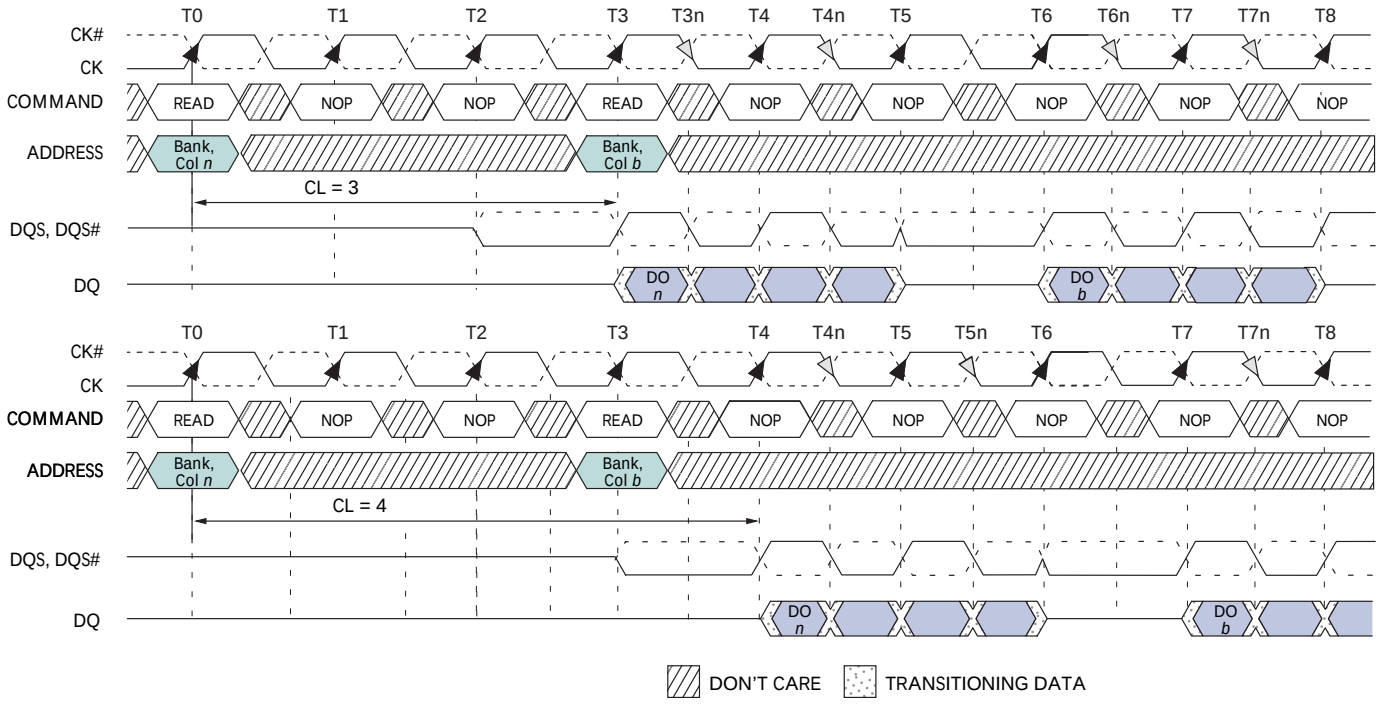
Figure 20: Consecutive READ Bursts



NOTE:

1. 1. DO *n* (or *b*) = data-out from column n (or column *b*).
2. Burst length = 4.
3. Three subsequent elements of data-out appear in the programmed order following DO *n*.
4. Three subsequent elements of data-out appear in the programmed order following DO *b*.
5. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.
6. Example applies only when READ commands are issued to same device.

Figure 21: Nonconsecutive READ Bursts



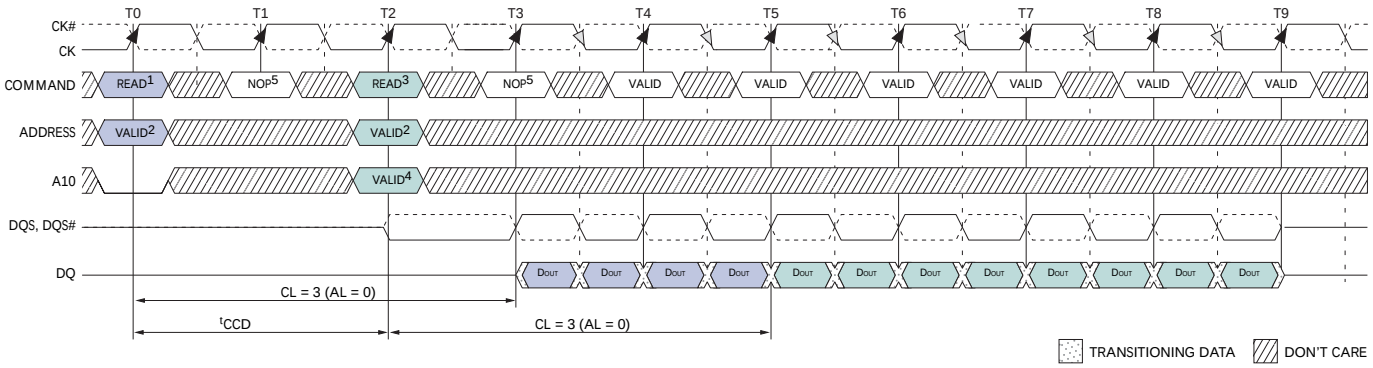
NOTE:

1. DO *n* (or *b*) = data-out from column *n* (or column *b*).
2. Burst length = 4.
3. Three subsequent elements of data-out appear in the programmed order following DO *n*.
4. Three subsequent elements of data-out appear in the programmed order following DO *b*.
5. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.
6. Example applies when READ commands are issued to different devices or nonconsecutive READs.

Nonconsecutive read data is illustrated in Figure 21 on page 34. Full-speed random read accesses within a page (or pages) can be performed. DDR2 SDRAM supports the use of concurrent auto precharge timing, which is shown in Table 7 on page 36.

DDR2 SDRAM does not allow interrupting or truncating of any READ burst using BL = 4 operations. Once the BL = 4 READ command is registered, it must be allowed to complete the entire READ burst. However, a READ (with AUTO PRECHARGE disabled) using BL = 8 operation may be interrupted and truncated ONLY by another READ burst as long as the interruption occurs on a four-bit boundary due to the 4*n* prefetch architecture of DDR2 SDRAM. READ burst BL = 8 operations may not be interrupted or truncated with any command except another READ command as shown in Figure 22 on page 35.

Figure 22: READ Interrupted by READ



NOTE:

1. Burst length = 8 required, AUTO PRECHARGE must be disabled (A10 = LOW).
2. READ command can be issued to any valid bank and row address (READ command at T0 and T2 can be either same bank or different bank).
3. Interupting READ command must be issued exactly 2 x ^{t}CK from previous READ.
4. AUTO PRECHARGE can be either enabled (A10 = HIGH) or disabled (A10 = LOW) by the interupting READ command.
5. NOP or COMMAND INHIBIT commands are valid. PRECHARGE command cannot be issued to banks used for READs at T0 and T2.
6. Example shown uses additive latency = 0; CAS Latency = 3, BL = 8, shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.

Table 7: READ Using Concurrent Auto Precharge

BL = burst length.

FROM COMMAND (BANK *n*)	TO COMMAND (BANK *m*)	MINIMUM DELAY (WITH CONCURRENT AUTO PRECHARGE)	UNITS
READ with Auto Precharge	READ or READ w/AP	(BL/2)	^{t}CK
	WRITE or WRITE w/AP	(BL/2) + 2	^{t}CK
	PRECHARGE or ACTIVE	1	^{t}CK

Data from any READ burst must be completed before a subsequent WRITE burst is allowed. An example of a READ burst followed by a WRITE burst is shown in Figure 25. The ^{t}DQSS (MIN) case is shown; the ^{t}DQSS (MAX) case has a longer bus idle time. (^{t}DQSS [MIN] and ^{t}DQSS [MAX] are defined in the section on WRITEs.)

A READ burst may be followed by a PRECHARGE command to the same bank provided that AUTO PRECHARGE is not activated. Examples of READ to PRECHARGE are shown in Figure 23 for BL=4 and Figure 24 for BL=8. The delay from READ command to PRECHARGE command to the same bank is AL + BL/2 + tRTP - 2 clocks.

If A10 is HIGH when a READ command is issued, the READ with AUTO PRECHARGE function is engaged. The DDR2 SDRAM starts an AUTO PRECHARGE operation on the rising edge which is (AL + BL/2) cycles later than the READ with AP command if ^{t}RAS (MIN) and ^{t}RTP are satisfied. If ^{t}RAS (MIN) is not satisfied at the edge, the start point of AUTO PRECHARGE operation will be delayed until ^{t}RAS (MIN) is satisfied. If ^{t}RTP (MIN) is not satisfied at the edge, the start point of the AUTO PRECHARGE operation will be delayed until ^{t}RTP (MIN) is satisfied. In case the internal precharge is pushed out by ^{t}RTP, ^{t}RP starts at the point where the internal precharge happens (not at the next rising clock edge after this event). So for BL = 4 the minimum time from READ with AP to the next activate command becomes AL + (^{t}RTP + ^{t}RP)* (see Figure 23 on page 36); for BL = 8 the time from READ with AP to the next activate is AL + 2 clocks + (^{t}RTP + ^{t}RP)* (see Figure 24 on page 37), where * means each parameter term is divided by ^{t}CK and rounded up to the next integer. In any event, internal precharge does not start earlier than two clocks after the last four-bit prefetch.

Figure 23: READ to PRECHARGE BL = 4

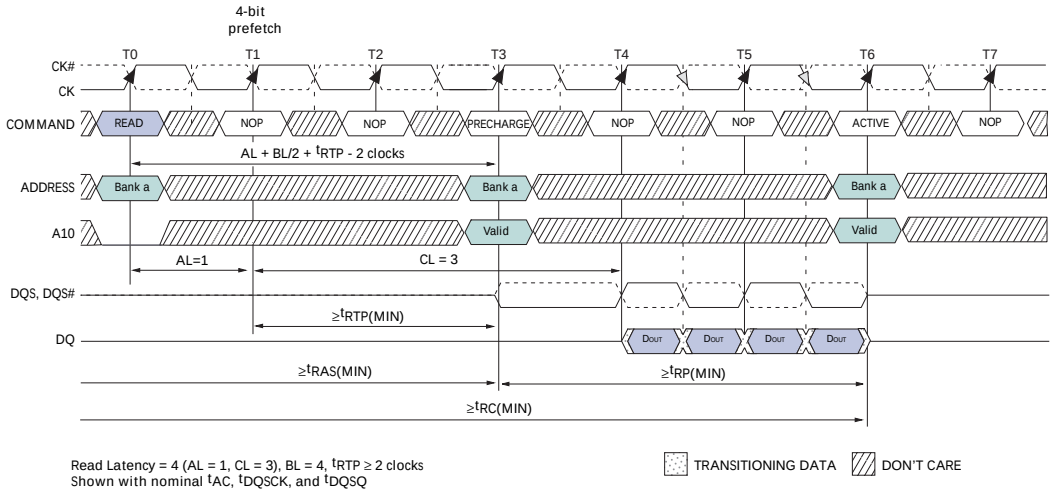


Figure 24: READ to PRECHARGE BL = 8

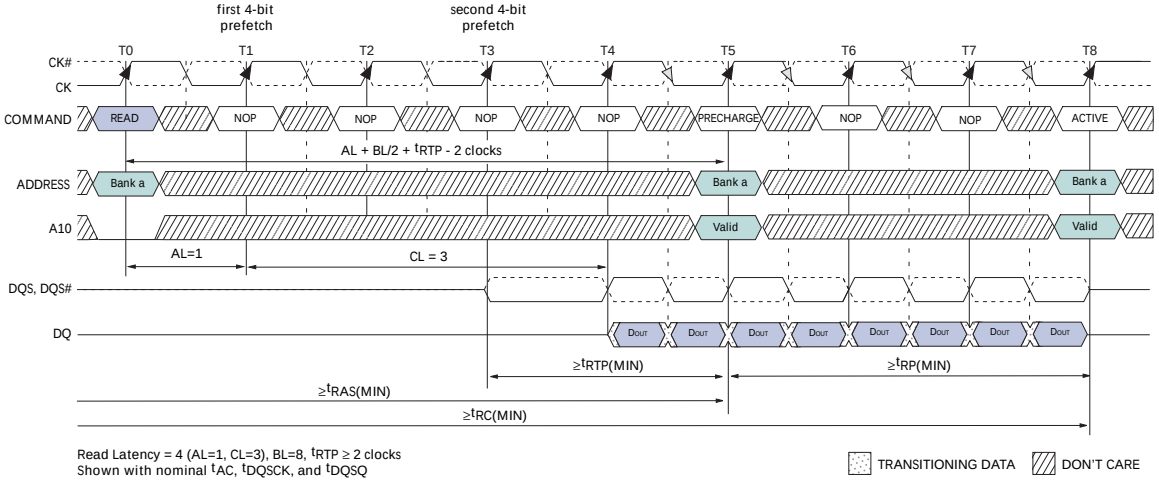


Figure 25: READ to WRITE

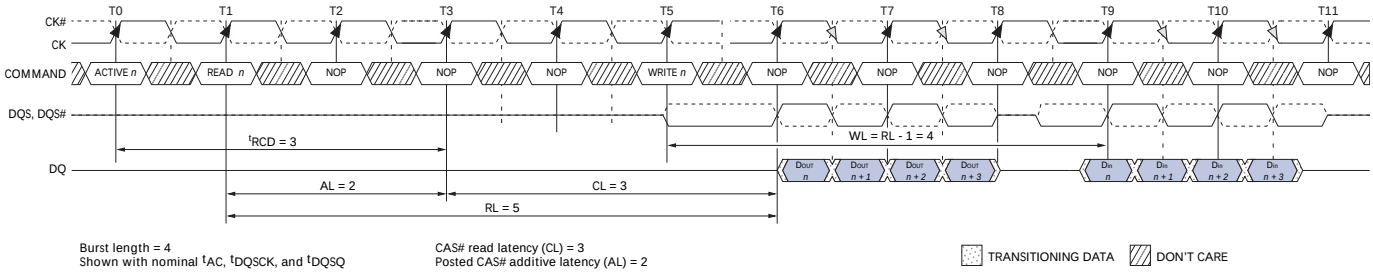
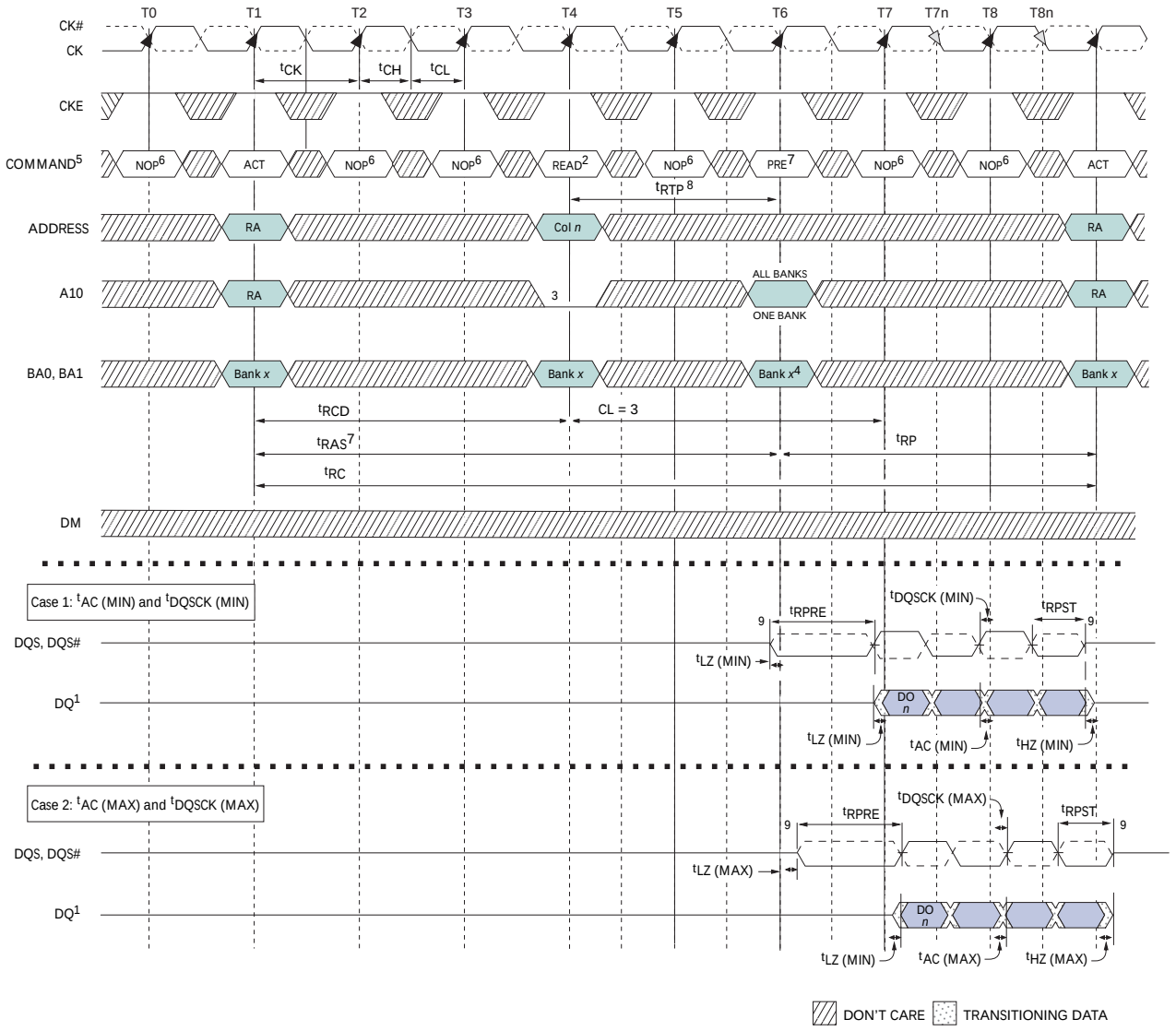


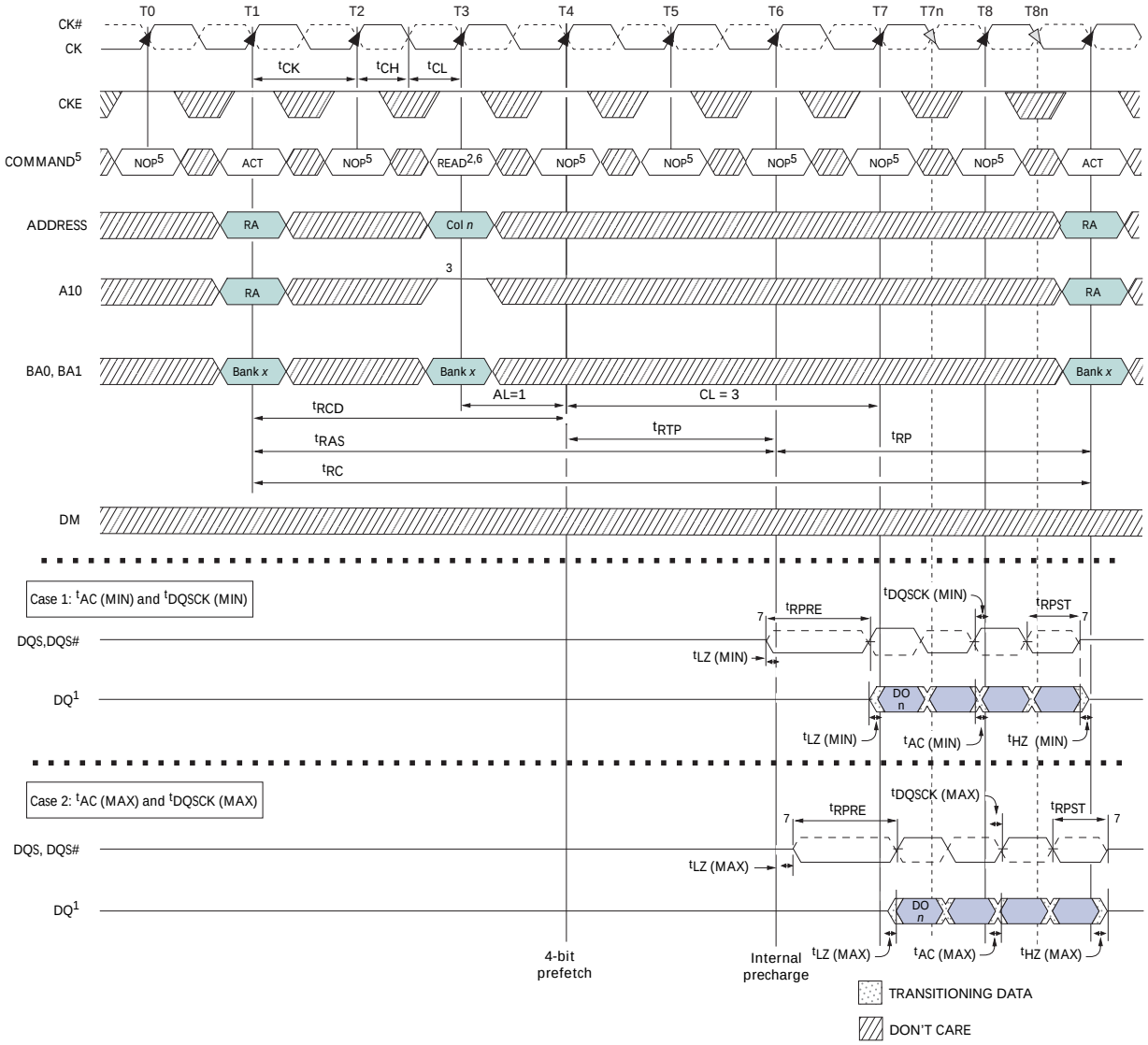
Figure 26: Bank Read – Without Auto Precharge



NOTE:

1. DO *n* = data-out from column *n*; subsequent elements are applied in the programmed order.
2. Burst length = 4 and AL = 0 in the case shown.
3. Disable auto precharge.
4. "Don't Care" if A10 is HIGH at T5.
5. PRE = PRECHARGE, ACT = ACTIVE, RA = row address, BA = bank address.
6. NOP commands are shown for ease of illustration; other commands may be valid at these times.
7. The PRECHARGE command can only be applied at T6 if ^{t}RAS minimum is met.
8. Read to Precharge = AL +BL/2 + ^{t}RTP-2 clocks.
9. I/0 pins, when entering or exiting HIGH-Z are not referenced to a specific voltage level, but when the device begins to drive or no longer drives, respecively.

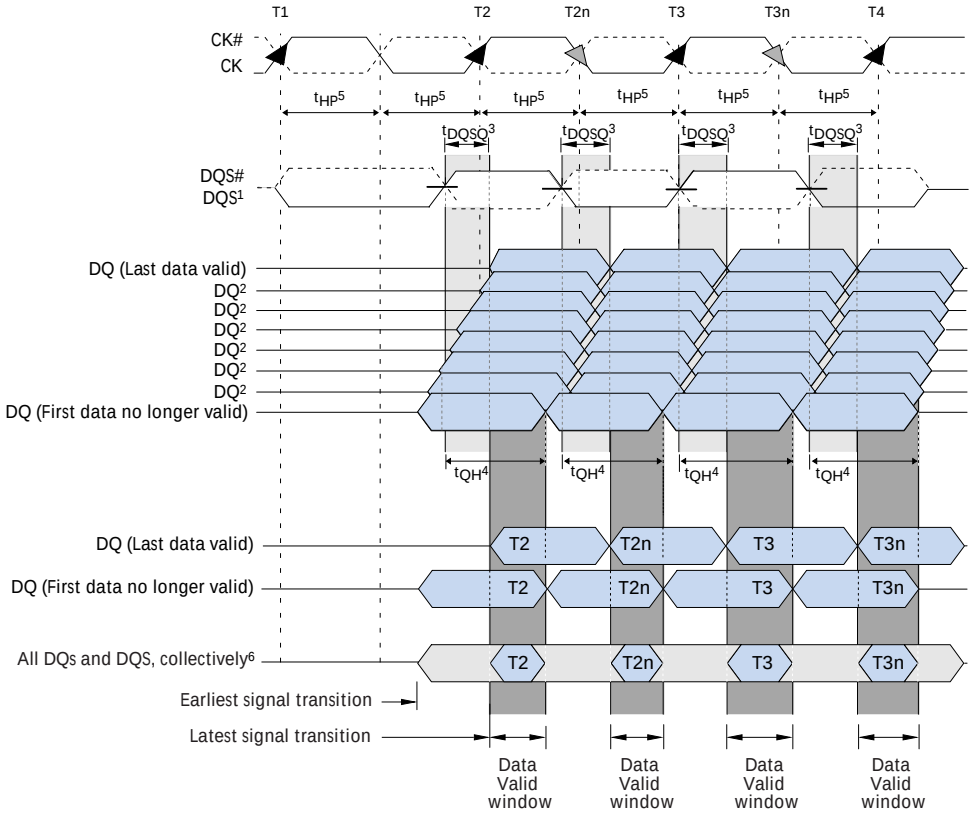
Figure 27: Bank Read – With Auto Precharge



NOTE:

1. DO *n* = data-out from column n; subsequent elements are applied in the programmed order.
2. Burst length = 4, RL = 4 (AL = 1, CL = 3) in the case shown.
3. Enable auto precharge.
4. ACT = ACTIVE, RA = row address, BA = bank address.
5. NOP commands are shown for ease of illustration; other commands may be valid at these times.
6. The DDR2 SDRAM internally delays auto precharge until both ^{t}RAS (MIN) and ^{t}RTP (MIN) have been satisfied.
7. I/0 pins, when entering or exiting HIGH-Z are not referenced to a specific voltage level, but when the device begins to drive or no longer drives, respecively.

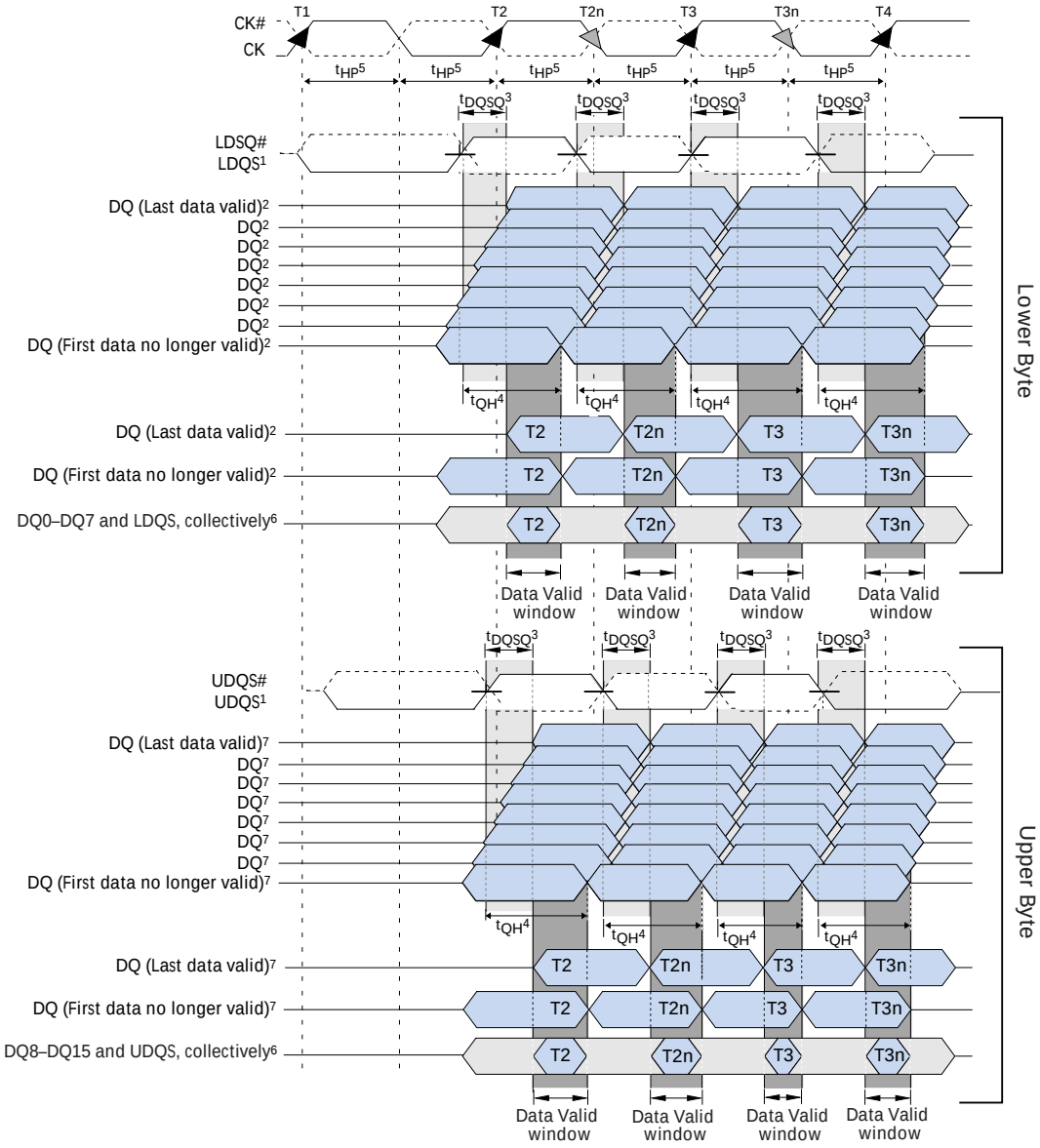
Figure 28: x4, x8 Data Output Timing – ^{t}DQSQ, ^{t}QH, and Data Valid Window



NOTE:

1. DQs transitioning after DQS transition define tDQSQ window. DQS transitions at T2 and at T2n are “early DQS,” at T3 are “nominal DQS,” and at T3n are "late DQS."
2. For a x4, only two DQs apply.
3. ^{t}DQSQ is derived at each DQS clock edge and is not cumulative over time and begins with DQS transitions and ends with the last valid transition of DQs .
4. ^{t}QH is derived from ^{t}HP: ^{t}QH = ^{t}HP - ^{t}QHS.
5. ^{t}HP is the lesser of ^{t}CL or ^{t}CH clock transitions collectively when a bank is active.
6. The data valid window is derived for each DQS transition and is defined as ^{t}QH minus ^{t}DQSQ.

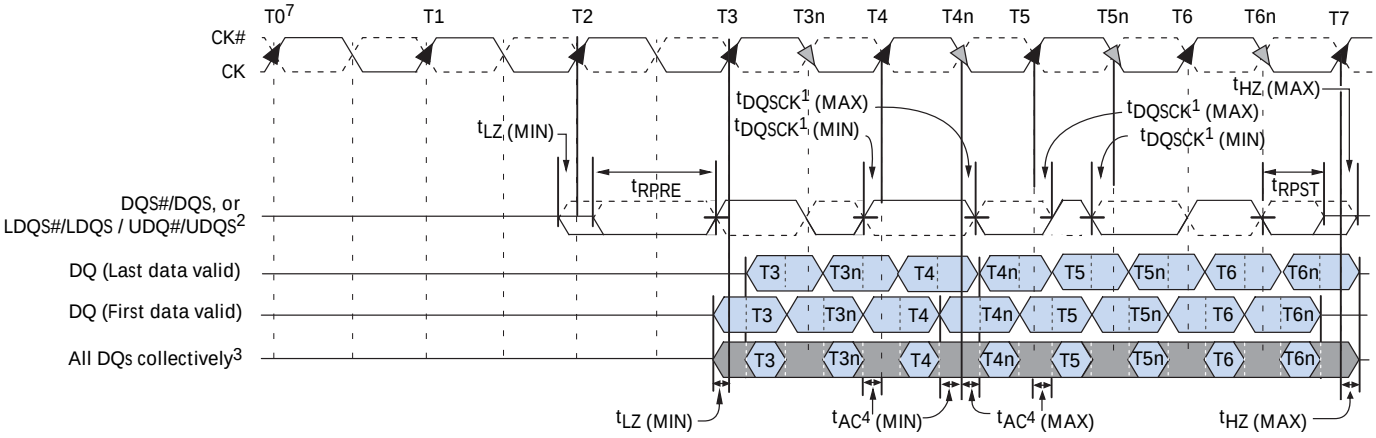
Figure 29: x16 Data Output Timing – ^{t}DQSQ, ^{t}QH, and Data Valid Window



NOTE:

1. DQs transitioning after DQS transitions define the ^{t}DQSQ window. LDQS defines the lower byte, and UDQS defines the upper byte.
2. DQ0, DQ1, DQ2, DQ3, DQ4, DQ5, DQ6, or DQ7.
3. ^{t}DQSQ is derived at each DQS clock edge and is not cumulative over time and begins with DQS transitions and ends with the last valid transition of DQs.
4. ^{t}QH is derived from ^{t}HP: ^{t}QH = ^{t}HP - ^{t}QHS.
5. ^{t}HP is the lesser of ^{t}CL or ^{t}CH clock transitions collectively when a bank is active.
6. The data valid window is derived for each DQS transition and is ^{t}QH minus ^{t}DQSQ.
7. DQ8, DQ9, DQ10, D11, DQ12, DQ13, DQ14, or DQ15.

Figure 30: Data Output Timing – tAC and tDQSCK



NOTE:

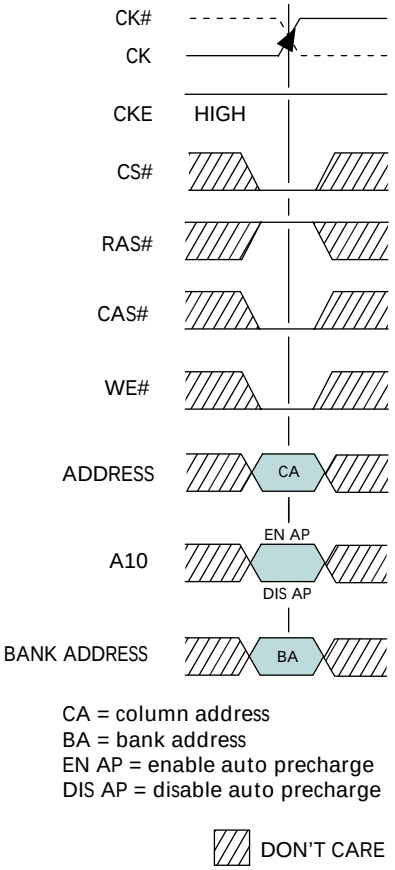
1. tDQSCK is the DQS output window relative to CK and is the"long-term" component of DQS skew.
2. DQs transitioning after DQS transitions define tDQSQ window.
3. All DQs must transition by tDQSQ after DQS transitions, regardless of tAC.
4. tAC is the DQ output window relative to CK and is the"long term" component of DQ skew.
5. tLZ (MIN) and tAC (MIN) are the first valid signal transitions.
6. tHZ (MAX) and tAC (MAX) are the latest valid signal transitions.
7. READ command with CL=3, AL=0 issued at T0.
8. I/0 pins, when entering or exiting HIGH-Z are not referenced to a specific voltage level, but when the device begins to drive or no longer drives, respecively.

WRITEs

WRITE Command

The WRITE command is used to initiate a burst write access to an active row. The value on the BA1-BA0 inputs selects the bank, and the address provided on inputs A0–*i* (where *i* = A9 for x8 and x16; or A9, A11 for x4) selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the write burst; if auto precharge is not selected, the row will remain open for subsequent accesses.

Figure 31: WRITE Command



Input data appearing on the DQs is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered LOW, the corresponding data will be written to memory; if the DM signal is registered HIGH, the corresponding data inputs will be ignored, and a write will not be executed to that byte/column location (Figure 41).

WRITE Operation

WRITE bursts are initiated with a WRITE command, as shown in Figure 31. DDR2 SDRAM uses Write Latency (WL) equal to Read Latency minus 1 clock cycle (WL = RL - 1 = AL + CL - 1). The starting column and bank addresses are provided with the WRITE command, and auto precharge is either enabled or disabled for that access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. For the generic WRITE commands used in the following illustrations, auto precharge is disabled.

During WRITE bursts, the first valid data-in element will be registered on the first rising edge of DQS following the WRITE command, and subsequent data elements will be registered on successive edges of DQS. The LOW state on DQS between the WRITE command and the first rising edge is known as the write preamble; the LOW state on DQS following the last data-in element is known as the write postamble.

The time between the WRITE command and the first corresponding rising edge of DQS (^{t}DQSS) is specified with a relatively wide range (from 75 percent to 125 percent of one clock cycle). All of the WRITE diagrams show the nominal case, and where the two extreme cases (i.e., ^{t}DQSS [MIN] and ^{t}DQSS [MAX]) might not be intuitive, they have also been included. Figure 32 shows the nominal case and the extremes of ^{t}DQSS for a burst of 4. Upon completion of a burst, assuming no other commands have been initiated, the DQs will remain High-Z and any additional input data will be ignored.

Data for any WRITE burst may be concatenated with a subsequent WRITE command to provide continuous flow of input data. The first data element from the new burst is applied after the last element of a completed burst. The new WRITE command should be issued *x* cycles after the first WRITE command, where *x* equals BL/2.

Figure 33 shows concatenated bursts of 4. An example of nonconsecutive WRITEs is shown in Figure 34. Full-speed random write accesses within a page or pages can be performed as shown in Figure 35. DDR2 SDRAM supports concurrent auto precharge options shown in Table 8.

DDR2 SDRAM does not allow interrupting or truncating any WRITE burst using BL = 4 operation. Once the BL = 4 WRITE command is registered, it must be allowed to complete the entire WRITE burst cycle. However, a WRITE (with AUTO PRECHARGE disabled) using BL = 8 operations may be interrupted and trun-

cated ONLY by another WRITE burst as long as the interruption occurs on a four-bit boundary due to the 4*n* prefetch architecture of DDR2 SDRAM. WRITE burst BL = 8 operations may NOT be interrupted or truncated with any command except another WRITE command as shown in Figure 36.

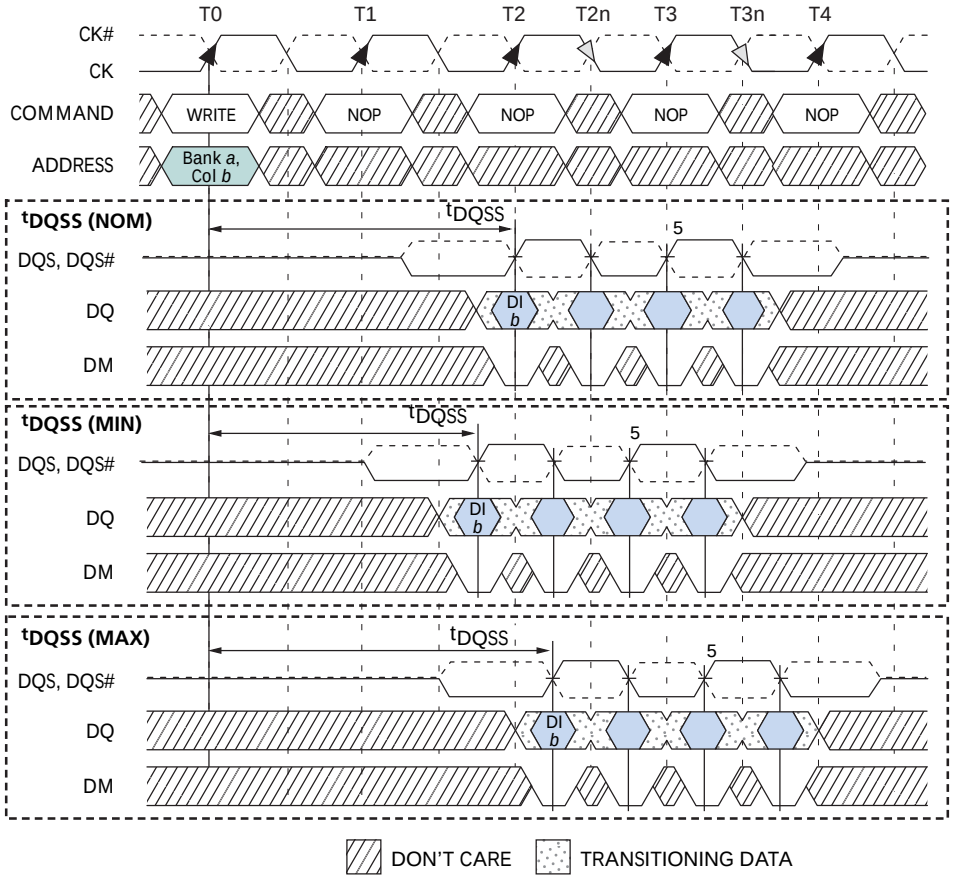
Data for any WRITE burst may be followed by a subsequent READ command. To follow a WRITE ^{t}WTR should be met as shown in Figure 37. ^{t}WTR is defined as Min(2 or ^{t}WTR/^{t}CK rounded up to the next integer). Data for any WRITE burst may be followed by a subsequent PRECHARGE command. ^{t}WR must be met as shown in Figure 31. ^{t}WR starts at the end of the data burst regardless of the data mask condition.

Table 8: WRITE Using Concurrent Auto Precharge

CL = CAS latency, BL = burst length

FROM COMMAND (BANK *n*)	TO COMMAND (BANK *m*)	MINIMUM DELAY (WITH CONCURRENT AUTO PRECHARGE)	UNITS
WRITE with Auto Precharge	READ or READ w/AP	(CL-1) + (BL/2) + ^{t}WTR	^{t}CK
	WRITE or WRITE w/AP	(BL/2)	^{t}CK
	PRECHARGE or ACTIVE	1	^{t}CK

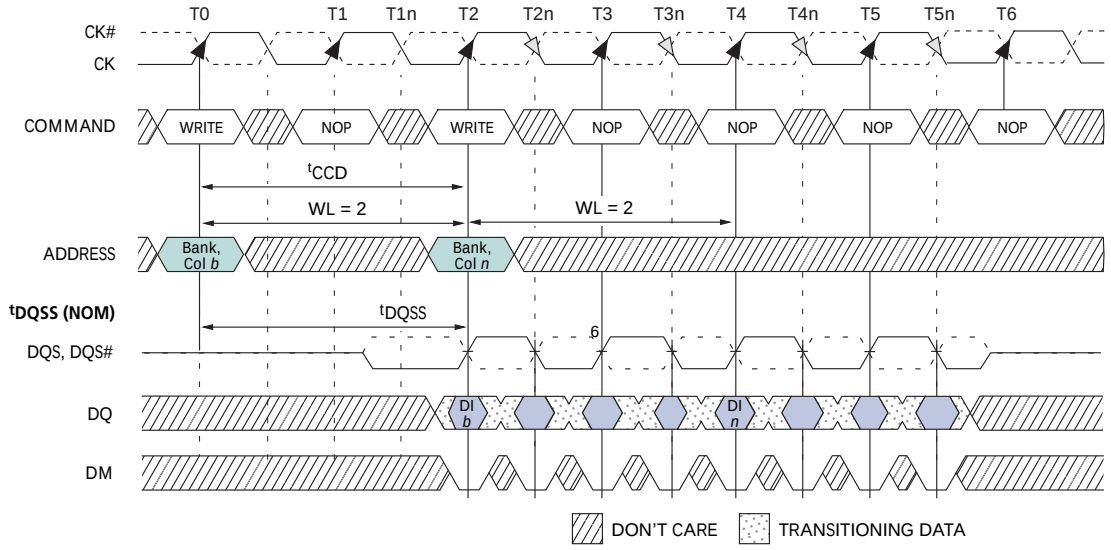
Figure 32: WRITE Burst



NOTE:

1. DI *b* = data-in for column *b*.
2. Three subsequent elements of data-in are applied in the programmed order following DI *b*.
3. A burst of 4 is shown with AL = 0, CL = 3; thus, WL = 2.
4. A10 is LOW with the WRITE command (auto precharge is disabled).
5. Subsequent rising DQS signals must align to the clock within ±0.25 ^{t}ck

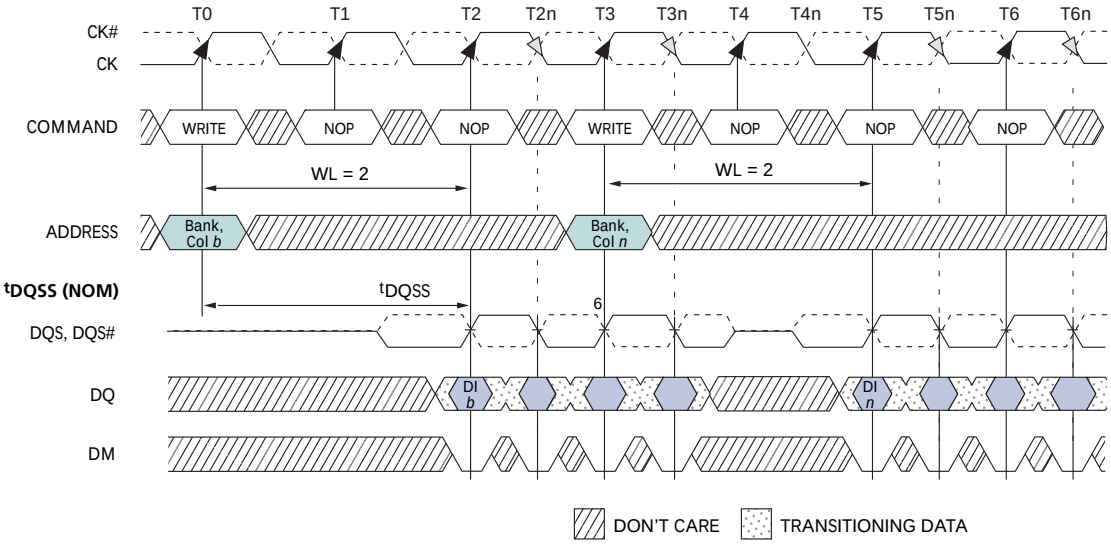
Figure 33: Consecutive WRITE to WRITE



NOTE:

1. DI *b*, etc. = data-in for column *b*, etc.
2. Three subsequent elements of data-in are applied in the programmed order following DI *b*.
3. Three subsequent elements of data-in are applied in the programmed order following DI *n*.
4. A burst of 4 is shown with AL = 0, CL = 3; thus, WL = 2.
5. Each WRITE command may be to any bank.
6. Subsequent rising DQS signals must align to the clock within ±0.25 ^{t}ck

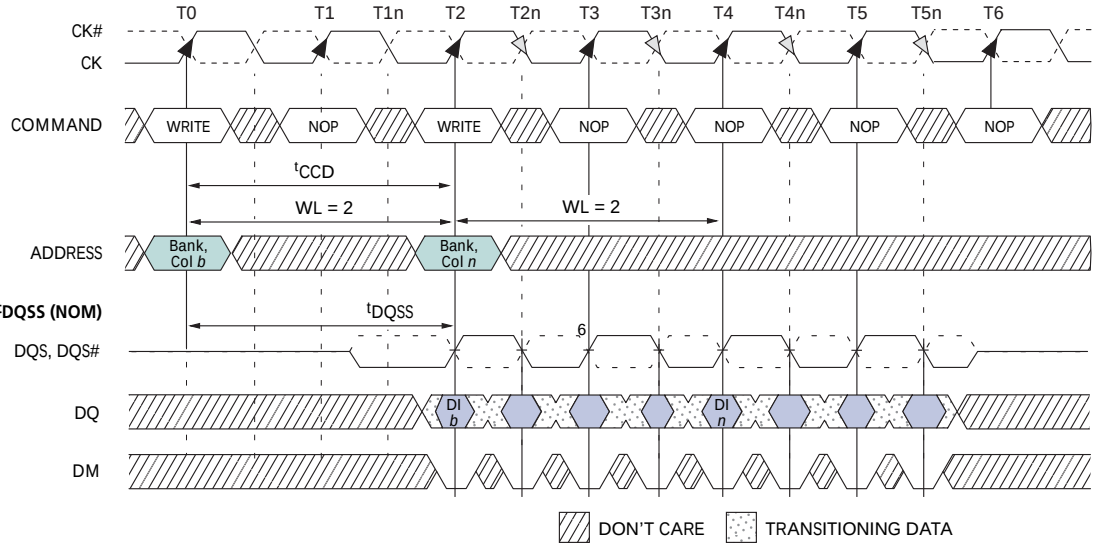
Figure 34: Nonconsecutive WRITE to WRITE



NOTE:

1. DI *b*, etc. = data-in for column *b*, etc.
2. Three subsequent elements of data-in are applied in the programmed order following DI *b*.
3. Three subsequent elements of data-in are applied in the programmed order following DI *n*.
4. A burst of 4 is shown. AL = 0, CL = 3; thus, WL = 2.
5. Each WRITE command may be to any bank.
6. Subsequent rising DQS signals must align to the clock within ±0.25 ^{t}ck

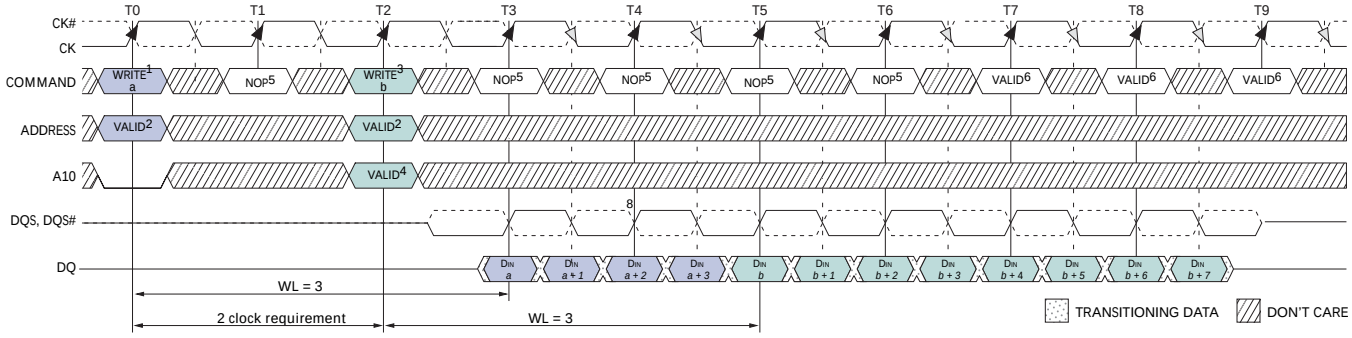
Figure 35: Random WRITE Cycles



NOTE:

1. DI *b*, etc. = data-in for column *b*, etc.
2. Three subsequent elements of data-in are applied in the programmed order following DI *b*.
3. Three subsequent elements of data-in are applied in the programmed order following DI *n*.
4. An burst of 4 is shown. AL = 0, CL = 3; thus, WL = 2.
5. Each WRITE command may be to any bank.
6. Subsequent rising DQS signals must align to the clock within ±0.25 ^{t}ck

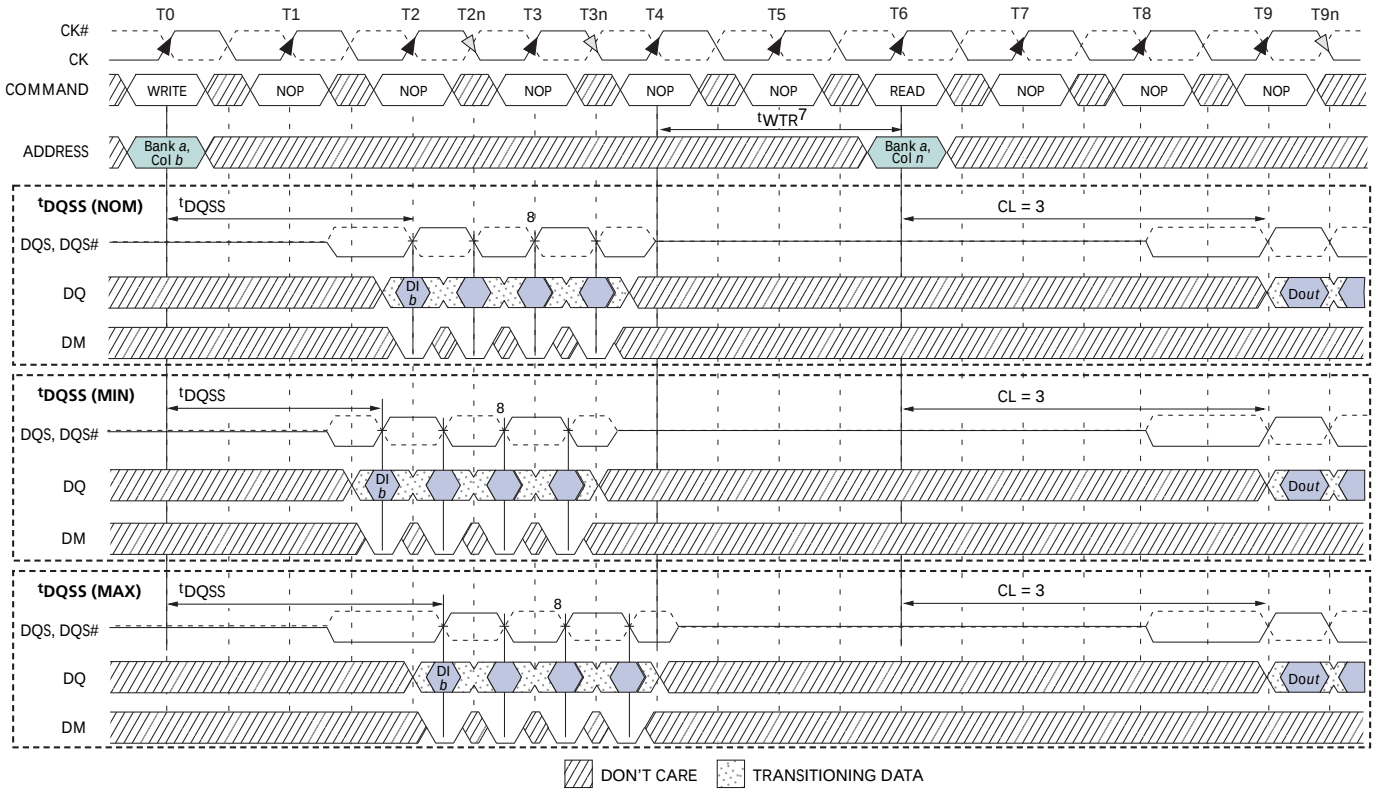
Figure 36: WRITE Interrupted by WRITE



NOTE:

1. Burst length = 8 required, AUTO PRECHARGE must be disabled (A10 = LOW).
2. WRITE command can be issued to any valid bank and row address (WRITE command at T0 and T2 can be either same bank or different bank).
3. Interupting WRITE command must be issued exactly 2 x ^{t}CK from previous WRITE.
4. AUTO PRECHARGE can be either enabled (A10 = HIGH) or disabled (A10 = LOW) by the interupting WRITE command.
5. NOP or COMMAND INHIBIT commands are valid. PRECHARGE command can not be issued to banks used for WRITEs at T0 and T2.
6. Earliest WRITE-to-PRECHARGE timing for WRITE at T0 is WL + BL/2 + ^{t}WR where ^{t}WR starts with T7 and not T5 (since BL = 8 from MR and not the truncated length).
7. Example shown uses Additive Latency = 0; CAS Latency = 4, BL = 8.
8. Subsequent rising DQS signals must align to the clock within ±0.25 ^{t}ck

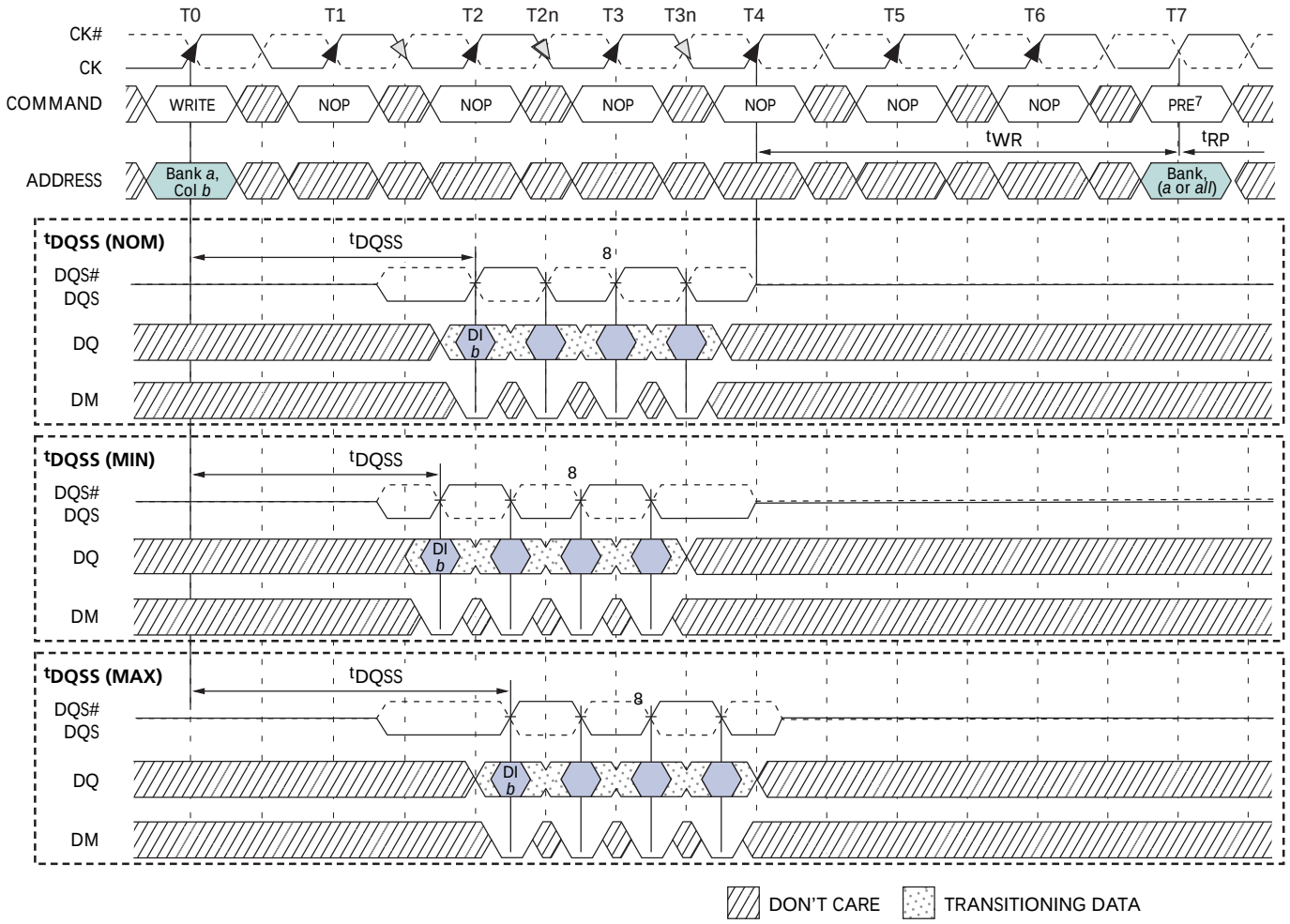
Figure 37: WRITE to READ



NOTE:

1. DI *b* = data-in for column *b*; Dout n = data out from column n.
2. A burst of 4 is shown; AL = 0, CL = 3; thus, WL = 2.
3. One subsequent element of data-in is applied in the programmed order following DI *b*.
4. ^{t}WTR is referenced from the first positive CK edge after the last data-in pair.
5. A10 is LOW with the WRITE command (auto precharge is disabled).
6. ^{t}WTR is defined as Min(2 or ^{t}WTR/^{t}CK rounded up to the next integer).
7. Required for any READ following a WRITE to the same device.
8. Subsequent rising DQS signals must align to the clock within ±0.25 ^{t}ck

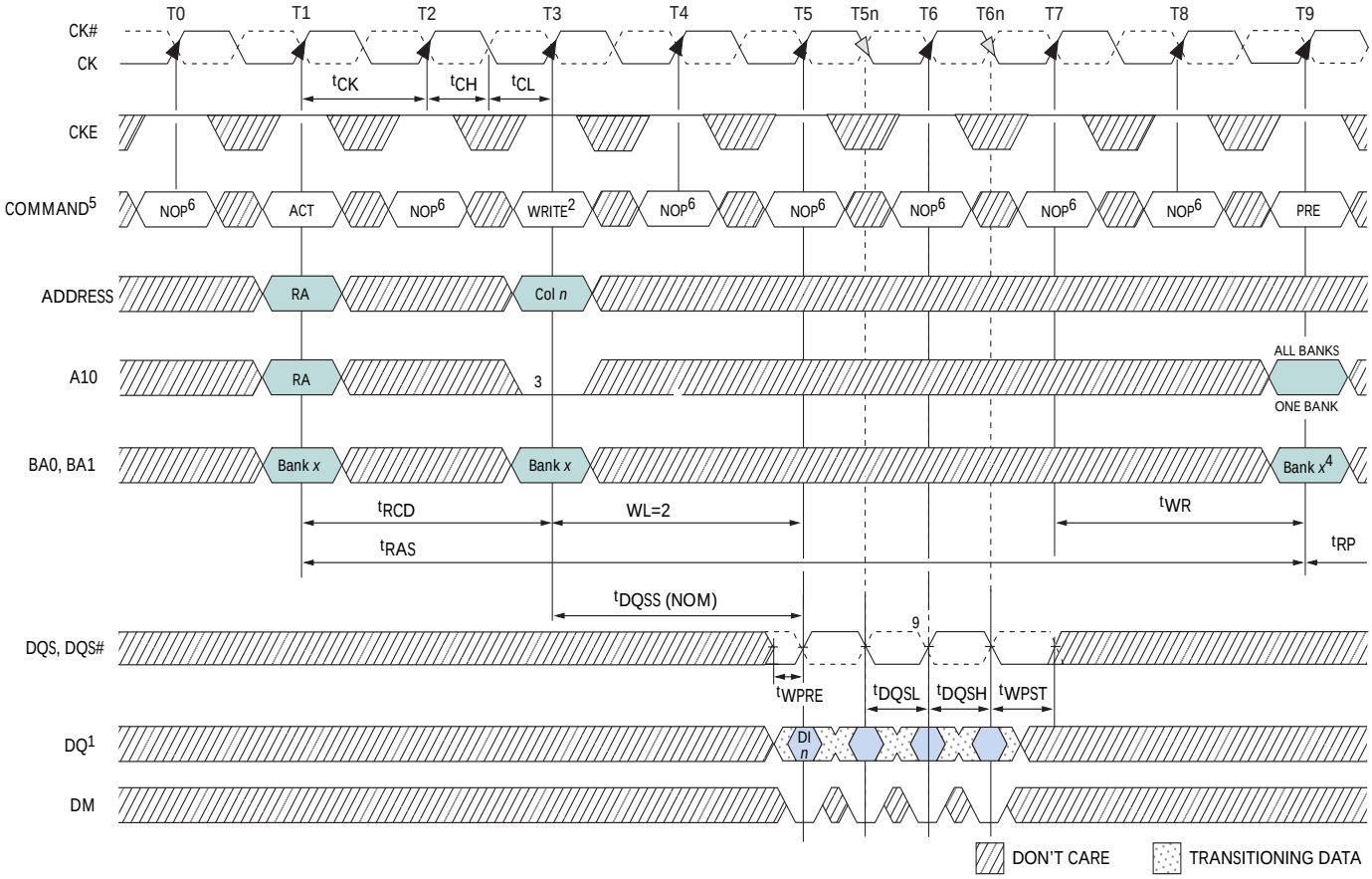
Figure 38: WRITE to PRECHARGE



NOTE:

1. DI *b* = data-in for column *b*.
2. Three subsequent elements of data-in are applied in the programmed order following DI *b*.
3. BL=4; CL = 3; AL = 0; thus, WL = 2.
4. ^{t}WR is referenced from the first positive CK edge after the last data-in pair.
5. The PRECHARGE and WRITE commands are to the same bank. However, the PRECHARGE and WRITE commands may be to different banks, in which case ^{t}WR is not required and the PRECHARGE command could be applied earlier.
6. A10 is LOW with the WRITE command (auto precharge is disabled).
7. PRE = PRECHARGE command.
8. Subsequent rising DQS signals must align to the clock within ±0.25 ^{t}ck

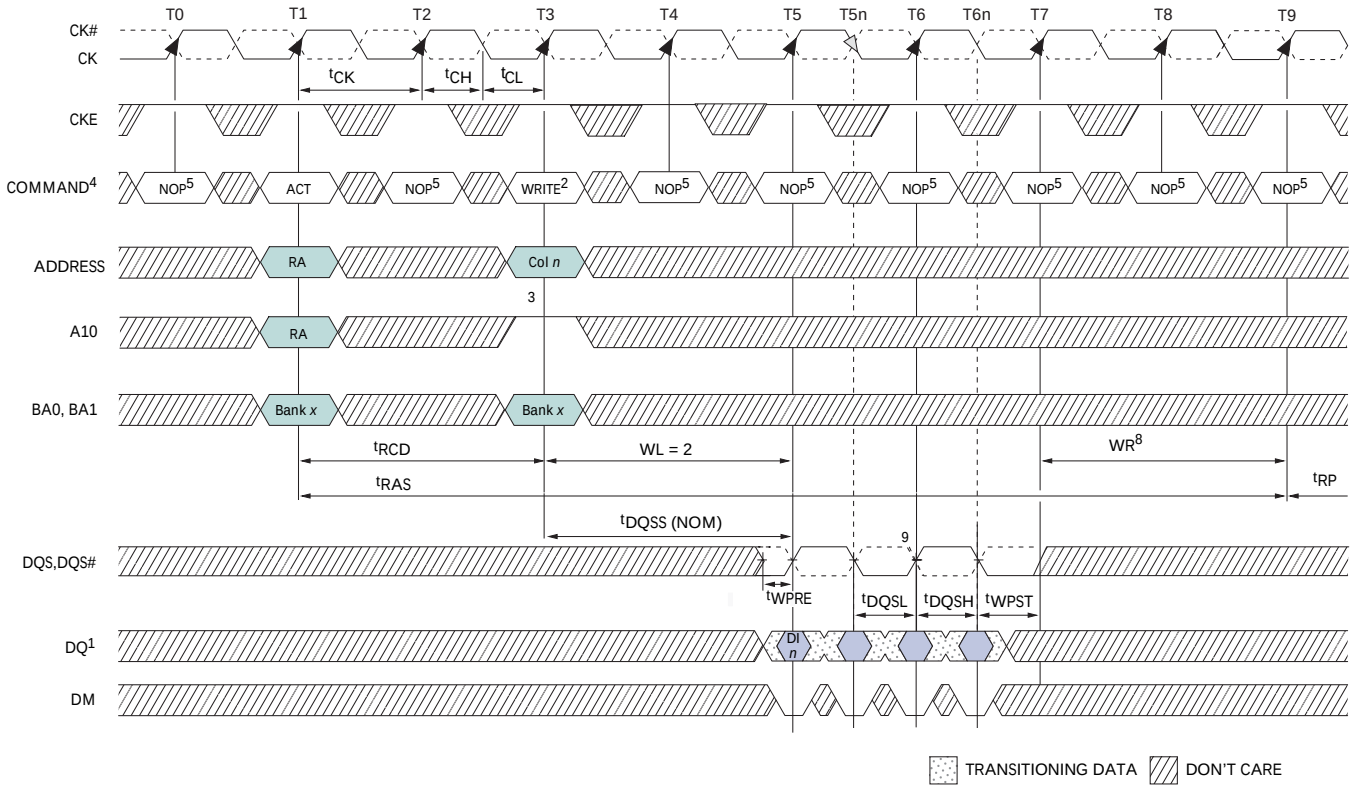
Figure 39: Bank Write–Without Auto Precharge



NOTE:

1. DI *n* = data-in from column n; subsequent elements are applied in the programmed order.
2. BL = 4, AL = 0, and WL = 2 in the case shown.
3. Disable auto precharge.
4. "Don't Care" if A10 is HIGH at T9.
5. PRE = PRECHARGE, ACT = ACTIVE, RA = row address, BA = bank address.
6. NOP commands are shown for ease of illustration; other commands may be valid at these times.
7. ^{t}DSH is applicable during ^{t}DQSS (MIN) and is referenced from CK T5 or T6.
8. ^{t}DSS is applicable during ^{t}DQSS (MAX) and is referenced from CK T6 or T7.
9. Subsequent rising DQS signals must align to the clock within ±0.25 ^{t}ck

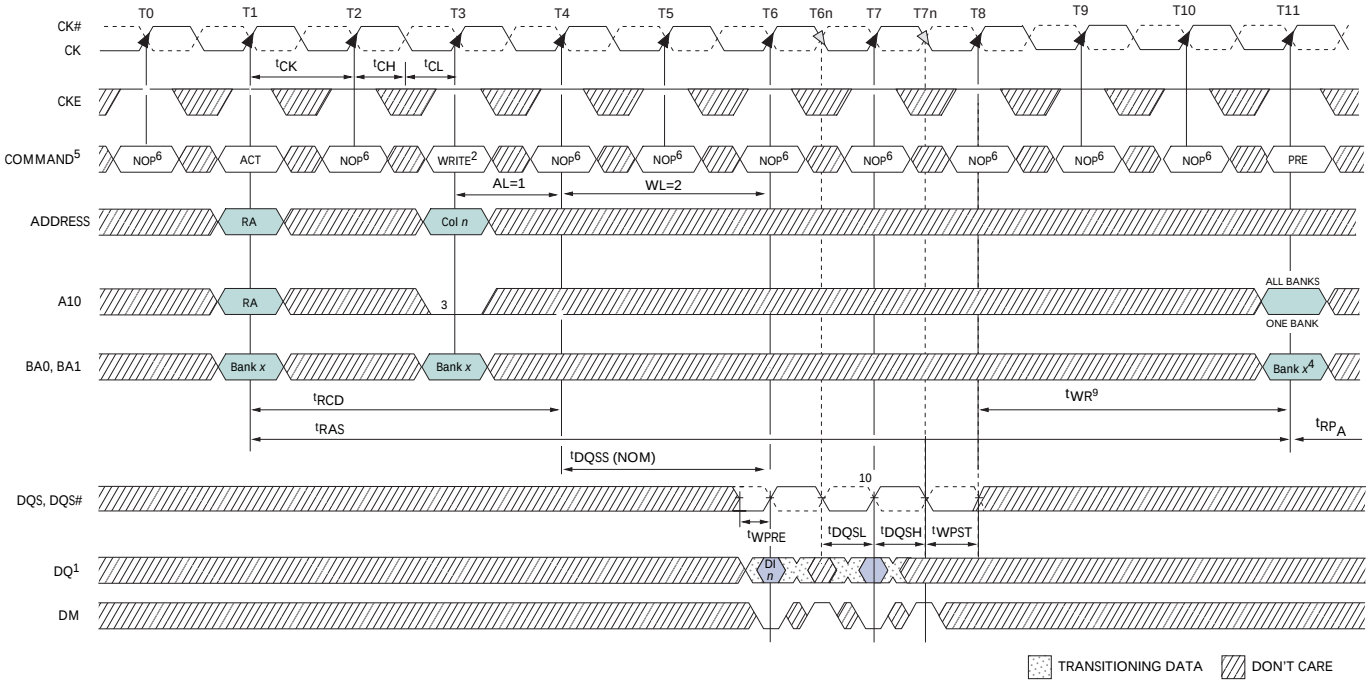
Figure 40: Bank Write–with Auto Precharge



NOTE:

1. DI *n* = data-in from column n; subsequent elements are applied in the programmed order.
2. Burst length = 4, AL = 0, and WL = 2 shown.
3. Enable auto precharge.
4. ACT = ACTIVE, RA = row address, BA = bank address.
5. NOP commands are shown for ease of illustration; other commands may be valid at these times.
6. ^{t}DSH is applicable during ^{t}DQSS (MIN) and is referenced from CK T5 or T6.
7. ^{t}DSS is applicable during ^{t}DQSS (MAX) and is referenced from CK T6 or T7.
8. WR is programmed via MR[11,10,9] and is calculated by dividing ^{t}WR(ns) by ^{t}CK and rounding up to the next integer value.
9. Subsequent rising DQS signals must align to the clock within ±0.25 ^{t}ck

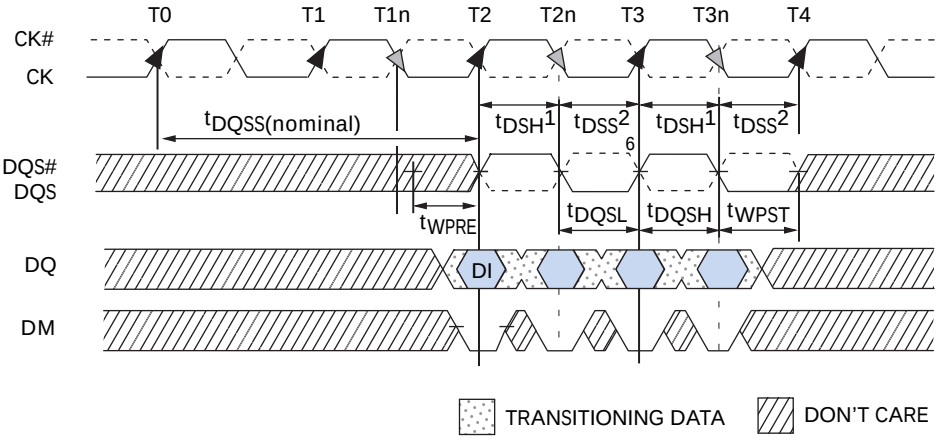
Figure 41: WRITE–DM Operation



NOTE:

1. DI *n* = data-in from column *n*; subsequent elements are applied in the programmed order.
2. Burst length = 4, AL = 1, and WL = 2 in the case shown.
3. Disable auto precharge.
4. "Don't Care" if A10 is HIGH at T11.
5. PRE = PRECHARGE, ACT = ACTIVE, RA = row address, BA = bank address.
6. NOP commands are shown for ease of illustration; other commands may be valid at these times.
7. ^{t}DSH is applicable during ^{t}DQSS (MIN) and is referenced from CK T6 or T7.
8. ^{t}DSS is applicable during ^{t}DQSS (MAX) and is referenced from CK T7 or T8.
9. ^{t}WR starts at the end of the data burst regardless of the data mask condition.
10. Subsequent rising DQS signals must align to the clock within ±0.25 ^{t}ck

Figure 42: Data Input Timing



NOTE:

1. ^{t}DSH (MIN) generally occurs during ^{t}DQSS (MIN).
2. ^{t}DSS (MIN) generally occurs during ^{t}DQSS (MAX).
3. WRITE command issued at T0.
4. For x16, LDQS controls the lower byte and UDQS controls the upper byte.
5. WRITE command with WL=2 (CL=3, AL=0) issued at T0.
6. Subsequent rising DQS signals must align to the clock within ±0.25 ^{t}ck

Precharge

PRECHARGE Command

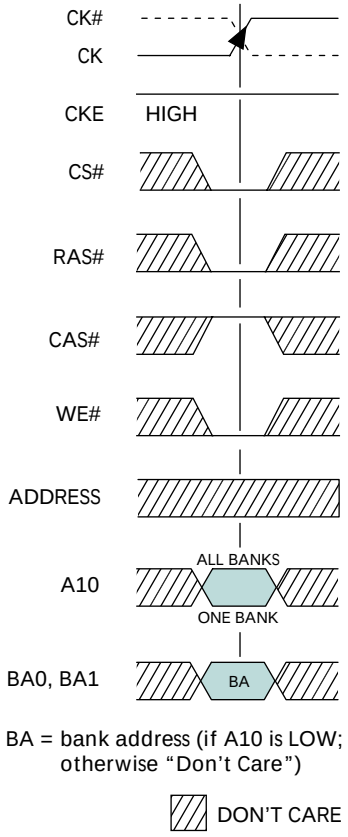
The PRECHARGE command, illustrated in Figure 43, is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row activation a specified time (^{t}RP) after the precharge command is issued, except in the case of concurrent auto precharge, where a READ or WRITE command to a different bank is allowed as long as it does not interrupt the data transfer in the current bank and does not violate any other timing parameters. Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command will be treated as a NOP if there is no open row in that bank (idle state) or if the previously open row is already in the process of precharging.

PRECHARGE Operation

Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA1-BA0 select the bank. Otherwise BA1-BA0 are treated as "Don't Care."

When all banks are to be precharged, inputs BA1-BA0 are treated as "Don't Care." Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. ^{t}RPA timing applies when the PRECHARGE(ALL) command is issued, regardless of the number of banks already open or closed. If a single-bank PRECHARGE command is issued, ^{t}RP timing applies.

Figure 43: PRECHARGE Command



Self Refresh

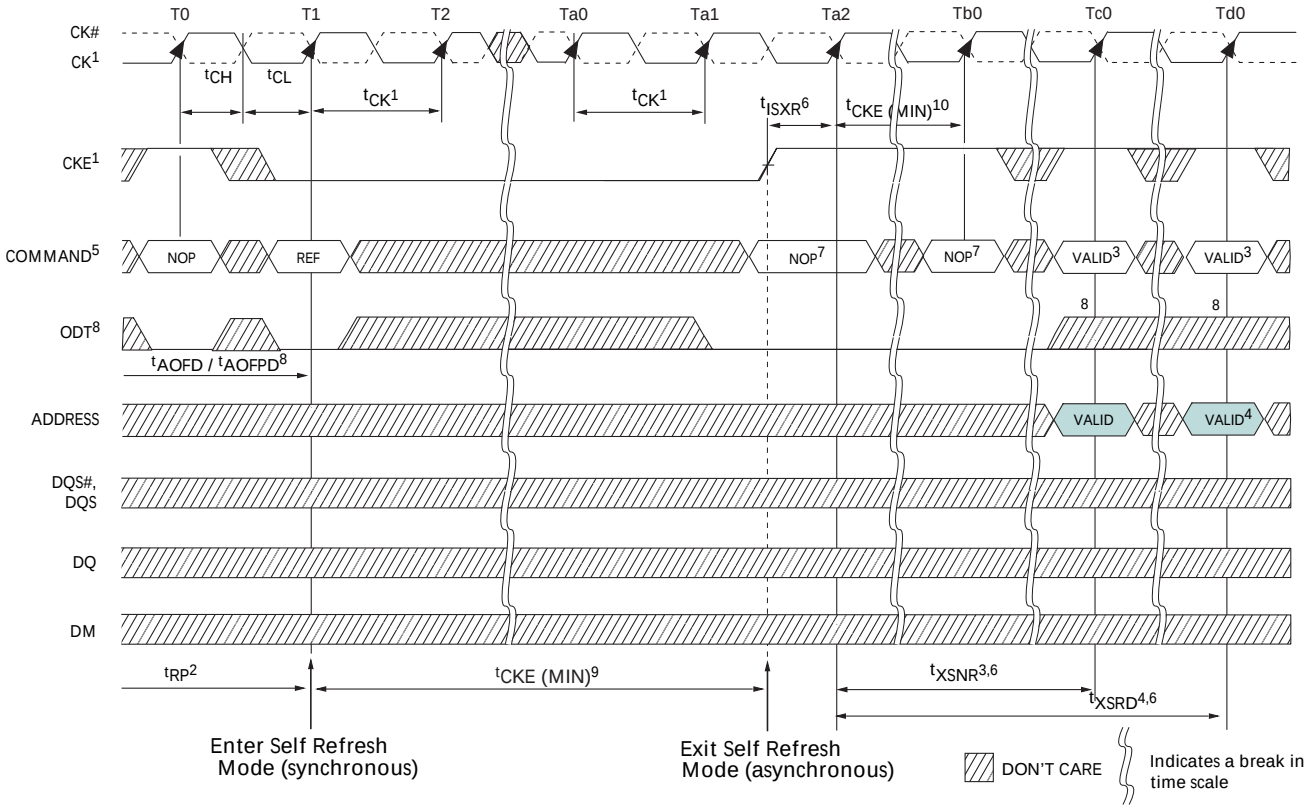
SELF REFRESH Command

The SELF REFRESH command can be used to retain data in the DDR2 SDRAM, even if the rest of the system is powered down. When in the self refresh mode, the DDR2 SDRAM retains data without external clocking. All power supply inputs (including V_{REF}) must be maintained at valid levels upon entry/exit AND during self refresh operation.

The SELF REFRESH command is initiated like a REFRESH command except CKE is (LOW). The DLL is automatically disabled upon entering self refresh and is automatically enabled upon exiting self refresh (200 clock cycles must then occur before a READ command can be issued). Clock should remain stable and meeting ^{t}CKE specifications at least 1 x ^{t}CK after entering self refresh mode. All command and address input signals except CKE are "Don't Care" during self refresh.

The procedure for exiting self refresh requires a sequence of commands. First, CK, CK# must be stable and meeting ^{t}CK specifications at least 1 x ^{t}CK prior to CKE going back HIGH. Once CKE is HIGH (^{t}CKE(min) has been satified with four clock registrations), the DDR2 SDRAM must have NOP or DESELECT commands issued for ^{t}XSNR because time is required for the completion of any internal refresh in progress. A simple algorithm for meeting both refresh and DLL requirements is to apply NOP or DESELECT commands for 200 clock cycles before applying any other command.

Figure 44: Self Refresh



NOTE:

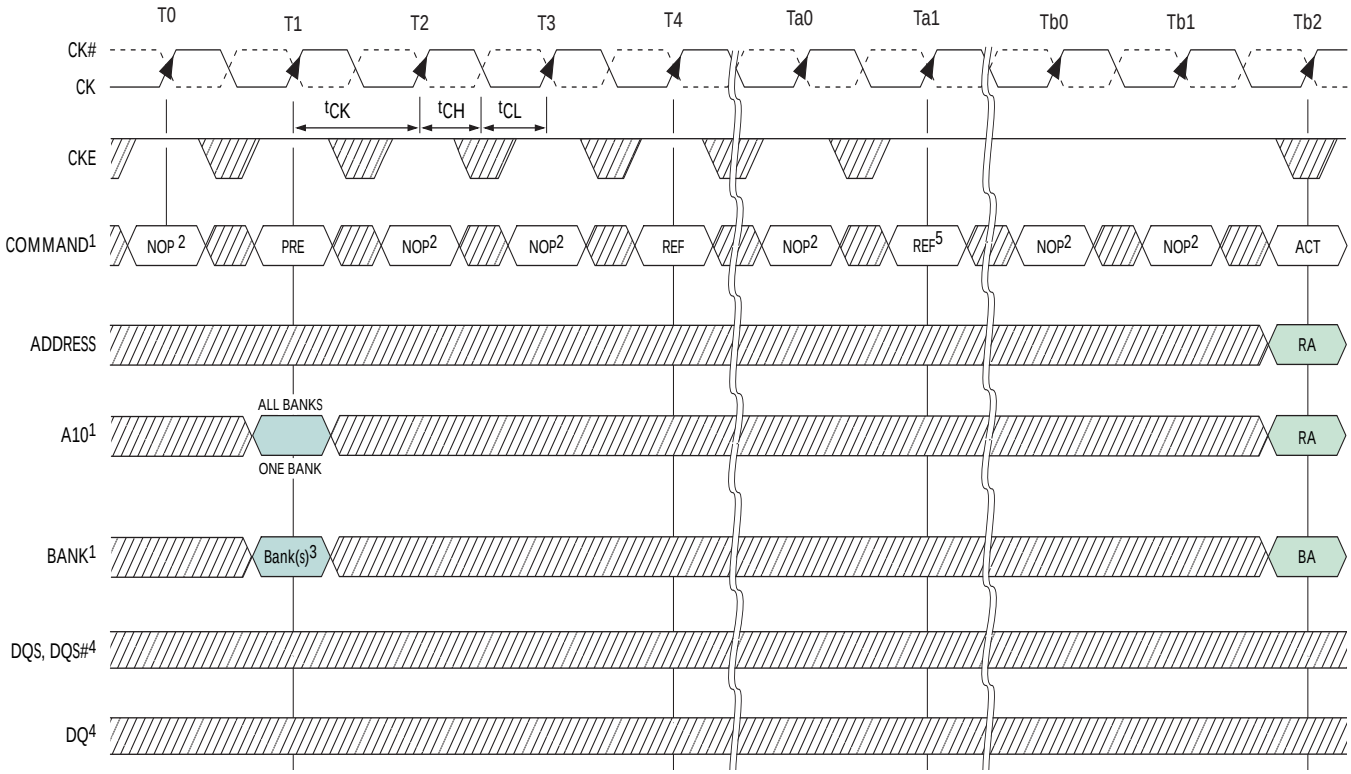
1. Clock must be stable and meeting ^{t}CK specifications at least 1 x ^{t}CK after entering self refresh and at least 1 x ^{t}CK prior to exiting self refresh mode.
2. Device must be in the all banks idle state prior to entering self refresh mode.
3. ^{t}XSNR is required before any non-READ command can be applied.
4. ^{t}XSRD (200 cycles of CK) is required before a READ command can be applied at state Td0.
5. REF = REFRESH command.
6. Self Refresh exit is asynchronous, however, ^{t}XSNR and ^{t}XSRD timing starts at the first rising clock edge where CKE HIGH satisfies ^{t}ISXR.
7. NOP or DESELECT commands are required prior to exiting SELF REFRESH until state Tc0, which allows any non-READ command.
8. ODT must be disabled and RTT off (^{t}AOFD and ^{t}AOFPD have been satisfied) prior to entering Self Refresh at state T1.
9. Once Self Refresh has been entered ^{t}CKE(min) must be satisfied prior to exiting self refresh.
10. CKE must stay high; ^{t}CKE(min) High = 3 clock registrations.

REFRESH

REFRESH Command

REFRESH is used during normal operation of the DDR2 SDRAM and is analogous to CAS#-BEFORE-RAS# (CBR) refresh. This command is nonpersistent, so it must be issued each time a refresh is required. The addressing is generated by the internal refresh controller. This makes the address bits a "Don't Care" during an REFRESH command. The 512Mb DDR2 SDRAM requires REFRESH cycles at an average interval of 7.8125µs (maximum). To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight REFRESH commands can be posted to any given DDR2 SDRAM, meaning that the maximum absolute interval between any REFRESH command and the next REFRESH command is 9 × 7.8125µs (70.3µs). The REFRESH period begins when the REFRESH command is registered and ends ^{t}RFC (min) later.

Figure 45: Refresh Mode



NOTE:

1. PRE = PRECHARGE, ACT = ACTIVE, AR = REFRESH, RA = row address, BA = bank address.
2. NOP commands are shown for ease of illustration; other valid commands may be possible at these times. CKE must be active during clock positive transitions.
3. "Don't Care" if A10 is HIGH at this point; A10 must be HIGH if more than one bank is active (i.e., must precharge all active banks).
4. DM, DQ, and DQS signals are all "Don't Care"/High-Z for operations shown.
5. The second REFRESH is not required and is only shown as an example of two back-to-back REFRESH commands.

Power-Down Mode

DDR2 SDRAMs support multiple power-down modes that allow a significant power savings over normal operating modes. The CKE input pin is used to enter and exit different power-down modes. Power-down entry and exit timings are shown in Figure 46. Detailed power-down entry conditions are shown in Figure 47 through Figure 54. The Truth Table for CKE is shown in Table 9 on page 60 for DDR2 SDRAM.

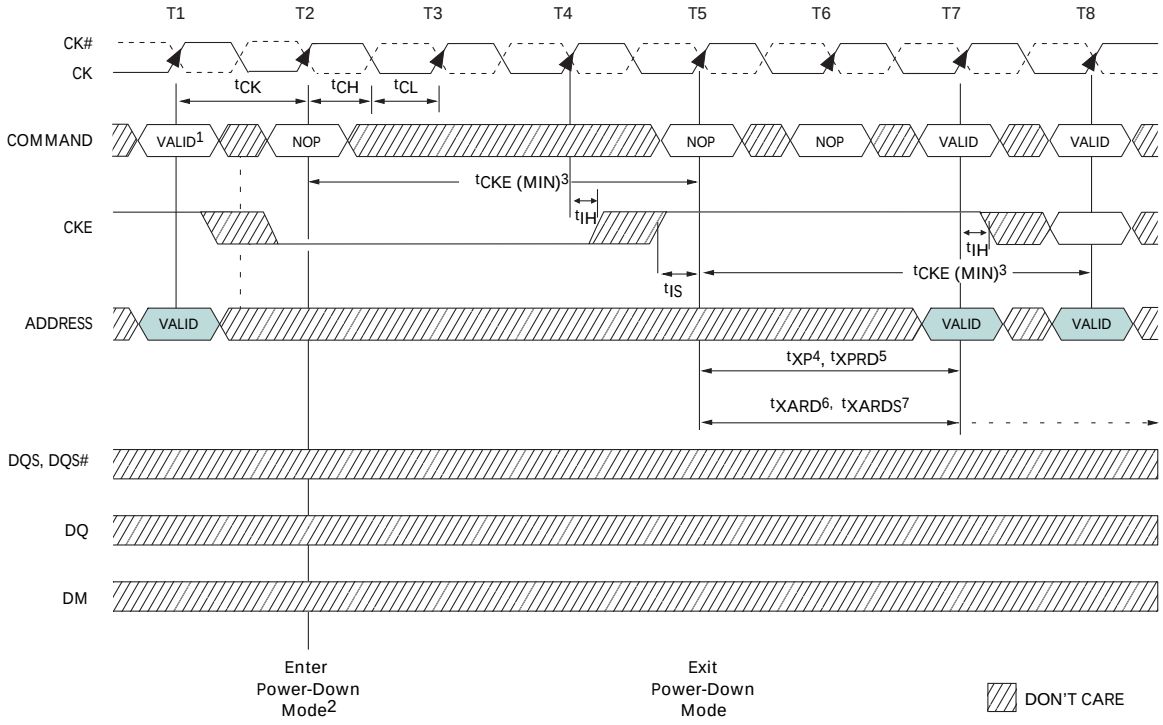
DDR2 SDRAMs require CKE to be registered high (active) at all times that an access is in progress: from the issuing of a READ or WRITE command until completion of the burst. Thus a clock suspend is not supported. For READs, a burst completion is defined when the read postamble is satisfied; for WRITEs, a burst completion is defined when the write postamble and ^{t}WR or ^{t}WTR are satisfied, and shown in Figure 49 and Figure 50. ^{t}WTR is defined as Min(2 or ^{t}WTR/^{t}CK rounded up to the next integer).

Power-down in Figure 46, is entered when CKE is registered LOW coincident with a NOP or DESELECT command. If power-down occurs when all banks are idle, this mode is referred to as precharge power-down. If power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, excluding CK, CK#, ODT, and CKE. For maximum power savings, the DLL is frozen during precharge power-down. Exiting active power-down requires the device to be at the same voltage and frequency as when it entered power-down. Exiting precharge power-down requires the device to be at the same voltage as when it entered power-down; however, the clock frequency is allowed to change (See "Precharge Power-Down Clock Frequency Change" on page 7.)

The maximum duration for either active or precharge power-down is limited by the refresh requirements of the device ^{t}RFC (MAX). The minimum duration for power-down entry and exit is limited by ^{t}CKE(min) parameter. While in power-down mode, CKE LOW, a stable clock signal, and stable power supply signals must be maintained at the inputs of the DDR2 SDRAM, while all other input signals are “Don’t Care” except ODT. Detailed ODT timing diagrams for different power-down modes are shown for Figure 3 on page 10 through Figure 8 on page 15.

The power-down state is synchronously exited when CKE is registered HIGH (in conjunction with a NOP or DESELECT command) as shown in Figure 46.

Figure 46: Power-Down



NOTE:

1. If this command is a PRECHARGE (or if the device is already in the idle state), then the power-down mode shown is pre-charge power-down. If this command is an ACTIVE (or if at least one row is already active), then the power-down mode shown is active power-down.
2. No column accesses are allowed to be in progress at the time power-down is entered.
3. ^{t}CKE (MIN) of 3 clocks means CKE must be registered on three consecutive positve clock edges. CKE must remain at the valid input level the entire time it takes to achieve the 3 clocks of registration. Thus, after any CKE transition, CKE may not trainsition from its valid level during the time period of ^{t}IS + 2 * ^{t}CK + ^{t}IH. CKE must not transition during its ^{t}IS and ^{t}IH window.
4. ^{t}XP timing is used for exit precharge power-down and active power-down to any non-READ command.
5. ^{t}XPRD timing is used for exit precharge power-down to any READ command
6. ^{t}XARD timing is used for exit active power-down to READ command if 'fast exit' is selected via MR (bit 12 = 0).
7. ^{t}XARDS timing is used for exit active power-down to READ command if 'slow exit' is selected via MR (bit 12 = 1).

Table 9: CKE Truth Table

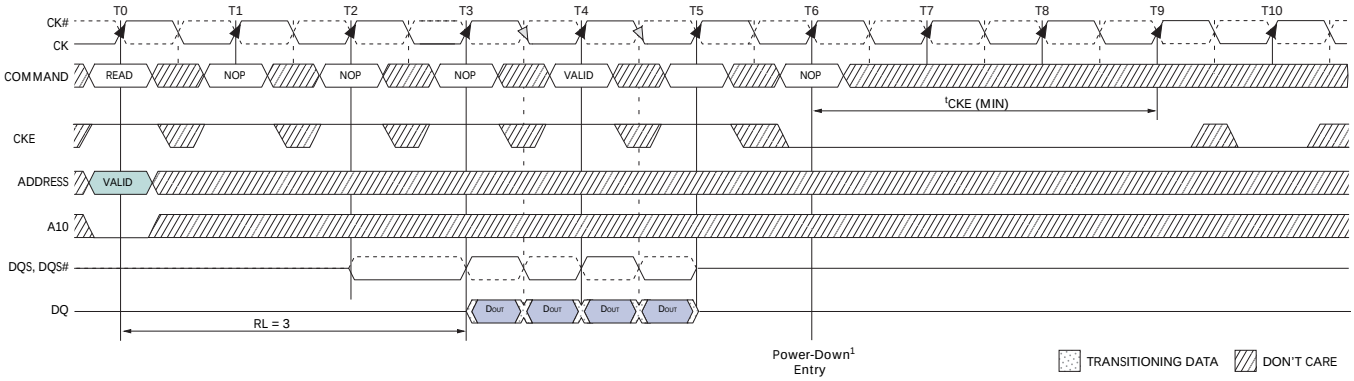
Notes 1–3, 12

CURRENT STATE	CKE		COMMAND (*n*) CS#,RAS#,CAS#,WE#	ACTION (*n*)	NOTES
	PREVIOUS CYCLE (*n*-1)	CURRENT CYCLE (*n*)			
Power Down	L	L	X	Maintain Power-Down	13, 14
	L	H	DESELECT or NOP	Power-Down Exit	4, 8
Self Refresh	L	L	X	Maintain Self Refresh	14
	L	H	DESELECT or NOP	Self Refresh Exit	4, 5, 9
Bank(s) Active	H	L	DESELECT or NOP	Active Power-Down Entry	4, 8, 10, 11
All Banks Idle	H	L	DESELECT or NOP	Precharge Power-Down Entry	4, 8, 10
	H	L	REFRESH	Self Refresh Entry	6, 9, 11
	H	H	Refer to Command Truth Table 1 on page 7		7

NOTE:

1. CKE (*n*) is the logic state of CKE at clock edge *n*; CKE (*n*-1) was the state of CKE at the previous clock edge.
2. Current state is the state of the DDR2 SDRAM immediately prior to clock edge *n*.
3. COMMAND (*n*) is the command registered at clock edge *n*, and ACTION (*n*) is a result of COMMAND (N).
4. All states and sequences not shown are illegal or reserved unless explicitely described elsewhere in this document.
5. On self refresh exit, DESELECT or NOP commands must be issued on every clock edge occurring during the ^{t}XSNR period. Read commands may be issued only after ^{t}XSRD (200 clocks) is satisfied.
6. Self refresh mode can only be entered from the all banks idle state.
7. Must be a legal command as defined in the Command Truth Table.
8. Valid commands for power-down entry and exit are NOP and DESELECT only.
9. Valid commands for Self Refresh Exit are NOP and DESELECT only.
10. Power-down and self refresh can not be entered while READ or WRITE operations, LOAD MODE operations, or PRECHARGE or REFRESH operations are in progress. See Power-Down and Self Refresh sections for a list of detailed restrictions.
11. Minimum CKE HIGH time is ^{t}CKE = 3 x ^{t}CK. Minimum CKE low time is ^{t}CKE = 3 x ^{t}CK. This requires a minimum of 3 clock cycles of registration.
12. The state of on-die termination (ODT) does not affect the states described in this table. The ODT function is not available during self refresh. See ODT section for more details and specific restrictions.
13. Power-down modes do not perform any refresh operations. The duration of power-down mode is therefore limited by the refresh requirements.
14. "X" means "Don't Care" (including floating around V_{REF}) in self refresh and power-down. However, ODT must be driven HIGH or LOW in power-down if the ODT function is enabled via EMR(1).

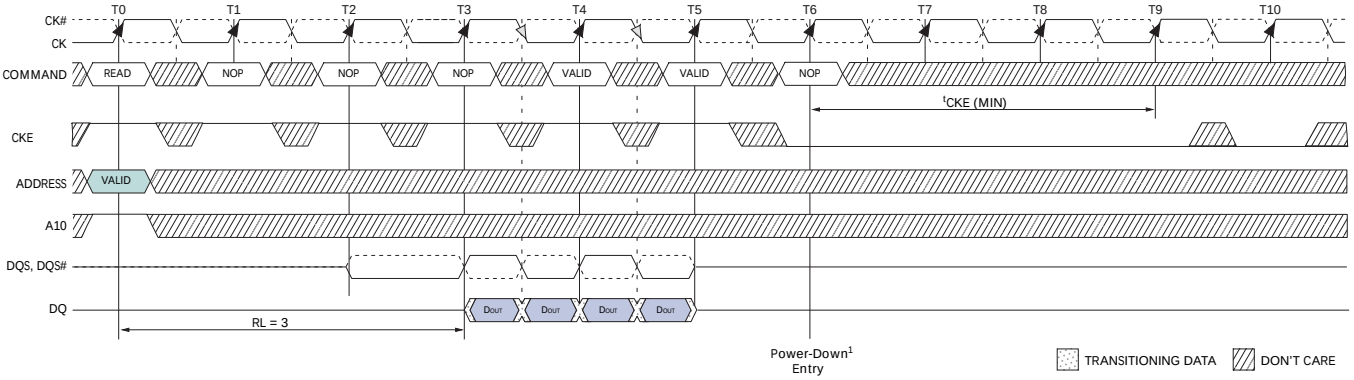
Figure 47: READ to Power-Down Entry



NOTE:

1. Power-down entry may occur after the READ burst completes.
2. In the example shown, READ burst completes at T5; earliest power-down entry is at T6.

Figure 48: READ with Auto Precharge to Power-Down Entry



NOTE:

1. Power-down entry may occur 1 x ^{t}CK after the internal precharge is issued and may be prior to ^{t}RP being satisfied.
2. Timing shown above assumes internal PRECHARGE was issued at T5 or earlier.
3. Refer to READ-to-PRECHARGE section for internal precharge timing details.

Figure 49: WRITE to Power-Down Entry

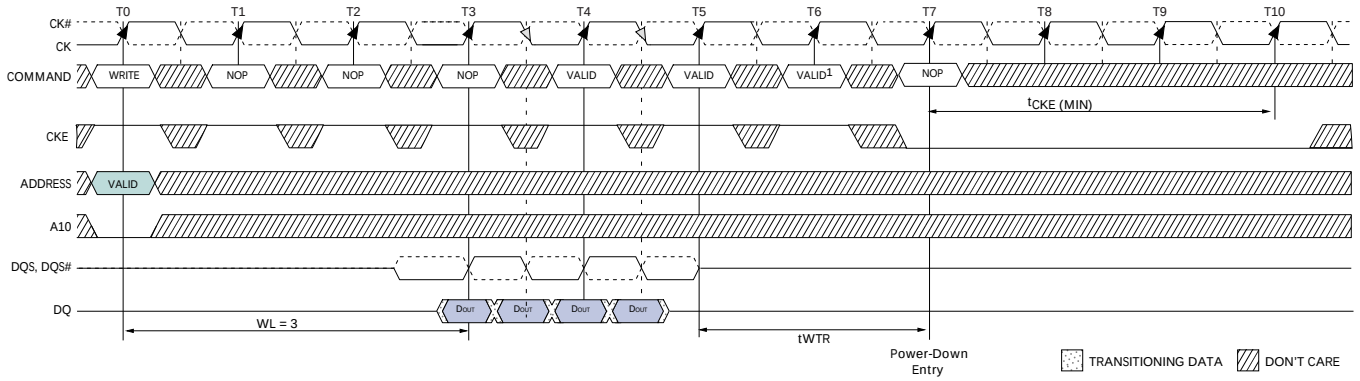
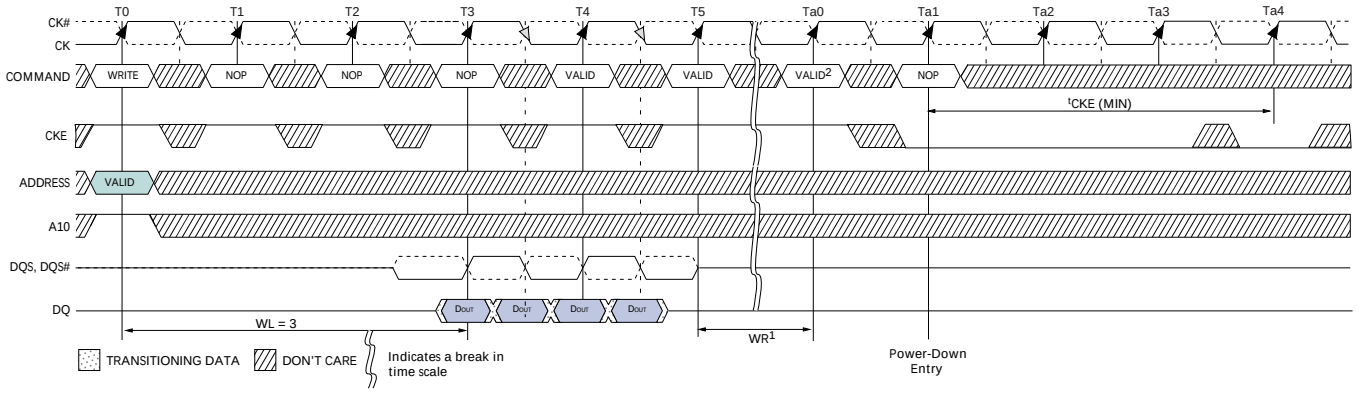


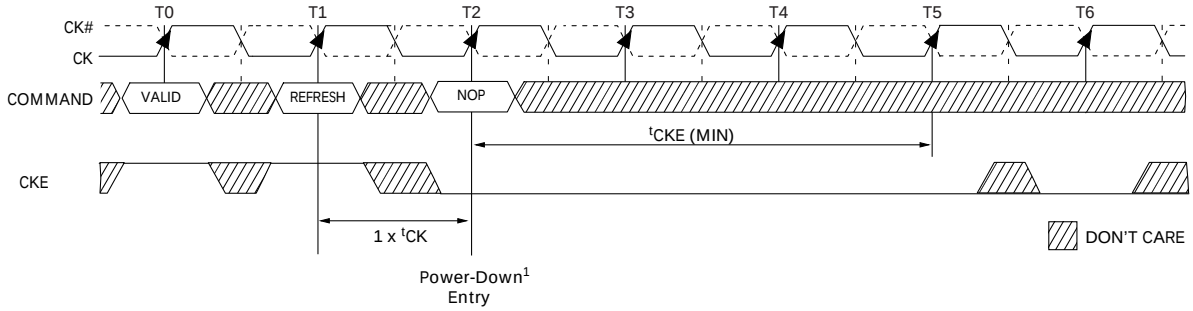
Figure 50: WRITE with Auto Precharge to Power-Down Entry



NOTE:

1. Write Recovery (WR) is programmed through MR[9,10,11] and represents [^{t}WR (MIN) ns / ^{t}CK] rounded up to next integer ^{t}CK.
2. Internal PRECHARGE occurs at Ta0 when WR has completed; power-down entry may occur 1 x ^{t}CK later at Ta1 prior to ^{t}RP being satisfied.

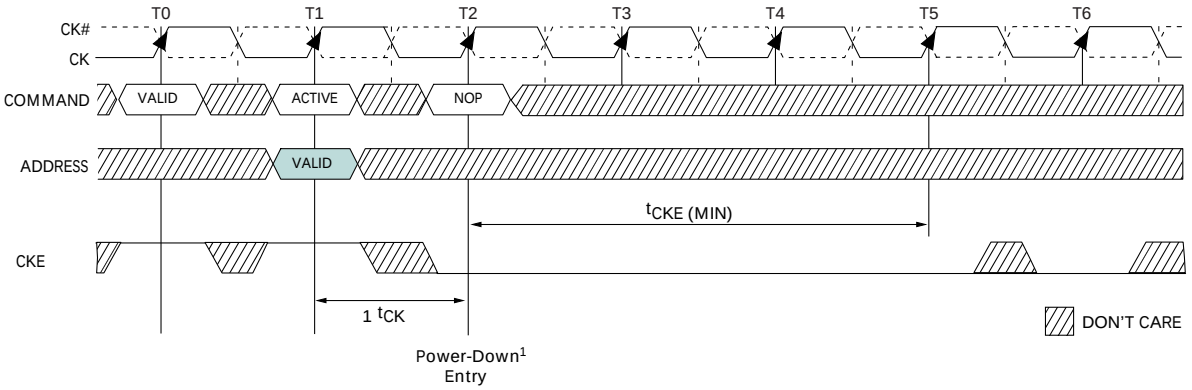
Figure 51: REFRESH command to Power-Down Entry



NOTE:

1. The earliest PRECHARGE power-down entry may occur is at T2 which is 1 x ^{t}CK after the REFRESH command. Precharge power down entry occurs prior to ^{t}RFC (MIN) being satisfied.

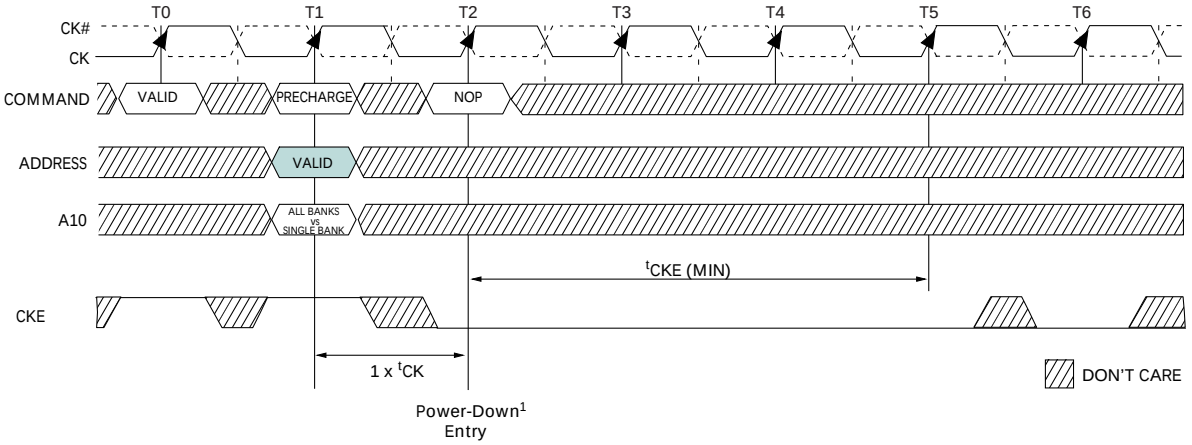
Figure 52: ACTIVE Command to Power-Down Entry



NOTE:

1. The earliest PRECHARGE power-down entry may occur is at T2, which is 1 x ^{t}CK after the ACTIVE command. Active power-down entry occurs prior to ^{t}RCD (MIN) being satisfied.

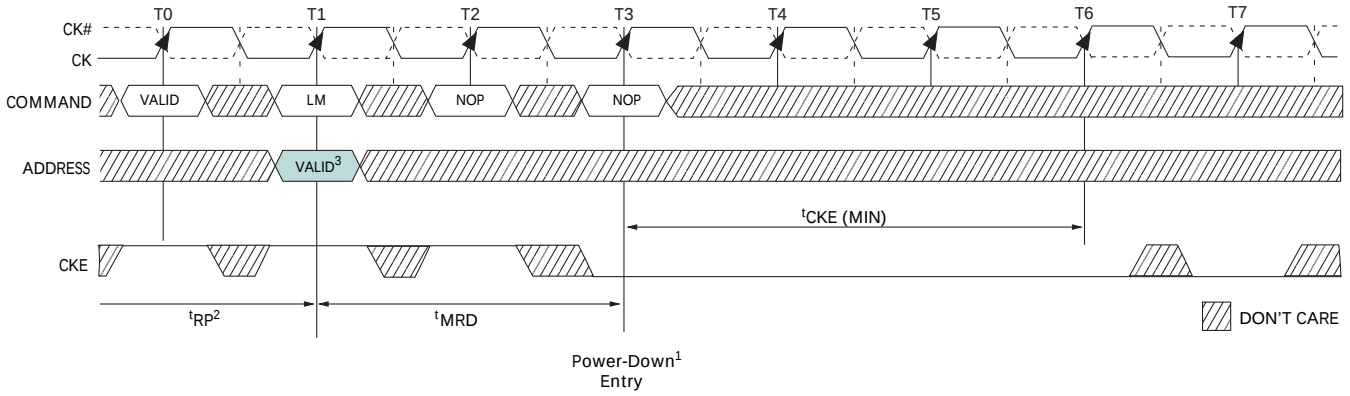
Figure 53: PRECHARGE Command to Power-Down Entry



NOTE:

1. The earliest power-down entry may occur is at T2, which is 1 x ^{t}CK after the PRECHARGE command. Power-down entry occurs prior to ^{t}RP (MIN) being satisfied.

Figure 54: LOAD MODE Command to Power-Down Entry



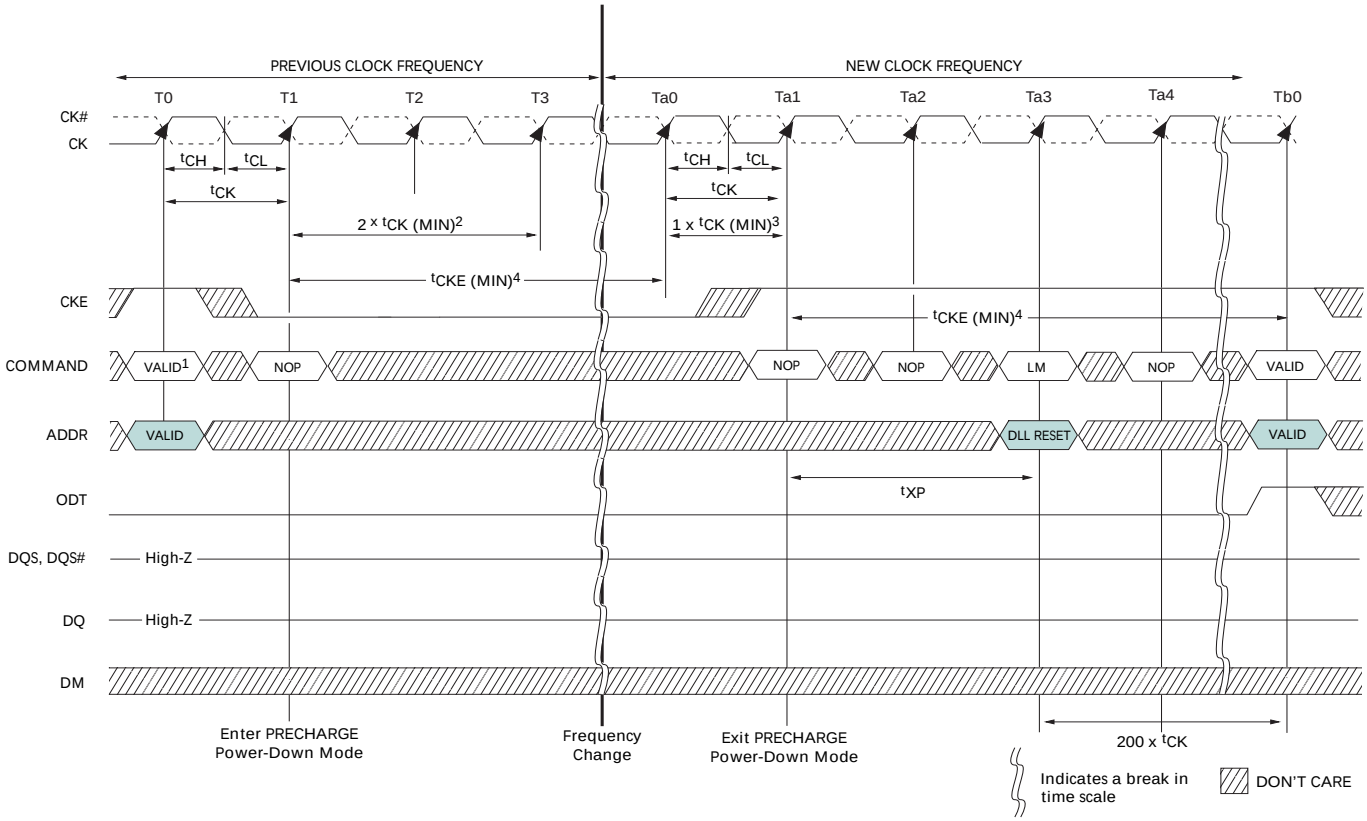
NOTE:

1. The earliest PRECHARGE power-down entry is at T3, which is after ^{t}MRD is satisfied.
2. All banks must be in the precharged state and ^{t}RP met prior to issuing LM command.
3. Valid address for LM command includes MR, EMR, EMR(2), and EMR(3) registers.

Precharge Power-Down Clock Frequency Change

When the DRAM is in precharged power-down mode, on-die termination (ODT) must be turned off and CKE must be at a logic LOW level. A minimum of two clocks must pass after CKE goes LOW before clock frequency may change. The DRAM input clock frequency is allowed to change only within minimum and maximum operating frequencies specified for the particular speed grade. During input clock frequency change, ODT and CKE must be held at stable LOW levels. Once the input clock frequency is changed, new stable clocks must be provided to the DRAM before precharge power-down may be exited and DLL must be RESET via EMR after precharge power-down exit. Depending on the new clock frequency an additional MR command may need to be issued to appropriately set the WR MR[11, 10, 9] register. During the DLL relock period of 200 cycles, ODT must remain off. After the DLL lock time, the DRAM is ready to operate with a new clock frequency.

Figure 55: Input Clock Frequency Change During PRECHARGE Power Down Mode



NOTE:

1. If this command is a PRECHARGE (or if the device is already in the idle state), then the power-down mode shown is precharge power-down, which is required prior to the clock frequency change.
2. A minimum of 2 x ^{t}CK is required after entering PRECHARGE power-down prior to changing clock frequencies.
3. Once the new clock frequency has changed and is stable, a minimum of 1 x ^{t}CK is required prior to exiting PRECHARGE power-down.
4. Minimum CKE HIGH time is ^{t}CKE = 3 x ^{t}CK. Minimum CKE low time is ^{t}CKE = 3 x ^{t}CK. This requires a minimum of 3 clock cycles of registration.

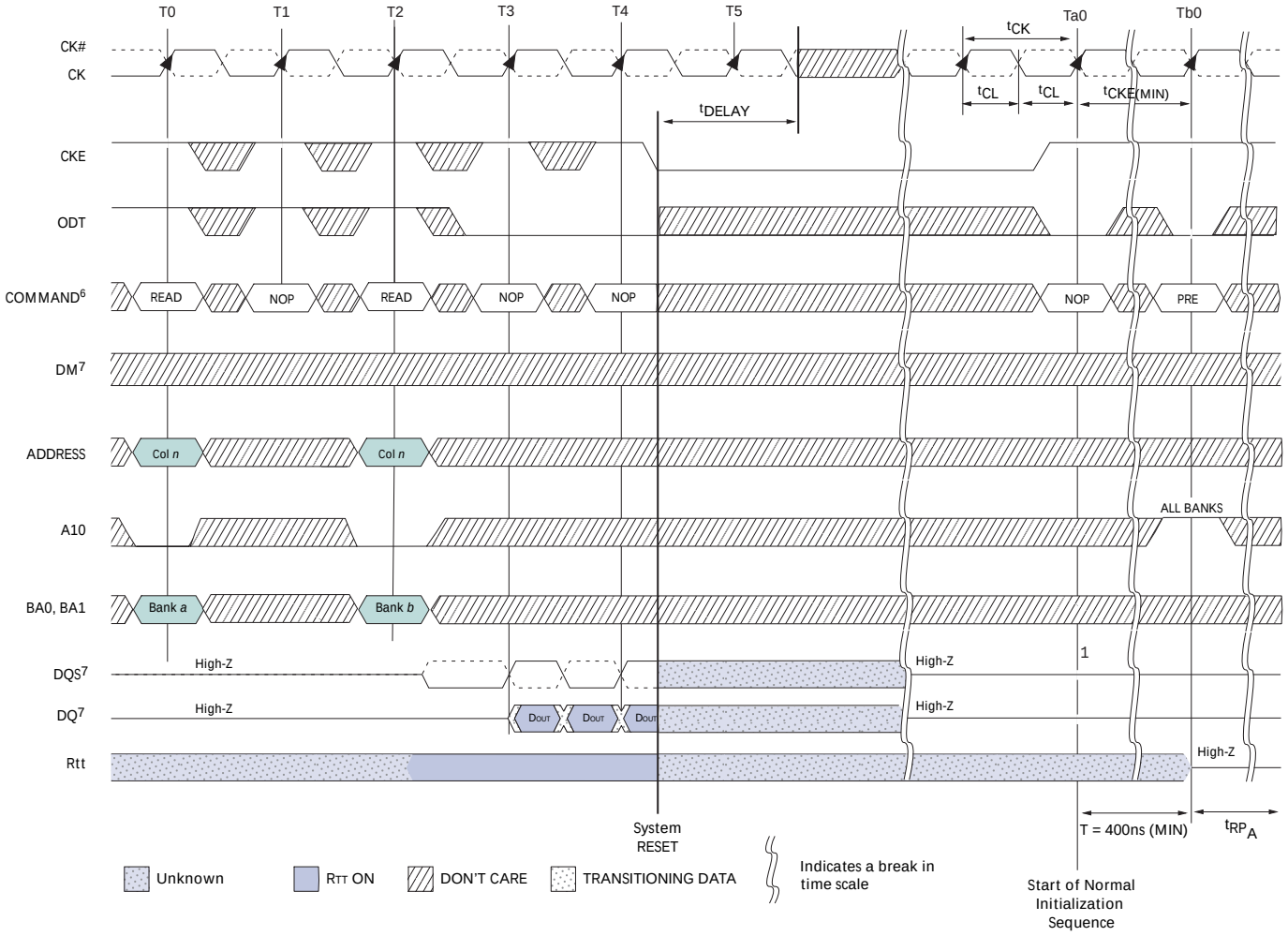
RESET Function (CKE LOW Anytime)

DDR2 SDRAM applications may go into a RESET state at any time during normal operation. If an application enters a reset condition, the CKE input pin is used to ensure the DDR2 SDRAM device resumes normal operation after reinitializing. All data will be lost during a reset condition; however, the DDR2 SDRAM device will continue to operate properly if the following conditions outlined in this section are satisfied.

The RESET condition defined here assumes all supply voltages (VDD, VDDQ, VDDL, and VREF) are stable and meet all DC specifications prior to, during, and after the RESET operation. All other input pins of the DDR2 SDRAM device are a "don't care" during RESET with the exception of CKE.

If CKE asynchronously drops LOW during any valid operation (including a READ or WRITE burst), the memory controller must satisfy the timing parameter tDELAY before turning off the clocks. Stable clocks must exist at the CK, CK# inputs of DRAM before CKE is raised HIGH, at which time the normal initialization sequence must occur (See "Initialization" on page 9). The DDR2 SDRAM is now ready for normal operation after the initialization sequence. Figure 56 shows the proper sequence for a RESET condition.

Figure 56: RESET Condition



For Initialization timing, see time sequence Ta0 in Figure 4, DDR2 Power-Up and Initialization, on page 10

NOTE:

1. In certain cases where a READ cycle is interupted, CKE going high may result in the completion of the burst.

ODT Timing

There are two timing categories for ODT, turn-on and turn-off. During active mode (CKE HIGH) and "fast-exit" power-down mode (any row of any bank open, CKE LOW, MR[bit12 = 0]), ^{t}AOND, ^{t}AON, ^{t}AOFD, and ^{t}AOF timing parameters are applied as shown in Figure 57 and Table 10 on page 68. During "slow-exit" power-down mode (any row of any bank open, CKE LOW, MR[bit12=1]) and precharge power-down mode (all banks/rows precharged and idle, CKE LOW), ^{t}AONPD and ^{t}AOFPD timing parameters are applied as shown in Figure 58 and Table 11 on page 69.

ODT turn-off timing prior to entering any power-down mode is determined by the parameter ^{t}ANPD (MIN) shown in Figure 59. At state T2 the ODT HIGH signal satisfies ^{t}ANPD (MIN) prior to entering power-down mode at T5. When ^{t}ANPD (MIN) is satisfied ^{t}AOFD and ^{t}AOF timing parameters apply. Figure 59 also shows the example where ^{t}ANPD (MIN) is NOT satisfied since ODT HIGH does not occur until state T3. When ^{t}ANPD (MIN) is NOT satisfied, ^{t}AOFPD timing parameters apply.

ODT turn-on timing prior to entering any power-down mode is determined by the parameter ^{t}ANPD shown in Figure 60. At state T2, the ODT HIGH signal satisfies ^{t}ANPD (MIN) prior to entering power-down mode at T5. When ^{t}ANPD (MIN) is satisfied ^{t}AOND and ^{t}AON timing parameters apply. Figure 60 also shows the example where ^{t}ANPD (MIN) is NOT satisfied since ODT HIGH does not occur until state T3. When ^{t}ANPD (MIN) is NOT satisfied, ^{t}AONPD timing parameters apply.

ODT turn-off timing after exiting any power-down mode is determined by the parameter ^{t}AXPD (MIN) shown in Figure 61. At state Ta1, the ODT LOW signal satisfies ^{t}AXPD (MIN) after exiting power-down mode at state T1. When ^{t}AXPD (MIN) is satisfied, ^{t}AOFD and ^{t}AOF timing parameters apply. Figure 61 also shows the example where ^{t}AXPD (MIN) is NOT satisfied since ODT LOW occurs at state Ta0. When ^{t}AXPD (MIN) is NOT satisfied, ^{t}AOFPD timing parameters apply.

ODT turn-on timing after exiting any power-down mode is determined by the parameter ^{t}AXPD (MIN) shown in Figure 62. At state Ta1, the ODT HIGH signal satisfies ^{t}AXPD (MIN) after exiting power-down mode at state T1. When ^{t}AXPD (MIN) is satisfied, ^{t}AOND and ^{t}AON timing parameters apply. Figure 62 also shows the example where ^{t}AXPD (MIN) is NOT satisfied since ODT HIGH occurs at state Ta0. When ^{t}AXPD (MIN) is NOT satisfied, ^{t}AONPD timing parameters apply.

Figure 57: ODT Timing for Active or "Fast-Exit" Power-Down Mode

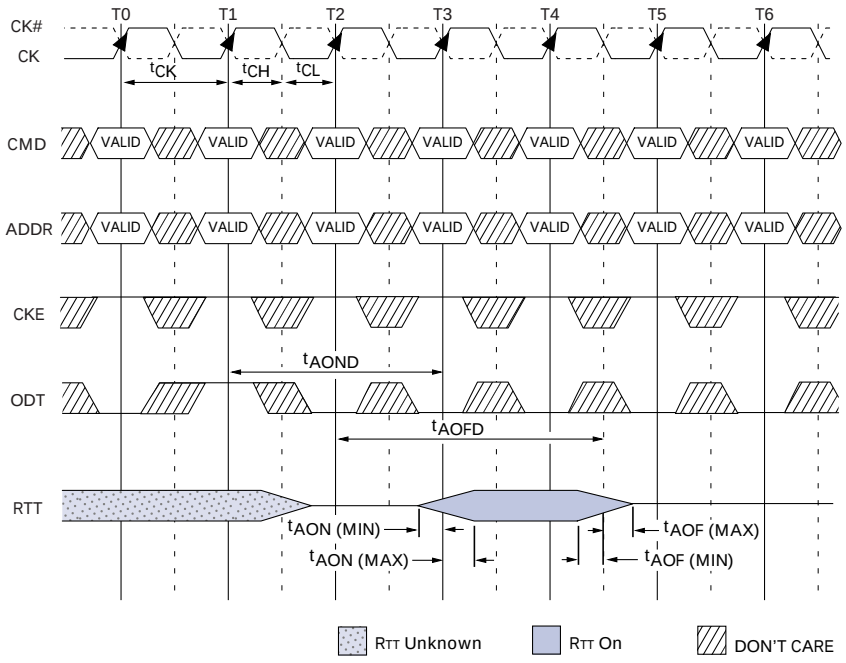


Table 10: ODT Timing for Active and "Fast-Exit" Power-Down Modes

PARAMETER	SYMBOL	MIN	MAX	UNITS
ODT turn-on delay	^{t}AOND	2	2	^{t}CK
ODT turn-on	^{t}AON	^{t}AC (MIN)	^{t}AC (MAX) + 1,000	ps
ODT turn-off delay	^{t}AOFD	2.5	2.5	^{t}CK
ODT turn-off	^{t}AOF	^{t}AC (MIN)	^{t}AC (MAX) + 600	ps

Figure 58: ODT timing for "Slow-Exit" or Precharge Power-Down Modes

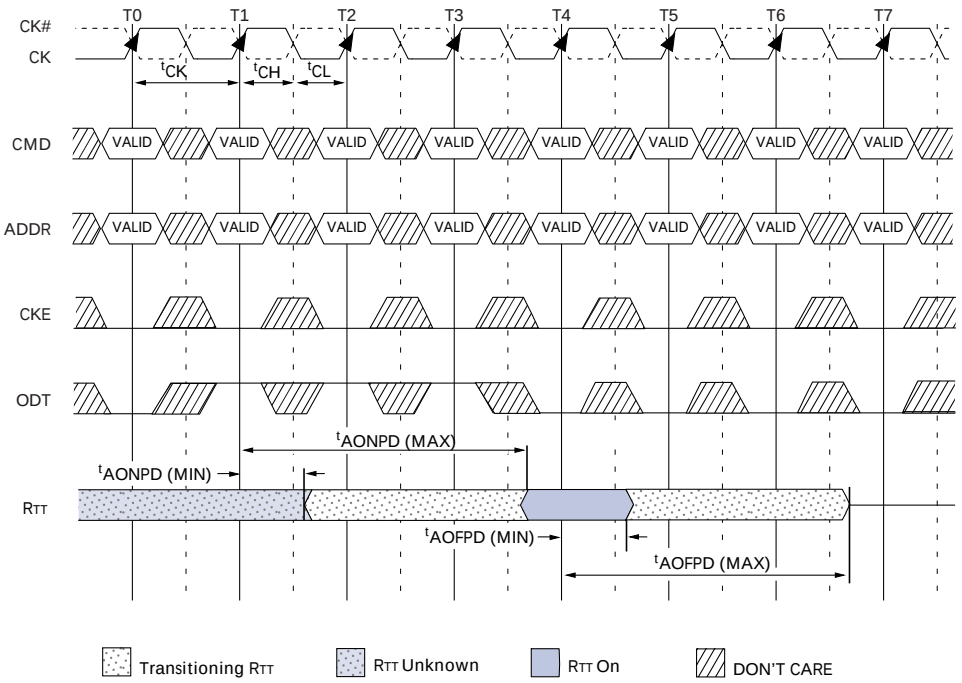


Table 11: ODT timing for "Slow-Exit" and Precharge Power-Down Modes

PARAMETER	SYMBOL	MIN	MAX	UNITS
ODT turn-on (power-down mode)	^{t}AONPD	^{t}AC (MIN) + 2,000	2 x ^{t}CK+^{t}AC (MAX) + 1,000	ps
ODT turn-off (power-down mode)	^{t}AOFPD	^{t}AC (MIN) + 2,000	2.5 x ^{t}CK + ^{t}AC (MAX) + 1,000	ps

Figure 59: ODT "Turn Off" Timings when Entering Power-Down Mode

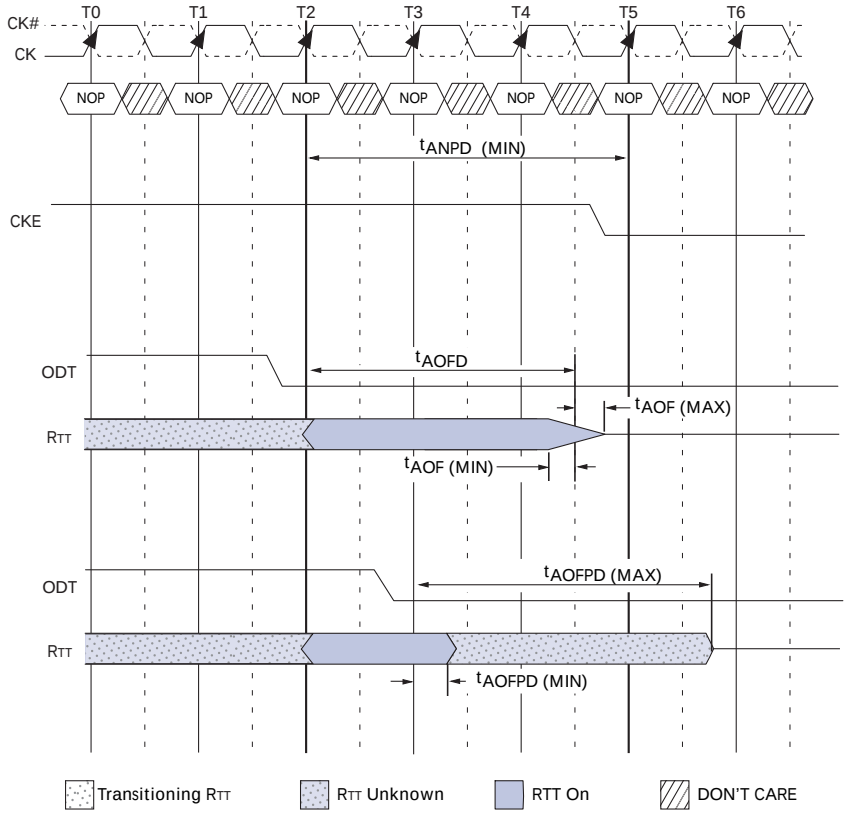


Table 12: ODT "Turn Off" Timings when Entering Power-Down Mode

PARAMETER	SYMBOL	MIN	MAX	UNITS
ODT turn-off delay	^{t}AOFD	2.5	2.5	^{t}CK
ODT turn-off	^{t}AOF	^{t}AC (MIN)	^{t}AC (MAX) + 600	ps
ODT turn-off (power-down mode)	^{t}AOFPD	^{t}AC (MIN) + 2,000	2.5 x ^{t}CK + ^{t}AC (MAX) + 1,000	ps
ODT to power-down entry latency	^{t}ANPD	3		^{t}CK

Figure 60: ODT "Turn-On" Timing when Entering Power-Down Mode

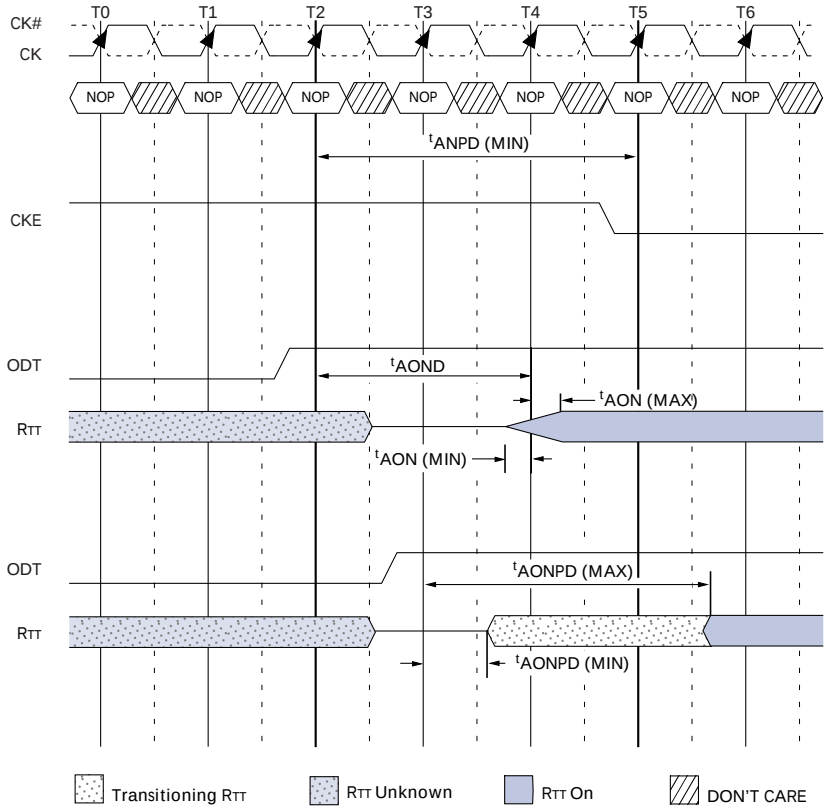


Table 13: ODT "Turn-On" Timing when Entering Power-Down Mode

PARAMETER	SYMBOL	MIN	MAX	UNITS
ODT turn-on delay	^{t}AOND	2	2	^{t}CK
ODT turn-on	^{t}AON	^{t}AC (MIN)	^{t}AC (MAX) + 1,000	ps
ODT turn-on (power-down mode)	^{t}AONPD	^{t}AC (MIN) + 2,000	2 x ^{t}CK + ^{t}AC (MAX) + 1,000	ps
ODT to power-down entry latency	^{t}ANPD	3		^{t}CK

Figure 61: ODT "Turn-Off" Timing when Exiting Power-Down Mode

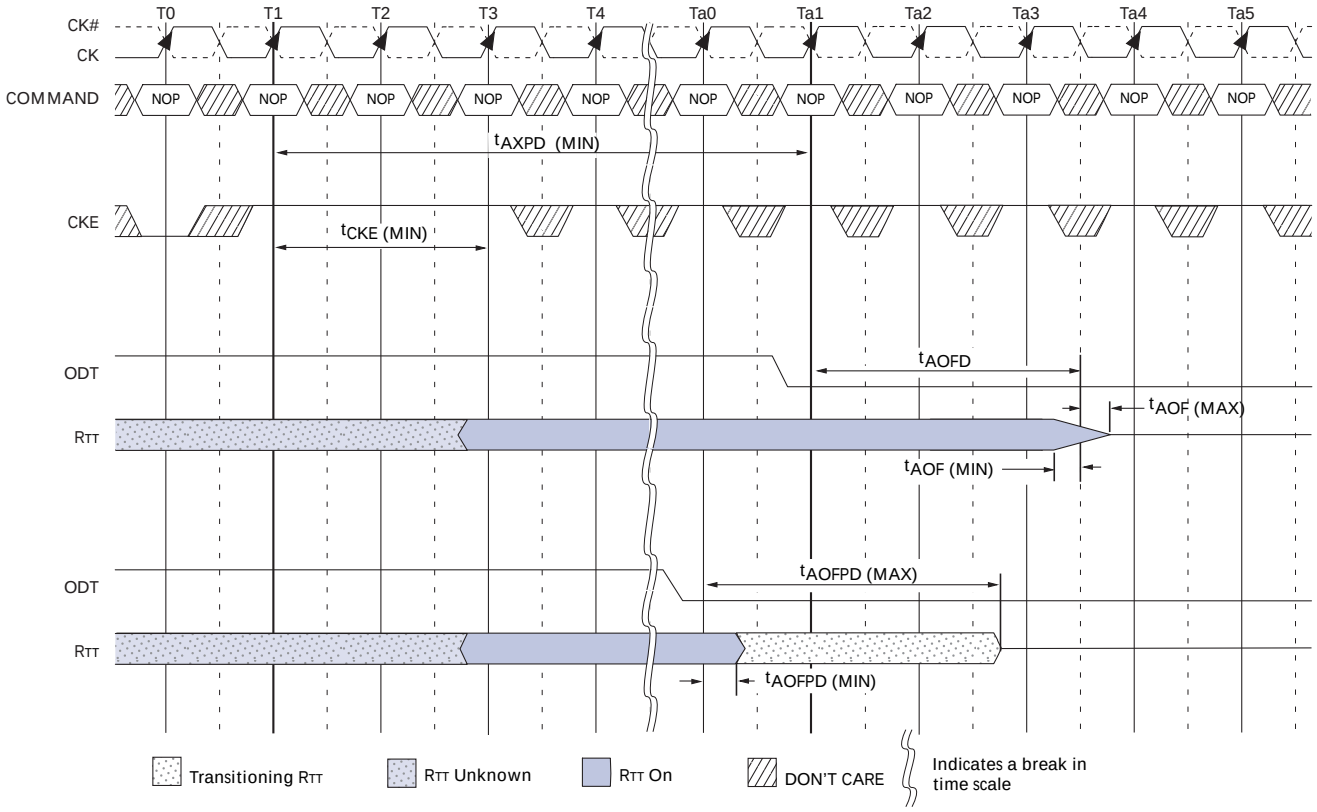


Table 14: ODT "Turn-Of" Timing when Exiting Power-Down Mode

PARAMETER	SYMBOL	MIN	MAX	UNITS
ODT turn-off delay	^{t}AOFD	2.5	2.5	^{t}CK
ODT turn-off	^{t}AOF	^{t}AC (MIN)	^{t}AC (MAX) + 600	ps
ODT turn-off (power-down mode)	^{t}AOFPD	^{t}AC (MIN) + 2,000	2.5 x ^{t}CK + ^{t}AC (MAX) + 1,000	ps
ODT to power-down exit latency	^{t}AXPD	8		^{t}CK

Figure 62: ODT "Turn On" Timing when Exiting Power-Down Mode

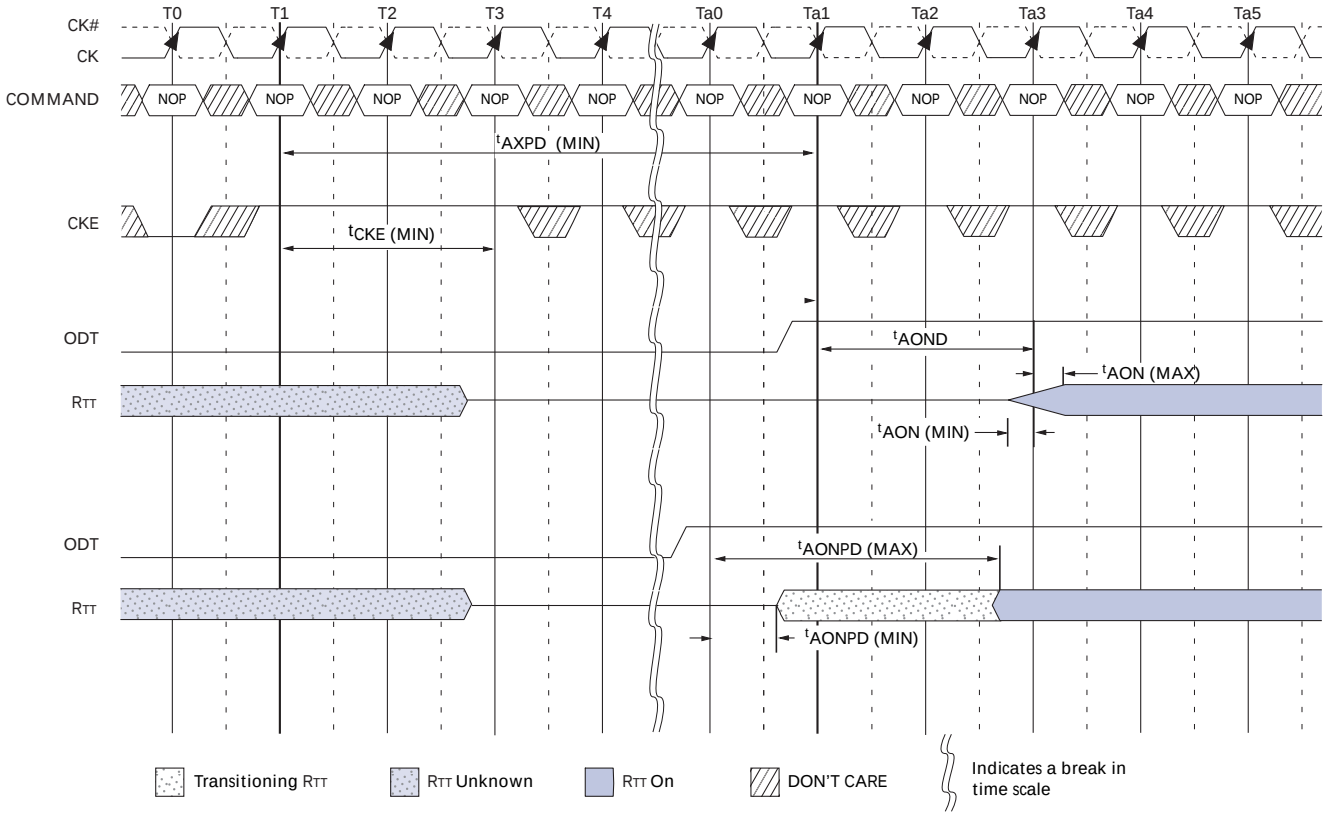


Table 15: ODT "Turn On" Timing when Exiting Power-Down Mode

PARAMETER	SYMBOL	MIN	MAX	UNITS
ODT turn-on delay	^{t}AOND	2	2	^{t}CK
ODT turn-on	^{t}AON	^{t}AC (MIN)	^{t}AC (MAX) + 1,000	ps
ODT turn-on (power-down mode)	^{t}AONPD	^{t}AC (MIN) + 2,000	2 x ^{t}CK + ^{t}AC (MAX) + 1,000	ps
ODT to power-down exit latency	^{t}AXPD	8		^{t}CK

Absolute Maximum Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

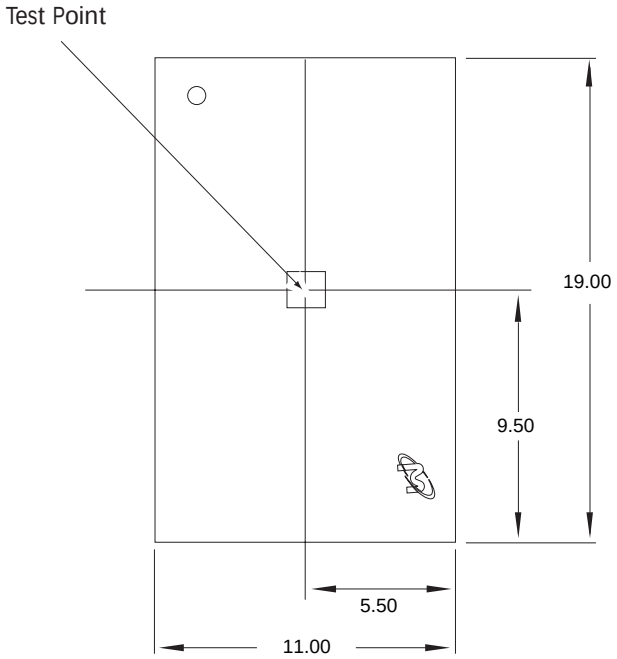
Table 16: Absolute Maximum DC Ratings

SYMBOL	PARAMETER	MIN	MAX	UNITS
VDD	VDD Supply Voltage Relative to VSS	-1.0	2.3	V
VDDQ	VDDQ Supply Voltage Relative to VSSQ	-0.5	2.3	V
VDDL	VDDL Supply Voltage Relative to VSSL	-0.5	2.3	V
VIN, VOUT	Voltage on any Pin Relative to VSS	-0.5	2.3	V
TSTG	Storage Temperature (T_{case})[1]	-55	100	°C
T_C	Operating Temperature (T_{case})[1,2]	0	85	°C
I_I	Input Leakage Current Any input 0V <= VIN <= VDD (All other pins not under test = 0V)	-5	5	uA
I_{OZ}	Output Leakage Current 0V <= VOUT <= VDDQ DQs and ODT are disabled	-5	5	uA
I_{VREF}	VREF Leakage Current VREF = Valid VREF level	-2	2	uA

NOTE:

1. MAX operating case temperature; T_C is measured in the center of the package illustrated in Figure 63.
2. Device functionality is not guaranteed if the DRAM device exceeds the maximum T_C during operation.

Figure 63: Example Temperature Test Point Location



11m x 19mm "BT" FBGA

AC and DC Operating Conditions

Table 17: Recommended DC Operating Conditions (SSTL_18)

All voltages referenced to V_{SS}

PARAMETER	SYMBOL	MIN	NOM	MAX	UNITS	NOTES
Supply Voltage	V_{DD}	1.7	1.8	1.9	V	1, 5
$V_{DD}L$ Supply Voltage	$V_{DD}L$	1.7	1.8	1.9	V	4, 5
I/O Supply Voltage	$V_{DD}Q$	1.7	1.8	1.9	V	4, 5
I/O Reference Voltage	$V_{REF}(DC)$	0.49 x $V_{DD}Q$	0.50 x $V_{DD}Q$	0.51 x $V_{DD}Q$	V	2
I/O Termination Voltage (system)	V_{TT}	$V_{REF}(DC)$ - 40	$V_{REF}(DC)$	$V_{REF}(DC)$ + 40	mV	3

NOTE:

1. V_{DD} and $V_{DD}Q$ must track each other. $V_{DD}Q$ must be less than or equal to V_{DD}.
2. V_{REF} is expected to equal $V_{DD}Q/2$ of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise (non-common mode) on V_{REF} may not exceed ±1% of the DC value. Peak-to-peak AC noise on V_{REF} may not exceed ±2 percent of $V_{REF}(DC)$. This measurement is to be taken at the nearest V_{REF} bypass capacitor.
3. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}.
4. $V_{DD}Q$ tracks with V_{DD}; $V_{DD}L$ tracks with V_{DD}.
5. $V_{SS}Q$ = $V_{SS}L$ = V_{SS}

Table 18: ODT DC Electrical Characteristics

All voltages referenced to V_{SS}

PARAMETER	SYMBOL	MIN	NOM	MAX	UNITS	NOTES
R_{TT} effective impedance value for 75Ω setting EMR (A6, A2) = 0, 1	$R_{TT}1(EFF)$	60	75	90	Ω	1
R_{TT} effective impedance value for 150Ω setting EMR (A6, A2) = 1, 0	$R_{TT}2(EFF)$	120	150	180	Ω	1
Deviation of VM with respect to $V_{DD}Q/2$	ΔVM	-6%		6%	%	2

NOTE:

1. $R_{TT}1(EFF)$ and $R_{TT}2(EFF)$ are determined by applying $V_{IH}(AC)$ and $V_{IL}(AC)$ to pin under test separately, then measure current $I(V_{IH}(AC))$ and $I(V_{IL}(AC))$ respectively.

$$R_{TT}(\mathrm{EFF}) = \frac{V_{IH}(AC) - V_{IL}(AC)}{I(V_{IH}(AC)) - I(V_{IL}(AC))}$$

2. Measure voltage (VM) at tested pin with no load.

$$\Delta VM = \left(\frac{2 \times VM}{V_{DD}Q} - 1\right) \times 100\%$$

Input Electrical Characteristics and Operating Conditions

Table 19: Input DC Logic Levels

All voltages referenced to V_{SS}

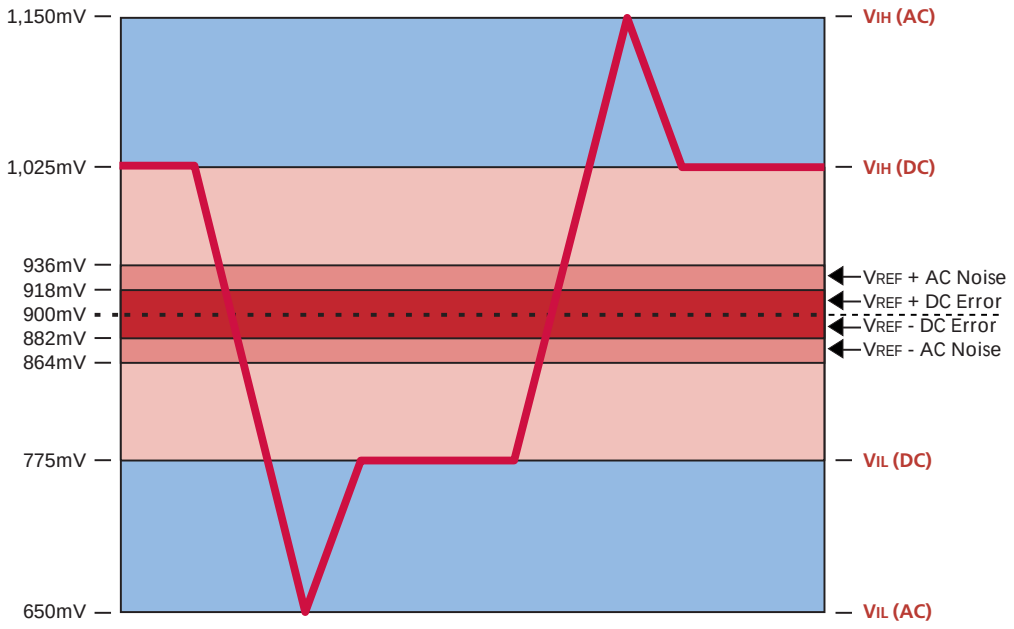
PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage	$V_{IH(DC)}$	$V_{REF(DC)}$ + 125	V_{DDQ} + 300	mV	
Input Low (Logic 0) Voltage	$V_{IL(DC)}$	-300	$V_{REF(DC)}$ - 125	mV	

Table 20: Input AC Logic Levels

All voltages referenced to V_{SS}

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage	$V_{IH(AC)}$	$V_{REF(DC)}$ + 250	-	mV	
Input Low (Logic 0) Voltage	$V_{IL(AC)}$	–	$V_{REF(DC)}$ - 250	mV	

Figure 64: Single-Ended Input Signal Levels



NOTE:

Numbers in diagram reflect nomimal values.

Table 21: Differential Input Logic Levels

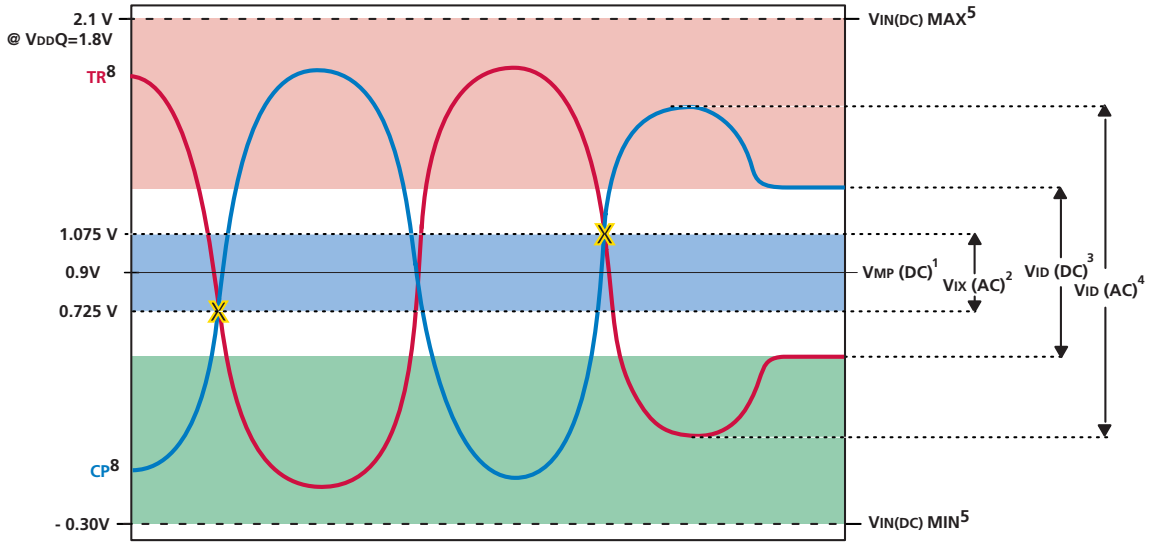
All voltages referenced to V_{SS}

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
DC Input Signal Voltage	V_{IN}(DC)	-300	V_{DDQ} + 300	mV	1
DC Differential Input Voltage	V_{ID}(DC)	250	V_{DDQ} + 600	mV	2
AC Differential Input Voltage	V_{ID}(AC)	500	V_{DDQ} + 600	mV	3
AC Differential Cross-Point Voltage	V_{IX}(AC)	0.50 x V_{DDQ} - 175	0.50 x V_{DDQ} + 175	mV	4
Input Midpoint Voltage	V_{MP}(DC)	850	950	mV	5

NOTE:

1. V_{IN} (DC) specifies the allowable DC execution of each input of differential pair such as CK, CK#, DQS, DQS#, LDQS, LDQS#, UDQS, UDQS#, and RDQS, RDQS#.
2. V_{ID} (DC) specifies the input differential voltage | V_{TR} - V_{CP} | required for switching, where V_{TR} is the true input (such as CK, DQS, LDQS, UDQS, RDQS) level and V_{CP} is the complementary input (such as CK#, DQS#, LDQS#, UDQS#, RDQS#). The minimum value is equal to V_{IH}(DC) - V_{IL}(DC). Differential input signal levels are shown in Figure 65.
3. V_{ID}(AC) specifies the input differential voltage | V_{TR} - V_{CP} | required for switching, where V_{TR} is the true input (such as CK, DQS, LDQS, UDQS, RDQS) level and V_{CP} is the complementary input (such as CK#, DQS#, LDQS#, UDQS#, RDQS#). The minimum value is equal to V_{IH}(AC) - V_{IL}(AC) from Table 20 on page 76.
4. The typical value of V_{IX} (AC) is expected to be about 0.5 x V_{DDQ} of the transmitting device and V_{IX}(AC) is expected to track variations in V_{DDQ}. V_{IX}(AC) indicates the voltage at which differential input signals must cross as shown in Figure 65.
5. V_{MP}(DC) specifies the input differential common mode voltage (V_{TR} + V_{CP})/2 where V_{TR} is the true input (CK, DQS) level and V_{CP} is the complementary input (CK#, DQS#). V_{MP}(DC) is expected to be about 0.5*V_{DDQ}.

Figure 65: Differential Input Signal Levels



NOTE:

1. This provides a minimum of 850mV to a maximum of 950mV and is expected to be V_{DDQ}/2.
2. TR and CP must cross in this region.
3. TR and CP must meet at least V_{ID}(DC) min when static and is centered around V_{MP}(DC).
4. TR and CP must have a minimum 500mV peak-to-peak swing.
5. TR and CP may not be more positive than V_{DDQ} + 0.3V or more negative than V_{SS} - 0.3V.
6. For AC operation, all DC clock requirements must also be satisfied.
7. Numbers in diagram reflect nominal values.
8. TR represents the CK, DQS, RDQS, LDQS and UDQS signals; CP represents CK#, DQS#, RDQS#, LDQS# and UDQS# signals.

Table 22: AC Input Test Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input setup timing measurement reference level BA1-BA0, A0-A13 (A12 x16), CS#, RAS#, CAS#, WE#, ODT, DM, UDM, LDM and CKE	V_{RS}	See Note 2			1, 2,
Input hold timing measurement reference level BA1-BA0, A0-A13 (A12 x16), CS#, RAS#, CAS#, WE#, ODT, DM, UDM, LDM and CKE	V_{RH}	See Note3			1, 3,
Input timing measurement reference level (single-ended) DQS for x4x8; UDQS, LDQS for x16	$V_{REF(DC)}$	V_{DDQ}*0.49	V_{DDQ}*0.51	V	1, 4
Input timing measurement reference level (differential) CK, CK# for x4,x8,x16 DQS, DQS# for x4,x8; RDQS, RDQS# for x8 UDQS, UDQS#, LDQS, LDQS# for x16	V_{RD}	$V_{IX(AC)}$		V	1, 5, 6

NOTE:

1. All voltages referenced to V_{SS}.
2. Input waveform setup timing ($^{t}IS_{b}$) is referenced from the input signal crossing at the $V_{IH(AC)}$ level for a rising signal and $V_{IL(DC)}$ for a falling signal applied to the device under test as shown in Figure 74.
3. Input waveform hold ($^{t}IH_{b}$) timing is referenced from the input signal crossing at the $V_{IL(DC)}$ level for a rising signal and $V_{IH(DC)}$ for a falling signal applied to the device under test as shown in Figure 74
4. Input waveform setup timing (^{t}DS) and hold timing (^{t}DH) for single-ended data strobe is referenced from the crossing of DQS, UDQS, or LDQS through the V_{REF} level applied to the device under test as shown in Figure 76.
5. Input waveform setup timing (^{t}DS) and hold timing (^{t}DH) when differential data strobe is enabled is referenced from the crosspoint of DQS,DQS# or UDQS,UDQS# or LDQS,LDQS# as shown in Figure 75.
6. Input waveform timing is referenced to the crossing point level (V_{IX}) of two input signals (V_{TR} and V_{CP}) applied to the device under test, where V_{TR} is the "true" input signal and V_{CP} is the "complementary" input signal shown in Figure 77.
7. See "Input Slew Rate Derating" on page 79.

Input Slew Rate Derating

For all input signals the total ^{t}IS (setup time) and ^{t}IH (hold time) required is calculated by adding the data sheet ^{t}IS(base) and ^{t}IH(base) value to the Δ^{t}IS and Δ^{t}IH derating value respectively. Example: ^{t}IS (total setup time) = ^{t}IS(base) + Δ^{t}IS

Setup (^{t}IS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VREF(DC) and the first crossing of VIH(AC)min. Setup (^{t}IS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VREF(DC) and the first crossing of VIL(AC)MAX. If the actual signal is always earlier than the nominal slew rate line between shaded 'VREF(DC) to AC region', use nominal slew rate for derating value (Figure 66 on page 80) If the actual signal is later than the nominal slew rate line anywhere between shaded 'VREF(DC) to ac region', the slew rate of a tangent line to the actual signal from the AC level to DC level is used for derating value (Figure 67 on page 80)

Hold (^{t}IH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(DC)MAX and the first crossing of VREF(DC). Hold (^{t}IH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(DC)MIN and the first crossing of VREF(DC). If the actual signal is always later than the nominal slew rate line between shaded 'dc to VREF(DC) region', use nominal slew rate for derating value (Figure 68 on page 81) If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to VREF(DC) region', the slew rate of a tangent line to the actual signal from the dc level to VREF(DC) level is used for derating value (Figure 69 on page 81)

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached VIH/IL(AC) at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach VIH/IL(AC)).

For slew rates in between the values listed in Table 23, the derating values may obtained by linear interpolation.

Table 23: Setup and Hold Time Derating Values

		CK,CK# DIFFERENTIAL SLEW RATE						
		2.0 V/NS		1.5 V/NS		1.0 V/NS		
		Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	UNITS
Command/ Address Slew rate (V/ns)	4.0	+187	+94	+217	+124	+247	+154	ps
	3.5	+179	+89	+209	+119	+239	+149	ps
	3.0	+167	+83	+197	+113	+227	+143	ps
	2.5	+150	+75	+180	+105	+210	+135	ps
	2.0	+125	+45	+155	+75	+185	+105	ps
	1.5	+83	+21	+113	+51	+143	+81	ps
	1.0	0	0	+30	+30	+60	+60	ps
	0.9	-11	-14	+19	+16	+49	+46	ps
	0.8	-25	-31	+5	-1	+35	+29	ps
	0.7	-43	-54	-13	-24	+17	+6	ps
	0.6	-67	-83	-37	-53	-7	-23	ps
	0.5	-110	-125	-80	-95	-50	-65	ps
	0.4	-175	-188	-145	-158	-115	-128	ps
	0.3	-285	-292	-255	-262	-225	-232	ps
	0.25	-350	-375	-320	-345	-290	-315	ps
	0.2	-525	-500	-495	-470	-465	-440	ps
	0.15	-800	-708	-770	-678	-740	-648	ps
	0.1	-1450	-1125	-1420	-1095	-1390	-1065	ps

Figure 66: Nominal Slew Rate for tIS

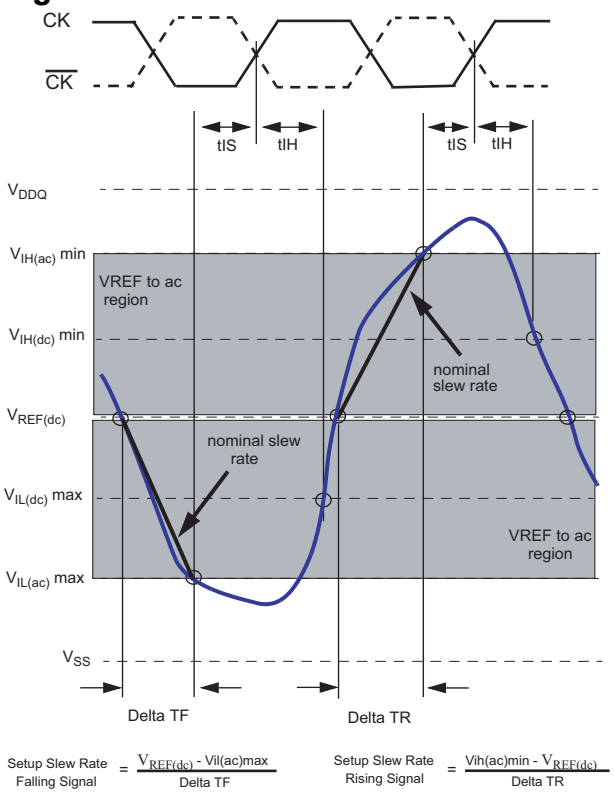


Figure 67: Tangent Line for tIS

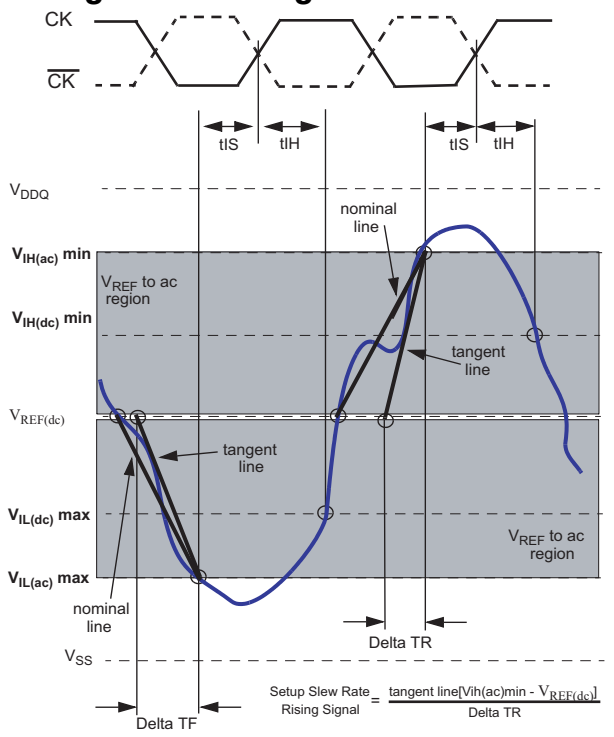


Figure 68: Nominal Slew Rate for tIH

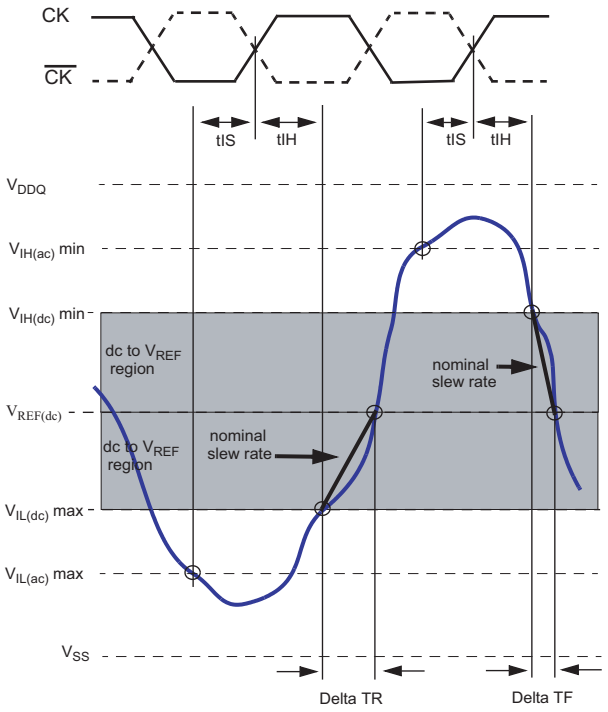
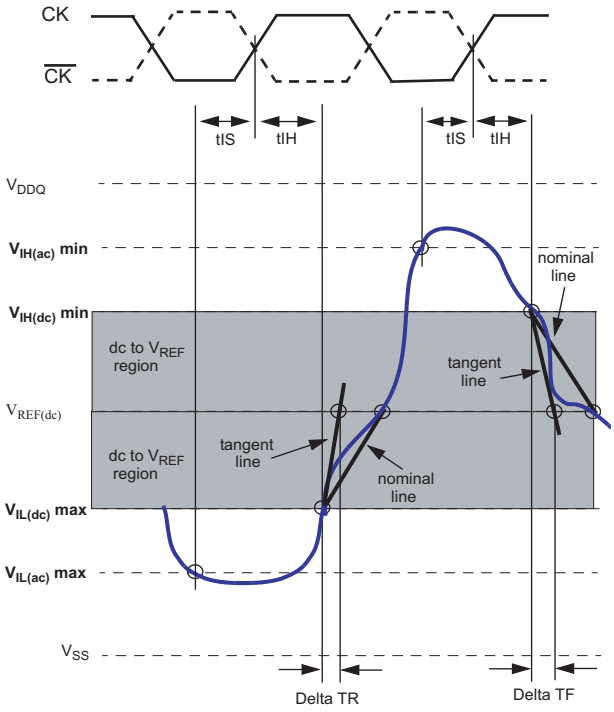


Figure 69: Tangent Line for tIH



$$\text{Hold Slew Rate Rising Signal} = \frac{\text{tangent line [} V_{REF(dc)} \text{ - Vil(dc)max]}}{\text{Delta TR}}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{\text{tangent line [Vih(dc)min - } V_{REF(dc)} \text{]}}{\text{Delta TF}}$$

Data Slew Rating

Table 24: ^{t}DS, ^{t}DH Derating Values

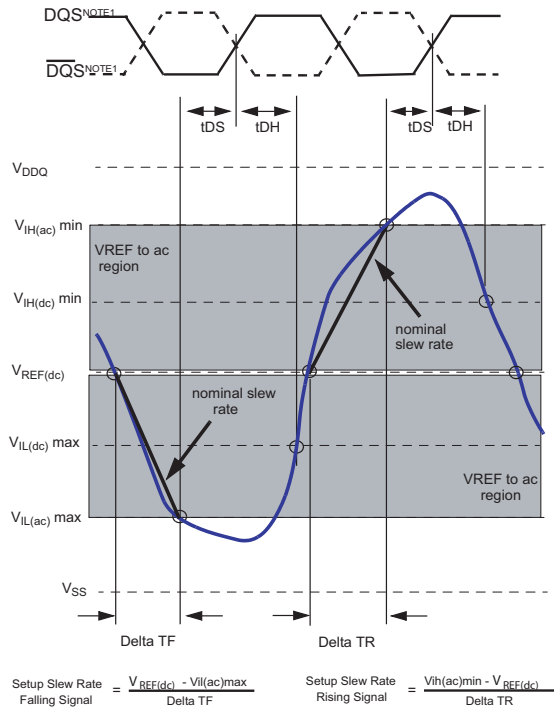
Note 1; all units in ps

		DQS,DQS# DIFFERENTIAL SLEW RATE																	
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4V/ns		1.2V/ns		1.0V/ns		0.8V/ns	
		Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH
DQ Slew rate V/ns	2.0	125	45	125	45	125	45	-	-	-	-	-	-	-	-	-	-	-	-
	1.5	83	21	83	21	83	21	95	33	-	-	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	0	0	12	12	24	24	-	-	-	-	-	-	-	-
	0.9	-	-	-11	-14	-11	-14	1	-2	13	10	25	22	-	-	-	-	-	-
	0.8	-	-	-	-	-25	-31	-13	-19	-1	-7	11	5	23	17	-	-	-	-
	0.7	-	-	-	-	-	-	-31	-42	-19	-30	-7	-18	5	-6	17	6	-	-
	0.6	-	-	-	-	-	-	-	-	-43	-59	-31	-47	-19	-35	-7	-23	5	-11
	0.5	-	-	-	-	-	-	-	-	-	-	-74	-89	-62	-77	-50	-65	-38	-53
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-127	-140	-115	-128	-103	-116

NOTE:

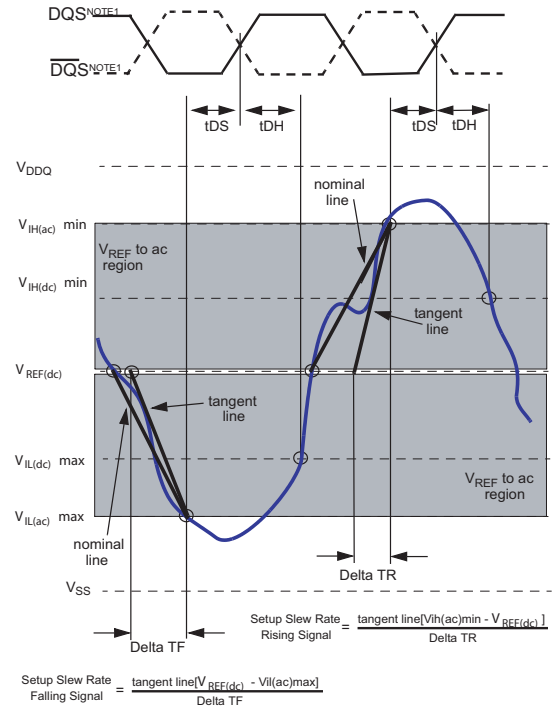
1. For all input signals the total ^{t}DS (setup time) and ^{t}DH (hold time) required is calculated by adding the datasheet value to the derating value listed in Table 24.
2. Setup (^{t}DS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and the first crossing of Vih(ac)min. Setup (^{t}DS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and the first crossing of Vil(ac)max. If the actual signal is always earlier than the nominal slew rate line between shaded '$V_{REF(dc)}$ to ac region', use nominal slew rate for derating value (see Figure 70) If the actual signal is later than the nominal slew rate line anywhere between shaded '$V_{REF(dc)}$ to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value (see Figure 71)
3. Hold (^{t}DH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of Vil(dc)max and the first crossing of $V_{REF(dc)}$. Hold (^{t}DH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of Vih(dc)min and the first crossing of $V_{REF(dc)}$. If the actual signal is always later than the nominal slew rate line between shaded 'dc level to $V_{REF(dc)}$ region', use nominal slew rate for derating value (see Figure 72) If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to $V_{REF(dc)}$ region', the slew rate of a tangent line to the actual signal from the dc level to $V_{REF(dc)}$ level is used for derating value (see Figure 73)
4. Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached $V_{IH/IL}$(ac) at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach $V_{IH/IL}$(ac).
5. For slew rates in between the values listed in Table 24, the derating values may obtained by linear interpolation.
6. These values are typically not subject to production test. They are verified by design and characterization.

Figure 70: Nominal Slew Rate for tDS



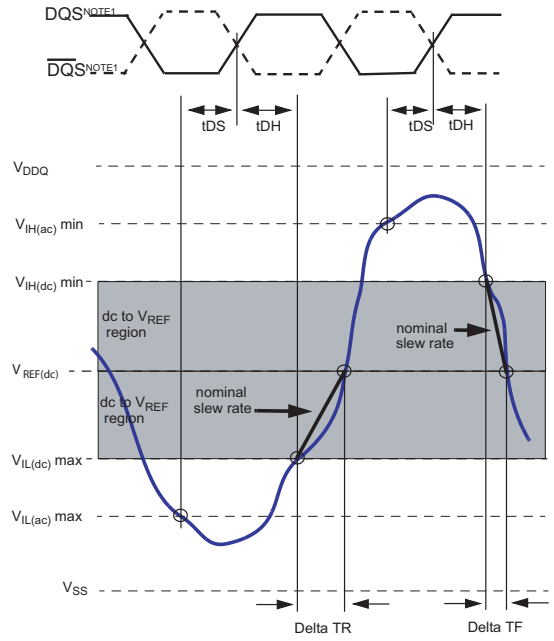
NOTE1 DQS, DQS# signals must be monotonic between Vil(dc)max and Vih(dc)min.

Figure 71: Tangent Line for tDS



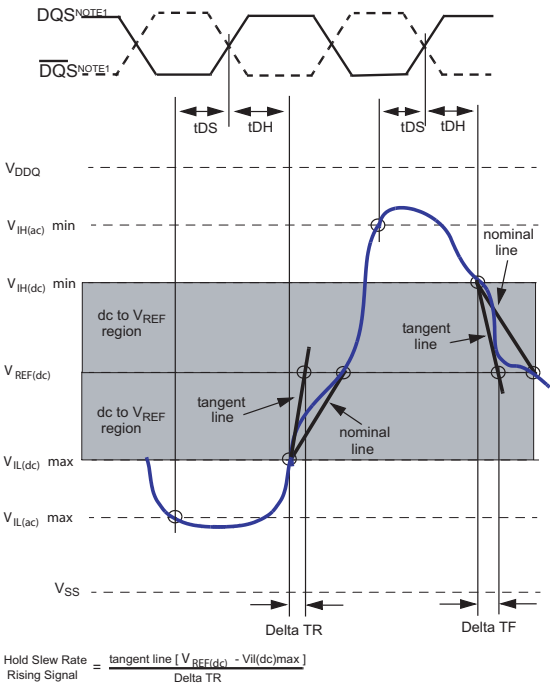
NOTE1 DQS, DQS# signals must be monotonic between Vil(dc)max and Vih(dc)min.

Figure 72: Nominal Slew Rate for tDH



NOTE1 DQS, DQS# signals must be monotonic between Vil(dc)max and Vih(dc)min.

Figure 73: Tangent Line for tDH



NOTE1 DQS, DQS# signals must be monotonic between Vil(dc)max and Vih(dc)min.

Figure 74: AC Input Test Signal Waveform Command/Address pins

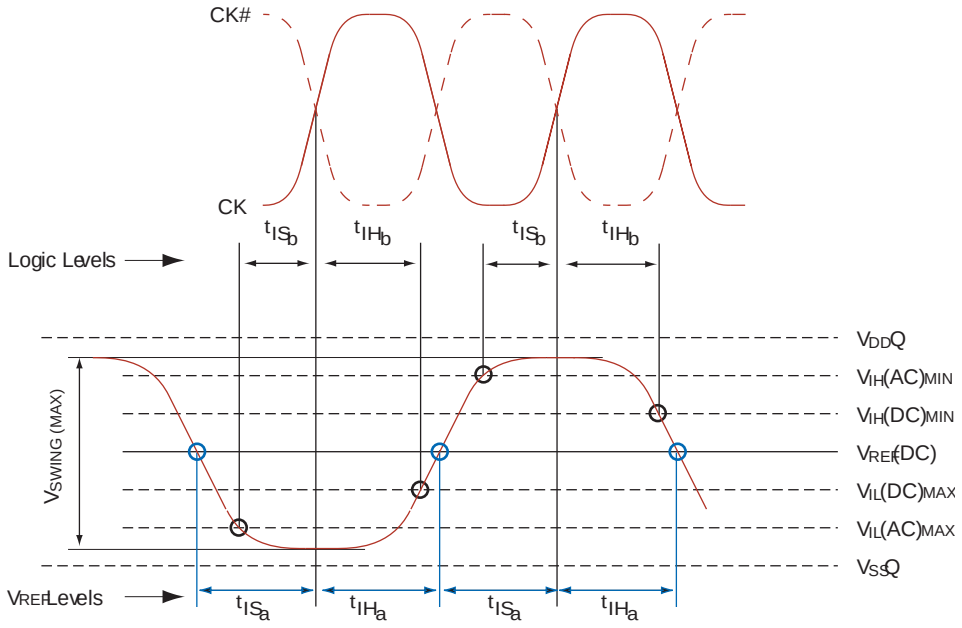


Figure 75: AC Input Test Signal Waveform for Data with DQS,DQS# (differential)

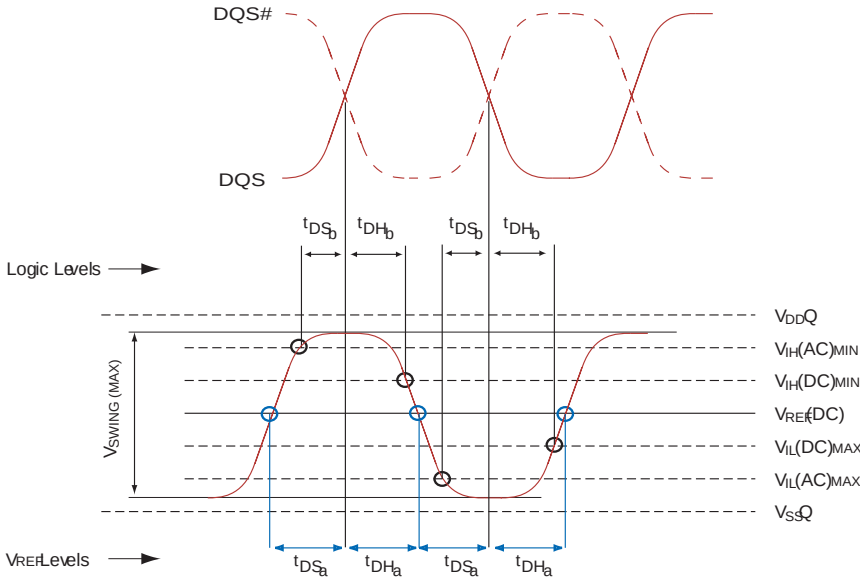


Figure 76: AC Input Test Signal Waveform for Data with DQS (single-ended)

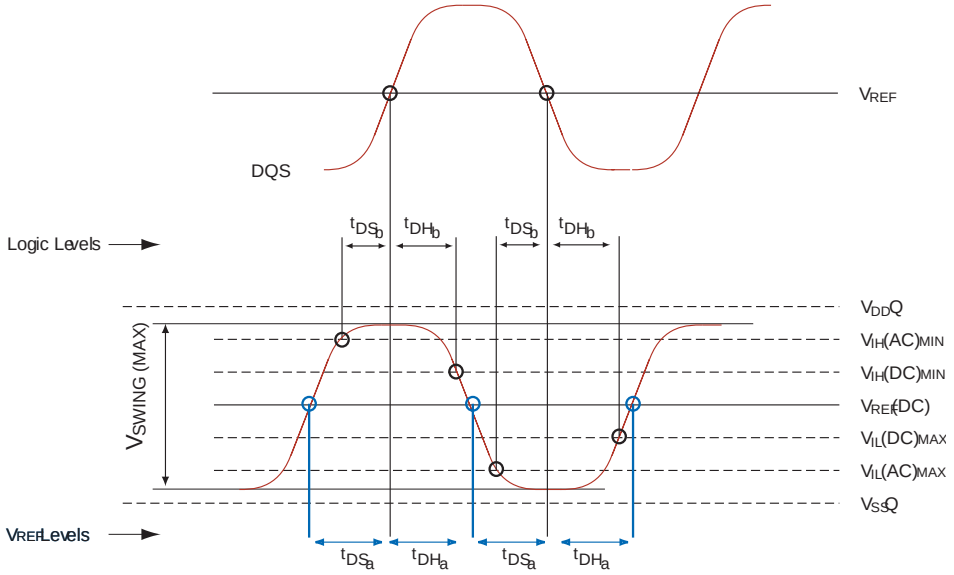
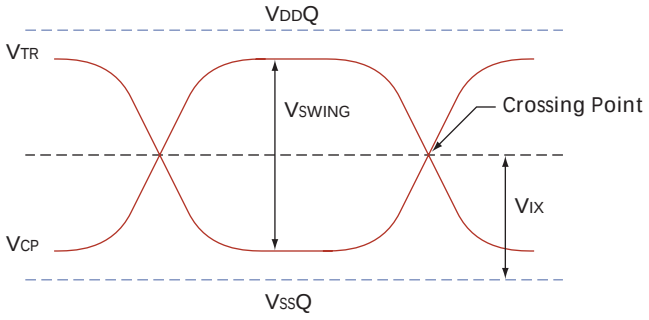


Figure 77: AC Input Test Signal Waveform (differential)



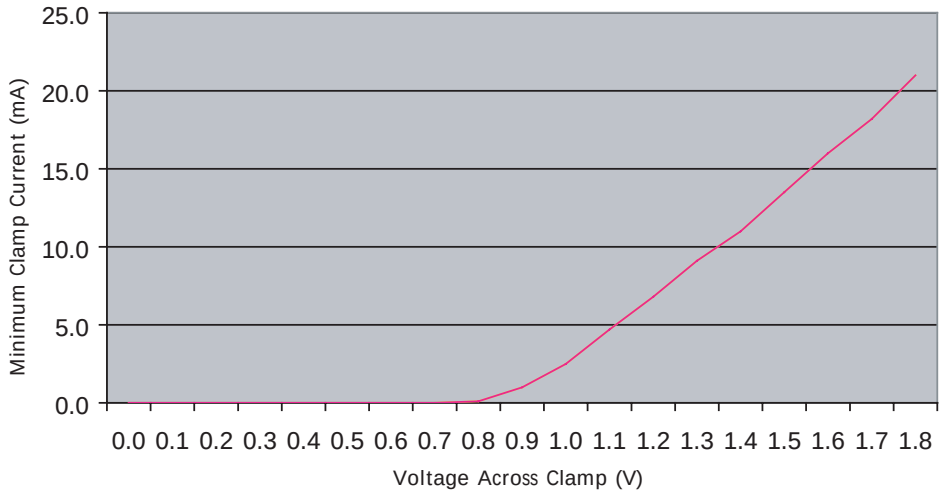
Power and Ground Clamp Characteristics

Power and ground clamps are provided on the following input-only pins: BA1-BA0, A0-A13 (A12 x16), CS#, RAS#, CAS#, WE#, ODT, and CKE.

Table 25: Input Clamp Characteristics

VOLTAGE ACROSS CLAMP (V)	MINIMUM POWER CLAMP CURRENT (mA)	MINIMUM GROUND CLAMP CURRENT (mA)
0.0	0.0	0.0
0.1	0.0	0.0
0.2	0.0	0.0
0.3	0.0	0.0
0.4	0.0	0.0
0.5	0.0	0.0
0.6	0.0	0.0
0.7	0.0	0.0
0.8	0.1	0.1
0.9	1.0	1.0
1.0	2.5	2.5
1.1	4.7	4.7
1.2	6.8	6.8
1.3	9.1	9.1
1.4	11.0	11.0
1.5	13.5	13.5
1.6	16.0	16.0
1.7	18.2	18.2
1.8	21.0	21.0

Figure 78: Input Clamp Characteristics



AC Overshoot/Undershoot Specification

Table 26: Address and Control Pins

Applies to BA1-BA0, A0-A13 (A12 x16), CS#, RAS#, CAS#, WE#, CKE, ODT

PARAMETER	SPECIFICATION	
	-5E	-37E
Maximum peak amplitude allowed for overshoot area (See Figure 79)	0.9V	0.9V
Maximum peak amplitude allowed for undershoot area (See Figure 80)	0.9V	0.9V
Maximum overshoot area above V_{DD} (See Figure 79)	0.75V-ns	0.56V-ns
Maximum undershoot area below V_{SS} (See Figure 80)	0.75V-ns	0.56V-ns

Table 27: Clock, Data, Strobe, and Mask Pins

Applies to DQ0–DQxx, DQS, DQS#, RDQS, RDQS#, UDQS, UDQS#, LDQS, LDQS#, DM, UDM, LDM

PARAMETER	SPECIFICATION	
	-5E	-37E
Maximum peak amplitude allowed for overshoot area (See Figure 79)	0.9V	0.9V
Maximum peak amplitude allowed for undershoot area (See Figure 79)	0.9V	0.9V
Maximum overshoot area above $V_{DD}Q$ (See Figure 79)	0.38V-ns	0.28V-ns
Maximum undershoot area below $V_{SS}Q$ (See Figure 80)	0.38V-ns	0.28V-ns

Figure 79: Overshoot

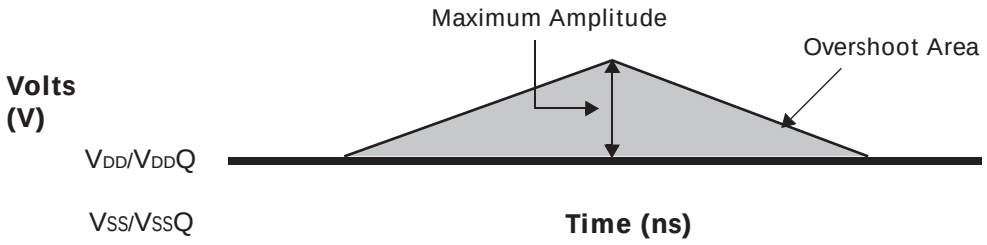
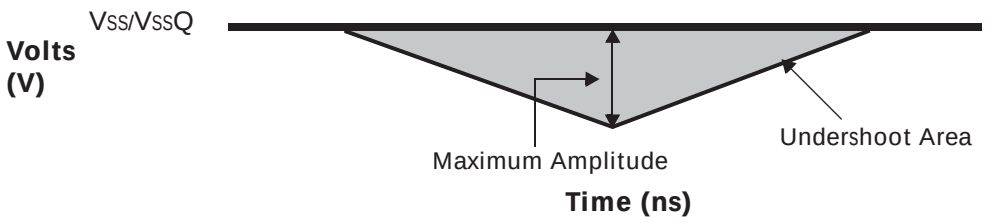


Figure 80: Undershoot



Output Electrical Characteristics and Operating Conditions

Table 28: Differential AC Output Parameters

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
AC Differential Cross-Point Voltage	$V_{OX}(AC)$	0.50 x $V_{DD}Q$ - 125	0.50 x $V_{DD}Q$ + 125	mV	1
AC Differential Voltage Swing	V_{SWING}	1.0		mV	

NOTE:

1. The typical value of $V_{OX}(AC)$ is expected to be about 0.5 x $V_{DD}Q$ of the transmitting device and V_{OX} (AC) is expected to track variations in $V_{DD}Q$. $V_{OX}(AC)$ indicates the voltage at which differential output signals must cross.

Figure 81: Differential Output Signal Levels

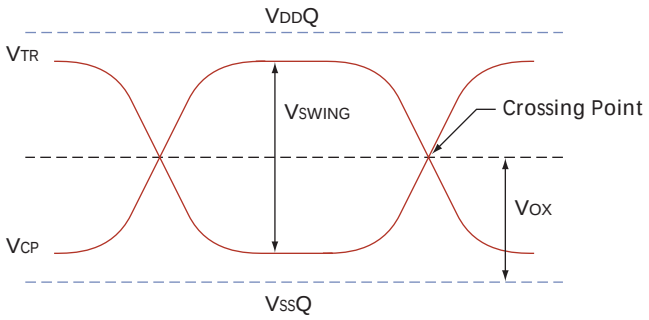


Table 29: Output DC Current Drive

PARAMETER	SYMBOL	VALUE	UNITS	NOTES
Output Minimum Source DC Current	I_{OH}	-13.4	mA	1,3,4
Output Minimum Sink DC Current	I_{OL}	13.4	mA	2,3,4

NOTE:

1. For I_{OH} (DC); $V_{DD}Q$ = 1.7V, V_{OUT} = 1420mV. (V_{OUT} - $V_{DD}Q$)/I_{OH} must be less than 21Ω for values of V_{OUT} between $V_{DD}Q$ and $V_{DD}Q$ - 280mV.
2. For I_{OL} (DC); $V_{DD}Q$ = 1.7V, V_{OUT} = 280mV. V_{OUT}/I_{OL} must be less than 21Ω for values of V_{OUT} between 0V and 280mV.
3. The DC value of V_{REF} applied to the receiving device is set to V_{TT}.
4. The values of I_{OH} (DC) and I_{OL} (DC) are based on the conditions given in Notes 1 and 2. They are used to test device drive current capability to ensure V_{IH} (MIN) plus a noise margin and V_{IL} (MAX) minus a noise margin are delivered to an SSTL_18 receiver. The actual current values are derived by shifting the desired driver operating point (See output IV curves) along a 21Ω load line to define a convenient driver current for measurement.

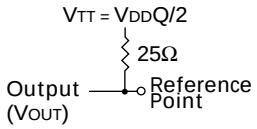
Table 30: Output Characteristics

PARAMETER	SYMBOL	MIN	NOM	MAX	UNITS	NOTES
Output impedance		12.6	18	23.4	Ω	1,2
Pull-up and Pull-down mismatch		0		4	Ω	1,2,3
Output slew rate		1.5		5	V/ns	1,4,5

NOTE:

1. Absolute specifications: 0°C ≤ T_{case} ≤ +85°C; $V_{DD}Q$ = +1.8V ±0.1V, V_{DD} = +1.8V ±0.1V.
2. Impedance measurement condition for output source DC current: $V_{DD}Q$ = 1.7V; V_{OUT} = 1420mV; (V_{OUT} - $V_{DD}Q$)/I_{OH} must be less than 23.4Ω for values of V_{OUT} between $V_{DD}Q$ and $V_{DD}Q$ - 280mV. Impedance measurement condition for output sink DC current: $V_{DD}Q$ = 1.7V; V_{OUT} = 280mV; V_{OUT}/I_{OL} must be less than 23.4Ω for values of V_{OUT} between 0V and 280mV.
3. Mismatch is absolute value between pull-up and pull-down, both are measured at same temperature and voltage.
4. Output slew rate for falling and rising edges is measured between V_{TT} - 250mV and V_{TT} + 250mV for single ended signals. For differential signals (e.g. DQS - DQS#) output slew rate is measured between DQS - DQS# = -500mV and DQS# - DQS = +500mV. Output slew rate is guaranteed by design, but is not necessarily tested on each device.
5. The absolute value of the slew rate as measured from V_{IL} (DC)MAX to V_{IH} (DC) MIN is equal to or greater than the slew rate as measured from V_{IL} (AC) MAX to V_{IH} (AC) MIN. This is guaranteed by design and characterization.

Figure 82: Output Slew Rate Load



Full Strength Pull-Down Driver Characteristics

Figure 83: Full Strength Pull-Down Characteristics

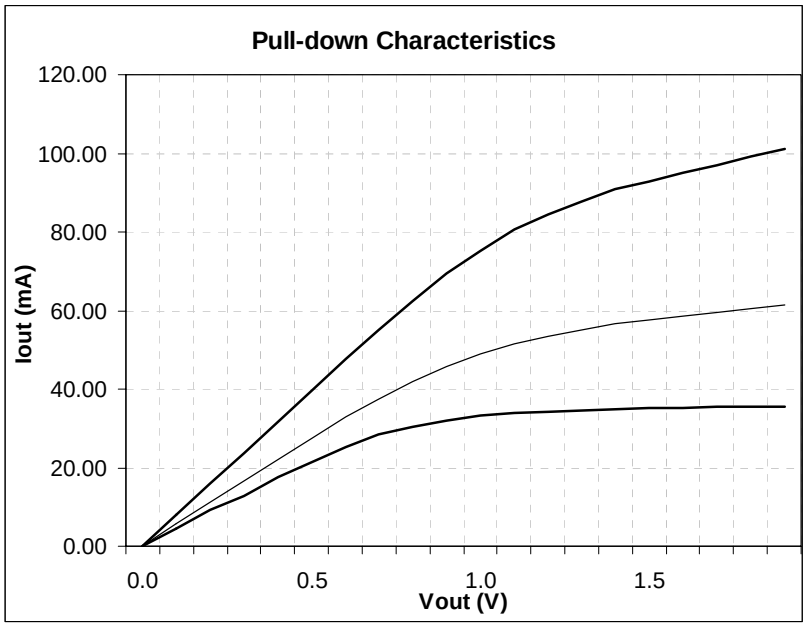


Table 31: Pulldown Current (mA)

VOLTAGE (V)	MINIMUM	NOMINAL	MAXIMUM
0.0	0.00	0.00	0.00
0.1	4.3	5.63	7.95
0.2	8.6	11.3	15.90
0.3	12.9	16.52	23.85
0.4	16.9	22.19	31.80
0.5	20.4	27.59	39.75
0.6	23.28	32.39	47.70
0.7	25.44	36.45	55.55
0.8	26.79	40.38	62.95
0.9	27.67	44.01	69.55
1.0	28.38	47.01	75.35
1.1	28.96	49.63	80.35
1.2	29.46	51.71	84.55
1.3	29.90	53.32	87.95
1.4	30.29	54.9	90.70
1.5	30.65	56.03	93.00
1.6	30.98	57.07	95.05
1.7	31.31	58.16	97.05
1.8	31.64	59.27	99.05
1.9	31.96	60.35	101.05

Full Strength Pull-Up Driver Characteristics

Figure 84: Full Strength Pull-up Characteristics

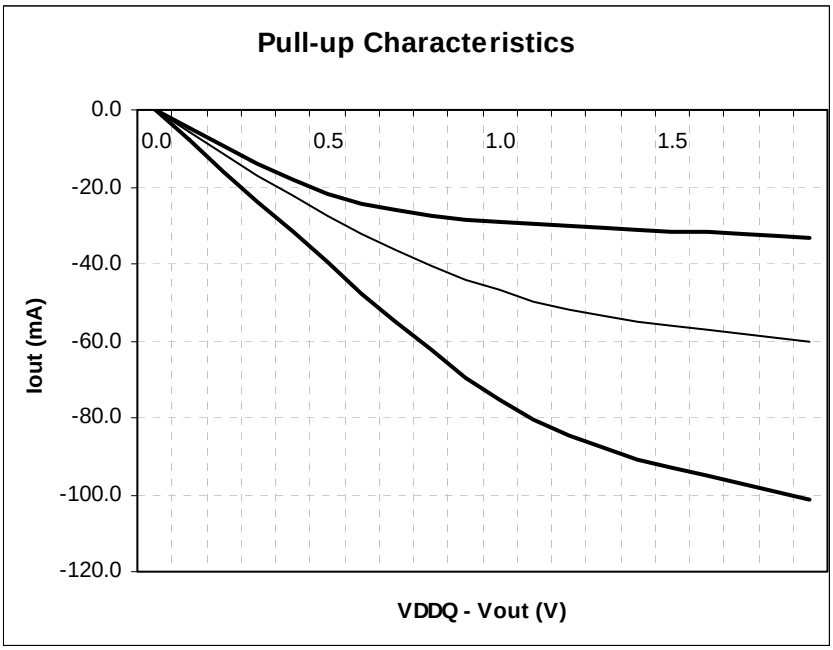


Table 32: Pull-Up Current (mA)

VOLTAGE (V)	MINIMUM	NOMINAL	MAXIMUM
0.0	0.00	0.00	-0.00
0.1	-4.3	-5.63	-7.95
0.2	-8.6	-11.3	-15.90
0.3	-12.9	-16.52	-23.85
0.4	-16.9	-22.19	-31.80
0.5	-20.4	-27.59	-39.75
0.6	-23.28	-32.39	-47.70
0.7	-25.44	-36.45	-55.55
0.8	-26.79	-40.38	-62.95
0.9	-27.67	-44.01	-69.55
1.0	-28.38	-47.01	-75.35
1.1	-28.96	-49.63	-80.35
1.2	-29.46	-51.71	-84.55
1.3	-29.90	-53.32	-87.95
1.4	-30.29	-54.90	-90.70
1.5	-30.65	-56.03	-93.00
1.6	-30.98	-57.07	-95.05
1.7	-31.31	-58.16	-97.05
1.8	-31.64	-59.27	-99.05
1.9	-31.96	-60.35	-101.05

FBGA Package Capacitance

Table 33: Input Capacitance

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: CK, CK#	CCK	1.0	2.0	pF	1
Delta Input Capacitance: CK, CK#	CDCK	–	0.25	pF	2
Input Capacitance: BA1-BA0, A0-A13 (A12 x16), CS#, RAS#, CAS#, WE#, CKE, ODT	CI	1.0	2.0	pF	1
Delta Input Capacitance: BA1-BA0, A0-A13 (A12 x16), CS#, RAS#, CAS#, WE#, CKE, ODT	CDI	–	0.25	pF	2
Input/Output Capacitance: DQs, DQS, DM, NF	CIO	2.5	4.0	pF	1
Delta Input/Output Capacitance: DQs, DQS, DM, NF	CDIO	–	0.5	pF	3

NOTE:

1. This parameter is sampled. V_{DD} = +1.8V ±0.1V, $V_{DD}Q$ = +1.8V ±0.1V, V_{REF} = V_{SS}, f = 100 MHz, T_{CASE} = 25°C, V_{OUT} (DC) = $V_{DD}Q/2$, V_{OUT} (peak to peak) = 0.1V. DM input is grouped with I/O pins, reflecting the fact that they are matched in loading.
2. The input capacitance per pin group will not differ by more than this maximum amount for any given device.
3. The I/O capacitance per DQS and DQ byte/group will not differ by more than this maximum amount for any given device.

IDD Specifications and Conditions

Table 34: DDR2 IDD Specifications and Conditions

Notes: 1–5; notes appear on page 95.

PARAMETER/CONDITION	SYMBOL	CONFIG	-37E	-5E	UNITS
Operating one bank active-precharge current; $^{t}CK = {}^{t}CK$ (IDD), $^{t}RC = {}^{t}RC$ (IDD), $^{t}RAS = {}^{t}RAS$ MIN (IDD); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	IDD0	x4, x8	80	80	mA
		x16	110	110	
Operating one bank active-read-precharge current; IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; $^{t}CK = {}^{t}CK$ (IDD), $^{t}RC = {}^{t}RC$ (IDD), $^{t}RAS = {}^{t}RAS$ MIN (IDD), $^{t}RCD = {}^{t}RCD$ (IDD); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W.	IDD1	x4, x8	95	90	mA
		x16	130	125	
Precharge power-down current; All banks idle; $^{t}CK = {}^{t}CK$ (IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.	IDD2P	x4, x8, x16	5	5	mA
Precharge quiet standby current; All banks idle; $^{t}CK = {}^{t}CK$ (IDD); CKE is HIGH, CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.	IDD2Q	x4, x8	40	35	mA
		x16	45	40	
Precharge standby current; All banks idle; $^{t}CK = {}^{t}CK$ (IDD); CKE is HIGH, CS# is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	IDD2N	x4, x8	45	40	mA
		x16	50	45	
Active power-down current; All banks open; $^{t}CK = {}^{t}CK$ (IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.	IDD3P	Fast PDN Exit MR[12] = 0	25	20	mA
		Slow PDN Exit MR[12] = 1	5	5	
Active standby current; All banks open; $^{t}CK = {}^{t}CK$(IDD), $^{t}RAS = {}^{t}RAS$ MAX (IDD), $^{t}RP = {}^{t}RP$(IDD); CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	IDD3N	x4, x8	45	40	mA
		x16	55	50	
Operating burst write current; All banks open, Continuous burst writes; BL = 4, CL = CL (IDD), AL = 0; $^{t}CK = {}^{t}CK$ (IDD), $^{t}RAS = {}^{t}RAS$ MAX (IDD), $^{t}RP = {}^{t}RP$ (IDD); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	IDD4W	x4, x8	130	110	mA
		x16	190	150	
Operating burst read current; All banks open, Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; $^{t}CK = {}^{t}CK$ (IDD), $^{t}RAS = {}^{t}RAS$ MAX (IDD), $^{t}RP = {}^{t}RP$ (IDD); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	IDD4R	x4, x8	145	115	mA
		x16	195	155	
Burst refresh current; $^{t}CK = {}^{t}CK$ (IDD); Refresh command at every ^{t}RFC (IDD) interval; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	IDD5	x4, x8	200	190	mA
		x16	210	200	

Table 34: DDR2 IDD Specifications and Conditions (Continued)

Notes: 1–5; notes appear on page 95.

PARAMETER/CONDITION	SYMBOL	CONFIG	-37E	-5E	UNITS
Self refresh current; CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING.	IDD6	x4, x8, x16	5	5	mA
Operating bank interleave read current; All bank interleaving reads, IOUT= 0mA; BL = 4, CL = CL (IDD), AL = tRCD (IDD)-1 x tCK (IDD); tCK = tCK (IDD), tRC = tRC(IDD), tRRD = tRRD(IDD), tRCD = tRCD(IDD); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data bus inputs are SWITCHING; See IDD7 Conditions for detail.	IDD7	x4, x8	260	230	mA
		x16	315	280	

NOTE:

1. IDD specifications are tested after the device is properly initialized. 0°C ≤ T_{CASE} ≤ 85°C.
   VDD = +1.8V ±0.1V, VDDQ = +1.8V ±0.1V, VDDL= +1.8V ±0.1V, VREF=VDDQ/2.
2. Input slew rate is specified by AC Parametric Test Conditions.
3. IDD parameters are specified with ODT disabled.
4. Data bus consists of DQ, DM, DQS, DQS#, RDQS, RDQS#, LDQS, LDQS#, UDQS, and UDQS#. IDD values must be met with all combinations of EMR bits 10 and 11.
5. Definitions for IDD Conditions:
   LOW is defined as VIN ≤ VIL (AC) (MAX).
   HIGH is defined as VIN ≥ VIH (AC) (MIN).
   STABLE is defined as inputs stable at a HIGH or LOW level.
   FLOATING is defined as inputs at VREF = VDDQ/2.
   SWITCHING is defined as inputs changing between HIGH and LOW every other clock cycle (once per two clocks) for address and control signals.
   Switching is defined as inputs changing between HIGH and LOW every other data transfer (once per clock) for DQ signals not including masks or strobes.

Table 35: General IDD Parameters

IDD PARAMETER	-37E	-5E	UNITS
CL (IDD)	4	3	tCK
tRCD (IDD)	15	15	ns
tRC (IDD)	60	55	ns
tRRD (IDD) - x4/x8	7.5	7.5	ns
tRRD (IDD) - x16	10	10	ns
tCK (IDD)	3.75	5	ns
tRAS MIN (IDD)	45	40	ns
tRAS MAX (IDD)	70,000	70,000	ns
tRP (IDD)	15	15	ns
tRFC (IDD)	127.5	127.5	ns

IDD7 Conditions

The detailed timings are shown below for IDD7. Changes will be required if timing parameter changes are made to the specification.

Table 36: IDD7 Timing Patterns

All Bank Interleave Read operation

SPEED GRADE	IDD7 TIMING PATTERNS FOR x4/x8/x16
-5E	A0 RA0 A1 RA1 A2 RA2 A3 RA3 D D D D
-37E	A0 RA0 D A1 RA1 D A2 RA2 D A3 RA3 D D D D D

NOTE:

1. Legend: A = active; RA = read auto precharge; D = deselect.
2. All banks are being interleaved at minimum ^{t}RC (IDD) without violating ^{t}RRD (IDD) using a burst length of 4.
3. Control and address bus inputs are STABLE during DESELECTs.
4. IOUT = 0mA.

Table 37: AC Operating Conditions (Sheet 1 of 4)

Notes: 1–5; notes appear on page 101; 0°C ≤ T_{case} ≤ +85°C; VDDQ = +1.8V ±0.1V, VDD = +1.8V ±0.1V

AC CHARACTERISTICS				-37E		-5E			
PARAMETER			SYMBOL	MIN	MAX	MIN	MAX	UNITS	NOTES
Clock	Clock cycle time	CL = 4	^tCK (4)	3,750	8,000	5,000	8,000	ps	16, 25
		CL = 3	^tCK (3)	5,000	8,000	5,000	8,000	ps	16, 25
	CK high-level width		^tCH	0.45	0.55	0.45	0.55	^tCK	19
	CK low-level width		^tCL	0.45	0.55	0.45	0.55	^tCK	19
	Half clock period		^tHP	MIN (^tCH, ^tCL)		MIN (^tCH, ^tCL)		ps	20
	Clock jitter		^tJIT	TBD	TBD	TBD	TBD	ps	18
Data	DQ output access time from CK/CK#		^tAC	-500	+500	-600	+600	ps	
	Data-out high-impedance window from CK/CK#		^tHZ		^tAC MAX		^tAC MAX	ps	8, 9
	Data-out low-impedance window from CK/CK#		^tLZ	^tAC MIN	^tAC MAX	^tAC MIN	^tAC MAX	ps	8, 10
	DQ and DM input setup time relative to DQS		^tDS_a	350		400		ps	7, 15, 22
	DQ and DM input hold time relative to DQS		^tDH_a	350		400		ps	7, 15, 22
	DQ and DM input setup time relative to DQS		^tDS_b	100		150		ps	7, 15, 22
	DQ and DM input hold time relative to DQS		^tDH_b	225		275		ps	7, 15, 22
	DQ and DM input pulse width (for each input)		^tDIPW	0.35		0.35		^tCK	
	Data hold skew factor		^tQHS		400		450	ps	
	DQ–DQS hold, DQS to first DQ to go nonvalid, per access		^tQH	^tHP -^tQHS		^tHP -^tQHS		ps	15, 17
	Data valid output window (DVW)		^tDVW	^tQH - ^tDQSQ		^tQH - ^tDQSQ		ns	15, 17

Table 37: AC Operating Conditions (Sheet 2 of 4)

Notes: 1–5; notes appear on page 101; 0°C ≤ T_{case} ≤ +85°C; VDDQ = +1.8V ±0.1V, VDD = +1.8V ±0.1V

AC CHARACTERISTICS			-37E		-5E			
PARAMETER		SYMBOL	MIN	MAX	MIN	MAX	UNITS	NOTES
Data Strobe	DQS input high pulse width	$^{t}DQSH$	0.35		0.35		^{t}CK	
	DQS input low pulse width	$^{t}DQSL$	0.35		0.35		^{t}CK	
	DQS output access time from CK/CK#	$^{t}DQSCK$	-450	+450	-500	+500	ps	
	DQS falling edge to CK rising – setup time	^{t}DSS	0.2		0.2		^{t}CK	
	DQS falling edge from CK rising – hold time	^{t}DSH	0.2		0.2		^{t}CK	
	DQS–DQ skew, DQS to last DQ valid, per group, per access	$^{t}DQSQ$		300		350	ps	15, 17
	DQS read preamble	$^{t}RPRE$	0.9	1.1	0.9	1.1	^{t}CK	36
	DQS read postamble	$^{t}RPST$	0.4	0.6	0.4	0.6	^{t}CK	36
	DQS write preamble setup time	$^{t}WPRES$	0		0		ps	12, 13
	DQS write preamble	$^{t}WPRE$	0.25		0.25		^{t}CK	
	DQS write postamble	$^{t}WPST$	0.4	0.6	0.4	0.6	^{t}CK	11
	Write command to first DQS latching transition	$^{t}DQSS$	WL - 0.25	WL + 0.25	WL - 0.25	WL + 0.25	^{t}CK	

Table 37: AC Operating Conditions (Sheet 3 of 4)

Notes: 1–5; notes appear on page 101; 0°C ≤ T_{case} ≤ +85°C; VDDQ = +1.8V ±0.1V, VDD = +1.8V ±0.1V

AC CHARACTERISTICS			-37E		-5E			
PARAMETER		SYMBOL	MIN	MAX	MIN	MAX	UNITS	NOTES
Command and Address	Address and control input pulse width for each input	^tIPW	0.6		0.6		^tCK	
	Address and control input setup time	^tIS_a	500		600			6, 22
	Address and control input hold time	^tIH_a	500		600			6, 22
	Address and control input setup time	^tIS_b	250		350			6, 22
	Address and control input hold time	^tIH_b	375		475			6, 22
	CAS# to CAS# command delay	^tCCD	2		2		^tCK	
	ACTIVE to ACTIVE (same bank) command	^tRC	55		55		ns	34
	ACTIVE bank *a* to ACTIVE bank *b* command	^tRRD (x4, x8)	7.5		7.5		ns	28
		^tRRD (x16)	10		10		ns	28
	ACTIVE to READ or WRITE delay	^tRCD	15		15		ns	
	Four Bank Activate period	^tFAW (x4, x8)	37.5		37.5		ns	31
	Four Bank Activate period	^tFAW (x16)	50		50		ns	31
	ACTIVE to PRECHARGE command	^tRAS	40	70,000	40	70,000	ns	21, 34
	Internal READ to precharge command delay	^tRTP	7.5		7.5		ns	24, 28
	Write recovery time	^tWR	15		15		ns	28
	Auto precharge write recovery + precharge time	^tDAL	$^tWR + ^tRP$		$^tWR + ^tRP$		ns	23
	Internal WRITE to READ command delay	^tWTR	7.5		10		ns	28
	PRECHARGE command period	^tRP	15		15		ns	32
	PRECHARGE ALL command period	^tRPA	$^tRP + ^tCK$		$^tRP + ^tCK$		ns	32
	LOAD MODE command cycle time	^tMRD	2		2		^tCK	
	CKE low to CK,CK# uncertainty	^tDELAY	4.375	4.375	5.83	5.83	ns	29
Refresh	REFRESH to Active or Refresh to Refresh command interval	^tRFC	105	70,000	105	70,000	ns	14
	Average periodic refresh interval	^tREFI		7.8		7.8	µs	14

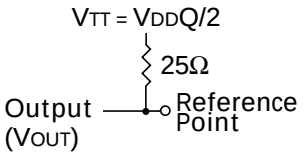
Table 37: AC Operating Conditions (Sheet 4 of 4)

Notes: 1–5; notes appear on page 101; 0°C ≤ T_{case} ≤ +85°C; VDDQ = +1.8V ±0.1V, VDD = +1.8V ±0.1V

AC CHARACTERISTICS			-37E		-5E			
PARAMETER		SYMBOL	MIN	MAX	MIN	MAX	UNITS	NOTES
Self Refresh	Exit self refresh to non-READ command	^{t}XSNR	^{t}RFC (MIN) + 10		^{t}RFC (MIN) + 10		ns	
	Exit self refresh to READ command	^{t}XSRD	200		200		^{t}CK	
	Exit self refresh timing reference	^{t}ISXR	250		350		ps	6, 30
ODT	ODT turn-on delay	^{t}AOND	2	2	2	2	^{t}CK	
	ODT turn-on	^{t}AON	^{t}AC (MIN)	^{t}AC (MAX) + 1,000	^{t}AC (MIN)	^{t}AC (MAX) + 1000	ps	26
	ODT turn-off delay	^{t}AOFD	2.5	2.5	2.5	2.5	^{t}CK	
	ODT turn-off	^{t}AOF	^{t}AC (MIN)	^{t}AC (MAX) + 600	^{t}AC (MIN)	^{t}AC (MAX) + 600	ps	27
	ODT turn-on (power-down mode)	^{t}AONPD	^{t}AC (MIN) + 2000	2 x ^{t}CK + ^{t}AC (MAX) + 1,000	^{t}AC (MIN) + 2,000	2 x ^{t}CK + ^{t}AC (MAX) + 1000	ps	
	ODT turn-off (power-down mode)	^{t}AOFPD	^{t}AC (MIN) + 2,000	2.5 x ^{t}CK + ^{t}AC (MAX) + 1,000	^{t}AC (MIN) + 2,000	2.5 x ^{t}CK + ^{t}AC (MAX) + 1,000	ps	
	ODT to power-down entry latency	^{t}ANPD	3		3		^{t}CK	
	ODT power-down exit latency	^{t}AXPD	8		8		^{t}CK	
Power-Down	Exit active power-down to READ command, MR[bit12=0]	^{t}XARD	2		2		tCK	
	Exit active power-down to READ command, MR[bit12=1]	^{t}XARDS	6 - AL		6 - AL		^{t}CK	
	Exit precharge power-down to any non-READ command.	^{t}XP	2		2		^{t}CK	
	Exit precharge power-down to READ command.	^{t}XPRD	6 - AL		6 - AL		^{t}CK	
	CKE minimum high/low time	^{t}CKE	3		3		^{t}CK	35

Notes

1. All voltages referenced to V_{SS}.
2. Tests for AC timing, I_{DD}, and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. Outputs measured with equivalent load:



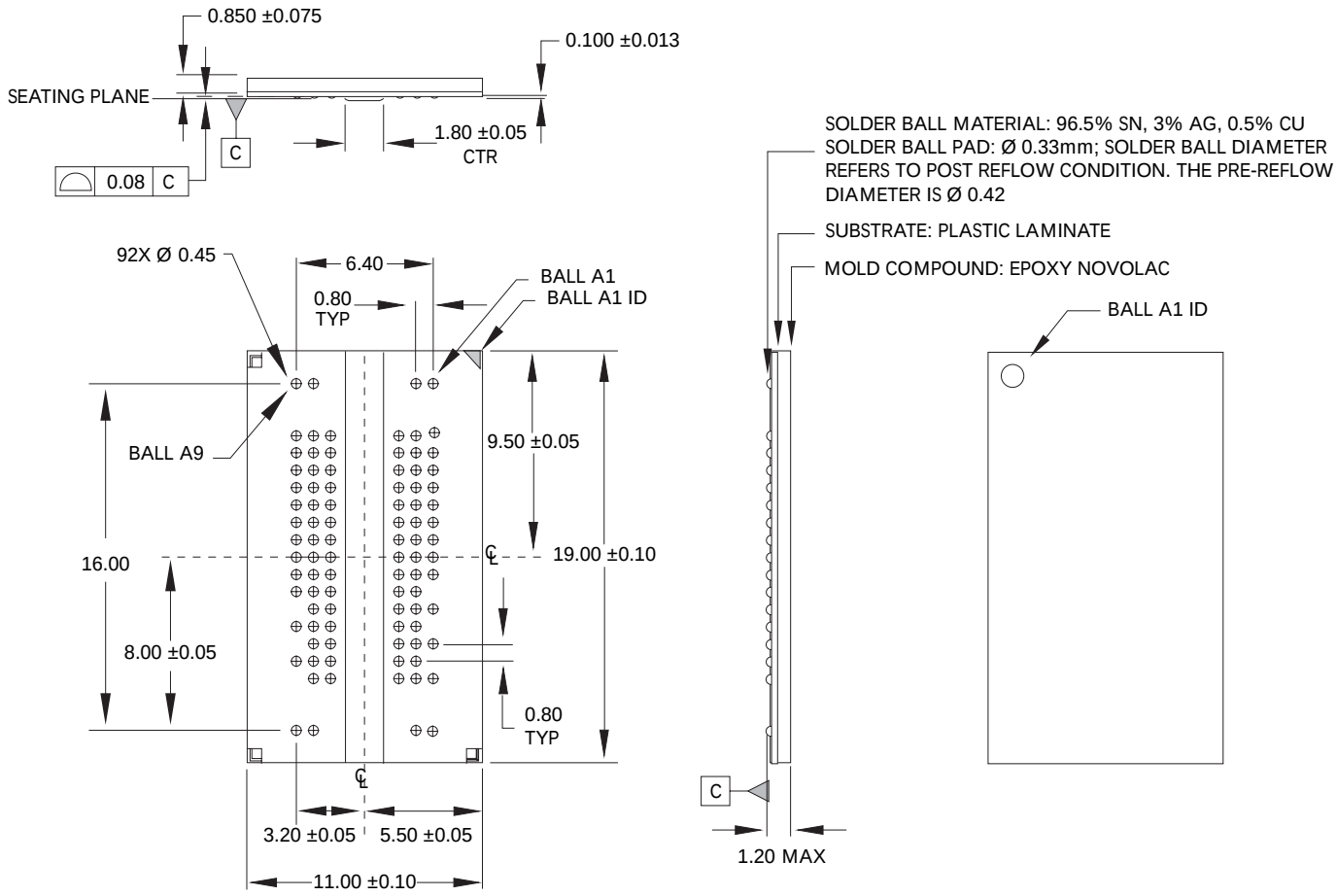
4. AC timing and I_{DD} tests may use a V_{IL}-to-V_{IH} swing of up to 1.0V in the test environment and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 1.0V/ns for signals in the range between V_{IL} (AC) and V_{IH} (AC). Slew rates less than 1.0V/ns require the timing parameters to be derated as specified.
5. The AC and DC input level specifications are as defined in the SSTL_18 standard (i.e., the receiver will effectively switch as a result of the signal crossing the AC input level and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [HIGH] level).
6. Command/Address minimum input slew rate is at 1.0V/ns. Command/Address input timing must be derated if the slew rate is not 1.0V/ns. This is easily accommodated using $^{t}IS_{b}$ and the Setup and Hold Time Derating Values table. ^{t}IS timing ($^{t}IS_{b}$) is referenced from V_{IH}(AC) for a rising signal and V_{IL}(AC) for a falling signal. ^{t}IH timing ($^{t}IH_{b}$) is referenced from V_{IH}(AC) for a rising signal and V_{IL}(DC) for a falling signal. The timing table also lists the $^{t}IS_{b}$ and $^{t}IH_{b}$ values for a 1.0V/ns slew rate; these are the "base" values.
7. Data minimum input slew rate is at 1.0V/ns. Data input timing must be derated if the slew rate is not 1.0V/ns. This is easily accommodated if the timing is referenced from the logic trip points. ^{t}DS timing ($^{t}DS_{b}$) is referenced from V_{IH}(AC) for a rising signal and V_{IL}(AC) for a falling signal. ^{t}IH timing ($^{t}IH_{b}$) is referenced from V_{IH}(DC) for a rising signal and V_{IL}(DC) for a falling signal. The timing table lists the $^{t}DS_{b}$ and $^{t}DH_{b}$ values for a 1.0V/ns slew rate.

   If the DQS/DQS# differential strobe feature is not enabled, timing is no longer referenced to the crosspoint of DQS/DQS#. Data timing is now referenced to V_{REF}, provided the DQS slew rate is not less than 1.0V/ns. If the DQS slew rate is less than 1.0V/ns, then data timing is now referenced to V_{IH}(AC) for a rising DQS and V_{IL}(DC) for a falling DQS.
8. ^{t}HZ and ^{t}LZ transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (^{t}HZ) or begins driving (^{t}LZ).
9. This maximum value is derived from the referenced test load. ^{t}HZ (MAX) will prevail over $^{t}DQSCK$ (MAX) + $^{t}RPST$ (MAX) condition.
10. ^{t}LZ (MIN) will prevail over a $^{t}DQSCK$ (MIN) + $^{t}RPRE$ (MAX) condition.
11. The intent of the Don't Care state after completion of the postamble is the DQS-driven signal should either be high, low or High-Z and that any signal transition within the input switching region must follow valid input requirements. That is if DQS transitions high (above V_{IH}DC(min) then it must not transition low (below V_{IH}(DC) prior to $^{t}DQSH$(min).
12. This is not a device limit. The device will operate with a negative value, but system performance could be degraded due to bus turnaround.
13. It is recommended that DQS be valid (HIGH or LOW) on or before the WRITE command. The case shown (DQS going from High-Z to logic LOW) applies when no WRITEs were previously in progress on the bus. If a previous WRITE was in progress, DQS could be HIGH during this time, depending on $^{t}DQSS$.
14. The refresh period is 64ms. This equates to an average refresh rate of 7.8125µs. However, a REFRESH command must be asserted at least once every 70.3µs or ^{t}RFC (MAX). To ensure all rows of all banks are properly refreshed, 8192 REFRESH commands must be issued every 64ms.
15. Referenced to each output group: x4 = DQS with DQ0-DQ3; x8 = DQS with DQ0–DQ7; x16 = LDQS with DQ0–DQ7; and UDQS with DQ8–DQ15.
16. CK and CK# input slew rate must be ≥ 1V/ns (≥ 2 V/ns if measured differentially).
17. The data valid window is derived by achieving other specifications - ^{t}HP. ($^{t}CK/2$), $^{t}DQSQ$, and

^{t}QH(^{t}QH=^{t}HP-^{t}QHS). The data valid window derates in direct proportion to the clock duty cycle and a practical data valid window can be derived.

18. ^{t}JIT specification is currently TBD.
19. MIN(^{t}CL, ^{t}CH) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. This value can be greater than the minimum specification limits for ^{t}CL and ^{t}CH). For example, ^{t}CL and ^{t}CH are = 50 percent of the period, less the half period jitter [^{t}JIT(HP)] of the clock source, and less the half period jitter due to cross talk [^{t}JIT(cross talk)] into the clock traces.
20. ^{t}HP (MIN) is the lesser of ^{t}CL minimum and ^{t}CH minimum actually applied to the device CK and CK# inputs.
21. READs and WRITEs with auto precharge *are* allowed to be issued before ^{t}RAS (MIN) is satisfied since ^{t}RAS lockout feature is supported in DDR2 SDRAM.
22. VIL/VIH DDR2 overshoot/undershoot. See "AC Overshoot/Undershoot Specification" on page 88.
23. ^{t}DAL = (nWR) + (^{t}RP/^{t}CK): For each of the terms above, if not already an integer, round to the next highest integer. ^{t}CK refers to the application clock period; nWR refers to the ^{t}WR parameter stored in the MR[11,10,9]. Example: For -37E at ^{t}CK = 3.75 ns with ^{t}WR programmed to four clocks. ^{t}DAL = 4 + (15 ns/3.75 ns) clocks = 4 +(4) clocks = 8 clocks.
24. The minimum READ to internal PRECHARGE time. This parameter is only applicable when ^{t}RTP/(2*^{t}CK) > 1. If ^{t}RTP/(2*^{t}CK) ≤ 1, then equation AL + BL/2 applies. Notwithstanding, ^{t}RAS (MIN) has to be satisfied as well. The DDR2 SDRAM will automatically delay the internal PRECHARGE command until ^{t}RAS (MIN) has been satisfied.
25. Operating frequency is only allowed to change during self refresh mode (See "Self Refresh" on page 34), precharge power-down mode (See "Power-Down Mode" on page 37), and system reset condition (see "RESET Function (CKE LOW Anytime)" on page 8.
26. ODT turn-on time ^{t}AON (MIN) is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn-on time ^{t}AON (MAX) is when the ODT resistance is fully on. Both are measured from ^{t}AOND.
27. ODT turn-off time ^{t}AOF (MIN) is when the device starts to turn off ODT resistance. ODT turn off time ^{t}AOF (MAX) is when the bus is in high impedance. Both are measured from ^{t}AOFD.
28. This parameter has a two clock minimum requirement at any ^{t}CK.
29. ^{t}DELAY is calculated from ^{t}IS + ^{t}CK + ^{t}IH so that CKE registration LOW is guaranteed prior to CK, CK# being removed in a system RESET condition. "RESET Function (CKE LOW Anytime)" on page 8.
30. ^{t}ISXR is equal to ^{t}IS and is used for CKE setup time during self refresh exit shown in Figure 31 on page 36.
31. No more than 4 bank ACTIVE commands may be issued in a given ^{t}FAW(min) period. ^{t}RRD(min) restriction still applies. The ^{t}FAW(min) parameter applies to all 8 bank DDR2 devices, regardless of the number of banks already open or closed.
32. tRPA timing applies when the PRECHARGE(ALL) command is issued, regardless of the number of banks already open or closed. If a single-bank PRECHARGE command is issued, ^{t}RP timing applies. ^{t}RPA(min) applies to all 8-bank DDR2 devices.
33. Value is minimum pulse width, not the number of clock registrations.
34. Applicable to Read cycles only. Write cycles generally require additional time due to Write recovery time (^{t}WR) during auto precharge.
35. ^{t}CKE (MIN) of 3 clocks means CKE must be registered on three consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the 3 clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of ^{t}IS + 2 * ^{t}CK + ^{t}IH.
36. This parameter is not referenced to a specific voltage level, but specified whwen the device output is no longer driving (^{t}RPST) or beginning to drive (^{t}RPRE).

Figure 85: Package Drawing (x4,x8,x16 Configurations) 11mm x 19mm FBGA



NOTE:
All dimensions are in millimeters.

Data Sheet Designation

Preliminary: Initial characterization limits, subject to change upon full characterization of production devices.

8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-3900
E-mail: prodmktg@micron.com, Internet: http://www.micron.com, Customer Comment Line: 800-932-4992