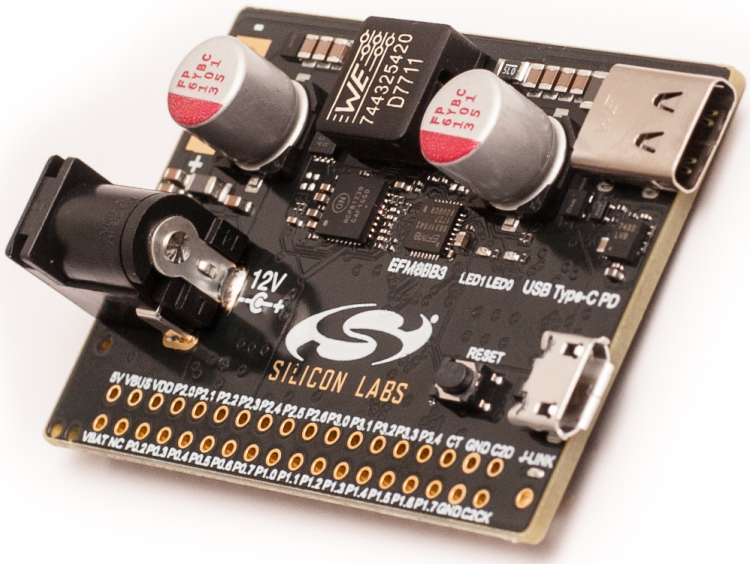
UG297: EFM8BB3 USB Type-C 60 W Charger Reference Design

SLRDK1001A is a reference design for a small and cost effective USB Type-C 60 W charger. A Silicon Labs EFM8BB3 Busy Bee microcontroller is used for USB Type-C Power Delivery (PD) negotiation.

The USB Type-C 60 W Charger Reference Design ships with a ready to use demo firmware that is capable of delivering up to 60 W output power.

An on-board SEGGER J-Link debugger enables easy customization and development.



KEY FEATURES

- EFM8BB3 Busy Bee Microcontroller
- USB Type-C Power Delivery
- 60 W output buck/boost converter supporting 5-20 V output voltage
- User LEDs/push buttons
- SEGGER J-Link on-board debugger
- Virtual COM Port
- 36 breakout pads for all I/Os

SOFTWARE SUPPORT

- Simplicity Studio™
- USB PD Libraries and Kernel

Table of Contents

1. Introduction

The SLRDK1001A USB Type-C 60 W Charger reference design showcases the EFM8BB3 Busy Bee as a USB Type-C Power Delivery (PD) controller, where it handles power contract negotiaton while interfacing an I2C controlled voltage regulator.

The voltage regulator is based on a buck boost controller IC with 4 external switching transistors, offering a conversion efficiency up to 95%. The boost converter can source up to 60 W output power (3.0 A at 20 V) for powering or charging a USB Type-C device such as a laptop, mobile phone, tablet etc.

The board is powered by an external 12 V input. For maximum output power, the external source has to be capable of delivering more than 65 W at 12 V. A DC jack connector allows for easy connection of commonly available off-the-shelf power adapters, while solder connectors offer a flexible option for connecting an input source.

To simplify application development, the board includes an on-board SEGGER J-Link debugger running on an EFM32 Giant Gecko MCU. The debugger also features a USB virtual COM port. The entire debugger design is located on the bottom side of the board so it is easy to distinguish from the actual reference design.

The board features are:

- EFM8BB3 Busy Bee USB PD controller
- 60 W buck boost converter
- 5.5 mm DC jack with 2.5 mm center pin for connecting a power adapter
- On-board J-Link debugger with a USB virtual COM port
- Area-effective design
- Breakout for all I/Os

1.1 Hardware Layout

The layout of the EFM8BB3 USB Type-C 60 W Charger Reference Design is shown below.

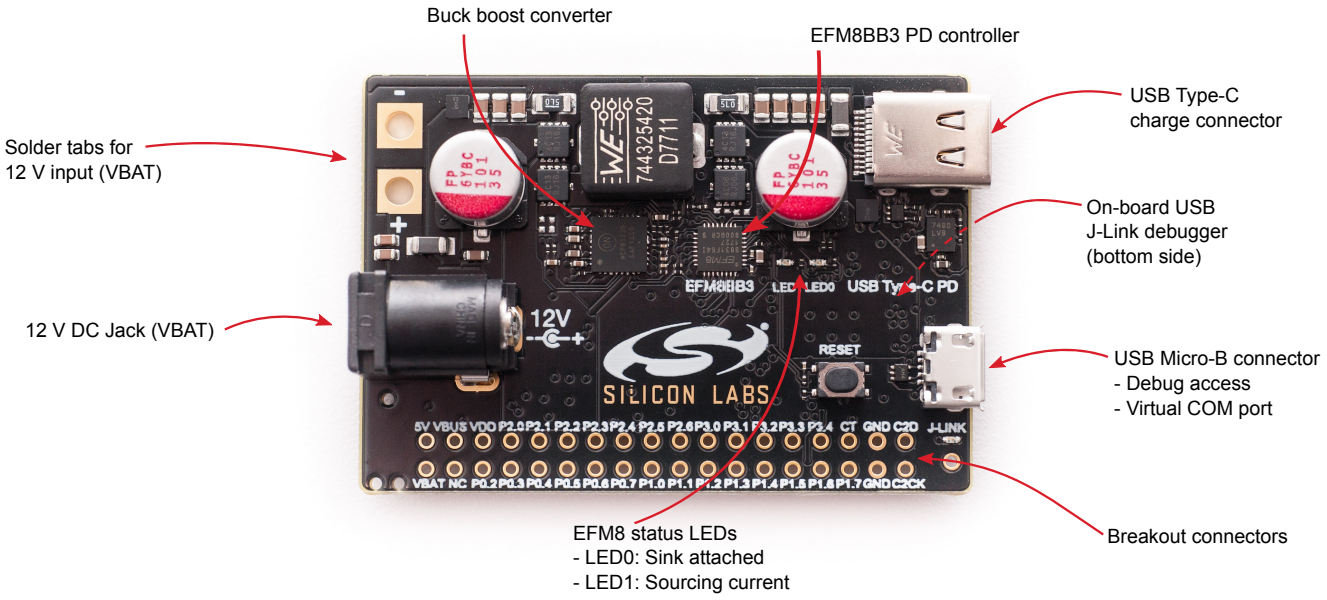


Figure 1.1. Hardware Layout

1.2 Getting Started

The USB Type-C 60 W Charger Reference Design ships with a ready to use demo firmware. Follow these steps to quickly try out the functionality of the design:

1. Connect a 12 V DC source to the DC jack connector or to the input terminals. Both LEDs will be off.
2. Connect a USB Type-C device (phone, tablet, laptop, etc.) to the board.
3. **LED0** will be on when a sink is attached. **LED1** turns on when the reference design starts sourcing current to the sink.

A more detailed description on how to get started with the USB Type-C rechargeable battery pack reference design can be found in QSG157: USB High Power Type-C 60 W Charger Reference Design Quick Start Guide. Further information can be found on the Silicon Labs web pages:

http://www.silabs.com/usb-type-c

1.3 Ordering Information

The EFM8BB3 Busy Bee USB Type-C 60 W Charger reference design can be obtained as a kit from Silicon Labs, SLRDK1001A.

Table 1.1. Ordering Information

Part Number	Description	Contents
SLRDK1001A	EFM8BB3 USB Type-C 60 W Charger Reference Design Kit	1x BRD5204A USB Type-C 60 W Charger Reference Design 1x USB 2.0 Type-C Cable 1x USB Type A to Micro-B cable

2. Hardware Description

2.1 Block Diagram

An overview of the EFM8BB3 USB Type-C 60 W Charger Reference Design is illustrated in the figure below.

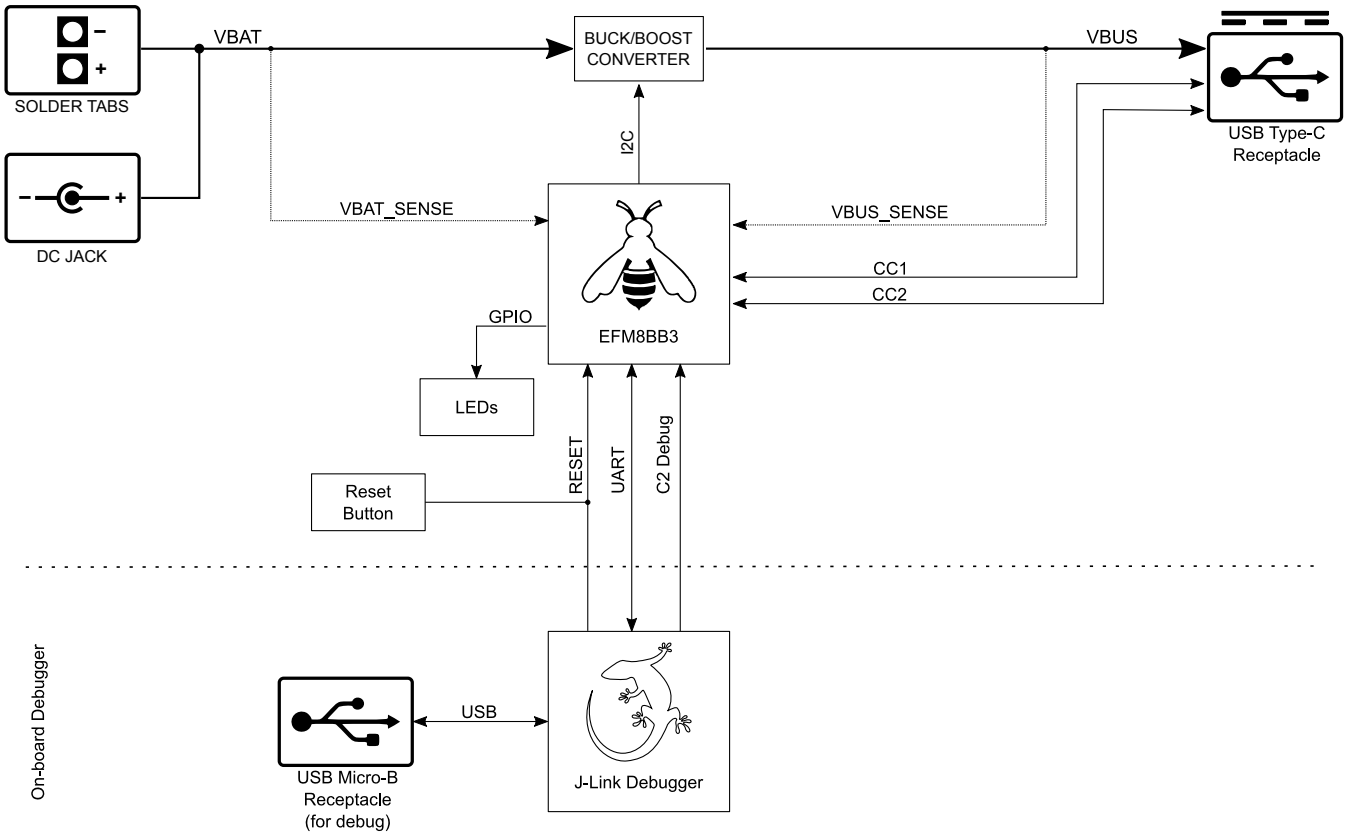


Figure 2.1. Kit Block Diagram

2.2 USB Type-C Connector

The USB Type-C connector is a charge-only port with USB Power Delivery support. It can source current, but has no data support.

When connected to another port that supports USB Power Delivery, the reference design offers maximum 60 W output power, i.e. up to 3 A current at 5 V, 9 V, 15 V and 20 V VBUS voltage. If the other port does not support USB Power Delivery, VBUS is fixed at 5 V and limited to 1.5 A.

2.2.1 USB Type-C Configuration Channel

USB Type-C feature a two-pin Configuration Channel which serves multiple purposes. Each pin has a pull-up or a pull-down resistor that are used for detecting a connection, determining plug orientation, and to identify each port as a current source or sink.

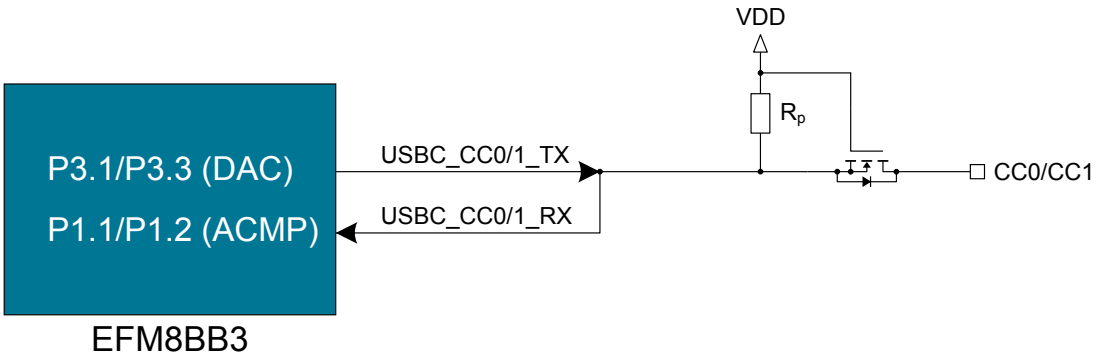


Figure 2.2. Configuration Channel

The EFM8BB3 USB Type-C 60 W Charger is a source-only, so each of the CC pins feature a pull-up resistor, R_p. A source's current capability is indicated by the value of the pull-up resistors. On SLRDK1001A, 12 kΩ pull-up resistors to 3.3 V are used, identifying it as a 5 V/1.5 A power source.

The EFM8BB3 continously monitors the voltage on Configuration Channel. When a sink is attached, its R_d pull-down will pull the channel to a lower voltage and a connection is detected. Since the USB Type-C cable itself only connects one of the CC pins through the cable, each port can determine the plug orientation based on which of the two pins the voltage change occurs.

When both ends support USB Power Delivery, the Configuration Channel is also used for negotiating a power contract between the ports. USB Power Delivery allows negotiating both the VBUS voltage and the maximum current. SLRDK1001A supports up to 60 W output power, i.e. VBUS voltages of 5 V, 9 V, 15 V and 20 V and a maximum current of 3.0 A. The USB Power Delivery communication is performed by the EFM8BB3 using the PD libraries provided by Silicon Labs.

When the charger is connected to a USB Type-C source or DRP (Dual-Role-Power) port, the other port's connection detection circuitry may apply up to 5.5 V on the CC line. If the charger is not powered by 12 V, this may lead to an overvoltage situation on the EFM8. To avoid this, an isolation transistor is added to each CC connection.

2.3 USB Micro-B Connector

The Debug USB port can be used for uploading code, debugging, and as a Virtual COM port, as described in 4. Debugging.

Note: When the board is powered from the Debug USB connector only, the NCP81239 is not powered. In this case, the EFM8BB3 can be programmed and debugged, but the converter can not be contacted over I2C, unless 12 V is also applied.

2.4 Input Voltage Connectors

For operation, the reference design requires a 12 V input voltage. The board features two ways of connecting this. A DC jack connector allows for easy connection of a standard off-the-shelf wall adapter, while solder tabs offer a flexible connection of any 12 V source.

The DC Jack is a 5.5 mm barrel connector with 2.5 mm center pin. The center pin is connected to +12 V while the sleeve is connected to ground.

Using a DC source that can supply more than 65 W / 5.5 A at 12 V is required in order to achieve the full output power.

2.5 VBUS Voltage Regulator

The VBUS voltage regulator is an I2C controlled NCP81239 4-switch buck boost controller with external switching FETs made for USB Power Delivery by ON Semiconductor. It is controlled by the EFM8BB3 through the SMBus interface.

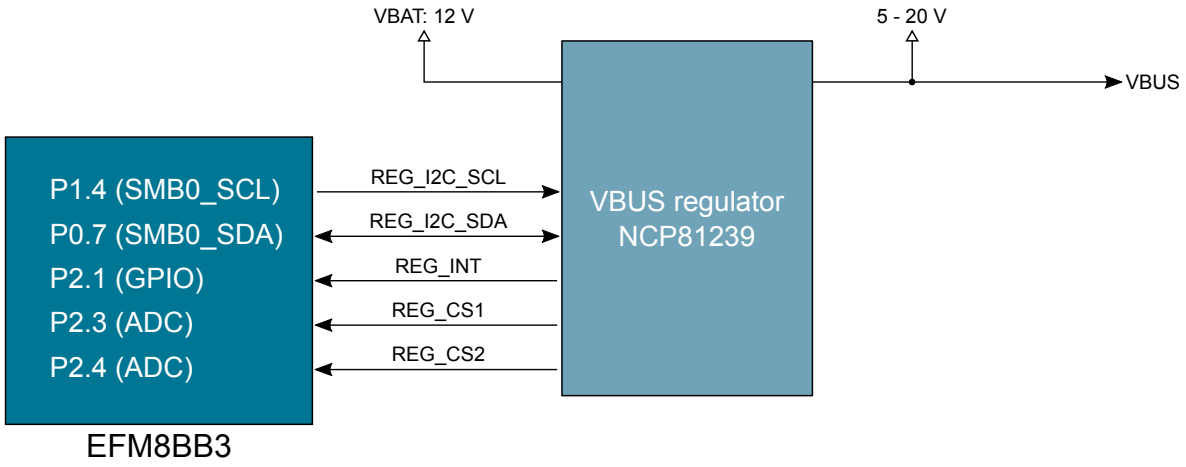


Figure 2.3. VBUS Voltage Converter Connections

The 12 V input is connected directly to the input of the boost converter, and the output is connected directly to the USB VBUS line of the Type-C connector.

The NPC81239 converter includes a current sensing circuit that can be used to monitor both the input and output current. The sensing circuit is based on a differential transconductance amplifier that converts the voltage difference over an external sense resistor to a current over an external load resistance. The voltage over the load resistance can be measured by an internal 7-bit A/D converter in the NCP81239 and read out over the I2C interface.

The EFM8BB3 built-in 12-bit ADC can also be used to measure the voltage over the load resistors. The input current is connected to P2.3, and the output current is connected to P2.4.

Table 2.1. NCP81239 Internal Current Measurement

	I_{VBAT}	I_{VBUS}
ADC Resolution	7 bits	
Conversion	$I_{VBAT} = ADC_{CS1} * 20.08\ mV / 0.6075\ \Omega$	$I_{VBUS} = ADC_{CS2} * 20.08\ mV / 0.2950\ \Omega$
1 LSB	33 mA	68 mA
Measurement range, I_{MAX}	4.2 A	8.6 A

Table 2.2. EFM8BB3 ADC Current Measurement

	I_{VBAT}	I_{VBUS}
Resolution	12 bits	
Conversion	$I_{VBAT} = ADC_{P2.3} * 0.8059\ mV / 0.6075\ \Omega$	$I_{VBUS} = ADC_{P2.4} * 0.8059\ mV / 0.2950\ \Omega$
1 LSB	1.3 mA	2.7 mA
Measurement range, I_{MAX} [1]	4.2 A	8.6 A

Note:
1. Depends on EFM8BB3 voltage reference selection

2.6 Power Supply

The EFM8BB3 and its associated circuits are powered by a 3.3 V low-dropout linear regulator (LDO) whenever 5 V is available from either the main regulator, or the USB Micro-B connector. Schottky diodes with low forward voltage drop are inserted between the LDO input and each power rail to prevent current from flowing between the sources. This topology is illustrated in the figure below and ensures that the EFM8 is powered up as long as at least one of the power sources are present.

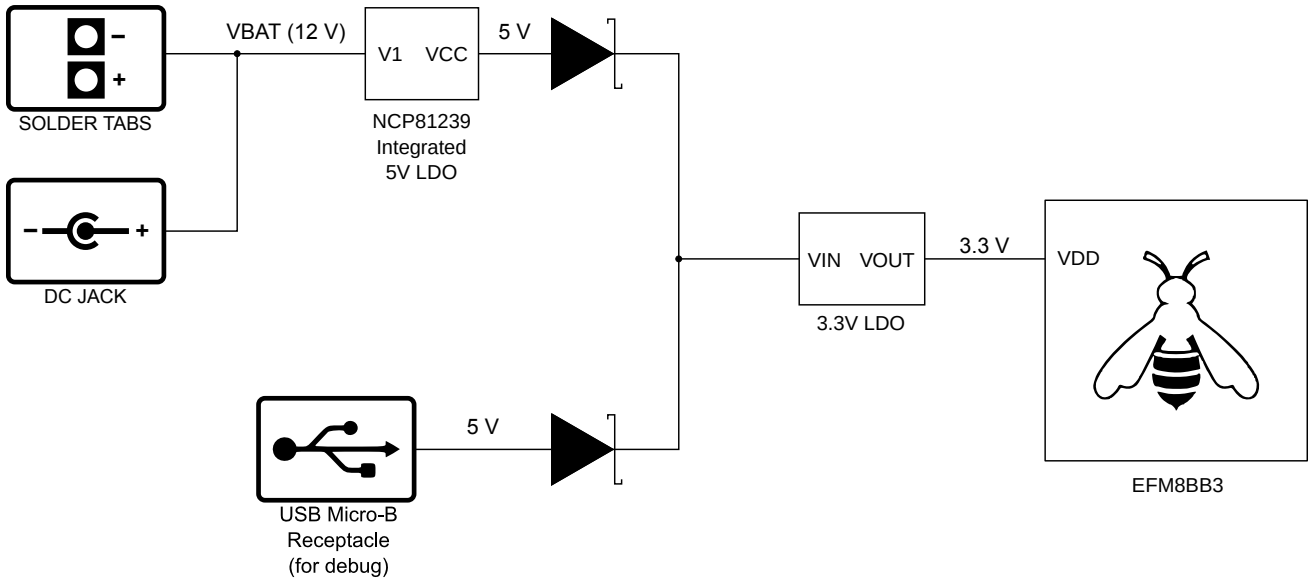


Figure 2.4. Power Supply

The output of the 3.3 V LDO is also used to power the on-board debugger circuit. However, most parts of the circuit will be powered down or in a low current state whenever the debug USB cable is not inserted in the USB Micro-B connector.

The primary 5 V comes from a built-in 5 V LDO in the NCP81239 which again is powered from the 12 V DC input. For development purposes, 5 V can also come from the debug USB connector, allowing the EFM8BB3 to be programmed also when 12 V is not connected.

Note: When the board is powered from the Debug USB connector only, the NCP81239 is not powered. In this case, the EFM8BB3 can be programmed and debugged, but the converter can not be contacted over I2C unless 12 V is also applied.

2.7 Miscellaneous

In addition to the boost converter and charge controller, the board contains some miscellaneous features:

- 2 user programmable indicator LEDs
- Voltage monitoring of battery and VBUS voltages
- RESET push button

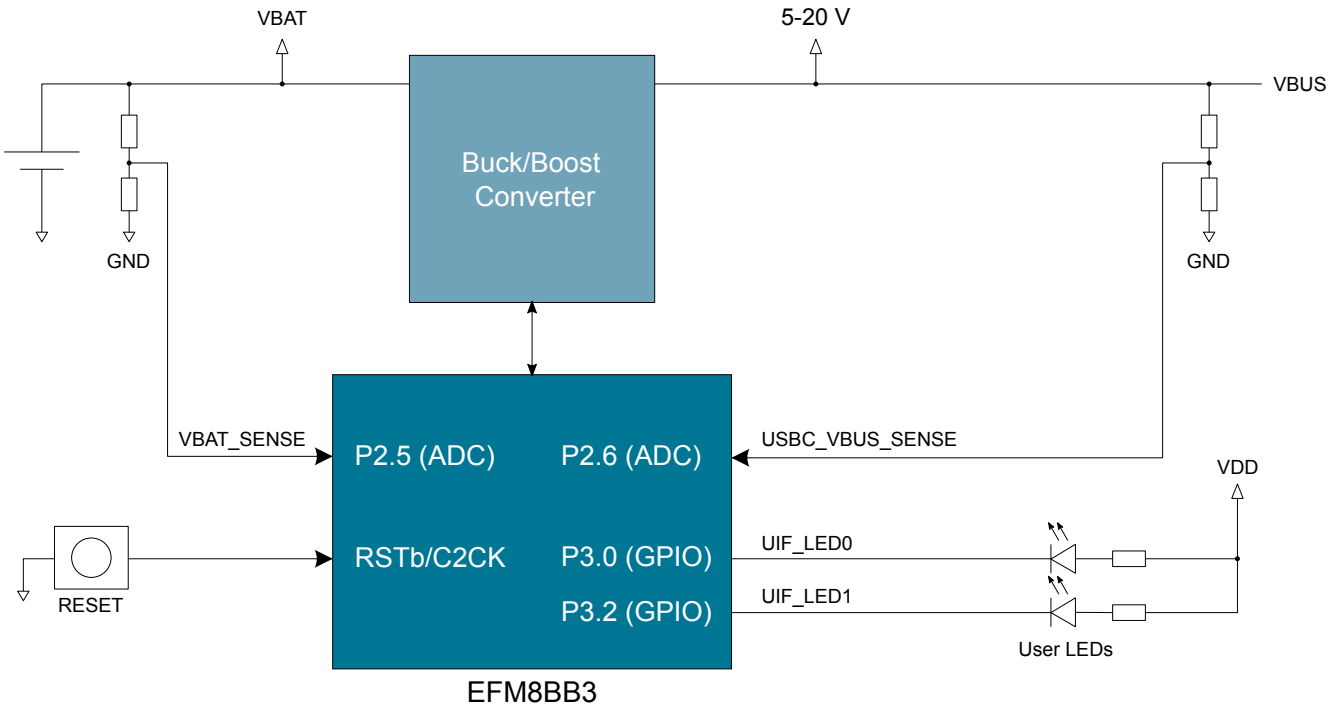


Figure 2.5. Miscellaneous Features

2.7.1 Reset Button

The board features a single button which is labeled RESET. The reset button is tied directly to the RSTb/C2CK pin of the EFM8, and a press on this button resets the microcontroller.

2.7.2 Voltage Monitoring

Resistor dividers are placed on both the input voltage net (VBAT) and the USB bus voltage net (VBUS), allowing the EFM8 firmware to measure a scaled version of these voltages using its internal ADC. VIN_SENSE (P2.5) and USBC_VBUS_SENSE (P2.6) measure these voltages scaled by 1:10.

2.8 Breakout Pads

Thirty-six breakout pads are provided for easy access to all EFM8 I/Os for monitoring and prototyping. The pads are located in two rows along the bottom edge of the board. The bottom row is named "J1", and the top row "J2". These pads enable connection of peripherals or add-on boards. Additionally, all voltage rails are also available on the breakout pads.

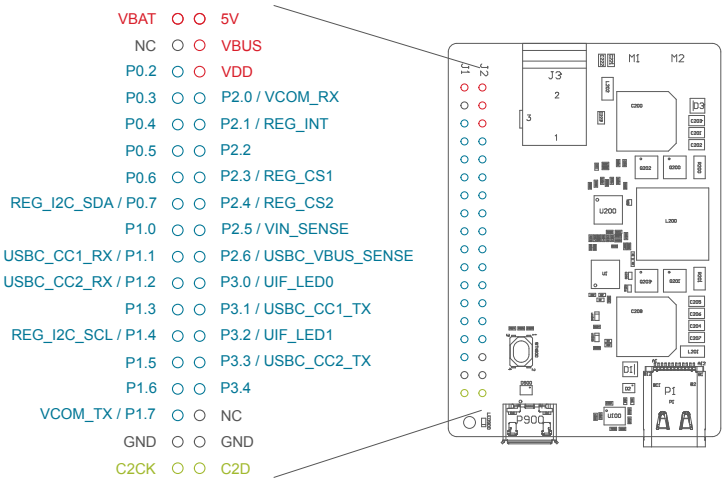


Figure 2.6. Breakout Pads

The table below includes an overview of the pin functionality on each breakout pad.

Table 2.3. Expansion Header Pinout

Pin	Function	Description
Lower Row Breakout Pins (J1)		
VBAT	Battery Voltage	Directly connected to the input battery voltage
NC	Not connected	–
P0.2	GPIO	Unused I/O
P0.3	Reserved	Used internally by PD library
P0.4	GPIO	Unused I/O
P0.5	Reserved	Used internally by PD library
P0.6	Reserved	Used internally by PD library
P0.7	REG_I2C_SDA	I2C interface to VBUS voltage regulator.
P1.0	GPIO	Unused I/O
P1.1	USBC_CC1_RX	USB Type-C configuration channel 1 receive
P1.2	USBC_CC2_RX	USB Type-C configuration channel 2 receive
P1.3	GPIO	
P1.4	REG_I2C_SCL	I2C interface to VBUS voltage regulator.
P1.5	Reserved	Used internally by PD library
P1.6	GPIO	Unused I/O
P1.7	VCOM_TX	Virtual COM Port transmit data from EFM8
GND	Ground	
C2CK	Reset/C2 clock	Reset and C2CK, connected to both RESET button and debugger

Pin	Function	Description
Upper Row Breakout Pins (J2)		
5V	5 V net	Output directly from boost converter. Input to charge controller
VBUS	USB Type-C VBUS	USB Type-C bus voltage
VDD	3.3 V	Power rail for EFM8 and on-board debugger
P2.0	VCOM_RX	Virtual COM Port receive data to EFM8
P2.1	REG_INT	Interrupt signal from VBUS voltage regulator.
P2.2	GPIO	Unused I/O
P2.3	REG_CS1	VBUS voltage regulator current sense output CS1
P2.4	REG_CS2	VBUS voltage regulator current sense output CS2
P2.5	VIN_SENSE	Input voltage sense pin: VIN * 0.099
P2.6	USBC_VBUS_SENSE	VBUS voltage sense pin: VBUS * 0.099
P3.0	UIF_LED0	General purpose indicator LED0
P3.1	USBC_CC1_TX	USB Type-C configuration channel 1 transmit
P3.2	UIF_LED1	General purpose indicator LED1
P3.3	USBC_CC2_TX	USB Type-C configuration channel 2 transmit
P3.4	GPIO	Unused I/O
NC	Not connected	
GND	Ground	
C2D	C2 Data	C2 Data for debugging of EFM8. Connected to on-board debugger.

3. Specifications

3.1 Electrical Specifications

3.1.1 Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit
DC input voltage	V_{VBAT}	-0.3		+25	V
Electrostatic discharge voltage – USB Type-C connector	V_{ESD_USB}			30	kV
Operating ambient temperature[1]	T_{AMB}	-40		+85	˚C

Note:

1. Actual limit will be less than +85˚C because of board self-heating, which again depends on output power.

3.1.2 Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
DC input voltage	V_{VBAT}	10	12	15	V
Input current [1]	I_{VBAT}	–	5.25	–	A
VBUS voltage range	V_{VBUS}	5		20	V
VBUS output voltage, 5 V	$V_{VBUS,5V}$	–	5.03	–	V
VBUS output voltage, 9 V	$V_{VBUS,9V}$	–	9.03	–	V
VBUS output voltage, 15 V	$V_{VBUS,15V}$	–	15.0	–	V
VBUS output voltage, 20 V	$V_{VBUS,20V}$	–	20.0	–	V
USB Type-C output current (without USB Power Delivery)	I_{VBUS}	–		1.5	A
5 V output voltage	V_{5V}	4.5	5		V
5 V output current[2]	I_{5V}	80	97		mA
VDD output voltage	V_{VDD}		3.3		V
VDD output current[2]	I_{VDD}	79	96		mA

Note:

1. V_{VBAT} = 12 V, V_{VBUS} = 20 V, I_{VBUS} = 3 A
2. Total output current, including board consumption.

3.2 Voltage Converter Performance

The VBUS regulator dissipates the most power when the output power is high and the input voltage is low. The table below contains efficiency measurements across input and output voltage.

Table 3.1. Voltage Converter Measured Typical Operating Values

V_{VBAT} [V]	I_{VBAT} [A]	V_{VBUS} [V]	I_{VBUS} [A]	P_{IN} [W]	P_{OUT} [W]	P_{LOSS} [W]	Eff. [%]
VBUS = 5 V							
10.0	1.61	5.03	3.00	16.1	15.1	1.01	93.7
12.0	1.35	5.02	3.00	16.2	15.1	1.14	93.0
15.0	1.10	5.03	3.00	16.4	15.1	1.34	91.8
VBUS = 9 V							
10.0	2.81	9.03	3.00	28.1	27.1	1.01	96.4
12.0	2.35	9.03	3.00	28.2	27.0	1.16	95.9
15.0	1.90	9.03	3.00	28.5	27.0	1.41	95.1
VBUS = 15 V							
10.0	4.72	15.0	3.00	47.2	45.0	2.13	95.5
12.0	3.90	15.0	3.00	46.8	45.0	1.76	96.2
15.0	3.10	15.0	3.00	46.5	45.0	1.50	96.8
VBUS = 20 V							
10.0	6.31	20.0	2.99	63.4	59.8	3.55	94.4
12.0	5.25	20.0	3.00	63.0	59.9	3.03	95.2
15.0	4.16	20.0	3.00	62.5	60.0	2.49	96.0

3.3 Thermal Characteristics

Even with a >95% efficient voltage regulator, the board will still have a significant power dissipation when delivering 60 W output power. This reference design displays a temperature increase in certain hot spots of up to 64˚C above the ambient temperature, when running at the maximum output power.

It is important to remember that external elements such encapsulation, air flow, etc., will have to be taken into account when designing a finished product. The purpose of this design is not to solve these design problems, but rather to effectively demonstrate the EFM8BB3 as a USB Power Delivery controller.

The thermal image below shows the typical heat distribution on the board when delivering 60 W output power from 12 V input. In this case, the efficiency was measured to 95.2%, and the power dissipated on the board is 3.0 W.

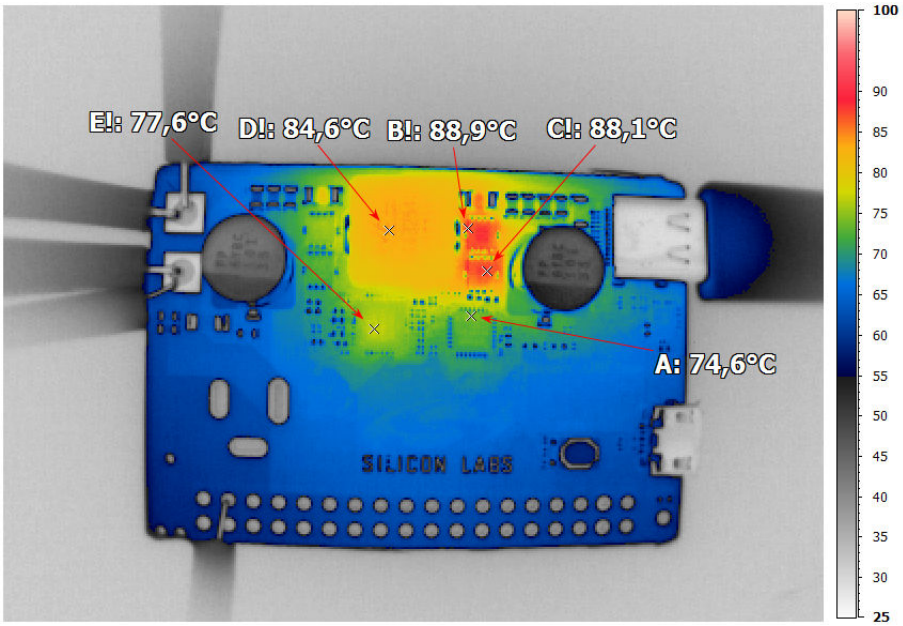


Figure 3.1. Thermal Image, 60 W Output to USB Type-C

4. Debugging

The EFM8BB3 USB Type-C 60 W Charger Reference Design contains an on-board fully functional SEGGER J-Link Debugger that interfaces to the target EFM8 using the Silicon Labs 2-Wire Interface (C2). The debugger allows the user to download code and debug applications running on the target EFM8. It also provides a USB virtual COM port (VCOM) that is directly connected to the target device's serial port, for general purpose communication between the running application and a host computer. The debugger is accessed through the USB Micro-B connector featured on the board.

4.1 On-board Debugger

The on-board debugger is a SEGGER J-Link debugger running on an EFM32 Giant Gecko. The debugger is directly connected to the debug and VCOM pins of the target EFM8. The on-board debugger enables easy customization and development without any external hardware. It is not considered part of the USB Type-C reference design.

When the debug USB cable is removed, the on-board debugger goes into a low power shutoff mode. This means that an application running on batteries batteries will not be affected by the on-board debugger power consumption. Since the I/O voltage rail of the debugger remains powered in the battery operated mode, the pins connected to the debug and VCOM interfaces maintain proper isolation and prevent leakage currents.

4.2 Virtual COM Port

An asynchronous serial connection to the on-board debugger is provided for application data transfer between a host computer and the target EFM8 through the debug USB port. This eliminates the need for an external serial port adapter.

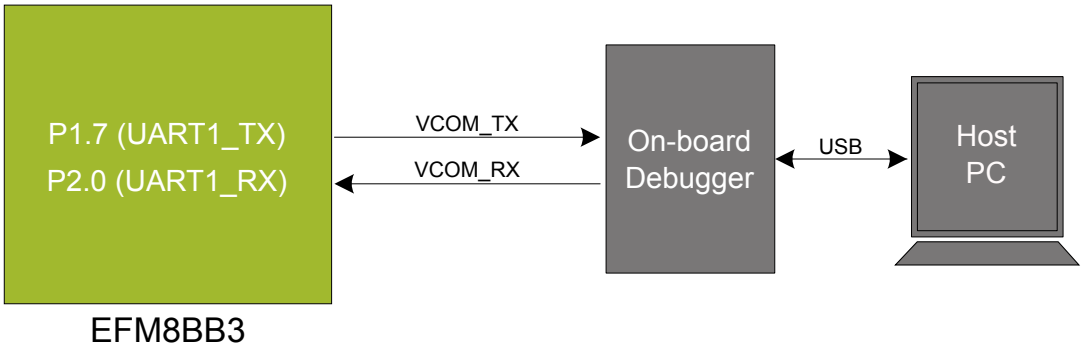


Figure 4.1. Virtual COM Port Interface

The virtual COM port consists of a physical UART between the target device and the board controller, and a logical function in the board controller that makes the serial port available to the host computer over the debug USB connection.

Table 4.1. Virtual COM Port Interface Pins

Signal	Description
VCOM_TX	Transmit data from the EFM8 to the on-board debugger.
VCOM_RX	Receive data from the on-board debugger to the EFM8.

The physical serial port configuration parameters for the target application running on the EFM8 are:

- Speed: 115200 bps
- Data bits: 8
- Parity bit: None
- Stop bits: 1
- Flow control: None

5. Schematics, Assembly Drawings, and BOM

Schematics, assembly drawings, and bill of materials (BOM) are available through when the kit documentation package has been installed.

6. Revision History and Errata

6.1 Kit Revision History

The kit revision can be found printed on the box label of the kit, as outlined in the figure below.

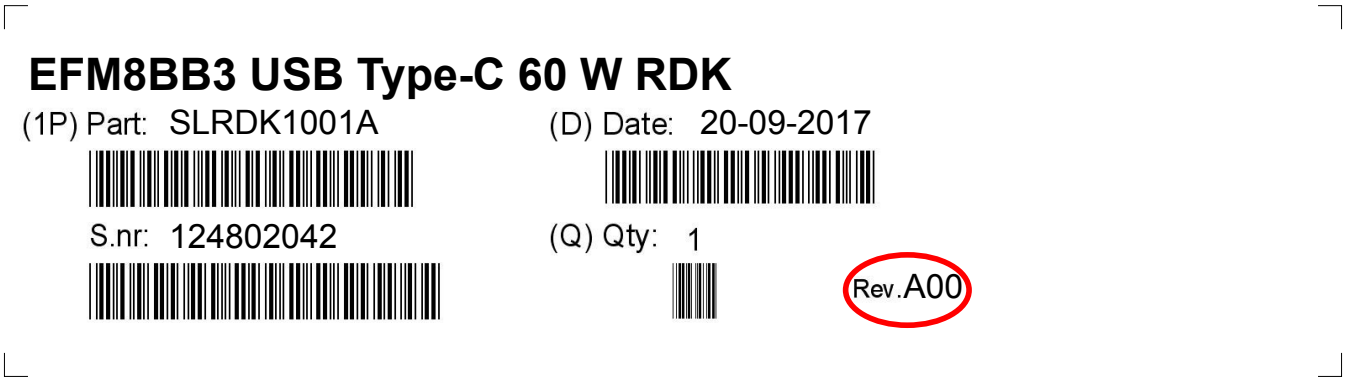


Figure 6.1. Revision Info

Table 6.1. SLRDK1001A Revision History

Kit Revision	Released	Description
A02	16 March 2018	Updated BRD5204A to revision A03.
A01	8 November 2017	Updated BRD5204A to revision A02.
A00	20 September 2017	Initial kit release, containing BRD5204A Revision A01.

6.2 BRD5204A Revision History

The revision of the board assembly is printed on the backside of the board.

Table 6.2. BRD5204A Revision History

Board Revision	Release Date	Description
A03	9 March 2018	Added isolation transistors to CC lines to protect EFM8 from potential overvoltage situations. Updated PCB5204A to Rev. A04.
A02	9 November 2017	Disconnected NCP81239 EN signal from EFM8BB3. Updated PCB5204A to Rev. A03.
A01	18 October 2017	Initial version.

6.3 BRD5204A Errata

Table 6.3. BRD5204A Errata

Board Revision	Problem	Description
A01, A02	No isolation transistor on CC lines.	These board revisions did not include isolation transistors on the USB_CC lines.
A01	Incorrect schematic.	The schematic for this board revision shows that the ENABLE signal for the NCP81239 is connected to an I/O on the EFM8BB3. This connection was cut after board assembly since the EFM8BB3 I/Os are pulled up to VDD out of reset. This would have caused the converter to apply 5 V to VBUS for a few milliseconds before the EFM8 firmware starts.

7. Document Revision History

Revision 1.1

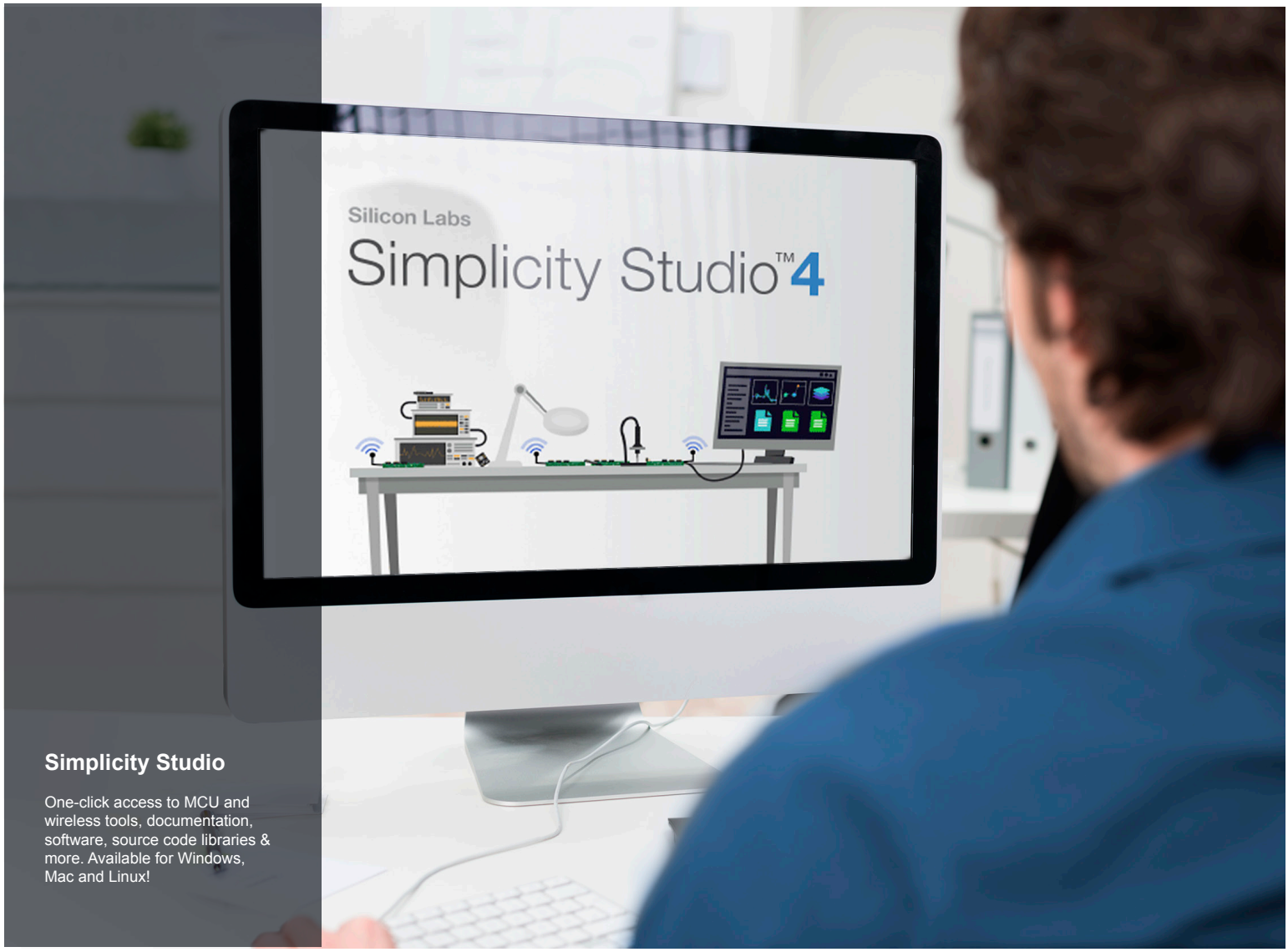
March 2017

- Added errata for missing CC isolation transistor on board revisions A01 and A02.
- Updated USB Type-C Configuration Channel section with information about isolation transistors.
- Added information about board revision A03 to BRD5204A Revision History section.
- Added information about kit revision A01 to SLRDK1001A Revision History section.

Revision 1.0

November 2017

- Initial version.



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