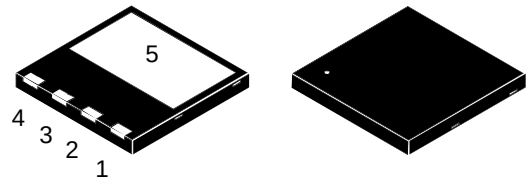
STL28N60DM2

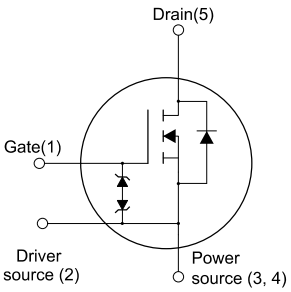
N-channel 600 V, 0.155 Ω typ., 21 A MDmesh™ DM2 Power MOSFET in a PowerFLAT™ 8x8 HV package

Datasheet - production data



PowerFLAT™ 8x8 HV

Figure 1: Internal schematic diagram



Features

Order code	V_{DS} @ $T_{Jmax.}$	$R_{DS(on)}$ max.	I_D	P_{TOT}
STL28N60DM2	650 V	0.175 Ω	21 A	140 W

- Fast-recovery body diode
- Extremely low gate charge and input capacitance
- Low on-resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

Applications

- Switching applications

Description

This high voltage N-channel Power MOSFET is part of the MDmesh™ DM2 fast recovery diode series. It offers very low recovery charge (Q_{rr}) and time (t_{rr}) combined with low $R_{DS(on)}$, rendering it suitable for the most demanding high efficiency converters and ideal for bridge topologies and ZVS phase-shift converters.

Table 1: Device summary

Order code	Marking	Package	Packing
STL28N60DM2	28N60DM2	PowerFLAT™ 8x8 HV	Tape and reel

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±25	V
I_D(1)	Drain current (continuous) at T_{case} = 25 °C	21	A
	Drain current (continuous) at T_{case} = 100 °C	14	
I_{DM}(1)(2)	Drain current (pulsed)	84	A
P_{TOT}(1)	Total dissipation at T_{case} = 25 °C	140	W
dv/dt(3)	Peak diode recovery voltage slope	50	V/ns
dv/dt(4)	MOSFET dv/dt ruggedness	50	V/ns
T_{stg}	Storage temperature	-55 to 150	°C
T_j	Operating junction temperature		

Notes:

(1) The value is limited by package.

(2) Pulse width limited by safe operating area.

(3) $I_{SD} \leq 21$ A, di/dt ≤ 900 A/µs, V_{DD} = 400 V, $V_{DS(peak)} < V_{(BR)DSS}$.

(4) $V_{DS} \leq 480$ V.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	0.89	°C/W
$R_{thj\text{-}amb}$(1)	Thermal resistance junction-ambient	45	

Notes:

(1) When mounted on a 1-inch² FR-4, 2oz Cu board.

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}(1)	Avalanche current, repetitive or not repetitive	4	A
E_{AS}(2)	Single pulse avalanche energy	350	mJ

Notes:

(1) Pulse width limited by T_{jmax}.

(2) starting T_j = 25 °C, $I_D = I_{AR}$, V_{DD} = 50 V.

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified)

Table 5: Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	600			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 600 V			1	µA
		V_{GS} = 0 V, V_{DS} = 600 V, T_{case} = 125 °C			100	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 10.5 A		0.155	0.175	Ω

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	1500	-	pF
C_{oss}	Output capacitance		-	70	-	
C_{rss}	Reverse transfer capacitance		-	1.6	-	
$C_{oss.eq}$(1)	Equivalent output capacitance	V_{GS} = 0 V, V_{DS} = 0 to 480 V	-	134	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	4.6	-	Ω
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 21 A, V_{GS} = 10 V (see *Figure 15: "Gate charge test circuit"*)	-	34	-	nC
Q_{gs}	Gate-source charge		-	8	-	
Q_{gd}	Gate-drain charge		-	18.5	-	

Notes:

(1) $C_{oss.eq}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 10.5 A R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 14: "Switching times test circuit for resistive load"* and *Figure 19: "Switching time waveform"*)	-	16	-	ns
t_r	Voltage rise time		-	7.3	-	
$t_{d(off)}$	Turn-off delay time		-	53	-	
t_f	Current fall time		-	9.3	-	

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}(1)	Source-drain current		-		21	A
I_{SDM}(1)(2)	Source-drain current (pulsed)		-		84	A
V_{SD}(3)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 21 A	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 21 A, di/dt = 100 A/µs, V_{DD} = 100 V (see *Figure 16: " Test circuit for inductive load switching and diode recovery times"*)	-	140		ns
Q_{rr}	Reverse recovery charge		-	0.5		µC
I_{RRM}	Reverse recovery current		-	7.4		A
t_{rr}	Reverse recovery time	I_{SD} = 21 A, di/dt = 100 A/µs, V_{DD} = 100 V, T_J = 150 °C (see *Figure 16: " Test circuit for inductive load switching and diode recovery times"*)	-	309		ns
Q_{rr}	Reverse recovery charge		-	2.6		µC
I_{RRM}	Reverse recovery current		-	16.8		A

Notes:

(1) The value is rated according to $R_{thj\text{-}case}$ and limited by package.

(2) Pulse width is limited by safe operating area.

(3) Pulse test: pulse duration = 300 µs, duty cycle 1.5%.

Table 9: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	I_{GS} = ±1 mA, I_D = 0 A	±30	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

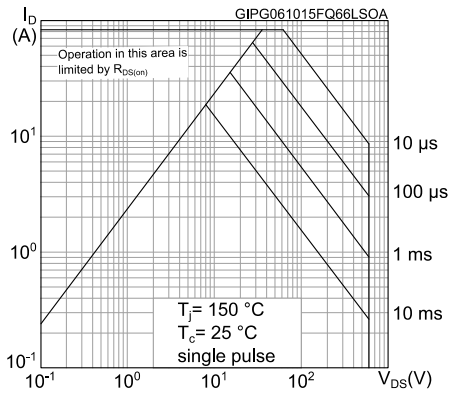


Figure 3: Thermal impedance

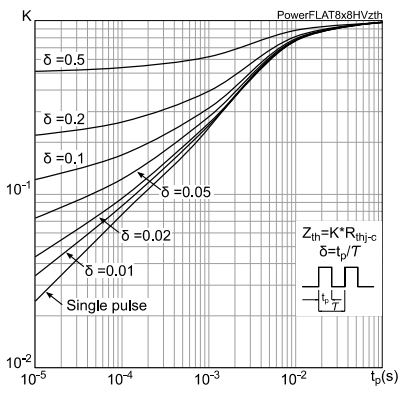


Figure 4: Output characteristics

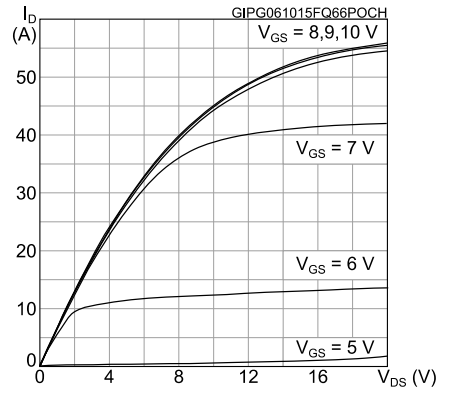


Figure 5: Transfer characteristics

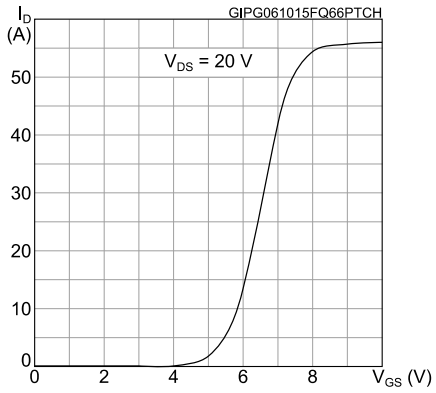


Figure 6: Gate charge vs gate-source voltage

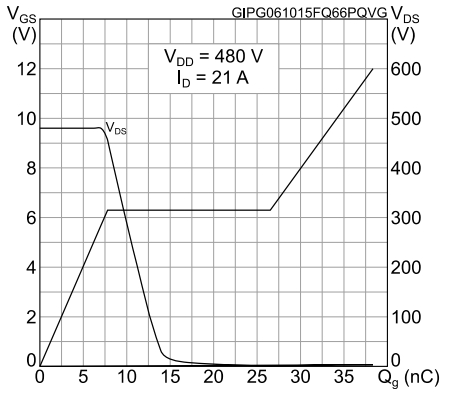


Figure 7: Static drain-source on-resistance

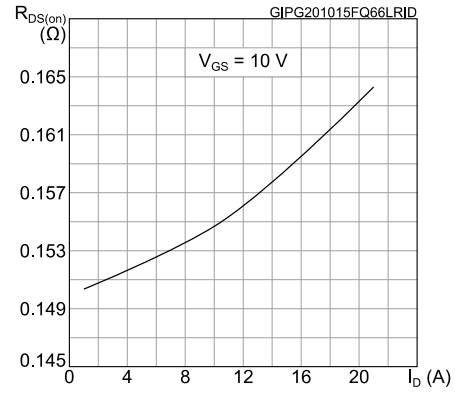


Figure 8: Capacitance variations

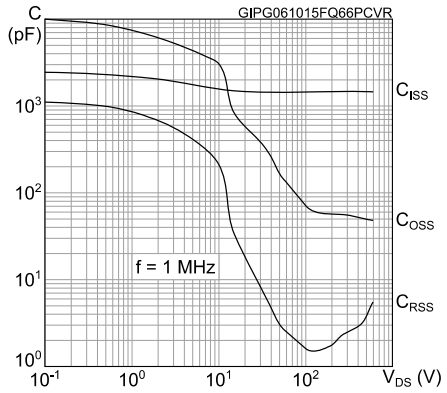


Figure 9: Normalized gate threshold voltage vs temperature

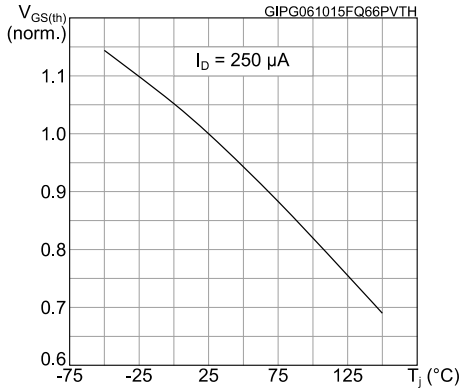


Figure 10: Normalized on-resistance vs temperature

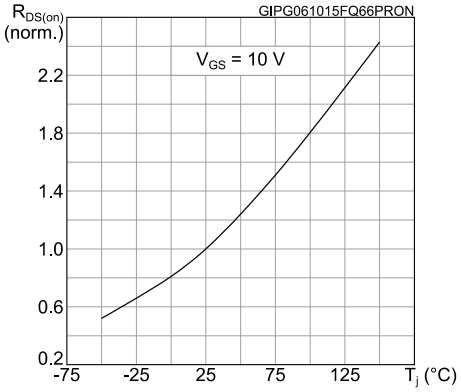


Figure 11: Normalized V(BR)DSS vs temperature

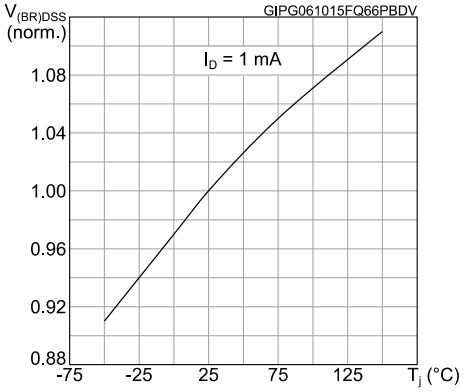


Figure 12: Output capacitance stored energy

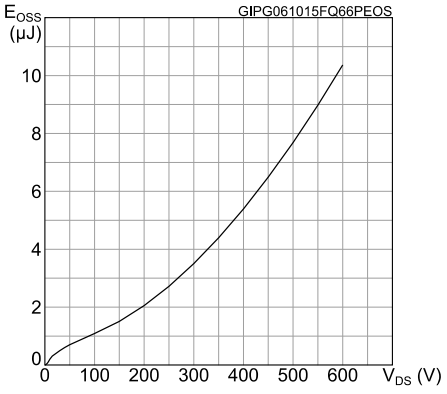
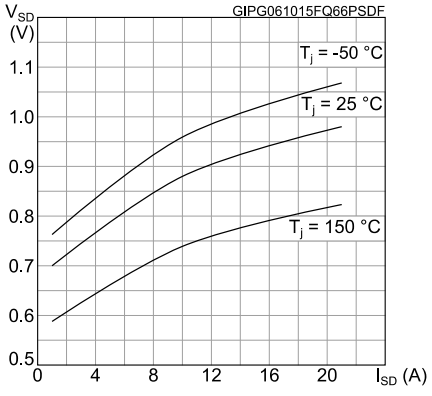


Figure 13: Source-drain diode forward characteristics



3 Test circuits

Figure 14: Switching times test circuit for resistive load

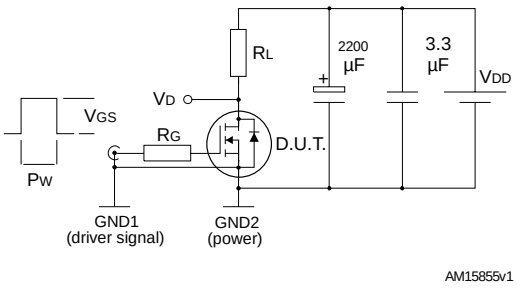


Figure 15: Gate charge test circuit

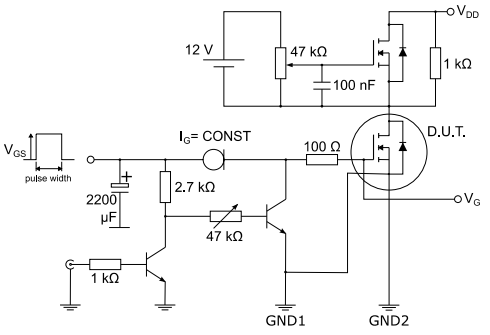


Figure 16: Test circuit for inductive load switching and diode recovery times

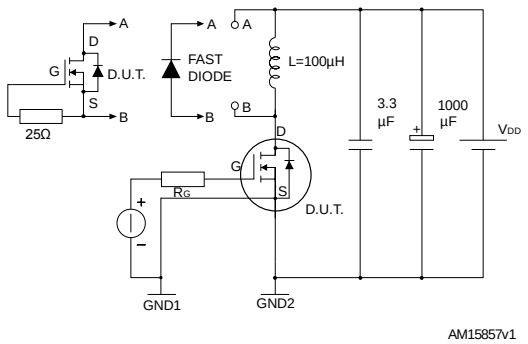


Figure 17: Unclamped inductive load test circuit

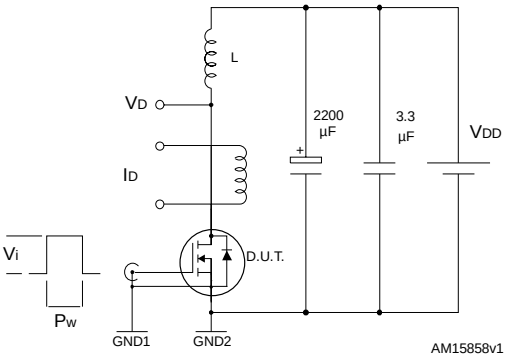


Figure 18: Unclamped inductive waveform

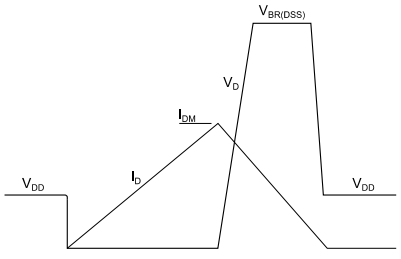
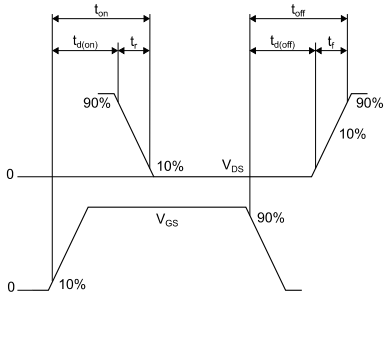


Figure 19: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 PowerFLAT 8x8 HV package information

Figure 20: PowerFLAT™ 8x8 HV package outline

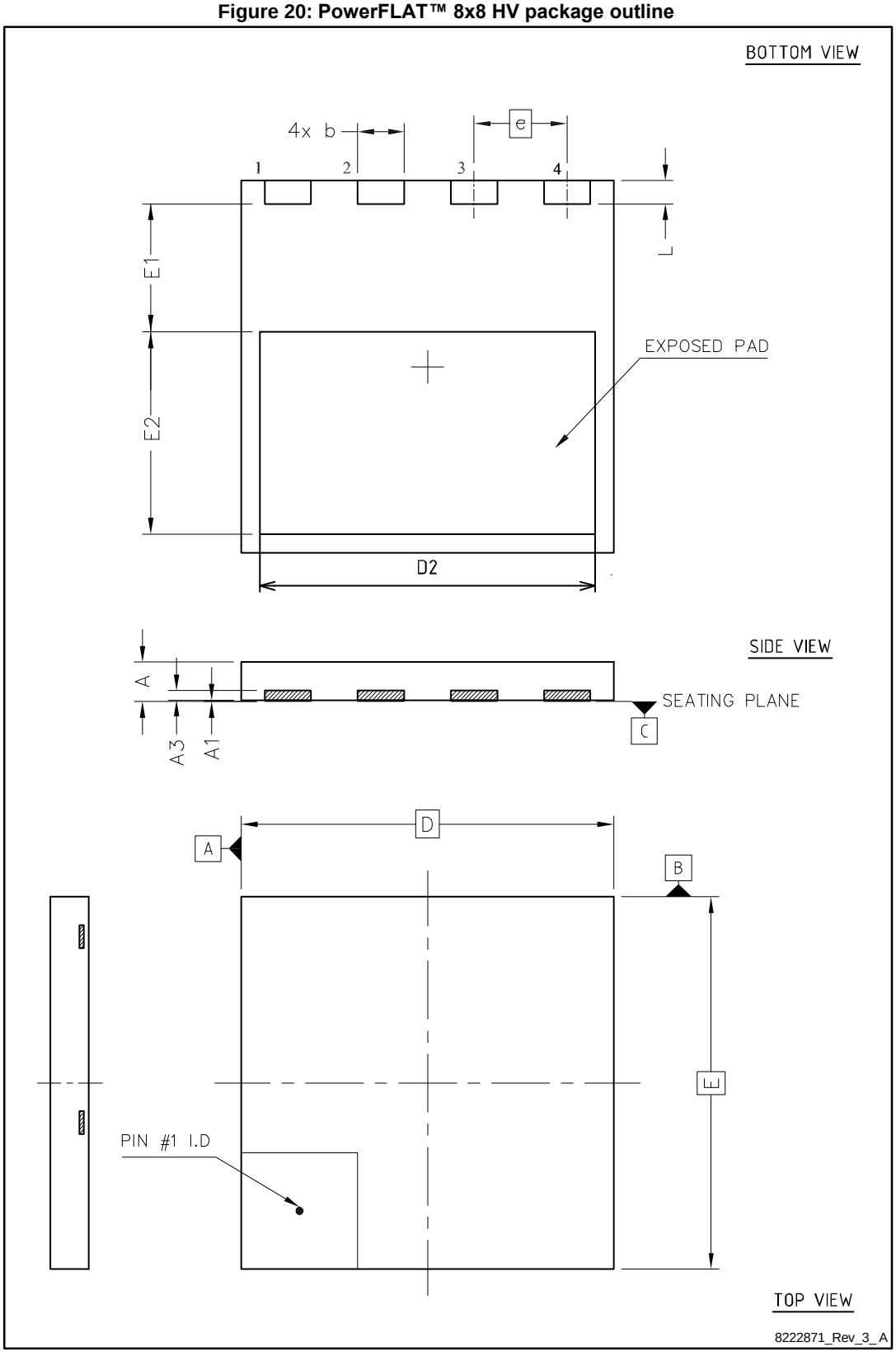
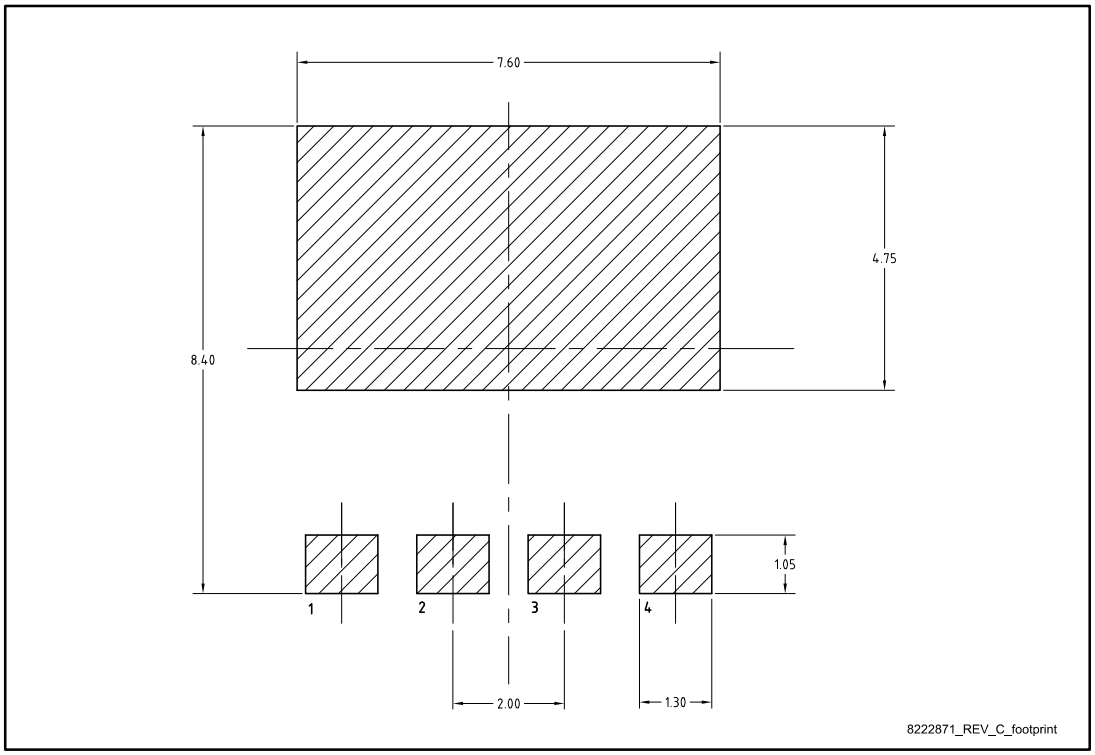


Table 10: PowerFLAT™ 8x8 HV mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.75	0.85	0.95
A1	0.00		0.05
A3	0.10	0.20	0.30
b	0.90	1.00	1.10
D	7.90	8.00	8.10
E	7.90	8.00	8.10
D2	7.10	7.20	7.30
E1	2.65	2.75	2.85
E2	4.25	4.35	4.45
e		2.00	
L	0.40	0.50	0.60

Figure 21: PowerFLAT™ 8x8 HV footprint



All dimensions are in millimeters.

4.2 PowerFLAT 8x8 HV packing information

Figure 22: PowerFLAT™ 8x8 HV tape

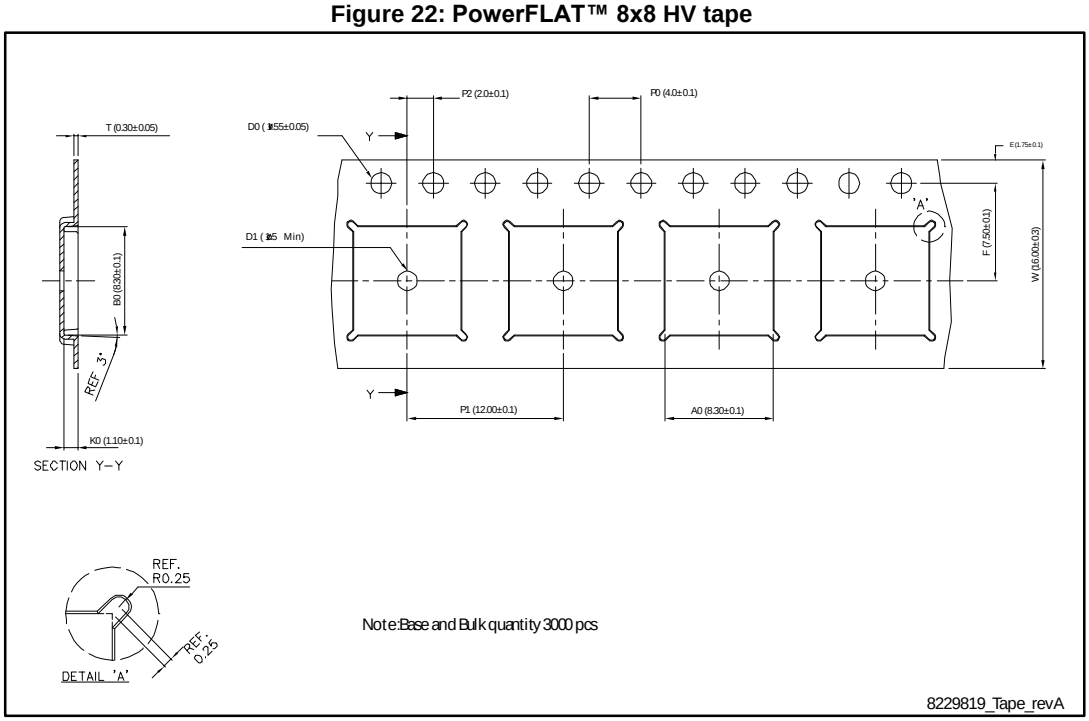


Figure 23: PowerFLAT™ 8x8 HV package orientation in carrier tape

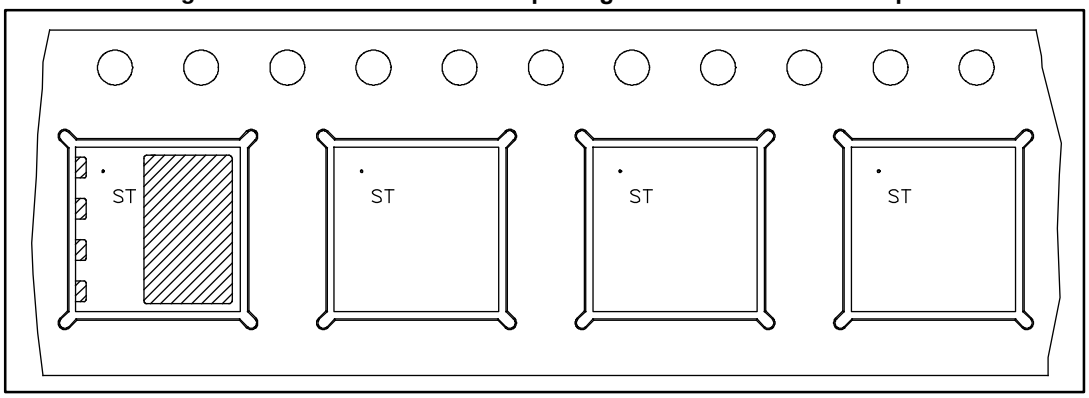
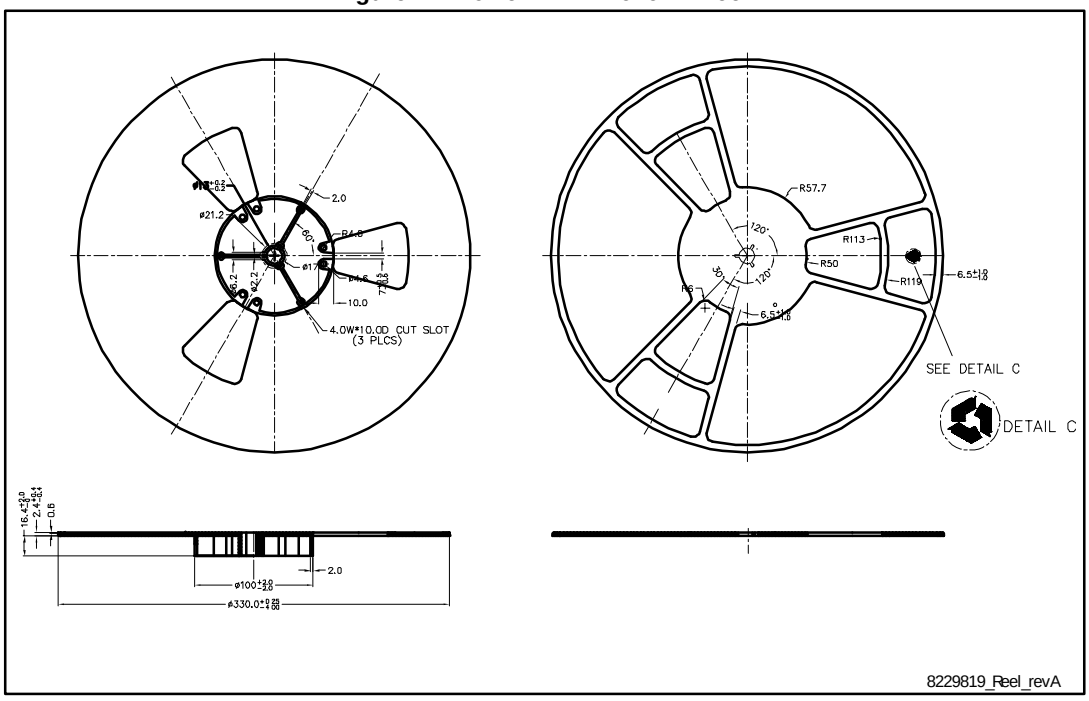


Figure 24: PowerFLAT™ 8x8 HV reel



5 Revision history

Table 11: Document revision history

Date	Revision	Changes
08-Aug-2014	1	First release.
16-Oct-2015	2	Text and formatting changes throughout document Datasheet status changed from preliminary to production data In section Electrical ratings: - added table Avalanche characteristics In section Electrical characteristics: - renamed table Static (was On /off states) Added section Electrical characteristics (curves) Updated section Test circuits Updated and renamed section Package information (was Package mechanical data)

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