

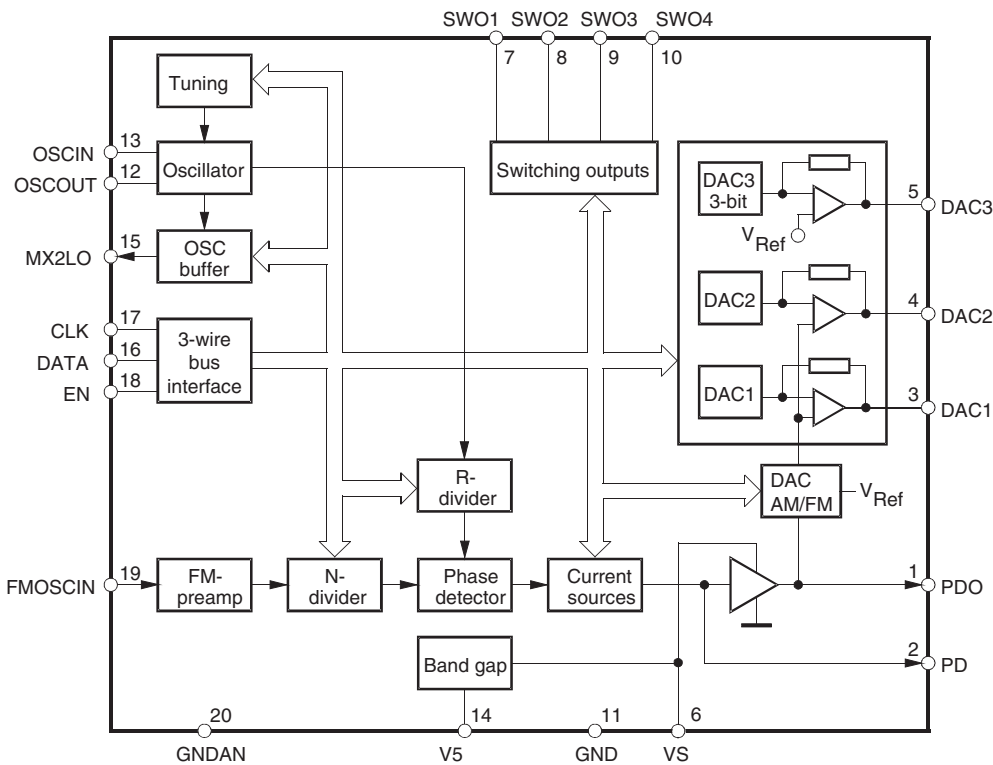
Features

- Reference Oscillator up to 15 MHz (Tuned)
- Oscillator Buffer Output (for AM Up/Down Conversion)
- Two Programmable 16-bit Dividers
- Fine-tuning Steps Possible
- Fast Response Time Due to Integrated Loop Push-pull Stage
- 3-wire Bus (Enable, Clock and Data; 3V and 5V Microcontrollers Acceptable)
- Four Programmable Switching Outputs (Open Drain)
- Three DACs for Software Controlled Tuner Alignment
- Low-power Consumption
- High Signal to Noise Ratio (SNR)
- Integrated Band Gap – Only One Supply Voltage Necessary

1. Description

The ATR4256 is a synthesizer IC for FM receivers and an AM up-conversion system in BiCMOS technology. Together with the AM/FM IC ATR4258 or ATR4255, it comprises a complete AM/FM car radio front-end, which is also recommended for RDS (Radio Data System) applications. It is controlled by a 3-wire bus and also contains switches and Digital to Analog Converters (DACs) for software-controlled alignment of the AM/FM tuner. The ATR4256 is the pin-compatible successor IC of U4256BM-R.

Figure 1-1. Block Diagram



Frequency Synthesizer for Radio Tuning

ATR4256



2. Pin Configuration

Figure 2-1. Pinning SSO20

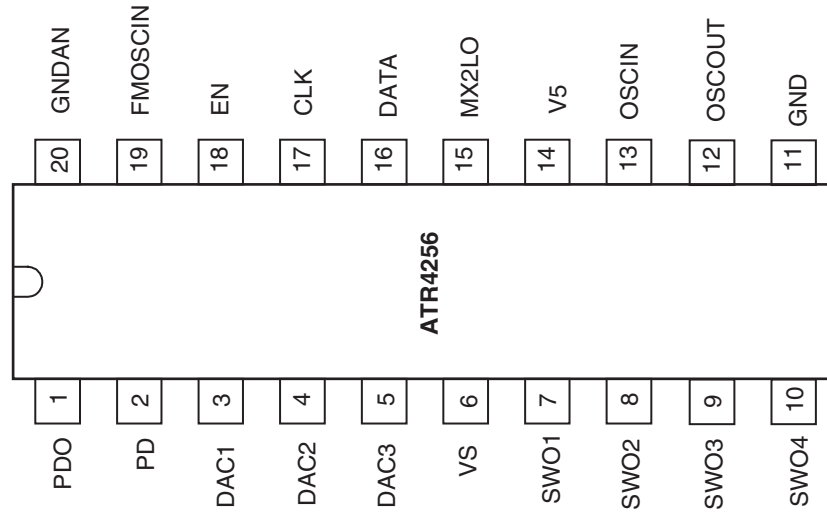


Table 2-1. Pin Description

| Pin | Symbol | Function |
|-----|---------|-------------------------------|
| 1 | PDO | Phase detector output |
| 2 | PD | Pulsed current output |
| 3 | DAC1 | Digital-to-analog converter 1 |
| 4 | DAC2 | Digital-to-analog converter 2 |
| 5 | DAC3 | Digital-to-analog converter 3 |
| 6 | VS | Supply voltage, analog part |
| 7 | SWO1 | Switching output 1 |
| 8 | SWO2 | Switching output 2 |
| 9 | SWO3 | Switching output 3 |
| 10 | SWO4 | Switching output 4 |
| 11 | GND | Ground, digital part |
| 12 | OSCOUT | Reference oscillator output |
| 13 | OSCIN | Reference oscillator input |
| 14 | V5 | Capacitor band gap |
| 15 | MX2LO | Oscillator buffer output |
| 16 | DATA | Data input |
| 17 | CLK | Clock |
| 18 | EN | Enable |
| 19 | FMOSCIN | FM-oscillator input |
| 20 | GNDAN | Ground, analog part |

3. Functional Description

For a tuned FM-broadcast receiver, the following parts are needed:

- Voltage-controlled Oscillator (VCO)
- Antenna Amplifier Tuned Circuit
- RF Amplifier Tuned Circuit

Typical modern receivers with electronic tuning are tuned to the desired FM frequency by the frequency synthesizer IC ATR4256. The special design allows the user to build software-controlled tuner alignment systems. Two programmable DACs (Digital-to-Analog Converter) support the computer-controlled alignment. The output of the PLL is a tuning voltage which is connected to the VCO of the receiver IC. The output of the VCO is equal to the desired station frequency plus the IF (10.7 MHz). The RF and the oscillator signal (VCO) are both input to the mixer that translates the desired FM-channel signal to the fixed IF signal. For FM, the double-conversion system of the receiver requires exactly 10.7 MHz for the first IF frequency, which determines the center frequency of the software-controlled integrated second IF filter.

If this oscillator tuning feature is not used, the internal capacitors have to be switched off and the oscillator has to be operated with high-quality external capacitors to ensure that the operational frequency is exactly 10.250 MHz.

When dimensioning the oscillator circuit, it is important that the additional capacitors enable the oscillator to operate through its complete tracking range. The oscillating ability depends very strongly on the used crystal oscillator. Initializing the oscillator should be established without switching any additional capacitors to guarantee that the oscillator starts to operate properly. Due to the lower quality of the integrated capacitors compared to discrete capacitors, the amount of the switched integrated capacitors should always be minimized. (If necessary reduce tracking range or use a different crystal oscillator.)

The ATR4256 has a very fast response time of maximum 800 μs (at 2 mA, $f_{\text{Step}} = 50 \text{ kHz}$, measured on the MPX signal). It has a high signal to noise ratio. Only one supply voltage is necessary, due to an integrated band gap.

4. Input/Output Interface Circuits

4.1 PDO (Pin 1)

PDO is the buffer amplifier output of the PLL. The bipolar output stage is a rail-to-rail amplifier.

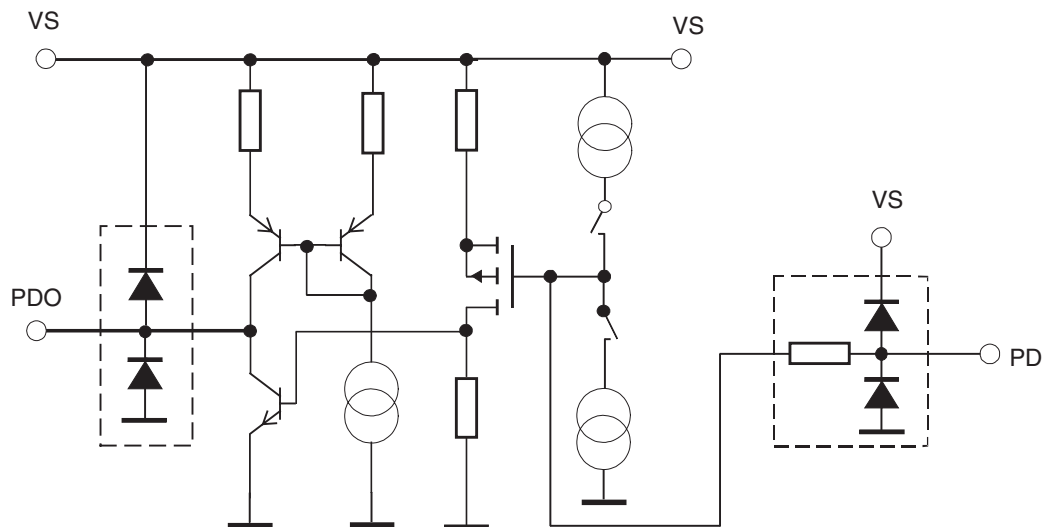
4.2 PD (Pin 2)

PD is the current charge pump output of the PLL. The current can be controlled by setting the appropriate bits. The loop filter has to be designed corresponding to the chosen pump current and the internal reference frequency. A recommendation can be found in the application circuit. The charge-pump current can be chosen by setting Bit 71 and Bit 70 as follows:

Table 4-1. Current Charge-pump Output

| IPD (μA) | B71 | B70 |
|-----------------------|-----|-----|
| 25 | 0 | 0 |
| 100 | 0 | 1 |
| 500 | 1 | 0 |
| 2000 | 1 | 1 |

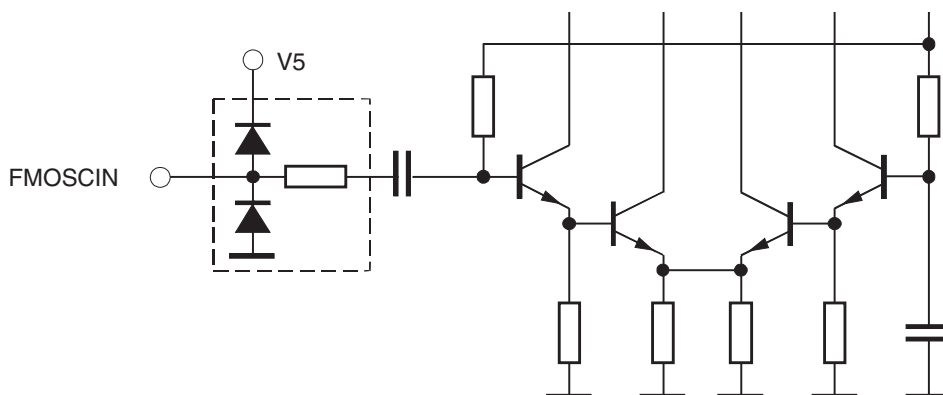
Figure 4-1. Internal Components at PDO Connection



4.3 FMOSCIN (Pin 19)

FMOSCIN is the preamplifier input for the FM oscillator signal.

Figure 4-2. Internal Components at FMOSCIN



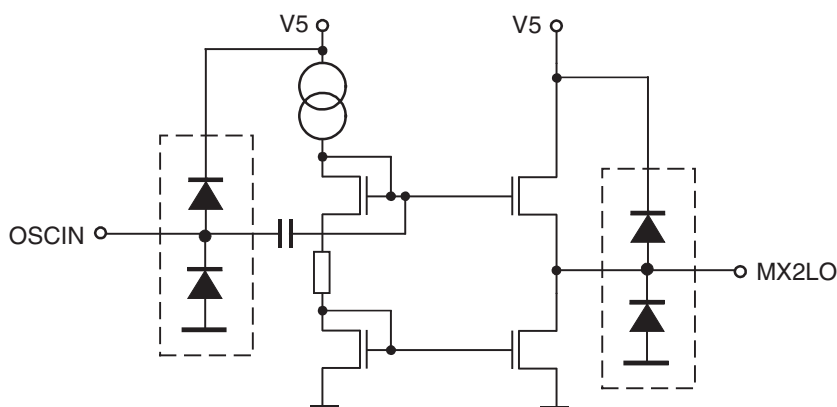
4.4 MX2LO (Pin 15)

MX2LO is the buffered output of the crystal oscillator. This signal can be used as a reference frequency for ATR4255 or ATR4258. The oscillator buffer output can be switched by the OSCB bit (B69) as follows.

Table 4-2. MX2LO Settings

| MX2LO AC Voltage | B69 |
|------------------|-----|
| ON | 0 |
| OFF | 1 |

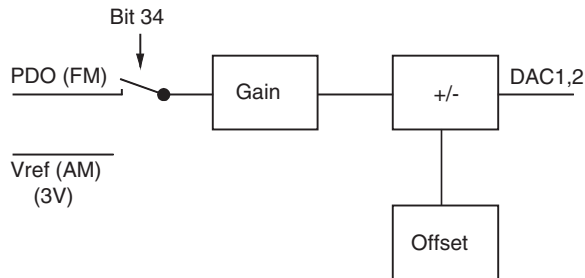
Figure 4-3. Internal Components at MX2LO



4.5 Function of DAC1, DAC2 in FM and AM Mode (Pin 3 and Pin 4)

For automatic tuner alignment, the DAC1 and DAC2 of the ATR4256 can be controlled by setting the gain of VPDO and offset values. Figure 4-4 shows the principle of the operation. In FM Mode the gain is in the range of $0.69 \times V_{(PDO)}$ to $2.16 \times V_{(PDO)}$. The offset range is $+0.56V$ to $-0.59V$. For alignment, DAC1 and DAC2 are connected to the varicaps of the preselection filters. For alignment, offset and gain are set to have the best tuner tracking.

Figure 4-4. Principal Operation for Alignment



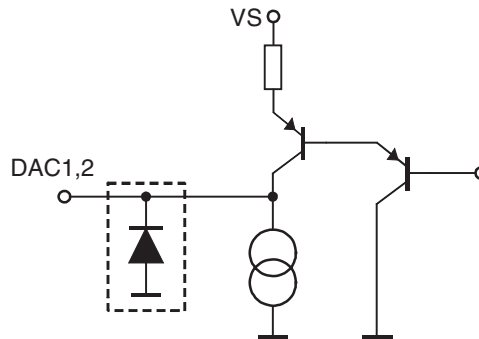
The DAC mode can be controlled by setting Bit 34 as follows

Table 4-3. DAC Mode

| DAC Mode | B34 |
|----------|-----|
| FM | 0 |
| AM | 1 |

If Bit 34 = 1 (AM Mode), then DAC1 and DAC2 can be used as standard DAC converters. The internal voltage of 3V is connected to the gain and offset input of DAC1 and DAC2 (only in AM Mode). The gain is in the range of $0.46 \times 3V$ to $3.03 \times 3V$. The offset range is $+1.46V$ to $-1.49V$.

Figure 4-5. Internal Components at DAC1 and DAC2 Output



4.6 DAC1, DAC2 in FM Mode (Pin 3 and Pin 4)

The gains of DAC1 and DAC2 have a range of $0.69 \times V_{(PDO)}$ to $2.16 \times V_{(PDO)}$. $V_{(PDO)}$ is the PLL tuning voltage output. This range is divided into 256 steps; one step is approximately $(2.16 - 0.46) \times V_{(PDO)} / 255 = 0.005764 \times V_{(PDO)}$. The gain of DAC1 can be controlled by B36 to B43 (bits 0 to 7 of DAC1 Gain), and the gain of DAC2 by B0 to B7 (bits 0 to 7 of DAC2 Gain) as follows:

Table 4-4. DAC Gain Setting, FM Mode

| Gain DAC1, Approximately | B43 | B42 | B41 | B40 | B39 | B38 | B37 | B36 | Decimal Gain |
|----------------------------|-----|-----|-----|-----|-----|-----|-----|-----|--------------|
| Gain DAC2, Approximately | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | Decimal Gain |
| $0.69 \times V_{(PDO)}$ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $0.69576 \times V_{(PDO)}$ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| $0.70153 \times V_{(PDO)}$ | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2 |
| $0.70729 \times V_{(PDO)}$ | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 3 |
| ... | ... | ... | ... | ... | ... | ... | ... | ... | ... |
| $0.99549 \times V_{(PDO)}$ | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 53 |
| ... | ... | ... | ... | ... | ... | ... | ... | ... | ... |
| $2.14847 \times V_{(PDO)}$ | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 253 |
| $2.15424 \times V_{(PDO)}$ | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 254 |
| $2.16 \times V_{(PDO)}$ | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 255 |

Offset = 31 (intermediate position)

The offset of DAC1 and DAC2 has a range of 0.56V to -0.59V. This range is divided into 64 steps; one step is approximately $1.15V / 63 = 18.25 \text{ mV}$. The offset of DAC1 can be controlled by B44 to B49 (bits 0 to 5 of DAC1 Offset), and the offset of DAC2 by B8 to B13 (bits 0 to 5 of DAC2 Offset) as follows:

Table 4-5. DAC Offset Setting, FM Mode

| Offset DAC1, Approximately | B49 | B48 | B47 | B46 | B45 | B44 | Decimal Gain |
|----------------------------|-----|-----|-----|-----|-----|-----|--------------|
| Offset DAC2, Approximately | B13 | B12 | B11 | B10 | B9 | B8 | Decimal Gain |
| 0.56V | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0.5417V | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0.5235V | 0 | 0 | 0 | 0 | 1 | 0 | 2 |
| 0.5052V | 0 | 0 | 0 | 0 | 1 | 1 | 3 |
| ... | ... | ... | ... | ... | ... | ... | ... |
| +0.0059V | 0 | 1 | 1 | 1 | 1 | 1 | 31 |
| ... | ... | ... | ... | ... | ... | ... | ... |
| 0.5535V | 1 | 1 | 1 | 1 | 0 | 1 | 61 |
| -0.5717V | 1 | 1 | 1 | 1 | 1 | 0 | 62 |
| -0.59V | 1 | 1 | 1 | 1 | 1 | 1 | 63 |

Gain = 53 (intermediate position)

4.7 DAC1, DAC2 in AM Mode (Pin 3 and Pin 4)

In AM mode the DAC input voltage $V_{(PDO)}$ is internally connected to 3V. The gains of DAC1 and DAC2 have a range of $0.46 \times 3V$ to $3.03 \times 3V$. $V_{(PDO)}$ is the PLL tuning voltage output. This range is divided into 256 steps; one step is approximately $(3.03 - 0.46) \times 3V / 255 = 0.01007 \times 3V$. The gain of DAC1 can be controlled by B36 to B43 (bits 0 to 7 of DAC1 Gain) and the gain of DAC2 by B0 to B7 (bits 0 to 7 of DAC2 gain) as follows:

Table 4-6. DAC Gain, AM Mode

| Gain DAC1, Approximately | B43 | B42 | B41 | B40 | B39 | B38 | B37 | B36 | Decimal Gain |
|--------------------------|-----|-----|-----|-----|-----|-----|-----|-----|--------------|
| Gain DAC2, Approximately | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | Decimal Gain |
| $0.4607 \times 3V$ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $0.4710 \times 3V$ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| $0.4812 \times 3V$ | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2 |
| $0.4915 \times 3V$ | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 3 |
| ... | ... | ... | ... | ... | ... | ... | ... | ... | ... |
| $1.0029 \times 3V$ | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 53 |
| ... | ... | ... | ... | ... | ... | ... | ... | ... | ... |
| $3.0097 \times 3V$ | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 253 |
| $3.0196 \times 3V$ | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 254 |
| $3.0296 \times 3V$ | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 255 |

Offset = 31 (intermediate position)

Remark: $V_{(PDO)}$ is 3V in AM mode.

The offset of DAC1 and DAC2 has a range of +1.46V to -1.49V. This range is divided into 64 steps; one step is approximately $2.95 V / 63 = 46.8 mV$. The offset DAC1 can be controlled by B44 to B49 (bits 0 to 5 of DAC1 Offset) and the offset of DAC2 by B8 to B13 (bits 0 to 5 of DAC2 Offset) as follows:

Table 4-7. DAC Offset, AM Mode

| Offset DAC1 Approximately | B49 | B48 | B47 | B46 | B45 | B44 | Decimal Gain |
|---------------------------|-----|-----|-----|-----|-----|-----|--------------|
| Offset DAC2 Approximately | B13 | B12 | B11 | B10 | B9 | B8 | Decimal Gain |
| 1.4606V | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1.4138V | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 1.3665V | 0 | 0 | 0 | 0 | 1 | 0 | 2 |
| 1.3196V | 0 | 0 | 0 | 0 | 1 | 1 | 3 |
| ... | ... | ... | ... | ... | ... | ... | ... |
| -0.0079V | 0 | 1 | 1 | 1 | 1 | 1 | 31 |
| ... | ... | ... | ... | ... | ... | ... | ... |
| -1.3975V | 1 | 1 | 1 | 1 | 0 | 1 | 61 |
| -1.4447V | 1 | 1 | 1 | 1 | 1 | 0 | 62 |
| -1.4917V | 1 | 1 | 1 | 1 | 1 | 1 | 63 |

Gain = 53 (intermediate position)

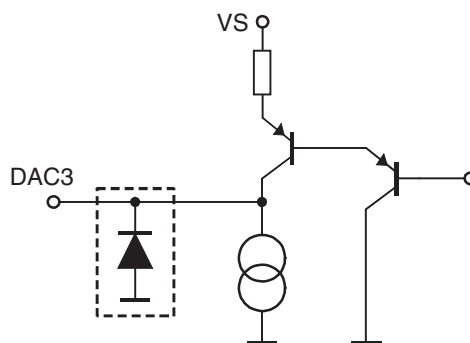
4.8 DAC3 (Pin 5)

The DAC3 output voltage can be controlled by B66 to B68 (bits 0 to 2 of DAC3) as follows:

Table 4-8. DAC3 Offset Setting

| DAC3 Offset, Approximately | B68 | B67 | B66 |
|----------------------------|-----|-----|-----|
| 0.55V | 0 | 0 | 0 |
| 1.25V | 0 | 0 | 1 |
| 1.90V | 0 | 1 | 0 |
| 2.60V | 0 | 1 | 1 |
| 3.30V | 1 | 0 | 0 |
| 4.10V | 1 | 0 | 1 |
| 4.80V | 1 | 1 | 0 |
| 5.45V | 1 | 1 | 1 |

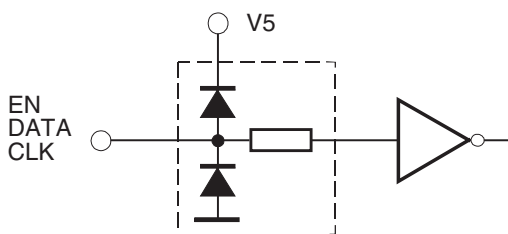
Figure 4-6. Internal Components at DAC3



4.9 EN, DATA, CLK (Pins 16 to 18)

All functions can be controlled via a 3-wire bus consisting of ENABLE, DATA and CLOCK. The bus is designed for microcontrollers which operate with 3V supply voltage. Details of the data transfer protocol are shown in [“3-wire Bus Description”](#) on page 12.

Figure 4-7. Internal Components at EN, DATA, CLK



4.10 SWO1, SWO2, SWO3 and SWO4 (Pins 7 to 10)

All switching outputs are “open drain” and can be set and reset by software control. Details are described in the data transfer protocol.

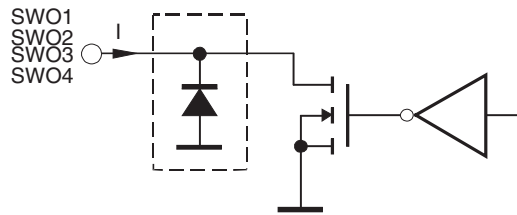
The switching output SWO1 to SWO4 can be controlled as follows (B30 to B33):

Table 4-9. SWO1 to SWO4 Setting

| Switch Output | B30 + X |
|---------------------------|---------|
| SWOx = ON (switch to GND) | 0 |
| SWOx = OFF | 1 |

X = 0 to 3

Figure 4-8. Internal Components at SWO1, SWO2, SWO3 and SWO4



4.11 OSCIN, OSCOUT (Pin 12 and Pin 13)

A crystal resonator (up to 15 MHz) is connected between OSCIN and OSCOUT in order to generate the reference frequency. By using the ATR4256 in connection with ATR4255 or ATR4258, the crystal frequency must be 10.25 MHz. The complete application circuit is shown in [Figure 6-2](#). If a reference is available, it can be applied at OSCIN. The minimum voltage should be 100 mVrms. In this case, pin OSCOUT has to be open.

The tuning capacity for the crystal oscillator has a range of 0.5 pF to 71.5 pF. The values are coded binary. The tuning can be controlled by B78 to B85 as follows:

Table 4-10. Crystal Tuning Capacitance

| B85 = 1 [pF] | B85 = 0 [pF] | B84 | B83 | B82 | B81 | B80 | B79 | B78 |
|--------------|--------------|-----|-----|-----|-----|-----|-----|-----|
| 0 | 8.0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0.5 | 8.5 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1.0 | 9.0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| 1.5 | 19.5 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| ... | ... | ... | ... | ... | ... | ... | ... | ... |
| 63.0 | 71.0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 63.5 | 71.5 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Figure 4-9. Internal Components at OSCIN and OSCOUT

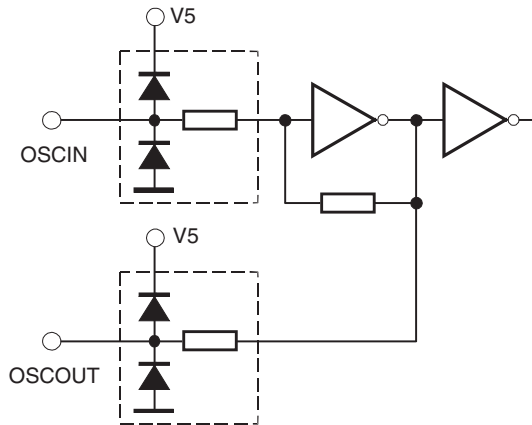
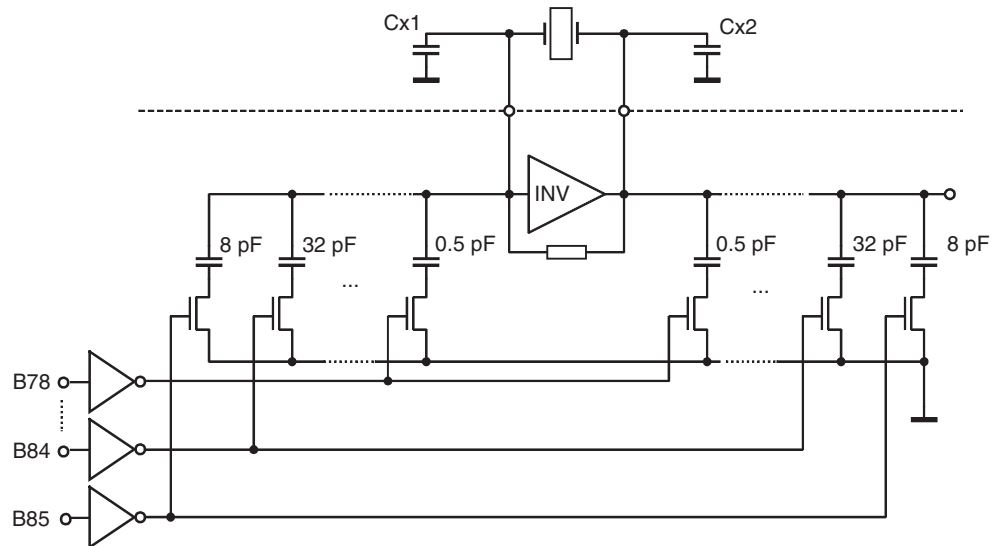
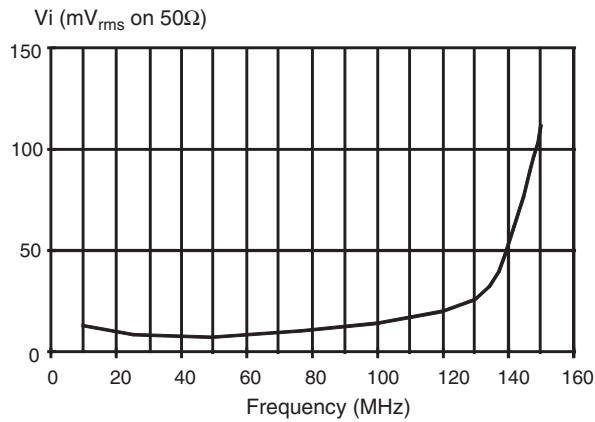


Figure 4-10. Internal Connection of Tuning Capacity for Crystal Oscillator



5. Application Information

Figure 5-1. FMOSCIN Sensitivity



6. 3-wire Bus Description

The register settings of ATR4256 are programmed by a 3-wire bus protocol. The bus protocol consists of separate commands. A defined number of bits are transmitted sequentially during each command.

One command is used to program all the bits of one register. The different registers available (see [“Data Transfer” on page 14](#)) are addressed by the length of the command (number of transmitted bits) and by two address bits, that are unique to each register of a given length. 16-bit registers are programmed by 16-bit commands and 24-bit registers are programmed by 24-bit commands.

Each bus command starts with a rising edge on the enable line (EN) and ends with a falling edge on EN. EN has to be kept HIGH during the bus command.

The sequence of transmitted bits during one command starts with the LSB of the first byte and ends with the MSB of the last byte of the register addressed. To transmit one bit (0 or 1) DATA has to be set to the appropriate value (LOW or HIGH) and a LOW to HIGH transition has to be performed on the clock line (CLK) while DATA is valid. The DATA is evaluated at the rising edges of CLK. The number of LOW to HIGH transitions on CLK during the HIGH period of EN is used to determine the length of the command.

The bus protocol and the register addressing of ATR4256 are compatible to the addressing used in ATR4255 and ATR4258. That means ATR4256 and ATR4255 (or ATR4258) can be operated on the same 3-wire bus as shown in the application circuit.

Figure 6-1. 3-wire Bus Timing Diagram

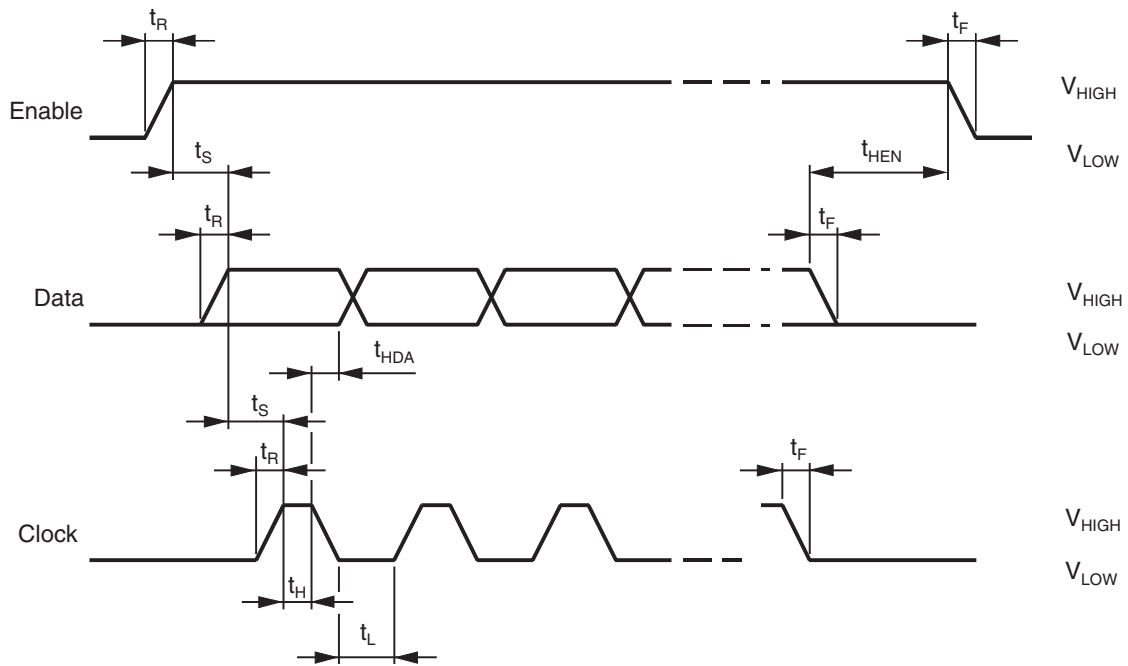
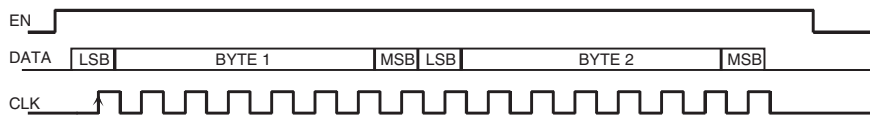
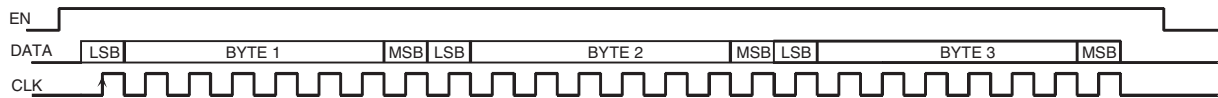


Figure 6-2. 3-wire Pulse Diagram

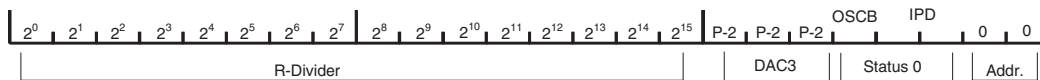
16-bit command



24-bit command



e.g. R-Divider



6.1 Data Transfer

Table 6-1. Control Registers

| A | | | | | | | | | | | | | | | | | | | | | | | |
|-------|---|----------|------------------------|------------------|------------------|------------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|-----|
| MSB | | BYTE 3 | | | | | LSB | MSB | | BYTE 2 | | | | | LSB | MSB | | BYTE 1 | | | | | LSB |
| ADDR. | | STATUS 0 | | | DAC3 | | | R-Divider | | | | | | | | | | | | | | | |
| 0 | 0 | IPD | OSCB 0=on, 1=off | P-2 ² | P-2 ¹ | P-2 ⁰ | 2 ¹⁵ | 2 ¹⁴ | 2 ¹³ | 2 ¹² | 2 ¹⁰ | 2 ¹¹ | 2 ⁹ | 2 ⁸ | 2 ⁷ | 2 ⁶ | 2 ⁵ | 2 ⁴ | 2 ³ | 2 ² | 2 ¹ | 2 ⁰ | |
| | | B71 | B70 | B69 | B68 | B67 | B66 | B65 | B64 | B63 | B62 | B61 | B60 | B59 | B58 | B57 | B56 | B55 | B54 | B53 | B52 | B51 | B50 |

| B | | | | | | | | | | | | | | | | | | | | | | | |
|-------|---|----------|---------------------|------------------------|------------------------|------------------------|------------------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| MSB | | BYTE 3 | | | | | LSB | MSB | | BYTE 2 | | | | | LSB | MSB | | BYTE 1 | | | | | LSB |
| ADDR. | | STATUS 1 | | | | | | N-Divider | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | AM=1 FM=0 DAC | SWO4 0=on, 1=off | SWO3 0=on, 1=off | SWO2 0=on, 1=off | SWO1 0=on, 1=off | 2 ¹⁵ | 2 ¹⁴ | 2 ¹³ | 2 ¹² | 2 ¹⁰ | 2 ¹¹ | 2 ⁹ | 2 ⁸ | 2 ⁷ | 2 ⁶ | 2 ⁵ | 2 ⁴ | 2 ³ | 2 ² | 2 ¹ | 2 ⁰ |
| | | B35 | B34 | B33 | B32 | B31 | B30 | B29 | B28 | B27 | B26 | B25 | B24 | B23 | B22 | B21 | B20 | B19 | B18 | B17 | B16 | B15 | B14 |

| C | | | | | | | | | | | | | | | |
|-------|---|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| MSB | | BYTE 2 | | | | | LSB | MSB | | BYTE 1 | | | | | LSB |
| ADDR. | | DAC1 OFFSET | | | | | | DAC1 GAIN | | | | | | | |
| 0 | 0 | O-2 ⁵ | O-2 ⁴ | O-2 ³ | O-2 ² | O-2 ¹ | O-2 ⁰ | G-2 ⁷ | G-2 ⁶ | G-2 ⁷ | G-2 ⁵ | G-2 ⁴ | G-2 ³ | G-2 ² | G-2 ⁰ |
| | | B49 | B48 | B47 | B46 | B45 | B44 | B43 | B42 | B41 | B40 | B39 | B38 | B37 | B36 |

| D | | | | | | | | | | | | | | | |
|-------|---|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| MSB | | BYTE 2 | | | | | LSB | MSB | | BYTE 1 | | | | | LSB |
| ADDR. | | DAC2 OFFSET | | | | | | DAC2 GAIN | | | | | | | |
| 0 | 1 | O-2 ⁵ | O-2 ⁴ | O-2 ³ | O-2 ² | O-2 ¹ | O-2 ⁰ | G-2 ⁷ | G-2 ⁶ | G-2 ⁷ | G-2 ⁵ | G-2 ⁴ | G-2 ³ | G-2 ² | G-2 ⁰ |
| | | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |

| E | | | | | | | | | | | | | | | |
|-------|---|----------------------------|-------|-------|------|------|------|------|----------|--------|-----|-----|-----|-----|-----|
| MSB | | BYTE 2 | | | | | LSB | MSB | | BYTE 1 | | | | | LSB |
| ADDR. | | Oscillator tuning function | | | | | | | Not used | | | | | | |
| 1 | 0 | 8 pF | 32 pF | 16 pF | 8 pF | 4 pF | 2 pF | 1 pF | 0.5 pF | X | X | X | X | X | X |
| | | B85 | B84 | B83 | B82 | B81 | B80 | B79 | B78 | B77 | B76 | B75 | B74 | B73 | B72 |

7. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

| Parameters | Symbol | Value | Unit |
|---|-----------|--------------|------|
| Analog supply voltage, pin 6 | V_S | 8 to 12 | V |
| Input voltage BUS; pins 16, 17 and 18 | V_I | -0.3 to +5.3 | V |
| Output current switches; pins 7, 8, 9 and 10 (see Figure 4-8 on page 10) | I_O | -1 to +5 | mA |
| Drain voltage switches; pins 7, 8, 9 and 10 | V_{OD} | 15 | V |
| Ambient temperature range | T_{amb} | -40 to +85 | °C |
| Storage temperature range | T_{stg} | -40 to +125 | °C |
| Junction temperature | T_j | 125 | °C |
| Electrostatic handling M.M. | V_{ESD} | 300 | V |

8. Thermal Resistance

| Parameters | Symbol | Value | Unit |
|---|------------|-------|------|
| Junction ambient, when soldering to PCB | R_{thJA} | 140 | K/W |

9. Operating Range

All voltages are referred to GND (Pin 11)

| Parameters | Symbol | Min. | Typ. | Max. | Unit |
|--|-----------|------|------|-------|------|
| Supply voltage range, pin 6 | V_S | 8 | 8.5 | 12 | V |
| Ambient temperature | T_{amb} | -40 | | +85 | °C |
| Input frequency FMOSCIN, pin 19 | f_{in} | 15 | | 160 | MHz |
| Programmable N, R divider | SF | 2 | | 65535 | |
| Crystal reference oscillator, pins 12 and 13 | fXTAL | 0.1 | | 15 | MHz |

10. Electrical Characteristics

Test Conditions (unless otherwise specified): $V_S = 8.5V$, $T_{amb} = 25^\circ C$.

| No. | Parameters | Test Conditions | Pin | Symbol | Min. | Typ. | Max. | Unit | Type* |
|----------|--|---|-------------|----------------|-----------|-------|-------------|--|--------|
| 1 | Supply Voltage | | | | | | | | |
| 1.1 | Analog supply voltage | | 6 | V_S | 8 | 8.5 | 12 | V | A |
| 2 | Supply Current | | | | | | | | |
| 2.1 | Analog supply current | | 6 | I_S | 5 | 10 | 25 | mA | A |
| 3 | OSCIN | | | | | | | | |
| 3.1 | Input voltage | f = 0.1 to 15 MHz | 13 | OSC | 100 | | | mV _{rms} | B |
| 4 | OSC Buffer (MX2LO) | | | | | | | | |
| 4.1 | Output AC voltage | At pin15: 47 pF and 1 k Ω | 15 | V_{MX2LO} | 80 | 120 | 200 | mV _{pp} | B |
| 4.2 | Output DC voltage | | 15 | V_{MX2LO} | 1.8 | 2.0 | 2.2 | V | A |
| 5 | FMOSCIN | | | | | | | | |
| 5.1 | Input voltage | f = 15 to 120 MHz f = 120 to 160 MHz | 19 | FMOSC FMOSC | 40 150 | | | mV _{rms} mV _{rms} | B B |
| 6 | Pulsed Current Output PD | | | | | | | | |
| 6.1 | Output current B71 to B70 = "00" | PD = 2.5V | 2 | $\pm IPD$ | 20 | 25 | 30 | μA | A |
| 6.2 | Output current B71 to B70 = "01" | PD = 2.5V | 2 | $\pm IPD$ | 80 | 100 | 120 | μA | A |
| 6.3 | Output current B71 to B70 = "10" | PD = 2.5V | 2 | $\pm IPD$ | 400 | 500 | 600 | μA | A |
| 6.4 | Output current B71 to B70 = "11" | PD = 2.5V | 2 | $\pm IPD$ | 1500 | 2000 | 2400 | μA | A |
| 6.5 | Leakage current | PD = 2.5V | 2 | $\pm IPDL$ | | | 20 | nA | A |
| 7 | PDO | | | | | | | | |
| 7.1 | Saturation voltage HIGH | | 3, 4 | | 8.0 | | 8.5 | V | A |
| 7.2 | Saturation voltage LOW | | 3, 4 | | 0 | | 0.4 | V | A |
| 8 | SWO1, SWO2, SWO3, SWO4 (Open Drain) | | | | | | | | |
| 8.1 | Output leakage current HIGH | Pin 7, 8, 9, 10 over R against 8.5V | 7, 8, 9, 10 | I_{SWOH} | | | 100 | nA | A |
| 8.2 | Output voltage LOW | I = 1 mA | 7, 8, 9, 10 | V_{SWOL} | | 100 | 400 | mV | A |
| 9 | DAC1, DAC2 | | | | | | | | |
| 9.1 | Output current | | 3, 4 | $I_{DAC1,2}$ | | | 1 | mA | C |
| 9.2 | Output voltage | | 3, 4 | $V_{DAC1,2}$ | 0.3 | | $V_S - 0.6$ | V | A |
| 9.3 | Maximum offset range (FM) | Offset = 0, Gain = 53 | 3, 4 | | 0.45 | 0.56 | 0.65 | V | A |
| 9.4 | Minimum offset range (FM) | Offset = 63, Gain = 53 | 3, 4 | | -0.45 | -0.57 | -0.65 | V | A |

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

10. Electrical Characteristics (Continued)

Test Conditions (unless otherwise specified): $V_S = 8.5V$, $T_{amb} = 25^\circ C$.

| No. | Parameters | Test Conditions | Pin | Symbol | Min. | Typ. | Max. | Unit | Type* |
|-----------|--|-------------------------|-------------|--------------------------|-------------|------|-------------|----------|-------|
| 9.5 | Maximum gain range (FM) | Gain = 255, Offset = 31 | 3, 4 | | 0.63 | 0.69 | 0.75 | | A |
| 9.6 | Minimum gain range (FM) | Gain = 0, Offset = 31 | 3, 4 | | 2.1 | 2.16 | 2.23 | | A |
| 10 | DAC3 | | | | | | | | |
| 10.1 | Output current | | 5 | I_{DAC3} | | | 1 | mA | C |
| 10.2 | Output voltage | B68 to B66 = "000" | 5 | V_{DAC3} | 0.4 | 0.55 | 0.7 | V | A |
| 10.3 | Output voltage | B68 to B66 = "001" | 5 | V_{DAC3} | 1.1 | 1.25 | 1.4 | V | A |
| 10.4 | Output voltage | B68 to B66 = "010" | 5 | V_{DAC3} | 1.8 | 1.90 | 2.1 | V | A |
| 10.5 | Output voltage | B68 to B66 = "011" | 5 | V_{DAC3} | 2.4 | 2.60 | 2.8 | V | A |
| 10.6 | Output voltage | B68 to B66 = "100" | 5 | V_{DAC3} | 3.2 | 3.30 | 3.5 | V | A |
| 10.7 | Output voltage | B68 to B66 = "101" | 5 | V_{DAC3} | 3.8 | 4.10 | 4.3 | V | A |
| 10.8 | Output voltage | B68 to B66 = "110" | 5 | V_{DAC3} | 4.5 | 4.80 | 5.0 | V | A |
| 10.9 | Output voltage | B68 to B66 = "111" | 5 | V_{DAC3} | 5.2 | 5.45 | 5.7 | V | A |
| 11 | 3-wire Bus, ENABLE, DATA, CLOCK | | | | | | | | |
| 11.1 | Input voltage HIGH LOW | | 16 to 18 | V_{BUSH} V_{BUSL} | 2.7 -0.3 | | 5.3 +0.8 | V V | A |
| 11.2 | Clock frequency | | 17 | | | | 1.0 | MHz | A |
| 11.3 | Period of CLK HIGH LOW | | 17 | t_H t_L | 250 250 | | | ns ns | D |
| 11.4 | Rise time EN, DATA, CLK | | 16 to 18 | t_r | | | 400 | ns | D |
| 11.5 | Fall time EN, DATA, CLK | | 16 to 18 | t_f | | | 100 | ns | D |
| 11.6 | Set-up time | | 16 to 18 | t_s | 100 | | | ns | D |
| 11.7 | Hold time EN | | 18 | t_{HEN} | 250 | | | ns | D |
| 11.8 | Hold time DATA | | 16 | t_{HDA} | 0 | | | ns | D |

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Figure 10-1. Application Circuit

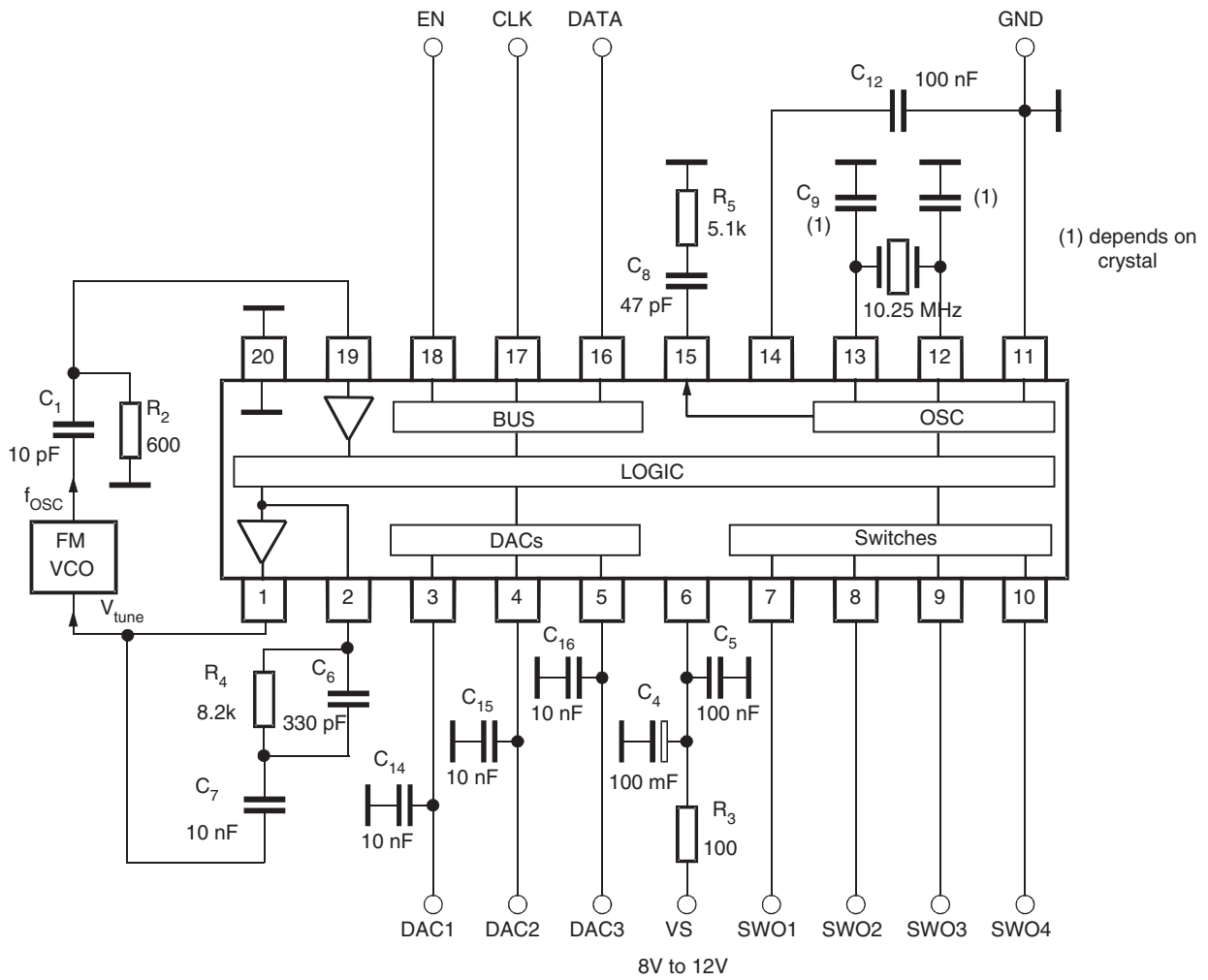
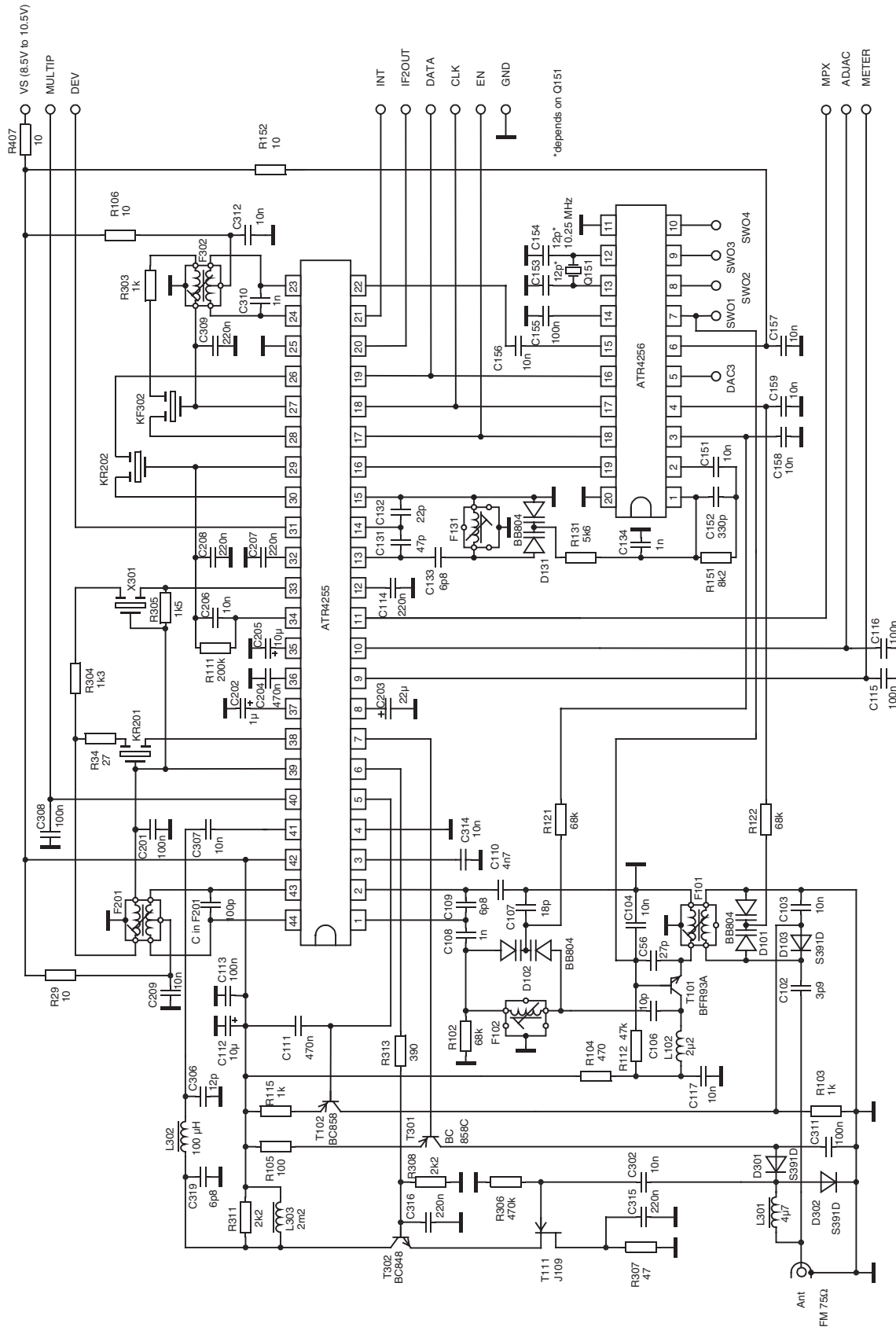


Figure 10-2. Application Board Schematic



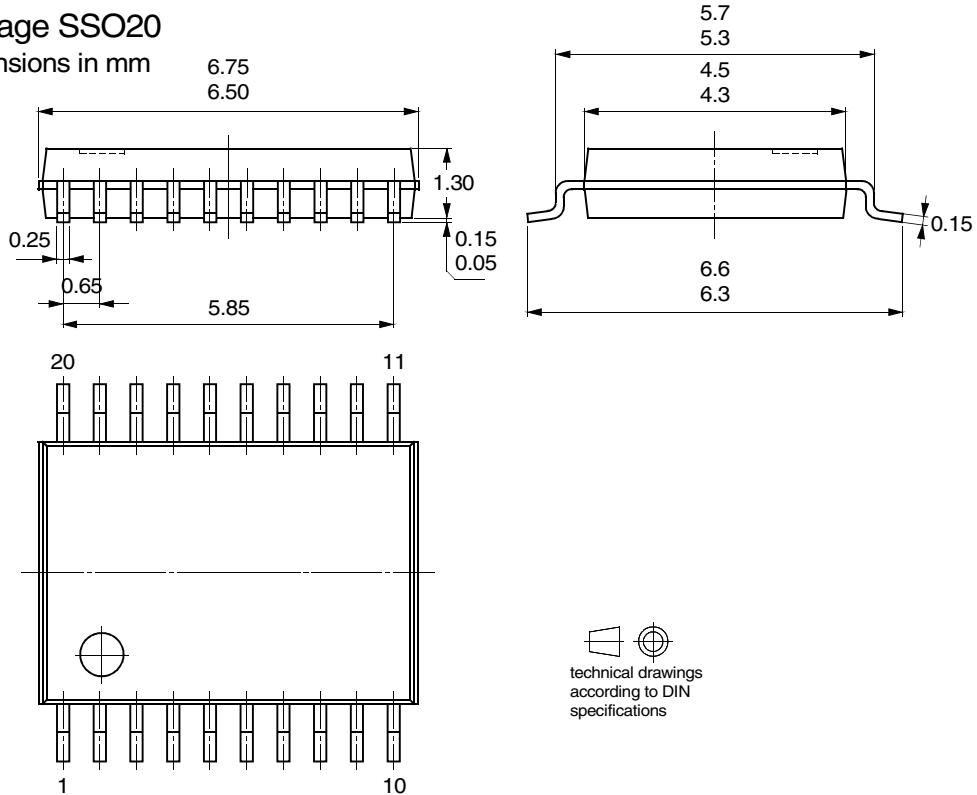
11. Ordering Information

| Extended Type Number | Package | Remarks |
|----------------------|---------|------------------|
| ATR4256-TKSY | SSO20 | Tube |
| ATR4256-TKQY | SSO20 | Taped and reeled |

12. Package Information

Package SSO20

Dimensions in mm



technical drawings
according to DIN
specifications

13. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

| Revision No. | History |
|------------------|--|
| 4867D-AUDR-01/08 | <ul style="list-style-type: none"> Section 9 "Operating Range" on page 15 changed |
| 4867C-AUDR-10/07 | <ul style="list-style-type: none"> Put datasheet in the newest template EI. Char. table: row 5.1 changed |
| 4867B-AUDR-06/06 | <ul style="list-style-type: none"> Put data sheet in a new template Pb-free logo on page 1 deleted |



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