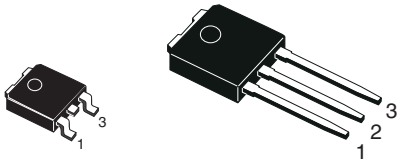
STD90N02L
STD90N02L-1

N-channel 25V - 0.0052Ω - 60A - DPAK - IPAK
STripFET™ III Power MOSFET

Features

Type	V_{DSS}	$R_{DS(on)}$ Max	I_D
STD90N02L	25V	<0.006Ω	60A
STD90N02L-1	25V	<0.006Ω	60A

- $R_{DS(ON)}$ * Qg industry's benchmark
- Conduction losses reduced
- Switching losses reduced
- Low threshold device
- In compliance with the 2002/95/ec european directive



DPAK IPAK

Application

- Switching applications

Description

This series of products utilizes the latest advanced design rules of ST's proprietary STripFET™ technology. This is suitable for the most demanding DC-DC converter application where high efficiency is to be achieved.

Figure 1. Internal schematic diagram

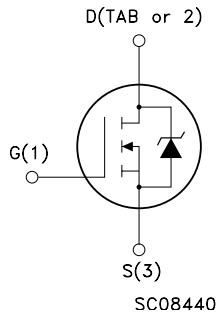


Table 1. Device summary

Order codes	Marking	Package	Packaging
STD90N02L-1	D90N02L	IPAK	Tube
STD90N02L	D90N02L	DPAK	Tape & reel

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{spike} (1)	Drain-source voltage rating	30	V
V_{DS}	Drain-source voltage (V_{GS} = 0)	25	V
V_{DGR}	Drain-gate voltage (R_{GS} = 20kΩ)	25	V
V_{GS}	Gate-source voltage	± 20	V
I_D (2)	Drain current (continuous) at T_C = 25°C	60	A
I_D	Drain current (continuous) at T_C = 100°C	42	A
I_{DM} (3)	Drain current (pulsed)	240	A
P_{TOT}	Total dissipation at T_C = 25°C	70	W
	Derating factor	0.47	W/°C
E_{AS} (4)	Single pulse avalanche energy	360	mJ
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 175	°C

1. Guaranteed when external Rg=4.7Ω and Tf<Tfmax
2. Value limited by wire bonding
3. Pulse width limited by safe operating area
4. Starting Tj = 25°C, I_D = 30A, V_{DD} = 15V

Table 3. Thermal data

Symbol	Parameter	Value	Unit
Rthj-case	Thermal resistance junction-case max.	2.14	°C/W
Rthj-amb	Thermal resistance junction-amb max.	100	°C/W
T_l	Maximum lead temperature for soldering purpose	275	°C

2 Electrical characteristics

(Tcase =25°C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 25mA, V_{GS}= 0	25			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 20V, V_{DS} = 20V,Tc = 125°C			1 10	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ±20V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 250µA	1	1.8		V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS}= 10V, I_D= 30A V_{GS}= 5V, I_D= 15A		0.0052 0.007	0.006 0.011	Ω Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} =10V, I_D = 18A		27		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} =16V, f=1MHz, V_{GS}=0		2050 545 70		pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD}=10V, I_D = 60A V_{GS} =5V *(see Figure 17)*		17 7.7 3.5	22	nC nC nC
R_G	Gate input resistance	f=1MHz Gate DC Bias =0 test signal level =20mV open drain	0.5	1.5	3	Ω
Q_{OSS} (2)	Output charge	V_{DS} =10V, V_{GS} =0V		14		nC

1. Pulsed: pulse duration = 300µs, duty cycle 1.5%
2. Q_{oss}= C_{oss} * D Vin, C_{oss} = C_{gd} + $C_{gd.}$ (see *Buck converter*)

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD}=10V, I_D=30A, R_G=4.7Ω, V_{GS}=5V *(see Figure 16)*		12 110 18 8		ns ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}	Source-drain current Source-drain current (pulsed)				60 240	A A
V_{SD} (1)	Forward on voltage	I_{SD}=30A, V_{GS}=0			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD}=60A, di/dt = 100A/µs, V_{DD}=15V, Tj=150°C *(see Figure 18)*		36 65 3.6		ns nC A

1. Pulsed: pulse duration = 300µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

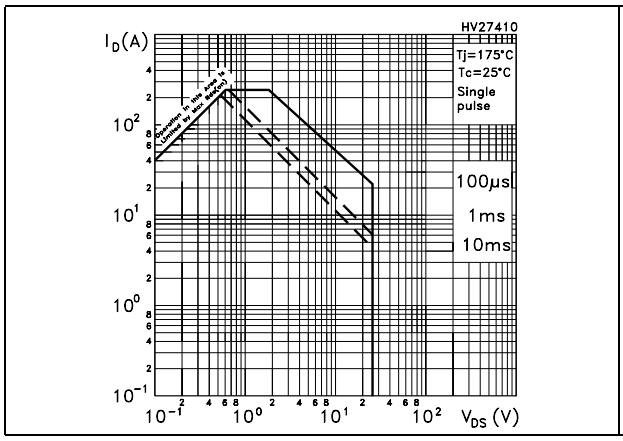


Figure 3. Thermal impedance

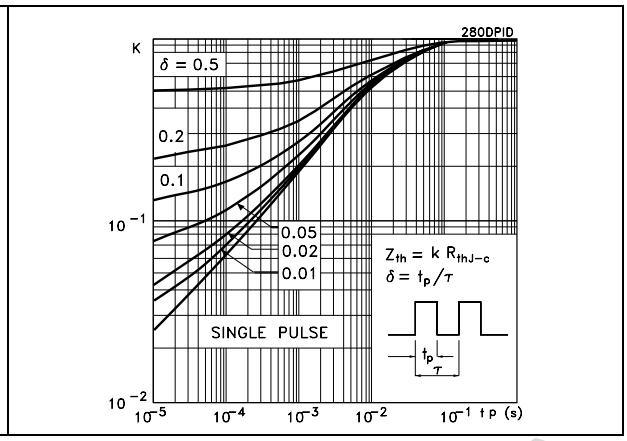


Figure 4. Output characteristics

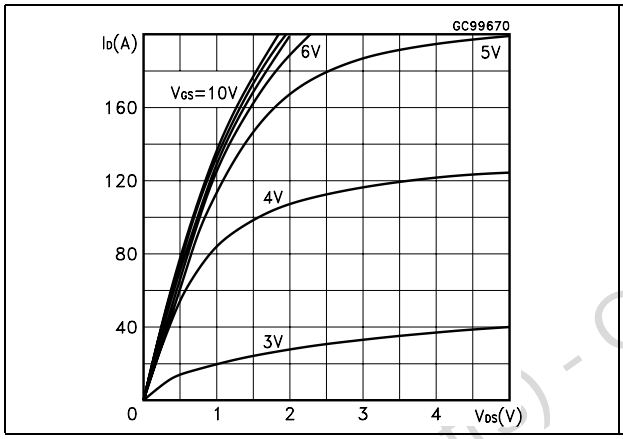


Figure 5. Transfer characteristics

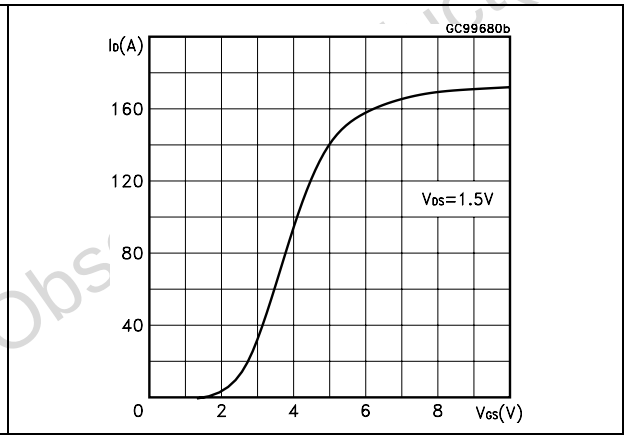


Figure 6. Transconductance

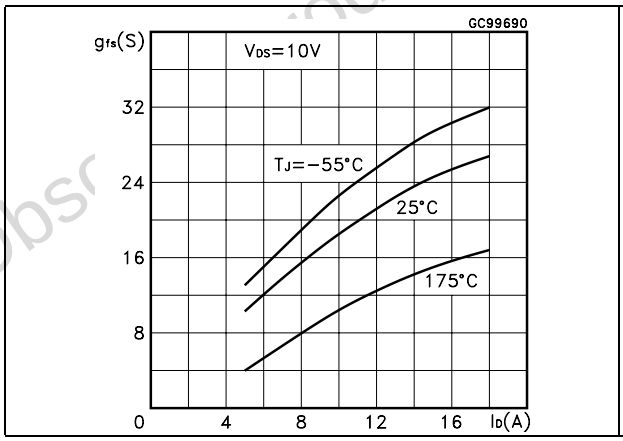


Figure 7. Static drain-source on resistance

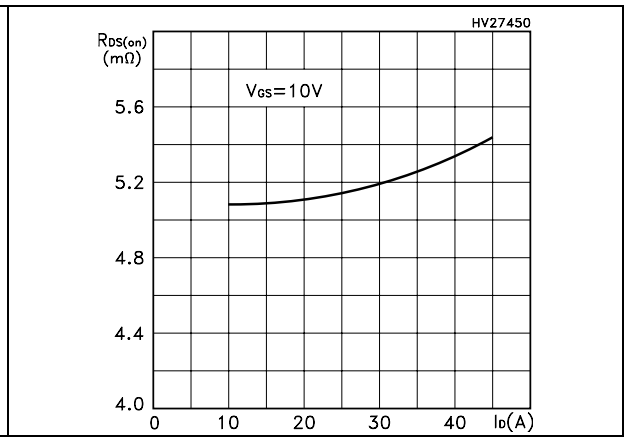


Figure 8. Gate charge vs gate-source voltage

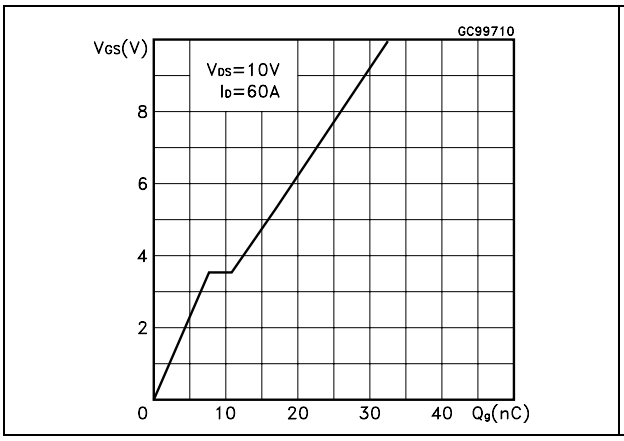


Figure 9. Capacitance variations

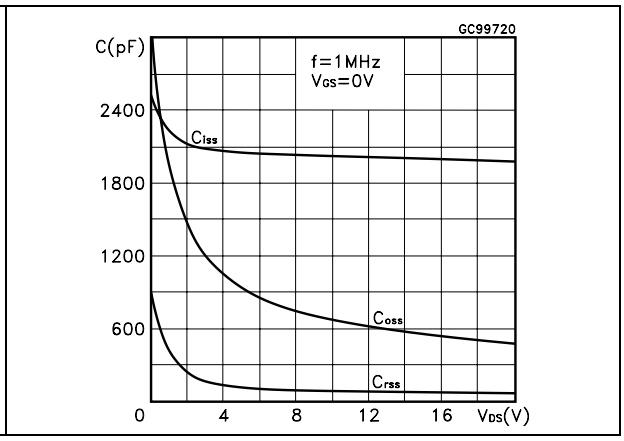


Figure 10. Normalized gate threshold voltage vs temperature

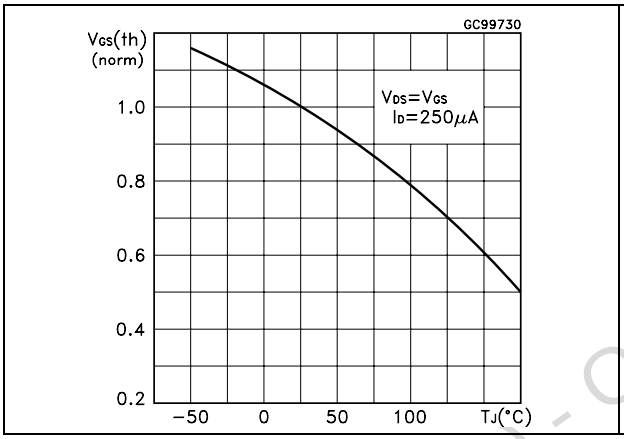


Figure 11. Normalized on resistance vs temperature

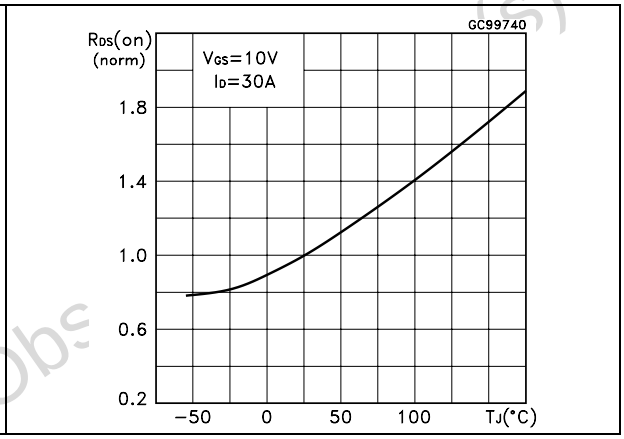


Figure 12. Source-drain diode forward characteristics

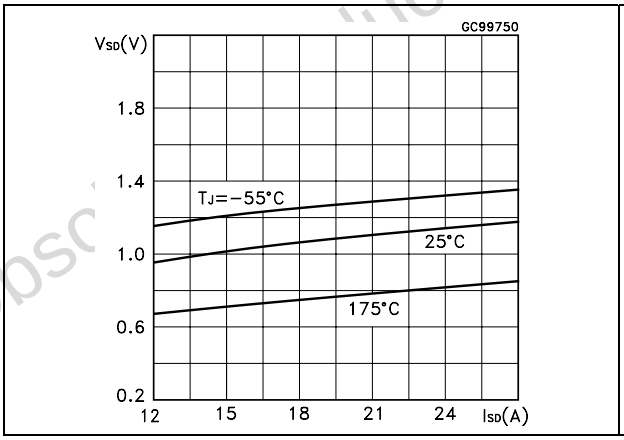


Figure 13. Normalized B_{VDSS} vs temperature

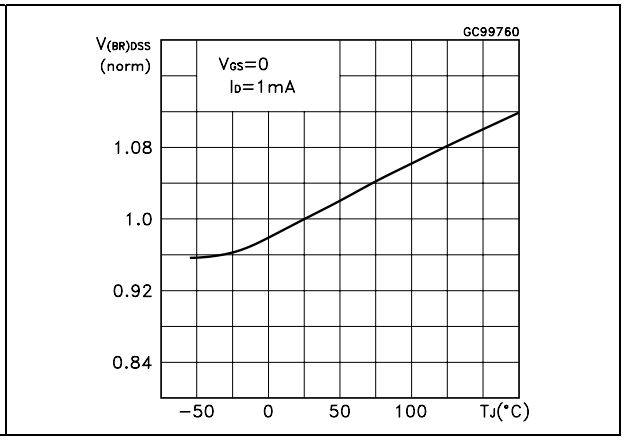
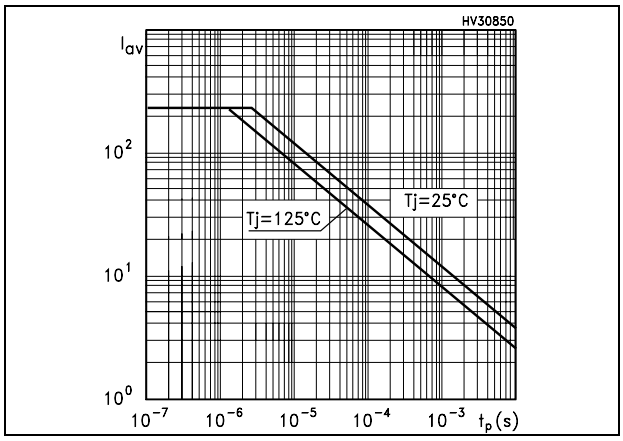


Figure 14. Allowable I_{AV} vs time in avalanche



The previous curve gives the single pulse safe operating area for unclamped inductive loads, under the following conditions:

$P_{D(AVE)} = 0.5*(1.3*B_{VDSS} *I_{AV})$

$E_{AS(AR)} = P_{D(AVE)} *t_{AV}$

Where:

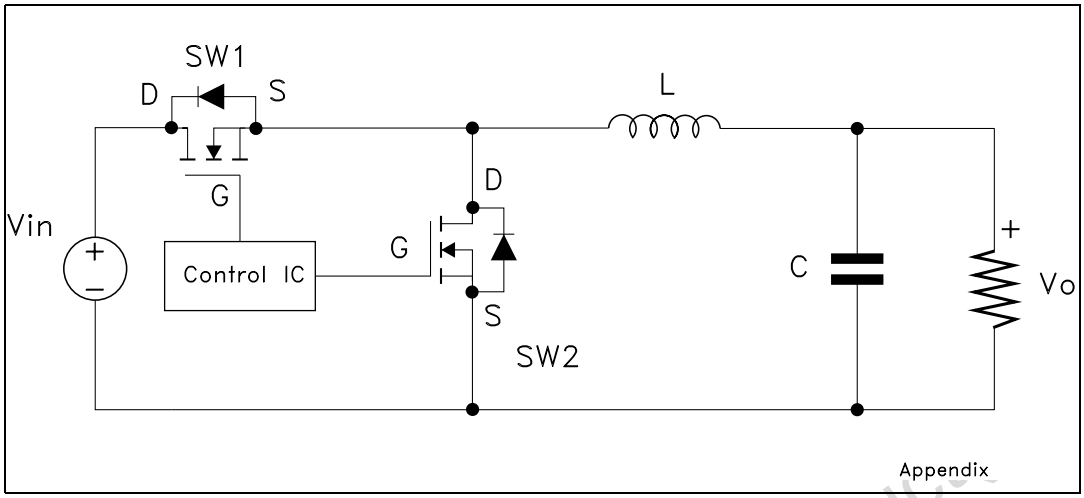
I_{AV} is the allowable current in avalanche

$P_{D(AVE)}$ is the average power dissipation in avalanche (single pulse)

t_{AV} is the time in avalanche

3 Buck converter

Figure 15. Synchronous buck converter



The power losses associated with the FETs in a Synchronous Buck converter can be estimated using the equations shown in the table below. The formulas give a good approximation, for the sake of performance comparison, of how different pairs of devices affect the converter efficiency. However a very important parameter, the working temperature, is not considered. The real device behavior is really dependent on how the heat generated inside the devices is removed to allow for a safer working junction temperature.

The low side (SW2) device requires:

Very low $R_{DS(on)}$ to reduce conduction losses

Small Q_{GLS} to reduce the gate charge losses

Small C_{OSS} to reduce losses due to output capacitance

Small Q_{rr} to reduce losses on SW1 during its turn-on

The C_{gd}/C_{gs} ratio lower than Vth/Vgg ratio especially with low drain to source voltage to avoid the cross conduction phenomenon.

The high side (SW1) device requires:

Small R_G and L_G to allow higher gate current peak and to limit the voltage feedback on the gate

Small Q_G to have a faster commutation and to reduce gate charge losses

Low $R_{DS(on)}$ to reduce the conduction losses

Table 8. Power losses

		High side switch (SW1)	Low side switch (SW2)
$P_{conduction}$		$R_{DS(on)} \bullet I_L^2 \bullet \delta$	$R_{DS(on)} \bullet I_L^2 \bullet (1-\delta)$
$P_{switching}$		$_{in} \bullet (Q_{gsth(SW1)} + Q_{gd(SW1)}) \bullet f \bullet \frac{I}{i}$	Zero voltage switching
P_{diode}	recovery	Not applicable	$^1V_{in} \bullet Q_{rr(SW2)} \bullet f$
	conduction	Not applicable	$V_{f(SW2)} \bullet I_L \bullet t_{deadtime} \bullet f$
$P_{gate(Qg)}$		$Q_{g(SW1)} \bullet V_{gg} \bullet f$	$Q_{gls(SW2)} \bullet V_{gg} \bullet f$
P_{Qoss}		$\frac{V_{in} \bullet Q_{oss(SW1)} \bullet f}{2}$	$\frac{V_{in} \bullet Q_{oss(SW2)} \bullet f}{2}$

Table 9. Power losses parameters

Parameter	Meaning
d	Duty-cycle
Q_{gsth}	Post threshold gate charge
Q_{gls}	Third quadrant gate charge
Pconduction	On state losses
Pswitching	On-off transition losses
Pdiode	Conduction and reverse recovery diode losses
Pgate	Gate driver losses
P_{Qoss}	Output capacitance losses

4 Test circuits

Figure 16. Switching times test circuit for resistive load

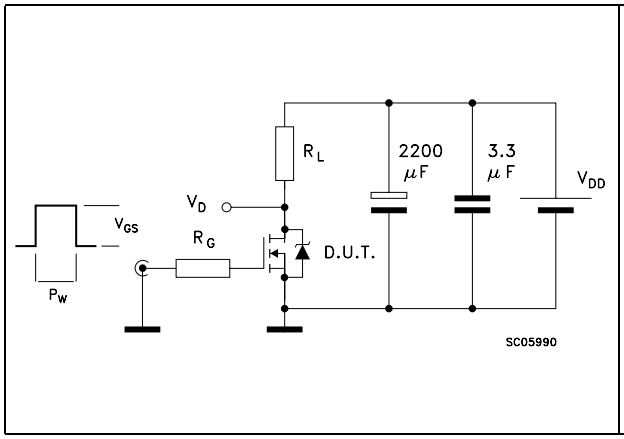


Figure 17. Gate charge test circuit

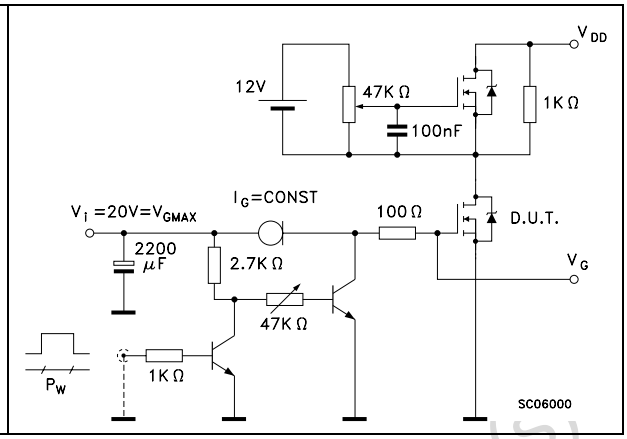


Figure 18. Test circuit for inductive load switching and diode recovery times

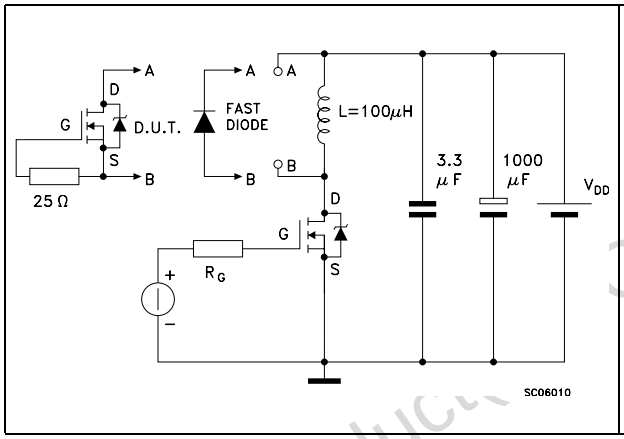


Figure 19. Unclamped inductive load test circuit

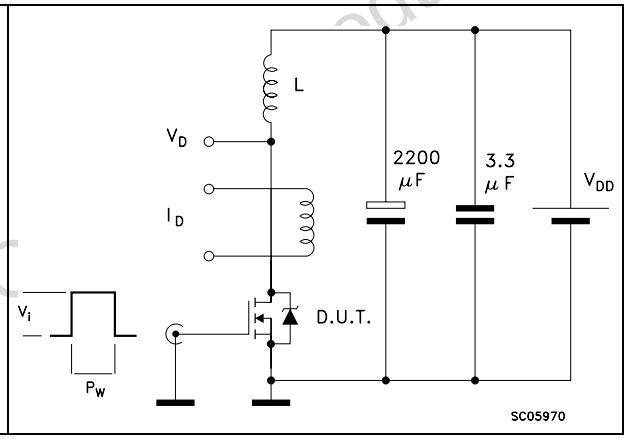


Figure 20. Unclamped inductive waveform

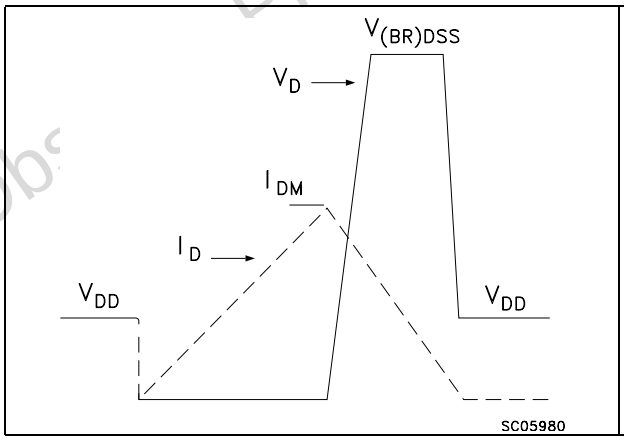
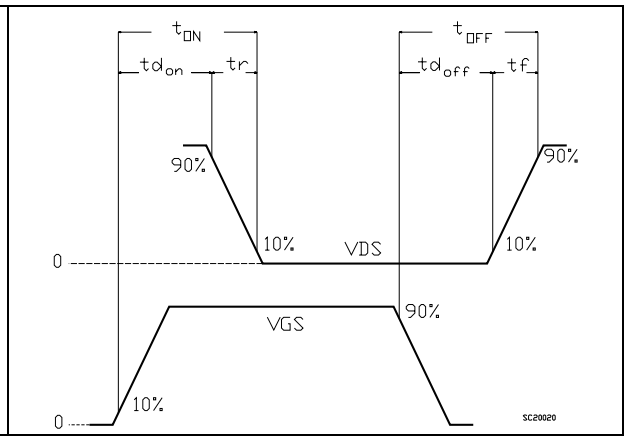


Figure 21. Switching time waveform

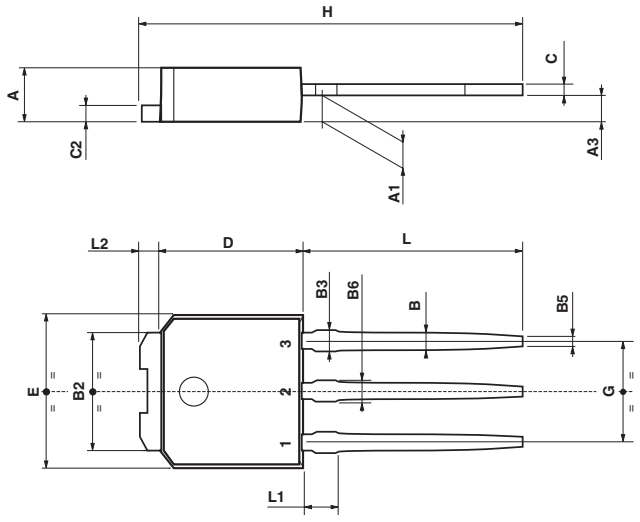


5 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at:*www.st.com*

TO-251 (IPAK) MECHANICAL DATA

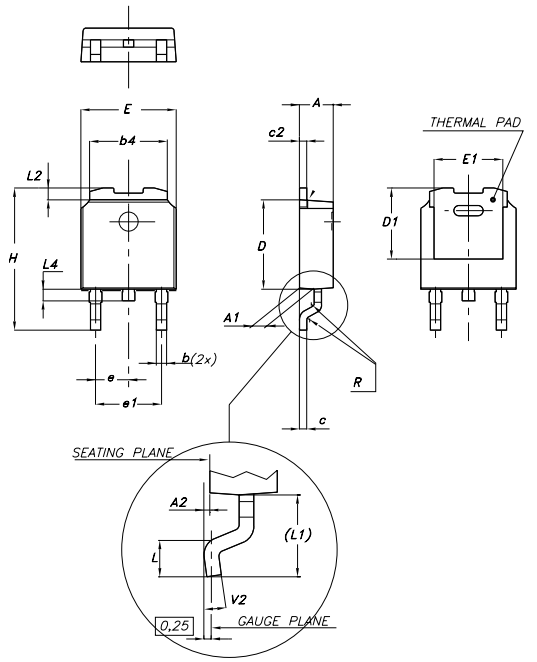
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
B	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039



0068771-E

DPAK MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
b4	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
D1		5.1			0.200	
E	6.4		6.6	0.252		0.260
E1		4.7			0.185	
e		2.28			0.090	
e1	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L	1			0.039		
(L1)		2.8			0.110	
L2		0.8			0.031	
L4	0.6		1	0.023		0.039
R		0.2			0.008	
V2	0°		8°	0°		8°



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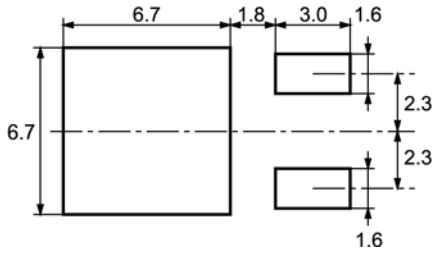
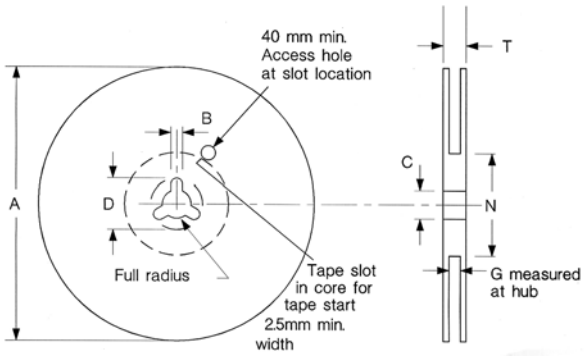
6 Package mechanical data

DPAK FOOTPRINT



All dimensions are in millimeters

TAPE AND REEL SHIPMENT



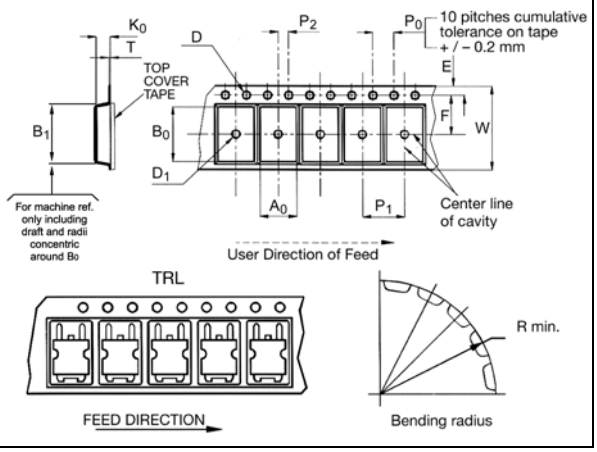
REEL MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	16.4	18.4	0.645	0.724
N	50		1.968	
T		22.4		0.881

BASE QTY	BULK QTY
2500	2500

TAPE MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	6.8	7	0.267	0.275
B0	10.4	10.6	0.409	0.417
B1		12.1		0.476
D	1.5	1.6	0.059	0.063
D1	1.5		0.059	
E	1.65	1.85	0.065	0.073
F	7.4	7.6	0.291	0.299
K0	2.55	2.75	0.100	0.108
P0	3.9	4.1	0.153	0.161
P1	7.9	8.1	0.311	0.319
P2	1.9	2.1	0.075	0.082
R	40		1.574	
W	15.7	16.3	0.618	0.641



7 Revision history

Table 10. Document revision history

Date	Revision	Changes
29-Aug-2005	1	First release
07-Apr-2006	2	New template
03-May-2006	3	New value on *Table 4*, new curve *(see Figure 14)*
24-Oct-2007	4	Corrected value on *Table 6*, Updated BV_{dss} value

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