

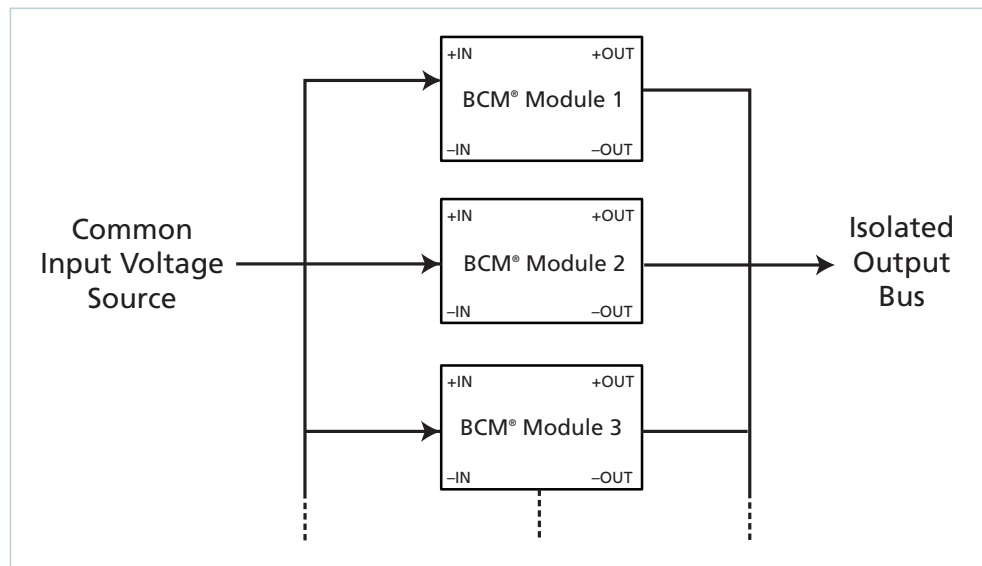
Using BCM® Bus Converters in High Power Arrays

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Contents	Page	Introduction
Introduction	1	This application note provides methods and guidelines for designing BCM® bus converters into high power arrays.
Theory	1	
Design	1	Theory
Symmetrical Input / Output Resistances	2	BCM modules current share when their respective inputs and outputs are connected in parallel. Sharing accuracy is a function of a) input and output interconnect impedance matching, b) the output impedances (R_{OUT}) of the BCM modules, and c) uniform cooling.
R_{OUT} Matching	2	
Uniform Cooling	3	In theory, a very large number of modules can be paralleled. In practice arrays larger than 10 become difficult due to "a" and "c" above. Please contact Vicor Applications Engineering if you are designing an array with more than 10 modules.
Arrays Powered From Multiple Inputs	3	
Design Example	4	Since bus converters are isolated transformers, their outputs may be paralleled with inputs powered from different sources. The lower the R_{OUT} of the module, the more closely input voltages must match to avoid excessive current imbalance. As such, the input voltages must be equal to ensure evenly distributed sharing.
General Guidelines	6	
Conclusion	6	

Figure 1.
 BCM parallel array block diagram

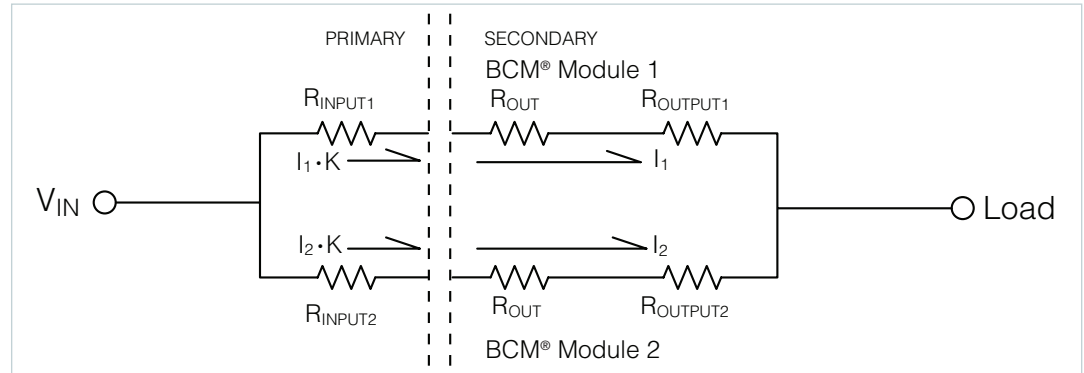


Symmetrical Input / Output Resistances

The primary design concern for a high power array is the layout of a symmetrical input and output feed. Figure 2 represents a simplified model of BCM® bus converter sharing for an array of 2.

In this case, the circuit has been reduced to its core elements and each BCM module is represented as a resistor with resistance R_{OUT} . This model can easily be expanded to represent larger arrays.

Figure 2.
Simplified model of BCM®
module sharing



If $R_{INPUT1} = R_{INPUT2}$ and $R_{OUTPUT1} = R_{OUTPUT2}$ then the current through both legs will be equal. An increase in $R_{OUTPUT1}$ will decrease I_1 proportionally. It is important to note, however, that an increase in R_{INPUT1} will decrease I_1 to the square of the K factor. For BCM modules having a small K factor ($\ll 1$) the matching of the input impedance is less critical. For example, assume the following:

$$K = 1/32$$

$$R_{OUT} = 10 \text{ mohm}$$

$$R_{OUTPUT1} = R_{OUTPUT2} = R_{INPUT1} = 0.$$

$$R_{INPUT2} = 1 \text{ ohm}$$

$$\text{Solving for } \frac{I_1}{I_2} :$$

$$I_1 \cdot R_{OUT} + (I_1 \cdot K \cdot R_{INPUT1}) \cdot K = I_2 \cdot R_{OUT} + (I_2 \cdot K \cdot R_{INPUT2}) \cdot K$$

$$R_{INPUT1} = 0 \text{ so:}$$

$$I_1 \cdot R_{OUT} = I_2 \cdot R_{OUT} + I_2 \cdot K_2 \cdot R_{INPUT2}$$

Substituting values yields:

$$I_1 \cdot \frac{1}{100} = I_2 \cdot \left(\frac{1}{100} + \frac{1}{1024} \right)$$

$$\frac{I_1}{I_2} = \frac{11}{10}$$

This indicates that BCM module 1 carries approximately 10% more current with a 1 ohm impedance in series with the input of BCM module 2 for $K=1/32$. However, if K were equal to 1, then BCM module 1 would carry essentially 100% of the current.

R_{OUT} Matching

R_{OUT} is specified as a range in the BCM® bus converter data sheet and has a positive temperature coefficient with the specified range that reinforces sharing. As the modules temperature increases due to increased dissipation, the R_{OUT} increases. This decreases the amount of current flowing through that BCM module in an array, reducing the module power dissipation.

Uniform Cooling

Due to the positive temperature coefficient of R_{OUT}, BCM modules mounted close to each other and cooled equally will tend to equalize power dissipation.

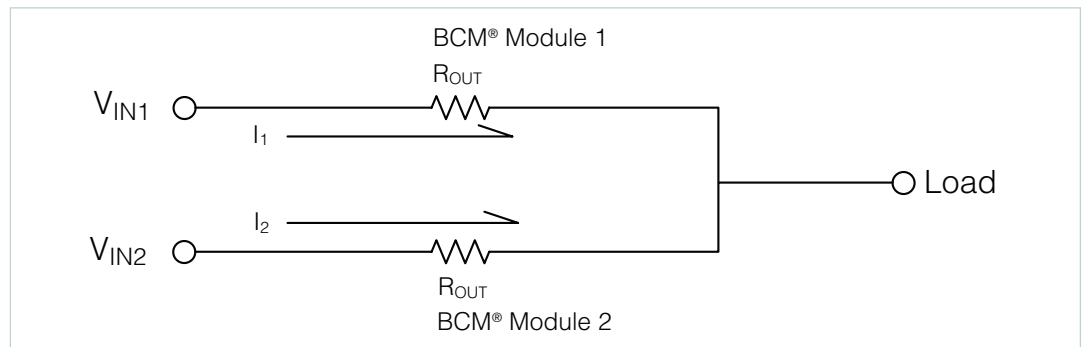
The true power limitation on the module is based on dissipation. Therefore, the module that has a lower R_{OUT} may have a higher current when connected in an array (thus a higher power), but given that its dissipation is the same as neighboring units in an array, it will have similar MTBF characteristics.

The power rating of an array of BCM modules is equal to the power rating of the individual module times the number of modules in an array. Even under the ideal circumstances, the current through each module will not be equal, so under full power conditions the current may not be perfectly balanced. However, assuming that the module array is cooled equally, and the input and output impedances are matched, a current imbalance is acceptable if the dissipation of this BCM module is the same as others in the array. It is important never to exceed the maximum rated DC current of the module under any circumstances.

Arrays Powered From Multiple Inputs

Figure 3 addresses an arrangement in which the BCM modules are powered from separate inputs.

Figure 3.
Parallel arrays from separate inputs



In this example, input and output impedances are considered negligible. If V_{IN1} = V_{IN2} then the currents in both legs are equal. However assume the following:

$$V_{IN1} = 48 \text{ V}$$

$$V_{IN2} = 49 \text{ V}$$

$$R_{OUT} = 1 \text{ mohm}$$

$$K = 1/32$$

$$I_{LOAD} = 100 \text{ A}$$

The two BCM modules must satisfy the following equation:

$$V_{IN1} \cdot K \cdot I_{OUT1} \cdot R_{OUT} = V_{IN2} \cdot K \cdot I_{OUT2} \cdot R_{OUT}$$

Also,

$$I_{OUT1} + I_{OUT2} = 100 \text{ A}$$

Solving the simultaneous equations for I_{OUT1} and I_{OUT2} yields:

$$I_{OUT1} = 35 \text{ A}$$

$$I_{OUT2} = 65 \text{ A}$$

The same technique can be extended to include arrays with a larger number of BCM modules.

If $V_{IN1} - V_{IN2} > I_{OUT1} \cdot R_{OUT}$, then BCM® module 1 will attempt to backfeed current through BCM module 2 to increase V_{IN2} . To prevent reverse current in this situation, diodes can be added in series with +In of each BCM module.

Design Example

Figure 4 shows an example array of 7 high voltage input 300 W BCM bus converters to provide a total power of 2.1 kW. Table 1 illustrates the measured currents for the laboratory layout shown in Figure 5. Even with less than ideal layout conditions (long wires, separate boards, use of standoffs to carry current), the overall sharing of the array is within 5%.

BCM modules switch at >1 MHz and have an effective output ripple of 2 times the switching frequency, so output filtering is provided using a small point-of-load capacitor in conjunction with trace inductance. The use of the input inductors confines the high-frequency ripple current of each module. Some input inductance between the modules inputs is necessary to minimize interactions between parallel connected modules and allow for proper operation for the array. Input inductance also reduces EMI and promotes the overall stability of the system by reducing (or eliminating) beat frequencies caused by the asynchronous switching of the BCM modules.

Connecting the PC pins of the BCM modules in the array allows all units in the array to be enabled and disabled simultaneously. Simultaneous startup is required in cases where the array will start up into more current than one BCM module is sized to handle.

Figure 4.
BCM® bus converter array
using 7 modules

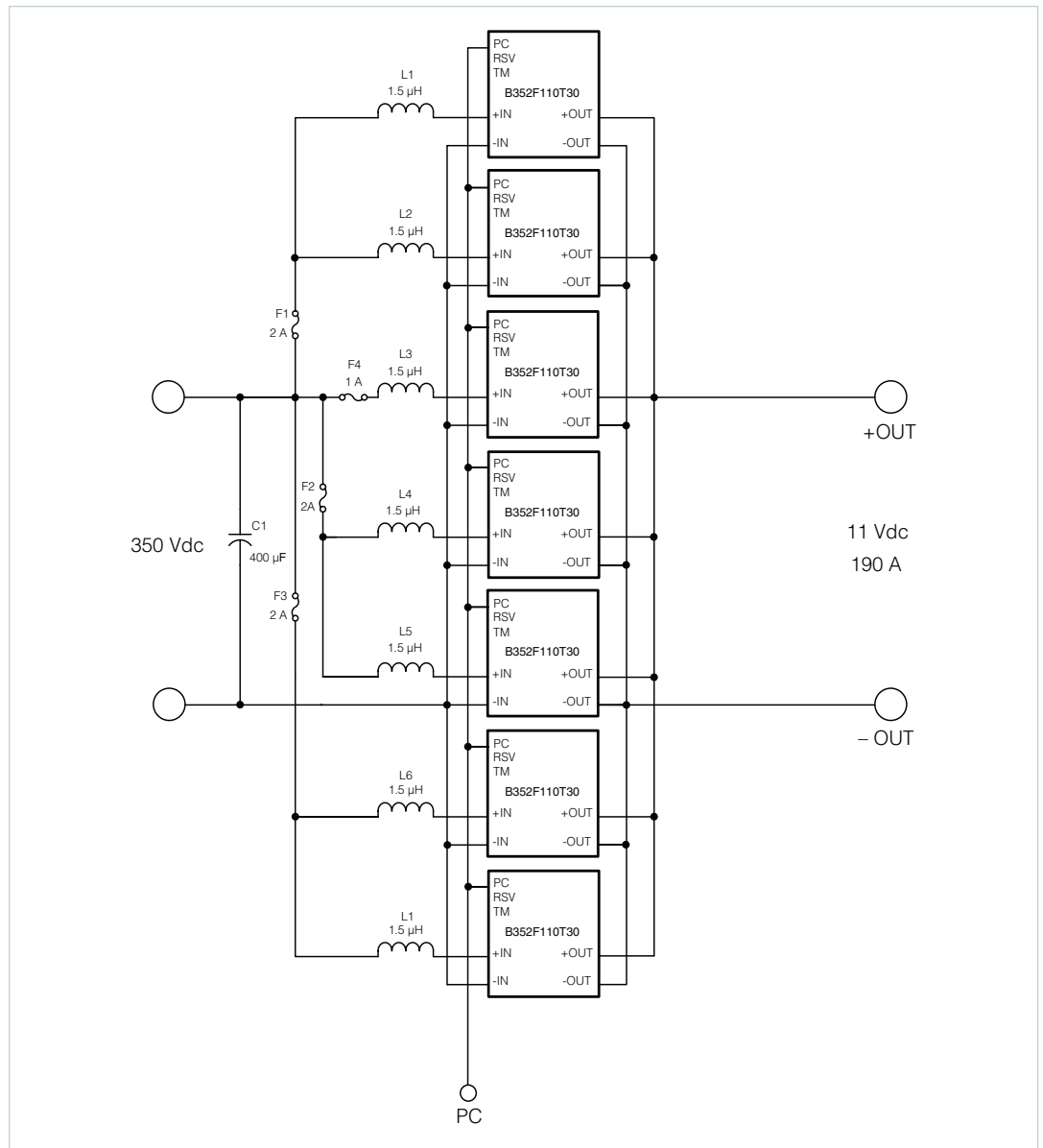
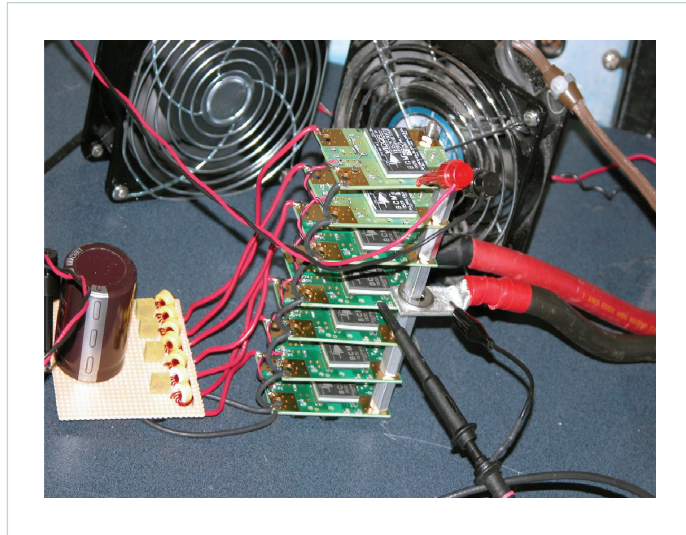


Table1.
7 BCM® bus converter array
current sharing

Module #	48 A Load (6.86 A / BCM)		95 A Load (13.6 A / BCM)		143 A Load (20.4 A / BCM)		192 A Load (27.5 A / BCM)	
	I _{BCM}	% Deviation	I _{BCM}	% Deviation	I _{BCM}	% Deviation	I _{BCM}	% Deviation
U1	5.9	14.0	12.6	7.4	19.2	5.9	27.6	0.4
U2	7.1	3.4	13.2	2.9	19.9	2.5	27.3	0.7
U3	6.7	2.4	13.6	0.0	20.6	1.0	27.7	0.7
U4	7.4	7.9	14.4	5.9	21.3	4.4	27.4	0.4
U5	7.1	3.4	14.0	2.9	20.8	2.0	27.5	0.0
U6	7.2	5.0	14.0	2.9	20.9	2.5	27.7	0.7
U7	6.8	0.9	13.5	0.7	20.4	0.0	27.2	1.1
Worst Case deviation from nominal (%)		14.0		7.4		5.9		1.1

Figure 5.
Laboratory demonstration
of the 7 BCM®
bus converter array



General Guidelines

1. Always ensure that the BCM® bus converters are fused according to safety agency requirements.
2. PC pins of BCM modules should be connected together to enable and disable the modules simultaneously.
3. All signal and power traces should be laid out on the PCB to minimize noise coupling and impedance. For more details on PCB layout guidelines, please see [AN:005](#).
4. An inductor should be placed in series with the +In of each BCM bus converter in the array to minimize high frequency circulating currents in the primary as well as beat frequencies caused by asynchronous switching.
5. BCM modules fed from different sources with outputs in parallel must have appropriately matched inputs as the input voltage matching plays a critical role in current sharing.
6. In large arrays, routing issues may cause mismatching input and output impedances to each BCM module. In that case, varying trace widths should be used to equalize impedances between close and distant modules.
7. In large arrays, it may be difficult to match cooling for each BCM module in the array. In that case, heat sink design or airflow routing should be adjusted to equalize module cooling as much as possible. To optimize reliability, overall temperature should be as low as possible.
8. Load capacitors should be placed near the load. Refer to the BCM datasheet for the maximum output capacitor value in an array. In cases where the load bypassing capacitance must be placed near the BCMs, they should be created with individual capacitors distributed across each BCM output, rather than lumped on a single BCM output.

Conclusion

High power arrays can be created using the bus converters in parallel provided that care is taken in designing the input and output connections. BCM modules share inherently with inputs and outputs connected in parallel, with the positive temperature coefficient of R_{OUT} reinforcing sharing. Assuming equal cooling, an array can operate at full power with accurate sharing and no derating. The array should be designed based on guidelines that optimize protection, efficiency, reliability, and minimize noise.

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