MX29VS128F

MULTIPLEXED, Burst Mode

Read While Write Flash Memory

Contents

1. FEATURES

Characteristics

Burst Length

- Burst Mode - Continuous linear
- Linear burst length - 8/16 word with wrap around

Sector Architecture

- Multi-bank Architecture (8 banks)
- Read while write operation
- Four 16 Kword sectors on top/ bottom of address range
- 127 sectors are 64 KWord sectors

Power Supply Operations

- 1.8V for read, program and erase operations (1.70V to 1.95V)
- Deep power down mode

Performance

High Performance

- 30 µs - Word programming time
- 7.5 µs - Effective word programming time utilizing a 32 word Write Buffer at VCC level
- 2.5 µs - Effective word programming time of utilizing a 32 word Write Buffer at ACC level

Sector Erase Time

- 500 ms for 16 Kword sectors
- 1000 ms for 64 Kword sectors

Read Access Time

- Burst access time: 7 ns (at industrial temperature range)
- Asynchronous random access time: 80 ns
- Synchronous random access time: 75 ns

Secure Silicon Sector Region

- 128 words for the factory & customer secure silicon sector

Power Dissipation

- Typical values: 8 bits switching,
  CL = 10 pF at 108 MHz, CIN excluded
- 20 mA for Continuous burst read mode
- 30 mA for Program/Erase Operations (max.)
- 30 uA for Standby mode

Program/Erase Cycles

- 100,000 cycles typical

Data Retention

- 20 years

Hardware Features

- Supports multiplexing data and address for reduced I/O count.
- A15–A0 multiplexed as Q15–Q0 Sector Architecture

Hardware Sector Protection

- All sectors locked when WP#/ACC = VIL

Package

- 56-Ball Thin FBGA (Fine-Pitch Ball Grid Array)
- All packaged devices are RoHS Compliant and Halogen-free.

Handshaking Feature

- Allows system to determine the read operation of burst data with minimum possible latency by monitoring RDY.

Software Features

Advanced Security Features

- Volatile Sector Protection
- A command sector protection method that protects individual sectors from being programmed or erased.
- Secured Silicon Sectors can be locked or in-system at VCC level.

Electronic Identification

- Software command set compatible with JEDEC 42.4 standards
- Common Flash Interface (CFI) supported

Erase Suspend/Erase Resume

- Erase operation will be halted when the bank receives an Erase Suspend command. And will be restarted when the bank receives the Erase Resume command.

Program Suspend/Program Resume

- Program operation will be halted when the bank receives a Program Suspend command. It will be restarted when the bank receives the Program Resume command.

Write Condition Bits

- Provides a software method of providing write condition bits to indicate the status of program and erase operations.

2. GENERAL INFORMATION

2-1. Operating Speeds

Clock Speed	Burst Access (ns)	Synch. Initial Access (ns)	Asynch. Initial Access (ns)	Output Loading
108 MHz	7	75	80	10 pF

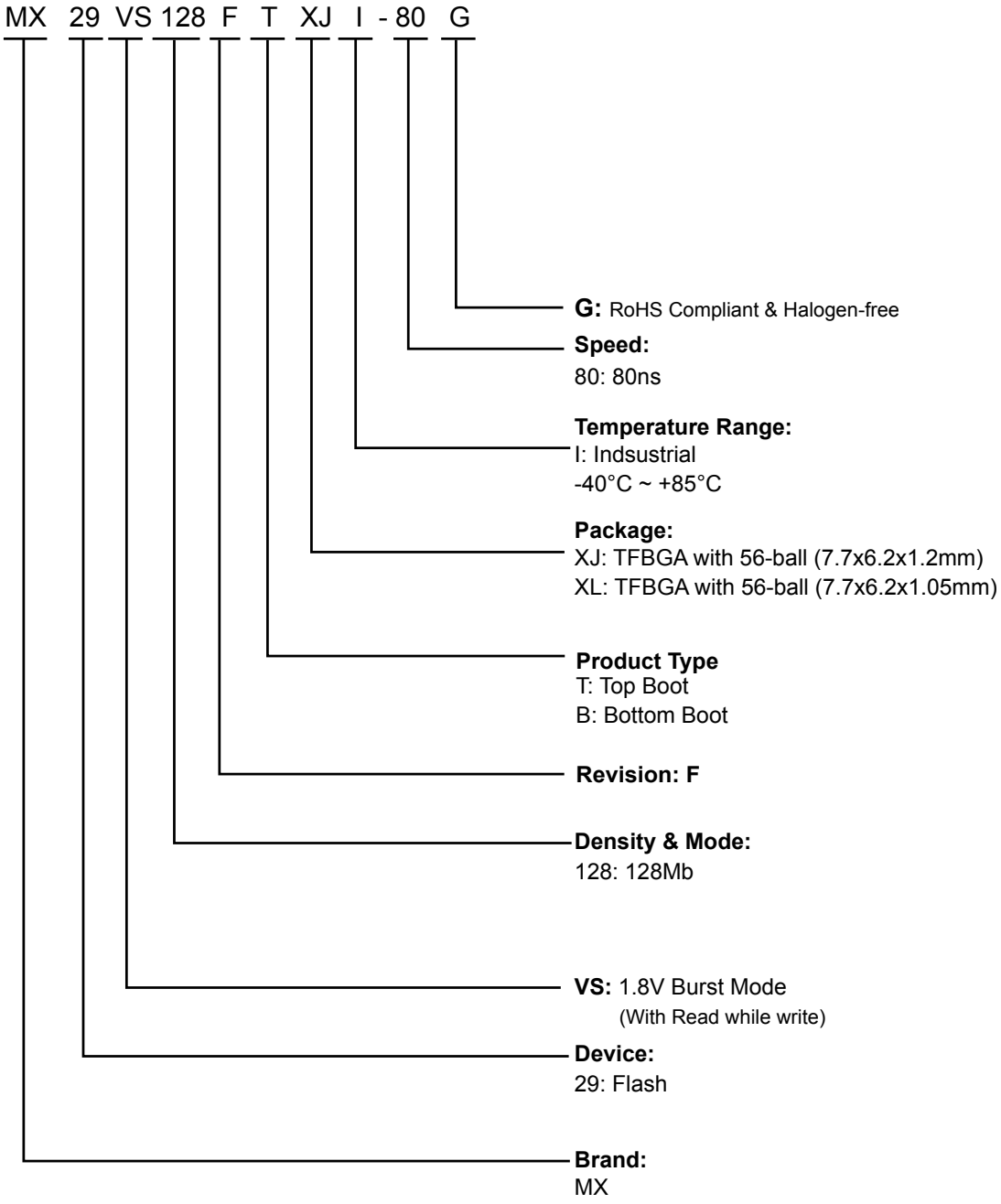
The operating temperature range is from -40°C to +85°C.

2-2. Ordering Information

Part Number	Access Time (ns)	Package	Remark
MX29VS128FTXJI-80G	80	56 TFBGA	VI/O=VCC
MX29VS128FBXJI-80G	80	56 TFBGA	VI/O=VCC
MX29VS128FTXLI-80G*	80	56 TFBGA	VI/O=VCC
MX29VS128FBXLI-80G*	80	56 TFBGA	VI/O=VCC

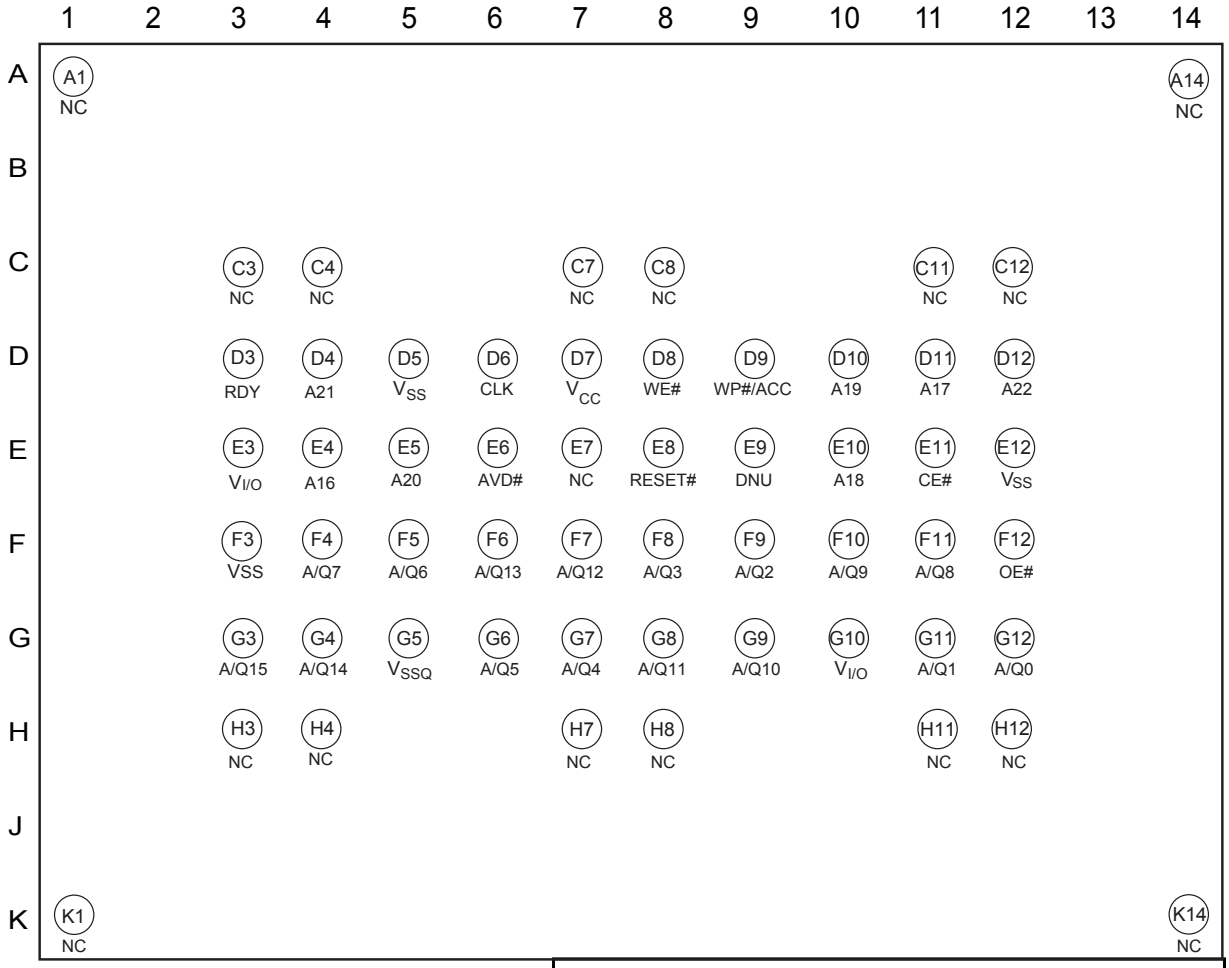
***NOTE**: * = Advanced Information*

2-3. Part Name Description

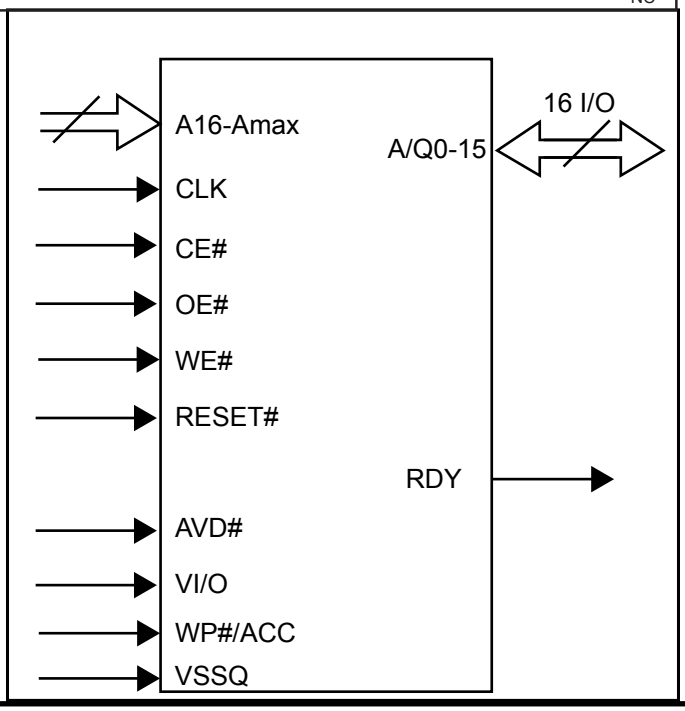


3. PIN CONFIGURATION / SYMBOL DESCRIPTION

56-Ball Thin FBGA



3-1. Logic Symbol



3-2. Pin Descriptions

SYMBOL	DESCRIPTIONS		
A22-A16	Input pins for Address		
A/Q15-A/Q0	Input pins for Address and Multiplex Input/Output pins for Data		
WP#/ACC	Write Protect/Input pin for Programming Acceleration		
AVD#	An Input pin for Address Valid, to indicate the following input are address information or data information. (A/Q15-A/Q0 are multiplex pins and A22-A16 are address pins only)		
	VIL	Asynchronous Mode	To indicate valid address
		Burst Mode	To latch starting address on rising edge of CLK
	VIH	Data will be inputted from A/Q15-A/Q0, A22-A16 will be ignored by device.	
CE#	Input pin for Chip Enable		
CLK	The first rising edge of CLK pin will start when both AVD# low latches address input and activates burst mode operation.		
NC	No Connection		
OE#	Input pin for Output Enable		
RESET#	Input pin for Hardware Reset, reset operation starts when voltage goes low.		
RDY	Output pin for Ready signal. For further information please refer to Configuration Register Table.		
VCC	Power Supply pin (1.70V-1.95V) for Device		
VI/O	Power Supply pin (1.70V-1.95V) for Input/Output		
WE#	Input pin for Write Enable		
VSS	Ground pin for Device		
VSSQ	Ground pin for Input/Output		
DNU	Do Not Use (DNU pin can be connected to VCC, Ground, Floating, but cannot connect to voltage > 1.5Vcc)		

***NOTES**:*

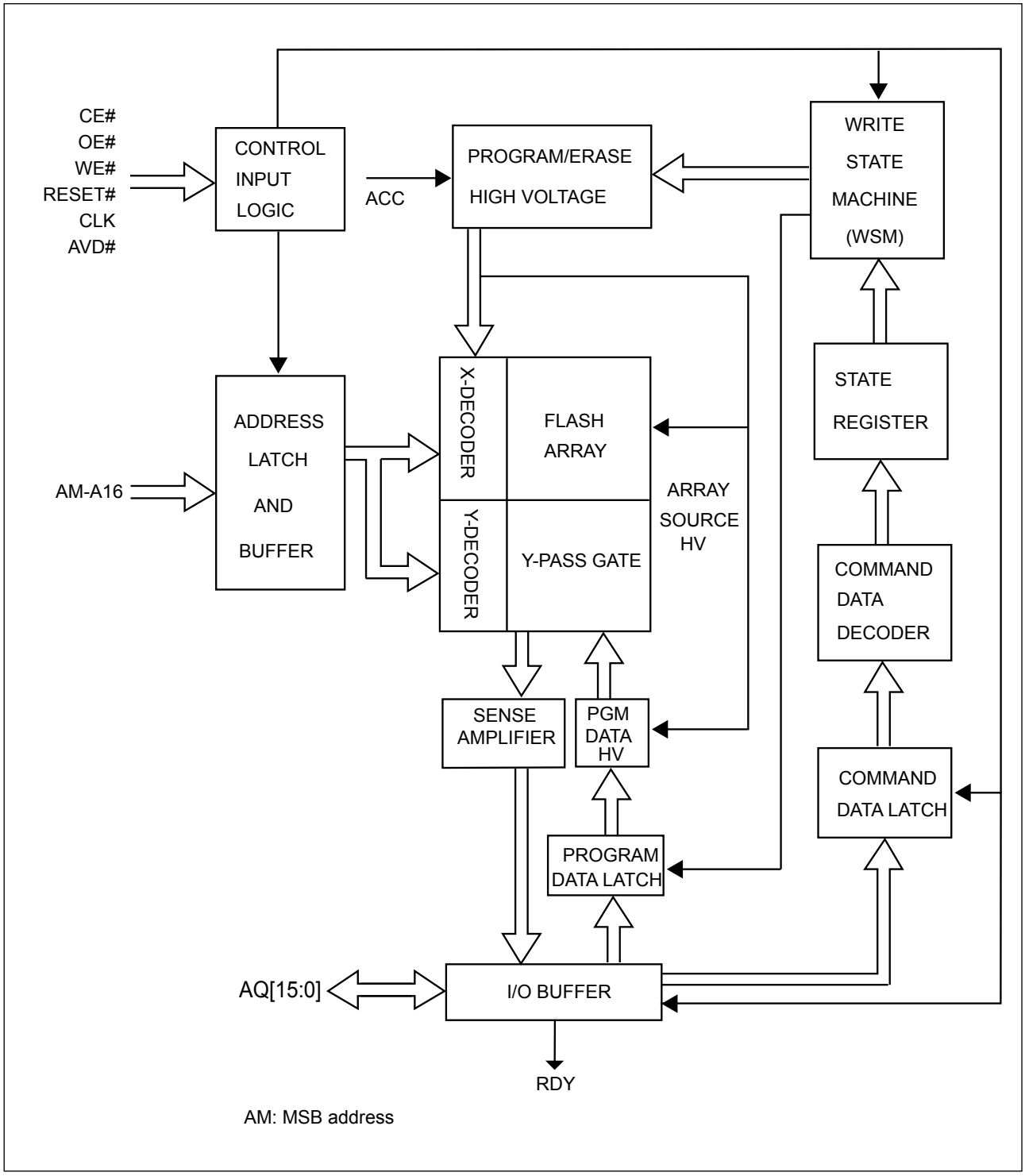
1. *WP#/ACC=Vhv enters into the ACC programming mode. WP#/ACC=VIL, erase/program function disabled.*

   WP#/ACC should keep VIH for all other cases. It must not be left floated or unconnected; inconsistent behavior of the device may result.

2. *VI/O Voltage must tight up with VCC.*

   VI/O = VCC = 1.70V to 1.95V

4. BLOCK DIAGRAM



4-1. Block & Address Structure

The main flash memory array is organized as Word mode (x16). The details of the address ranges and the corresponding sector addresses are shown in Table 1.

The device is consisted of five memory address areas as below:

- Main Flash Array area
- Secured Silicon Sector area
- Device ID & CFI area
- Configuration Register area
- SSS (Secured Silicon Sector) Lock Bit

To facilitate the data read flexibility, this device enables the "Address Mapping" feature that could have user to define the non-main array areas to be read as the main array area by mapping the address into the intended main array.

For address range being marked as mapping area but not defined will output invalid data.

Each bank can be operated in the following three modes:

- Normal Read Mode

- Program/Erase (PE) Mode

- Address Mapping (AM) Mode

First two modes can be operated in any bank, but AM mode can only be operated in bank0. In addition, at any time, only one bank is available to use the PE or AM mode.

- **Normal Read Mode:** The device will be in Normal Read Mode in following status: Hardware Reset, Power on, command reset, Exit from PE mode.
- **PE Mode:** The Program & Erase operation can be conducted in the bank, however, in the same bank, no read is allowed. Other non-PE-mode banks are available for Read operation at the same time. This is the "Read-While-Write" operation.
- **AM Mode:** One of the non-main-aray address is mapped in a bank. Only one bank may be in AM mode, all other banks may not be in AM or PE mode. Before entering AM mode, all P/E operation should be finished. The attempt of entering PE mode or AM mode when the other bank is in PE or AM mode will be ignored.

Simultaneous operation of one bank in AM mode, the other bank for Normal Read mode is allowed.

The AM mode can only be operated in lowest address bank. The mapping address of AM mode should be within the assigned lowest address bank address area.

- The Secured Silicon Sector, SSS Lock bit, and Configuration Register can be programmed in AM mode per the mapped address. During above operation, it switches from AM mode to PE mode. Device ID/ CFI is factory programming only.

Table 1-1. Sector Address Table (Top Boot)

Bank	Sector Size (Kwords)	Sector	Address Range
0	64	SA0	000000h-00FFFFh
	64	SA1	010000h-01FFFFh
	64	SA2	020000h-02FFFFh
	64	SA3	030000h-03FFFFh
	64	SA4	040000h-04FFFFh
	64	SA5	050000h-05FFFFh
	64	SA6	060000h-06FFFFh
	64	SA7	070000h-07FFFFh
	64	SA8	080000h-08FFFFh
	64	SA9	090000h-09FFFFh
	64	SA10	0A0000h-0AFFFFh
	64	SA11	0B0000h-0BFFFFh
	64	SA12	0C0000h-0CFFFFh
	64	SA13	0D0000h-0DFFFFh
	64	SA14	0E0000h-0EFFFFh
	64	SA15	0F0000h-0FFFFFh
1	64	SA16	100000h-10FFFFh
	64	SA17	110000h-11FFFFh
	64	SA18	120000h-12FFFFh
	64	SA19	130000h-13FFFFh
	64	SA20	140000h-14FFFFh
	64	SA21	150000h-15FFFFh
	64	SA22	160000h-16FFFFh
	64	SA23	170000h-17FFFFh
	64	SA24	180000h-18FFFFh
	64	SA25	190000h-19FFFFh
	64	SA26	1A0000h-1AFFFFh
	64	SA27	1B0000h-1BFFFFh
	64	SA28	1C0000h-1CFFFFh
	64	SA29	1D0000h-1DFFFFh
	64	SA30	1E0000h-1EFFFFh
	64	SA31	1F0000h-1FFFFFh
2	64	SA32	200000h-20FFFFh
	64	SA33	210000h-21FFFFh
	64	SA34	220000h-22FFFFh
	64	SA35	230000h-23FFFFh
	64	SA36	240000h-24FFFFh
	64	SA37	250000h-25FFFFh
	64	SA38	260000h-26FFFFh
	64	SA39	270000h-27FFFFh
	64	SA40	280000h-28FFFFh
	64	SA41	290000h-29FFFFh
2	64	SA42	2A0000h-2AFFFFh
	64	SA43	2B0000h-2BFFFFh
	64	SA44	2C0000h-2CFFFFh
	64	SA45	2D0000h-2DFFFFh
	64	SA46	2E0000h-2EFFFFh
	64	SA47	2F0000h-2FFFFFh
3	64	SA48	300000h-30FFFFh
	64	SA49	310000h-31FFFFh
	64	SA50	320000h-32FFFFh
	64	SA51	330000h-33FFFFh
	64	SA52	340000h-34FFFFh
	64	SA53	350000h-35FFFFh
	64	SA54	360000h-36FFFFh
	64	SA55	370000h-37FFFFh
	64	SA56	380000h-38FFFFh
	64	SA57	390000h-39FFFFh
	64	SA58	3A0000h-3AFFFFh
	64	SA59	3B0000h-3BFFFFh
	64	SA60	3C0000h-3CFFFFh
	64	SA61	3D0000h-3DFFFFh
	64	SA62	3E0000h-3EFFFFh
	64	SA63	3F0000h-3FFFFFh
4	64	SA64	400000h-40FFFFh
	64	SA65	410000h-41FFFFh
	64	SA66	420000h-42FFFFh
	64	SA67	430000h-43FFFFh
	64	SA68	440000h-44FFFFh
	64	SA69	450000h-45FFFFh
	64	SA70	460000h-46FFFFh
	64	SA71	470000h-47FFFFh
	64	SA72	480000h-48FFFFh
	64	SA73	490000h-49FFFFh
	64	SA74	4A0000h-4AFFFFh
	64	SA75	4B0000h-4BFFFFh
	64	SA76	4C0000h-4CFFFFh
	64	SA77	4D0000h-4DFFFFh
	64	SA78	4E0000h-4EFFFFh
	64	SA79	4F0000h-4FFFFFh
5	64	SA80	500000h-50FFFFh
	64	SA81	510000h-51FFFFh
	64	SA82	520000h-52FFFFh
	64	SA83	530000h-53FFFFh
	64	SA84	540000h-54FFFFh

Bank	Sector Size Kwords	Sector	Address Range
5	64	SA85	550000h-55FFFFh
	64	SA86	560000h-56FFFFh
	64	SA87	570000h-57FFFFh
	64	SA88	580000h-58FFFFh
	64	SA89	590000h-59FFFFh
	64	SA90	5A0000h-5AFFFFh
	64	SA91	5B0000h-5BFFFFh
	64	SA92	5C0000h-5CFFFFh
	64	SA93	5D0000h-5DFFFFh
	64	SA94	5E0000h-5EFFFFh
	64	SA95	5F0000h-5FFFFFh
6	64	SA96	600000h-60FFFFh
	64	SA97	610000h-61FFFFh
	64	SA98	620000h-62FFFFh
	64	SA99	630000h-63FFFFh
	64	SA100	640000h-64FFFFh
	64	SA101	650000h-65FFFFh
	64	SA102	660000h-66FFFFh
	64	SA103	670000h-67FFFFh
	64	SA104	680000h-68FFFFh
	64	SA105	690000h-69FFFFh
	64	SA106	6A0000h-6AFFFFh
	64	SA107	6B0000h-6BFFFFh
	64	SA108	6C0000h-6CFFFFh
	64	SA109	6D0000h-6DFFFFh
	64	SA110	6E0000h-6EFFFFh
	64	SA111	6F0000h-6FFFFFh
7	64	SA112	700000h-70FFFFh
	64	SA113	710000h-71FFFFh
	64	SA114	720000h-72FFFFh
	64	SA115	730000h-73FFFFh
	64	SA116	740000h-74FFFFh
	64	SA117	750000h-75FFFFh
	64	SA118	760000h-76FFFFh
	64	SA119	770000h-77FFFFh
	64	SA120	780000h-78FFFFh
	64	SA121	790000h-79FFFFh
	64	SA122	7A0000h-7AFFFFh
	64	SA123	7B0000h-7BFFFFh
	64	SA124	7C0000h-7CFFFFh
	64	SA125	7D0000h-7DFFFFh
	64	SA126	7E0000h-7EFFFFh
	16	SA127	7F0000h-7F3FFFh
	16	SA128	7F4000h-7F7FFFh
	16	SA129	7F8000h-7FBFFFh
	16	SA130	7FC000h-7FFFFFh

Table 1-2. Sector Address Table (Bottom Boot)

Bank	Sector Size (Kwords)	Sector	Address Range
0	16	SA0	000000h-003FFFh
	16	SA1	004000h-007FFFh
	16	SA2	008000H-00BFFFh
	16	SA3	00C000h-00FFFFh
	64	SA4	010000h-01FFFFh
	64	SA5	020000h-02FFFFh
	64	SA6	030000h-03FFFFh
	64	SA7	040000h-04FFFFh
	64	SA8	050000h-05FFFFh
	64	SA9	060000h-06FFFFh
	64	SA10	070000h-07FFFFh
	64	SA11	080000h-08FFFFh
	64	SA12	090000h-09FFFFh
	64	SA13	0A0000h-0AFFFFh
	64	SA14	0B0000h-0BFFFFh
	64	SA15	0C0000h-0CFFFFh
	64	SA16	0D0000h-0DFFFFh
	64	SA17	0E0000h-0EFFFFh
	64	SA18	0F0000h-0FFFFFh
1	64	SA19	100000h-10FFFFh
	64	SA20	110000h-11FFFFh
	64	SA21	120000h-12FFFFh
	64	SA22	130000h-13FFFFh
	64	SA23	140000h-14FFFFh
	64	SA24	150000h-15FFFFh
	64	SA25	160000h-16FFFFh
	64	SA26	170000h-17FFFFh
	64	SA27	180000h-18FFFFh
	64	SA28	190000h-19FFFFh
	64	SA29	1A0000h-1AFFFFh
	64	SA30	1B0000h-1BFFFFh
	64	SA31	1C0000h-1CFFFFh
	64	SA32	1D0000h-1DFFFFh
	64	SA33	1E0000h-1EFFFFh
	64	SA34	1F0000h-1FFFFFh
2	64	SA35	200000h-20FFFFh
	64	SA36	210000h-21FFFFh
	64	SA37	220000h-22FFFFh
	64	SA38	230000h-23FFFFh
	64	SA39	240000h-24FFFFh
	64	SA40	250000h-25FFFFh
	64	SA41	260000h-26FFFFh
	64	SA42	270000h-27FFFFh
	64	SA43	280000h-28FFFFh
	64	SA44	290000h-29FFFFh
	64	SA45	2A0000h-2AFFFFh
2	64	SA46	2B0000h-2BFFFFh
	64	SA47	2C0000h-2CFFFFh
	64	SA48	2D0000h-2DFFFFh
	64	SA49	2E0000h-2EFFFFh
	64	SA50	2F0000h-2FFFFFh
3	64	SA51	300000h-30FFFFh
	64	SA52	310000h-31FFFFh
	64	SA53	320000h-32FFFFh
	64	SA54	330000h-33FFFFh
	64	SA55	340000h-34FFFFh
	64	SA56	350000h-35FFFFh
	64	SA57	360000h-36FFFFh
	64	SA58	370000h-37FFFFh
	64	SA59	380000h-38FFFFh
	64	SA60	390000h-39FFFFh
	64	SA61	3A0000h-3AFFFFh
	64	SA62	3B0000h-3BFFFFh
	64	SA63	3C0000h-3CFFFFh
	64	SA64	3D0000h-3DFFFFh
	64	SA65	3E0000h-3EFFFFh
	64	SA66	3F0000h-3FFFFFh
4	64	SA67	400000h-40FFFFh
	64	SA68	410000h-41FFFFh
	64	SA69	420000h-42FFFFh
	64	SA70	430000h-43FFFFh
	64	SA71	440000h-44FFFFh
	64	SA72	450000h-45FFFFh
	64	SA73	460000h-46FFFFh
	64	SA74	470000h-47FFFFh
	64	SA75	480000h-48FFFFh
	64	SA76	490000h-49FFFFh
	64	SA77	4A0000h-4AFFFFh
	64	SA78	4B0000h-4BFFFFh
	64	SA79	4C0000h-4CFFFFh
	64	SA80	4D0000h-4DFFFFh
	64	SA81	4E0000h-4EFFFFh
	64	SA82	4F0000h-4FFFFFh
5	64	SA83	500000h-50FFFFh
	64	SA84	510000h-51FFFFh
	64	SA85	520000h-52FFFFh
	64	SA86	530000h-53FFFFh
	64	SA87	540000h-54FFFFh
	64	SA88	550000h-55FFFFh

Bank	Sector Size Kwords	Sector	Address Range
5	64	SA89	560000h-56FFFFh
	64	SA90	570000h-57FFFFh
	64	SA91	580000h-58FFFFh
	64	SA92	590000h-59FFFFh
	64	SA93	5A0000h-5AFFFFh
	64	SA94	5B0000h-5BFFFFh
	64	SA95	5C0000h-5CFFFFh
	64	SA96	5D0000h-5DFFFFh
	64	SA97	5E0000h-5EFFFFh
	64	SA98	5F0000h-5FFFFFh
6	64	SA99	600000h-60FFFFh
	64	SA100	610000h-61FFFFh
	64	SA101	620000h-62FFFFh
	64	SA102	630000h-63FFFFh
	64	SA103	640000h-64FFFFh
	64	SA104	650000h-65FFFFh
	64	SA105	660000h-66FFFFh
	64	SA106	670000h-67FFFFh
	64	SA107	680000h-68FFFFh
	64	SA108	690000h-69FFFFh
	64	SA109	6A0000h-6AFFFFh
	64	SA110	6B0000h-6BFFFFh
	64	SA111	6C0000h-6CFFFFh
	64	SA112	6D0000h-6DFFFFh
	64	SA113	6E0000h-6EFFFFh
	64	SA114	6F0000h-6FFFFFh
7	64	SA115	700000h-70FFFFh
	64	SA116	710000h-71FFFFh
	64	SA117	720000h-72FFFFh
	64	SA118	730000h-73FFFFh
	64	SA119	740000h-74FFFFh
	64	SA120	750000h-75FFFFh
	64	SA121	760000h-76FFFFh
	64	SA122	770000h-77FFFFh
	64	SA123	780000h-78FFFFh
	64	SA124	790000h-79FFFFh
	64	SA125	7A0000h-7AFFFFh
	64	SA126	7B0000h-7BFFFFh
	64	SA127	7C0000h-7CFFFFh
	64	SA128	7D0000h-7DFFFFh
	64	SA129	7E0000h-7EFFFFh
	64	SA130	7F0000h-7FFFFFh

5. BUS OPERATIONS

This chapter indicates the functions and utilizations of Bus Operations. Bus operations are started by the internal command register and executed by a bus interface or similar logic circuitry. The Command register does not occupy any memory addresses. It is stored in the format of latches and independent to the address and data information when executing the command.

The contents of the register acts as it is input to internal state machine. In addition, the state machine outputs determine the function of the device.

Table 2. shows all inputs, control level requirement, and resulting output for all the bus operations. Please read it for further information.

***NOTE**: Falling edge of AVD# determines when to disable the current burst cycle while a new burst read cycle is started by the rising edge of CLK.*

Table 2. Bus Operations

Operation	CE#	OE#	WE#	CLK	AVD#	Address	Data	RESET#
Synchronous Operations								
Latch Starting Burst Address by CLK	L	H	H	R	L	Addr In	Addr In	H
Advance Burst Read to Next Address	L	L	H	R	H	X	Output Valid	H
Terminate Current Burst Read Cycle	H	X	X	X	X	X	HighZ	H
Terminate Current Burst Read Cycle through RESET#	X	X	X	X	X	X	HighZ	L
Asynchronous Operations								
Asynchronous Read - Addresses Latched	L	H	H	L	R	Addr In	Addr In	H
Asynchronous Read - Data on Bus	L	L	H	L	H	X	Output Data	H
Asynchronous Program (AVD# Latched Addresses)	L	H	X	L	R	Addr In	Addr In	H
Asynchronous Program (WE# Latched Data)	L	H	R	L	H	X	Input Valid	H
Non-Operations								
Standby (CE#)	H	X	X	X	X	X	HighZ	H
Hardware Reset	X	X	X	X	X	X	HighZ	L

Legend:

L = 0; H = 1; X = VIL or VIH; R = Rising edge; h-l = High to low.

NOTES:

1. *WP#/ACC low protects all sectors.*
2. *A/Q0~A/Q15 are input (DIN) or output (DOUT) pins according to the requests of command sequence, sector protection.*
3. *In Word Mode, the addresses are AM to A0, AM: MSB of address.*

5-1. Status Register

Bits in Status Register can offer users to identify the state in device right now. For more details, please see the following tables:

Table 3-1.Status Register

Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	Device Ready	Erase Suspend	Erase Status	Program Status	RFU	Program Suspend	Sector Protect	Bank Status
Device Ready	1	0: Default	0: Default	0: Default	DC	0: Default	0: Default	0: Default
Device Busy	0	DC	DC	DC	DC	DC	DC	0: Busy in this bank
Device Busy	0	DC	DC	DC	DC	DC	DC	1: Busy in other bank
Invalid	1	DC	DC	DC	DC	DC	DC	1

NOTES:

1. *DC=Don't Care*
2. *Bit 0 will show which bank is busy if and only if Bit 7 is 0. Otherwise, Bit 0 can only become 0.*
3. *Bit 3 is RFU*

Table 3-2.Status Register - Erase Suspend

Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	Device Ready	Erase Suspend	Erase Status	Program Status	RFU	Program Suspend	Sector Protect	Bank Status
No Sector in Erase Suspend	1	0	DC	DC	DC	DC	DC	DC
One sector in Erase Suspend	1	1	DC	DC	DC	DC	DC	DC

NOTES:

1. *DC=Don't Care*
2. *After issuing Erase Suspend command, user should check Bit 7 to make sure the value is 1 before accessing other sectors in the same bank.*
3. *Bit 3 is RFU*

Table 3-3.Status Register - Erase Status

Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	Device Ready	Erase Suspend	Erase Status	Program Status	RFU	Program Suspend	Sector Protect	Bank Status
Erase Success	1	DC	0	DC	DC	DC	DC	DC
Erase Fail	1	DC	1	DC	DC	DC	DC	DC

NOTES:

1. *DC=Don't Care*
2. *Bit 5 will show the erase status of last erase operation. User may input "Clear Status Register" or "Hardware Reset" to return to the default value.*
3. *Bit 3 is RFU*

Table 3-4.Status Register - Program Status

Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	Device Ready	Erase Suspend	Erase Status	Program Status	RFU	Program Suspend	Sector Protect	Bank Status
Program Success	1	DC	DC	0	DC	DC	DC	DC
Program Fail	1	DC	DC	1	DC	DC	DC	DC

NOTES:

1. *DC=Don't Care*
2. *Bit 4 will show the program status of last program operation. User may input "Clear Status Register" or "Hardware Reset" to return to the default value.*
3. *Bit 3 is RFU*

Table 3-5.Status Register - Program Suspend

Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	Device Ready	Erase Suspend	Erase Status	Program Status	RFU	Program Suspend	Sector Protect	Bank Status
No Sector in Program Suspend	1	DC	DC	DC	DC	0	DC	DC
One Sector in Program Suspend	1	DC	DC	DC	DC	1	DC	DC

NOTES:

1. *DC=Don't Care*
2. *After issuing Program Suspend command, user should check Bit 7 to make sure the value is 1 before accessing other sectors in the same bank.*
3. *Bit 3 is RFU*

Table 3-6.Status Register - Protect Status

Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	Device Ready	Erase Suspend	Erase Status	Program Status	RFU	Program Suspend	Sector Protect	Bank Status
Unprotected Sector during Operation	1	DC	DC	DC	DC	DC	0	DC
Protected Sector during Operation	1	DC	DC	DC	DC	DC	1	DC

NOTES:

1. *DC=Don't Care*
2. *If last operation is failed due to the sector is protected Bit 1 will become 1. User may input "Clear Status Register" or "Hardware Reset" to return to the default value.*
3. *Bit 3 is RFU.*

5-2. Blank Check

Users can use Blank Check command to confirm the selected sector is erased.

It is not allowed for users to read the array while the Blank Check command is being executed in the same array. This will return unknown data.

Blank Check command is only valid in Asynchronous Read mode, which means the Configuration Register Bit 15(CR [15]) is 1. This command may not conduct if the device is in operations.

The operation process of Blank Check command is as follows: Command will be issued (Address 555h and Data 33h) on Sector X, while the device is in the Idle State (neither during program suspend nor erase suspend operations.) After the operation is completed, the device will return to the Idle State.

User may use the Read Status Register to confirm if the device is still busy and when compete if the sector is blank or not. Bit 5 in the Status Register will be zero if the sector is erased and will become one if it is not erased. In addition, Bit 7 & Bit 0 in the Status Register will show if the device is performing a Blank Check. The device will halt the operation and report the results immediately, if any bit is found has not been erased.

5-3. Non-Burst (Asynchronous) Read Operation

Upon device's power-up, non-burst mode read is as the default state. To perform a read operation, the system addresses the desired memory array or status register location by providing its address on the address pins and simultaneously enabling the chip by driving AVD# & CE# LOW, and WE# HIGH. The CLK keeps low during asynchronous read operation. The address is latched on the rising edge of AVD#; OE# will be driven low afterwards. A/Q15-A/Q0 output the data after previous operations is complete.

5-4. Burst (Synchronous) Read Operation

The device supports the following burst read modes:

- Burst Mode - Continuous linear

- Linear burst mode - 8/16 word with wrap around

5-4-1. Burst Mode - Continuous Linear

Burst read mode is enabled when configuration register bit 15 is set to 0.

The number of dummy cycles should be set (for tIACC for each burst session) before the clock signal is being activated. Before the burst read mode is activated, the number of dummy cycle will be determined by the setting configuration register command. See Configuration Register Chapter for details.

The process of the continuous burst read operation is as follows:

The rising edge of a CLK cycle while AVD# = VIL--> Initial word output tIACC --> Wait for dummy cycle --> Rising edge of each consecutive clock, following words output (tBACC) (Automatically increase the internal address counter)

1. For address boundary every 128 words, the first boundary starts with 00007Fh, next with 0000FFh by adding 128 words address; and etc.
2. Additional dummy cycles are needed if the start address for the output cannot be divided by 8.

   RDY status indicates the condition of the device by de-asserting.

There is a permanent internal address boundary in the device that occurs every 128 words. 1 or 2 dummy cycles are required while crossing boundary. Additional dummy cycles needed when starting burst address cannot be divided by 8.

Table 4-1. Address Latency for 10-13 Dummy Cycles

(+2dc only occures when crossing 128 words boundary)

Dummy Cycles	Word	Subsequent Clock Cycles After Initial Dummy Cycles									
10-13 Dummy Cycles	0	D0	D1	D2	D3	D4	D5	D6	D7	+2dc	D8
	1	D1	D2	D3	D4	D5	D6	D7	1dc	+2dc	D8
	2	D2	D3	D4	D5	D6	D7	1dc	1dc	+2dc	D8
	3	D3	D4	D5	D6	D7	1dc	1dc	1dc	+2dc	D8
	4	D4	D5	D6	D7	1dc	1dc	1dc	1dc	+2dc	D8
	5	D5	D6	D7	1dc	1dc	1dc	1dc	1dc	+2dc	D8
	6	D6	D7	1dc	1dc	1dc	1dc	1dc	1dc	+2dc	D8
	7	D7	1dc	1dc	1dc	1dc	1dc	1dc	1dc	+2dc	D8

Table 4-2. Address Latency for 9 Dummy Cycles

(+1dc only occures when crossing 128 words boundary)

Dummy Cycles	Word	Subsequent Clock Cycles After Initial Dummy Cycles									
9 Dummy Cycles	0	D0	D1	D2	D3	D4	D5	D6	D7	+1dc	D8
	1	D1	D2	D3	D4	D5	D6	D7	1dc	+1dc	D8
	2	D2	D3	D4	D5	D6	D7	1dc	1dc	+1dc	D8
	3	D3	D4	D5	D6	D7	1dc	1dc	1dc	+1dc	D8
	4	D4	D5	D6	D7	1dc	1dc	1dc	1dc	+1dc	D8
	5	D5	D6	D7	1dc	1dc	1dc	1dc	1dc	+1dc	D8
	6	D6	D7	1dc	1dc	1dc	1dc	1dc	1dc	+1dc	D8
	7	D7	1dc	1dc	1dc	1dc	1dc	1dc	1dc	+1dc	D8

Table 4-3. Address Latency for 8 Dummy Cycles

Dummy Cycles	Word	Subsequent Clock Cycles After Initial Dummy Cycles								
8 Dummy Cycles	0	D0	D1	D2	D3	D4	D5	D6	D7	D8
	1	D1	D2	D3	D4	D5	D6	D7	1dc	D8
	2	D2	D3	D4	D5	D6	D7	1dc	1dc	D8
	3	D3	D4	D5	D6	D7	1dc	1dc	1dc	D8
	4	D4	D5	D6	D7	1dc	1dc	1dc	1dc	D8
	5	D5	D6	D7	1dc	1dc	1dc	1dc	1dc	D8
	6	D6	D7	1dc	1dc	1dc	1dc	1dc	1dc	D8
	7	D7	1dc	1dc	1dc	1dc	1dc	1dc	1dc	D8

Table 4-4. Address Latency for 7 Dummy Cycles

Dummy Cycles	Word	Subsequent Clock Cycles After Initial Dummy Cycles								
7 Dummy Cycles	0	D0	D1	D2	D3	D4	D5	D6	D7	D8
	1	D1	D2	D3	D4	D5	D6	D7	D8	D9
	2	D2	D3	D4	D5	D6	D7	1dc	D8	D9
	3	D3	D4	D5	D6	D7	1dc	1dc	D8	D9
	4	D4	D5	D6	D7	1dc	1dc	1dc	D8	D9
	5	D5	D6	D7	1dc	1dc	1dc	1dc	D8	D9
	6	D6	D7	1dc	1dc	1dc	1dc	1dc	D8	D9
	7	D7	1dc	1dc	1dc	1dc	1dc	1dc	D8	D9

Table 4-5. Address Latency for 6 Dummy Cycles

Dummy Cycles	Word	Subsequent Clock Cycles After Initial Dummy Cycles								
6 Dummy Cycles	0	D0	D1	D2	D3	D4	D5	D6	D7	D8
	1	D1	D2	D3	D4	D5	D6	D7	D8	D9
	2	D2	D3	D4	D5	D6	D7	D8	D9	D10
	3	D3	D4	D5	D6	D7	1dc	D8	D9	D10
	4	D4	D5	D6	D7	1dc	1dc	D8	D9	D10
	5	D5	D6	D7	1dc	1dc	1dc	D8	D9	D10
	6	D6	D7	1dc	1dc	1dc	1dc	D8	D9	D10
	7	D7	1dc	1dc	1dc	1dc	1dc	D8	D9	D10

Table 4-6. Address Latency for 5 Dummy Cycles

Dummy Cycles	Word	Subsequent Clock Cycles After Initial Dummy Cycles								
5 Dummy Cycles	0	D0	D1	D2	D3	D4	D5	D6	D7	D8
	1	D1	D2	D3	D4	D5	D6	D7	D8	D9
	2	D2	D3	D4	D5	D6	D7	D8	D9	D10
	3	D3	D4	D5	D6	D7	D8	D9	D10	D11
	4	D4	D5	D6	D7	1dc	D8	D9	D10	D11
	5	D5	D6	D7	1dc	1dc	D8	D9	D10	D11
	6	D6	D7	1dc	1dc	1dc	D8	D9	D10	D11
	7	D7	1dc	1dc	1dc	1dc	D8	D9	D10	D11

Table 4-7. Address Latency for 4 Dummy Cycles

Dummy Cycles	Word	Subsequent Clock Cycles After Initial Dummy Cycles								
4 Dummy Cycles	0	D0	D1	D2	D3	D4	D5	D6	D7	D8
	1	D1	D2	D3	D4	D5	D6	D7	D8	D9
	2	D2	D3	D4	D5	D6	D7	D8	D9	D10
	3	D3	D4	D5	D6	D7	D8	D9	D10	D11
	4	D4	D5	D6	D7	D8	D9	D10	D11	D12
	5	D5	D6	D7	1dc	D8	D9	D10	D11	D12
	6	D6	D7	1dc	1dc	D8	D9	D10	D11	D12
	7	D7	1dc	1dc	1dc	D8	D9	D10	D11	D12

Table 4-8. Address Latency for 3 Dummy Cycles

Dummy Cycles	Word	Subsequent Clock Cycles After Initial Dummy Cycles								
3 Dummy Cycles	0	D0	D1	D2	D3	D4	D5	D6	D7	D8
	1	D1	D2	D3	D4	D5	D6	D7	D8	D9
	2	D2	D3	D4	D5	D6	D7	D8	D9	D10
	3	D3	D4	D5	D6	D7	D8	D9	D10	D11
	4	D4	D5	D6	D7	D8	D9	D10	D11	D12
	5	D5	D6	D7	D8	D9	D10	D11	D12	D13
	6	D6	D7	1dc	D8	D9	D10	D11	D12	D13
	7	D7	1dc	1dc	D8	D9	D10	D11	D12	D13

5-4-2. Linear Burst Mode - 8/16 Word with Wrap Around

Fixed amount of data (8 or 16 words) is output from continuous address for the linear wrap around mode. (in the unit of words). The origin burst read address is decided by the group where the origin address falls. The definition of groups is as illustrated in **Table 5** below.

If the system is in 16-Word Mode, the Subsequent Clock Cycles are needed. The detailed number of Subsequent Clock Cycles please see the table above. There is no need to have Subsequent Clock Cycles in 8-Word Mode.

8-, 16-Word Modes will be determined by the setting configuration register command. See **Configuration Register** Chapter for details.

Table 5. Burst Address Groups

Mode	Word Group Size	Word Group Address Ranges
8-Word Mode	8 words per group	0-7h, 8-Fh, 10-17,…
16-Word Mode	16 words per group	0-Fh, 10-1Fh, 20-2Fh,…

5-4-3. Reading Memory Array

Read mode is the default state after a power-up or a reset operation.

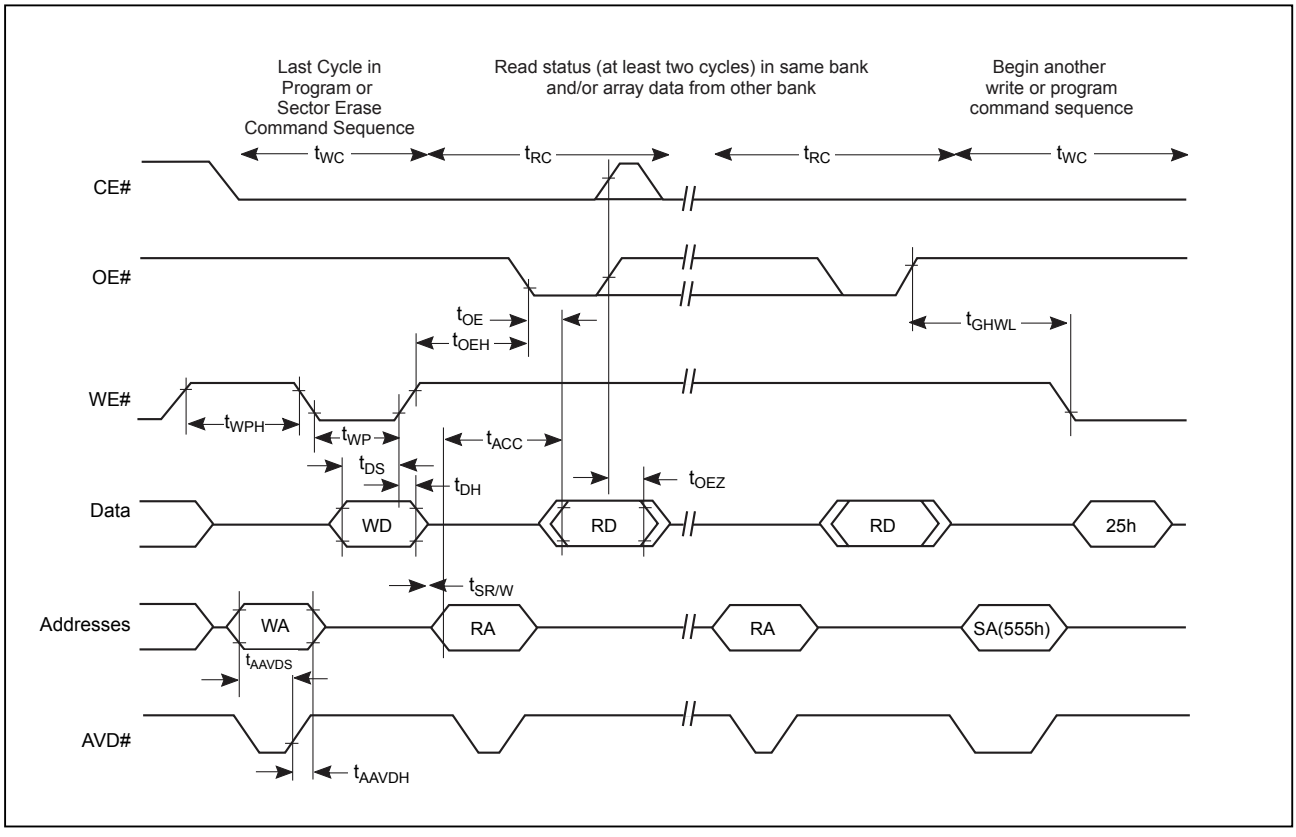
An erase operation will be paused (after a time delay less than tESL) and the bank will enter Erase-Suspended Read mode if the bank receives an Erase Suspend command while in the Sector Erase state. While in the Erase-Suspended Read mode, data can be programmed or read from any sector which is not being erased. Reading from addresses within sector (s) being erased is invalid.

If a program command is issued to any inactive (not currently being erased) sector during Erase-Suspended Read mode, the bank will perform the program operation and automatically return to Erase-Suspended Read mode after the program operation completes successfully.

While in Erase-Suspended Read mode, an Erase Resume command must be issued by the system to reactivate the erase operation. The erase operation will resume from where it was suspended and will continue the operation until it completely finishes or another Erase Suspend command is received.

After the memory bank completes an embedded operation (Chip Erase, Sector Erase, or Program) successfully, it will automatically return to idle state. If the embedded operation fails to complete, Bit 5 (Erase fail) or Bit 4(Program fail) in Status Register will become 1. The system may perform a "Clear Status Register" operation before the next operation.

Figure 1. Back-to-Back Read/Write Cycle Timings



NOTE:

Breakpoints in waveforms indicate that system may alternately read array data from the non-busy bank while checking the status of the program or erase operation in the busy bank. The system should read status twice to ensure valid information.

5-5. Program Operation

The program operation is combined by two parts,"Program to Buffer" and "Program Buffer to Flash". For further operation detail, please refer to 5-5-1. Write Buffer Programming Operation.

After the program command sequence has been executed, the internal write state machine (WSM) automatically executes the algorithms and timings necessary for programming and verification, which includes generating suitable program pulses, checking cell threshold voltage margins, and repeating the program pulse if any cells do not pass verification or have low margins. The internal controller protects cells that do pass verification and margin tests from being over-programmed by inhibiting further program pulses to these passing cells as weaker cells continue to be programmed.

With the internal WSM automatically controlling the programming process, users only need to enter the program command and data once.

Programming will only change the bit status from "1" to "0". It is not possible to change the bit status from "0" to "1" by programming. This can only be done with an erase operation. Furthermore, the internal write verification only checks and detects errors in cases where a "1" is not successfully programmed to "0".

Any commands written to the bank during programming will be ignored except, Read Status Register, hardware reset or program suspend. Hardware reset will terminate the program operation after a period of time not more than tPSL. When the program is complete or the program operation is terminated by a hardware reset, the bank will return to idle state. When program suspend is ready, the bank will enter program suspend read mode.

After the embedded program operation has begun, users can check for completion by reading the following bits in the status register table (Please refer to **Section 5-1. Status Register, Table 3-1 and 3-4).**

5-5-1. Write Buffer Programming Operation

The system is able to program up to 32 words in one programing operation. To trigger the Write Buffer Programming, start with the Program to Buffer command at Sector Address+555h. The second cycle writes the "word locations subtract one" number.

Following the operations above, system starts to write the mingling of address and data. After the programming of the first address or data, the "write-buffer-page" is selected. The following data should be within the above mentioned page. The "write-buffer-page" is selected by choosing address A22-A5. "Write-Buffer-Page" address has to be the same for all address/data write into the write buffer. If not, operation will be aborted and the system will return to initial state. At the same time, Bit 4 in Status Register will become 1. Users may input a "Clear Status Register" to clear this value before next operation.

Conditions which will lead to ABORT			
Condition 1	**Condition 2**	**Condition 3**	**Condition 4**
After inputting “Number of Locations" to Program, the value loaded is higher than the page buffer size.	During “Program to Buffer” period, address written in a sector is not assigned.	During “Program to Buffer” period, address/data written to “buffer-write-page” is not assigned by the “Starting Address”.	Input any other command except “Program to Buffer” after assigning the number of “data load”.

If the system has been aborted, Bit 4 in the status register will become 1. User may input command "Clear Status Register" to clear bit 4 before next operation.

To program the content of the write buffer page to Flash memory needs a Program Buffer to Flash command. The Write Buffer Programming operation can be suspended or resumed by the standard commands.

Once the Write Buffer Programming operation is finished, it will return to idle state. See **Table 6** and **Figure 2** below for the Write Buffer Programming command sequence

Write Buffer Programming can be conducted in any sequence. However the ID/CFI, Configuration Mode, SSS Lock Bit, and Secured Silicon Sector region are not functional when program operation is in progress. Multiple Write Buffer Programming operations on the same write buffer address range without intervening erases is available. Any bit in a write buffer address range can not be programmed from 0 back to 1.

5-5-2. Accelerated Program Operations

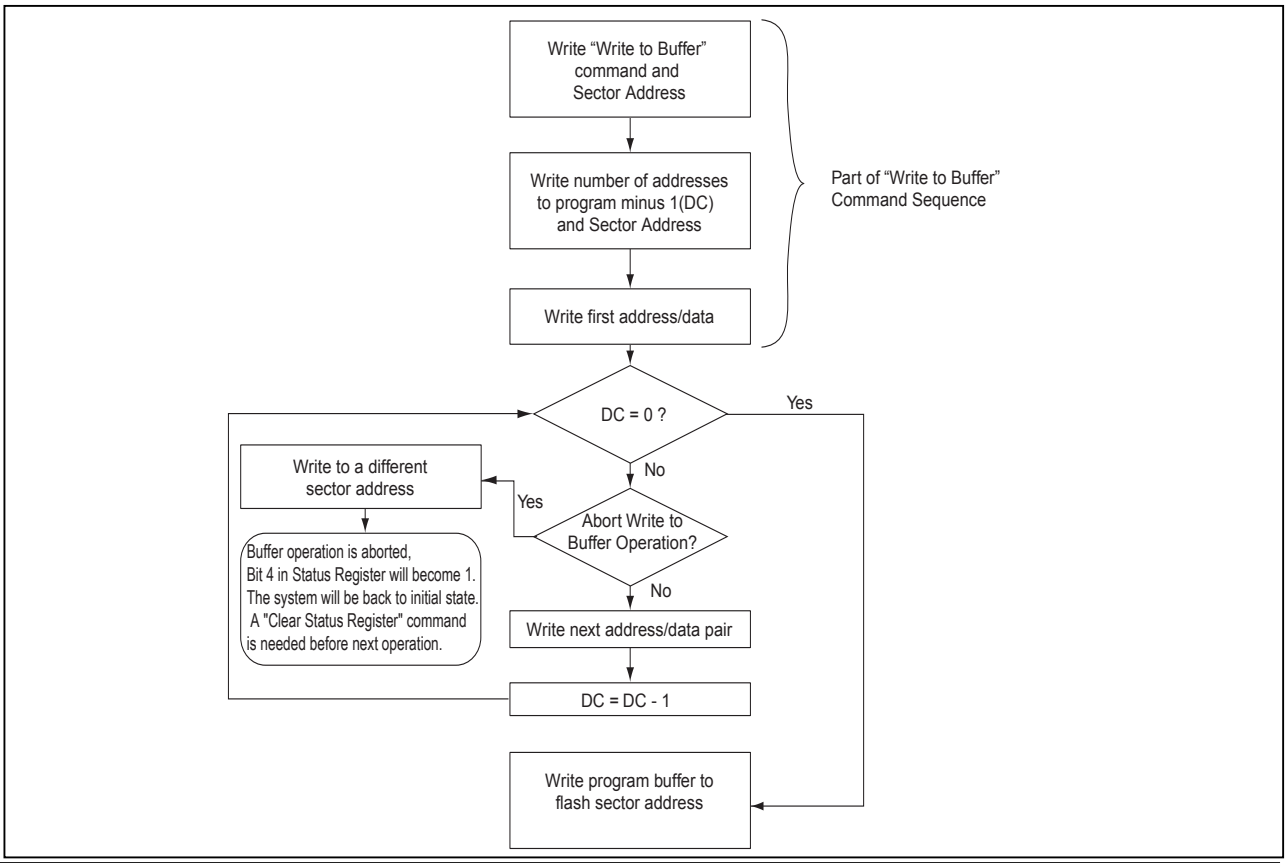
By applying high voltage (Vhv) to the WP#/ACC pin, the bank will enter the Accelerated Programming mode. During accelerated programming, the current drawn from the WP#/ACC pin is no more than ICP1.

Table 6. Write Buffer Programming Command Sequence

Sequence	Command	Address	Data	Remarks
1	Program to Buffer	SA+555h	0025h	
2	Indicate # of Program Locations	SA+2AAh	Word Count	(# of locations) - 1
3	Load 1st word	SA+Write Buffer Location	Write	Addresses need to be within write-buffer-page boundaries, but no need to be loaded in any order.
4-X	Load next word	SA+Write Buffer Location	Write	Same as above
X+1	Load last word	SA+Write Buffer Location	Write	Same as above
X+2	Program Buffer to Flash	SA+555h	0029h	This command must come after the last write buffer location loaded, or the operation will ABORT.
X+3	Bank goes busy			
Last	Status monitoring through Read Status Register			

NOTE: *SA=Sector Address*

Figure 2. Write Buffer Programming Operation



5-6. Erase Operation

There are two types of erase operations performed on the memory array -- Sector Erase and Chip Erase. Sector Erase operation erases one selected sector.

Sector erase will not be conducted if the selected sector is protected.

Chip erase will not be conducted if any of the sectors is in Locked Range Sector or SA0 is locked protected. It can be done after the those sectors are being un-protected.

5-6-1. Sector Erase

The sector erase operation is used to clear data within a sector by returning all the memory location to the “1” state. It requires two cycles to initiate the erase operation.

The first cycle is inputting SA (Note)+Address 555h and Data 80h. The second cycle is SA+Address 2AAh and Data 30. If the selected sector is protected, sector erase will not start and Bit 1 will become 1. User may input a "Clear Status Register" command to return Bit 1 to default value before next operation. Sector erase command sequence is as follows: SA+Set-up command -->SA+sector erase command.

NOTE: *SA=Sector Address*

After the embedded sector erase operation begins, all commands except Erase Suspend and Read Status Register will be ignored. The only way to interrupt the operation is with an Erase Suspend command or with a hardware reset. The hardware reset will completely abort the operation and return the bank to initial state.

Please refer to ***Section 5-1. Status Register, Tables 3-1*** and ***3-3***.

5-6-2. Chip Erase

The Chip Erase operation is used to erase all the data within the memory array. All memory cells containing a "0" will be returned to the erased state of "1". This operation requires 2 cycles to initiate the action. The first cycle is inputting SA (Note)+Address 555h and Data 80h. The second cycle is SA+2AAh and Data 10h.

During the chip erase operation, no other software commands except Read Status Register will be accepted, but if a hardware reset is received or the working voltage is too low, that chip erase will be terminated. After Chip Erase operation completes, the chip will automatically return to initial state. If any of the sectors is in Locked Range Sector or SA0 is locked, chip erase will not start.

The system is able to determine the status of the embedded chip erase operation.

5-6-3. Accelerated Sector Erase

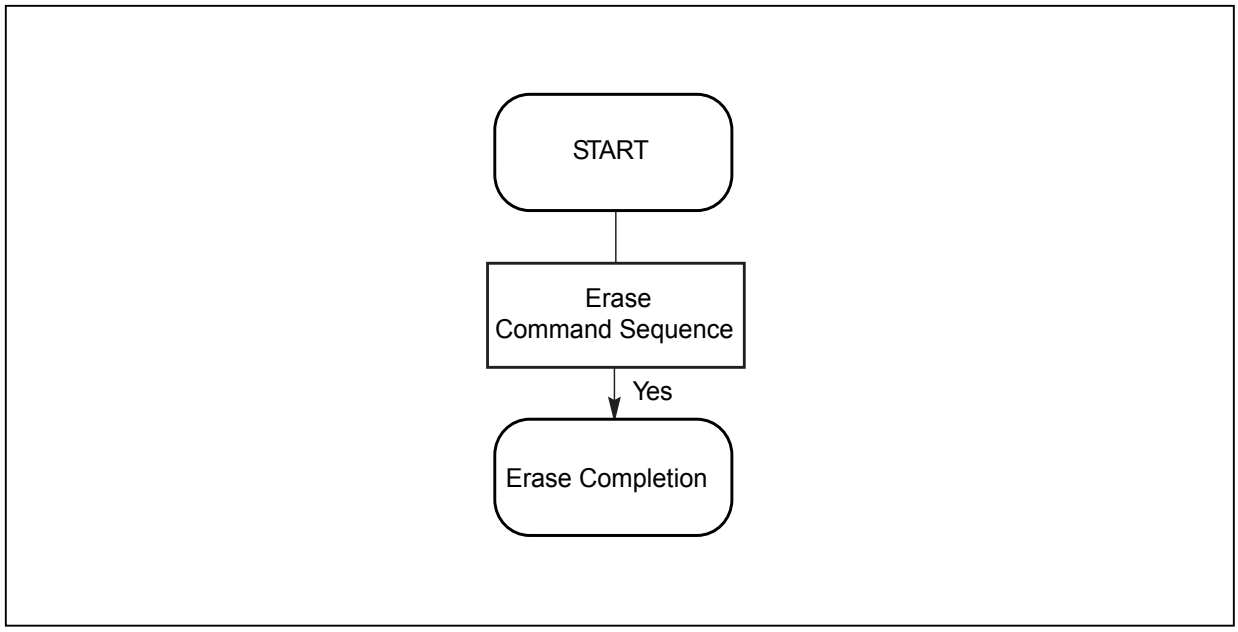
An accelerated erase function is provided to erase no more than 100 times per sector erase. Accelerated (ACC) erase operation should be conducted in the range of 30°C+/-10°C. The ACC erase provides much faster erase operation compare with standard erase operations.

Operations below are needed prior to ACC sector erase operation:

1. If the selected sector is protected, sector erase will not start and Bit 5 & Bit 1 will become 1. Users may input a "Clear Status Register" command to return the Bits to default value before next operation.
2. Vhv must be applied to ACC input at least 1 μs before executing step 3.

3. Sector erase command is issued.
4. Bit 7, Bit 5 and Bit 1 in Status Register should be monitored so to verify when erase operation is complete. This part is the same as in the standard erase operation.
5. ACC is lowered from Vhv to VCC.

Figure 3. Erase Operation



5-7. Program/Erase Suspend/Resume

5-7-1. Program Suspend/Program Resume

After a program operation begins, Program Suspend and Read Status Register are the only valid command that can be issued. The system will determine if the bank has entered the Program-Suspended Read mode through Bit 2 in Status Register.

After the bank has entered Program-Suspended mode, the system can read any sector (s) except that being programmed by the suspended program operation. Reading the array being program suspended is invalid. Whenever a suspend command is issued, user must issue a Program Resume command and check Bit 2 in Status Register, before issue another Program command. The system can use the Status Register bits shown in **Table 3-1** and **Table 3-5** to determine the current state of the bank.

When the bank is Program/Erase suspended, user is not allowed to enter AM Mode.

The Program suspend operation is as follows: Issuing Programming Suspend Command --> Bank's programming operation suspended paused within tPSL; Status Bits updated; Address defined --> Data to be read from non-suspended sectors.

Note that when an erase suspend is in operation, program suspend can also be conducted, data can then be read from non-suspended sectors.

The Program Resume command is valid only when the bank is in Program-Suspended mode.

For Program Resume, it operates as thus: Issuing Program Resume command --> Bank resumes programming (Status to be checked by Bit 2 in Status Register).

Please refer to ***Table 3-5. Status Register - Program Suspend***

It must exit the suspend by issuing resume command. After programming being resumed, another program suspend can be issued after 25us.

NOTE: *While a program operation is suspended and resumed more than once, a minimum delay of tPRS (Program Resume to Program Suspend) is required between next resume and suspend command.*

5-7-2. Erase Suspend/Erase Resume

After a sector erase operation begins, Erase Suspend, Read Status Register, and Hardware Reset are the only valid commands that can be issued. If the system issues an Erase Suspend command after the sector erase operation has already begun, the bank will not enter Erase-Suspended Read mode until tESL has elapsed. The system is able to determine if the bank has entered the Erase-Suspended Read mode through Bit 6 in Status Register.

After the bank has entered Erase-Suspended Read mode, the system can read or program any sector (s) except that being erased by the suspended erase operation. Reading any sector being erased or programmed will cause unknown state. Whenever a suspend command is issued, users must issue a resume command and check Bit 6 in Status Register before issue another erase command.

When the bank reads from a erase suspended sector during burst read mode, the burst read operation will soutput undefined value when crossing the boundary to the suspended sector. User may restart the burst operation by issuing new address and AVD# pulse.

The system is able to use the status register bits shown in **Table 3-1** and **3-2** to determine the current state of the bank.

The Sector Erase Resume command is valid only when the bank is in Erase-Suspended Read mode. After erase operation resumes, users can issue another Erase Suspend command, but there should be a 400us interval between Erase Resume and the next Erase Suspend command.

5-8. Configuration Register

A configuration register is used to set the various burst parameters: number of dummy cycles, burst length, RDY configuration, and synchronous mode active.

The **Configuration Register Table** displays the address bits of configuration register settings represent various device functions.

Table 7. Configuration Register

Function	CR Bit	Settings (Binary)
Enable Sync Read Mode	CR15	1 = Default Async Read Mode 0= Sync Read Mode
Programmable Dummy Cycles	CR14	0000 = Reserved 0001 = Data is valid on the 3rd active CLK rising edge after addresses are latched 0010 = Data is valid on the 4th active CLK rising edge after addresses are latched 0011 = Data is valid on the 5th active CLK rising edge after addresses are latched
	CR13	0100 = Data is valid on the 6th active CLK rising edge after addresses are latched 0101 = Data is valid on the 7th active CLK rising edge after addresses are latched 0110 = Data is valid on the 8th active CLK rising edge after addresses are latched 0111 = Data is valid on the 9th active CLK rising edge after addresses are latched
	CR12	1000 = Data is valid on the 10th active CLK rising edge after addresses are latched 1001 = Data is valid on the 11th active CLK rising edge after addresses are latched 1010 = Data is valid on the 12th active CLK rising edge after addresses are latched 1011 = Data is valid on the 13th active CLK rising edge after addresses are latched (Default)
	CR11	1100 = Reserved 1101 = Reserved 1110 = Reserved 1111 = Reserved
RDY Polarity	CR10	0 = RDY signal is active low 1 = RDY signal is active high (Default)
Reserved	CR9	1 = Default
RDY	CR8	0 = RDY active one clock cycle before data 1 = RDY active with data (Default)
Driver Strength	CR7	0 = Full driver strength (Default) 1 = Half driver strength
Reserved	CR6	1 = Default
Reserved	CR5	0 = Default
Reserved	CR4	0 = Default
Reserved	CR3	1 = Default
Burst Length	CR2	000 = Continuous (Default) 010 = Linear burst length - 8-Word with wrap around 011 = Linear burst length - 16-Word with wrap around (All other bit settings are reserved)
	CR1	
	CR0	

***NOTES**:*

1. *RDY Configuration - The device is able to set RDY to output VOH with valid data by default. RDY goes active one data cycle ahead of the active data. CR8 sets to "1" for RDY being active; "0" for RDY being active one cycle ahead of the valid data to be output.*
2. *RDY Polarity - Both devices have this default setting to indicate if the system is ready for CR10 to set to "1" when RDY is high. Set to "0" will set RDY to low. When RDY is low, RDY shows the device is ready.*

5-8-1. Set Configuration Register Command Sequence

The burst mode parameter is set by the configuration register. The following modes are configured: burst length, RDY configuration, synchronous mode active, and number of dummy cycles. Before entering burst mode, the configuration register needs to be set. User should issue Enter Configuration Register command first and then set configuration register by following 4 cycles.

- Cycle 1: SA+Address 555h & Data 25h.
- Cycle 2: SA+Address 2AAh & Data 00h.
- Cycle 3: SA+Address X00h & PD.
- Cycle 4: SA+ Address 555h & Data 29h.

To reset the bank to read mode, a software reset command needs to be issued. The bank's default state after power up or hardware reset is asynchronous read mode. Before entering synchronous mode, the register needs to be set. During bus operation, the register can not be modified.

***NOTE:** SA=Sector Address*

5-8-2. Configurable Dummy Cycle

The Configurable Dummy Cycle settings can be decided by the input frequency of the bank - The Configuration Bit (CR14–CR11) determines the setting. Refer to ***Table 8. Configuration Dummy Cycles vs Frequency*** as below.

The certain number of cycles for original burst read is set by configuration register command sequence in 5-8-1. The clock frequency determines the number of dummy cycles configured.

***NOTE:** After a power-up or hardware reset, the default setting of dummy cycle will be set to 13.*

In order to ensure the bank is set as expected, it is recommended that configuration register command sequence should be written even if the default dummy cycle value is desired. Default state can also be obtained by hardware reset.

Other setting not listed in the table above will be reserved as invalid.

If the setting CR[14:11] is not in legal setting as table listed, the bank will output CR[14:11] to 1011 and RDY will be disasserted.

5-8-3. Burst Length Configuration

Three different burst read modes are supported: 8 & 16 word linear burst read with wrap around; continuous burst read. The bank's default burst read is Burst Mode - Continuous linear. It launches with starting address till the burst read ends. When reaches the highest address, it wraps around to the lowest address. In 8 or 16 word liner burst read with wrap around, the wrap around occurs in the 8 or 16 word boundary.

Table 8. Configuration Dummy Cycles vs Frequency

CR [14:11]	Dummy Cycles	Freq Max (Mhz)
0001	3	27
0010	4	40
0011	5	54
0100	6	66
0101	7	80
0110	8	95
0111	9	104
1000	10	108

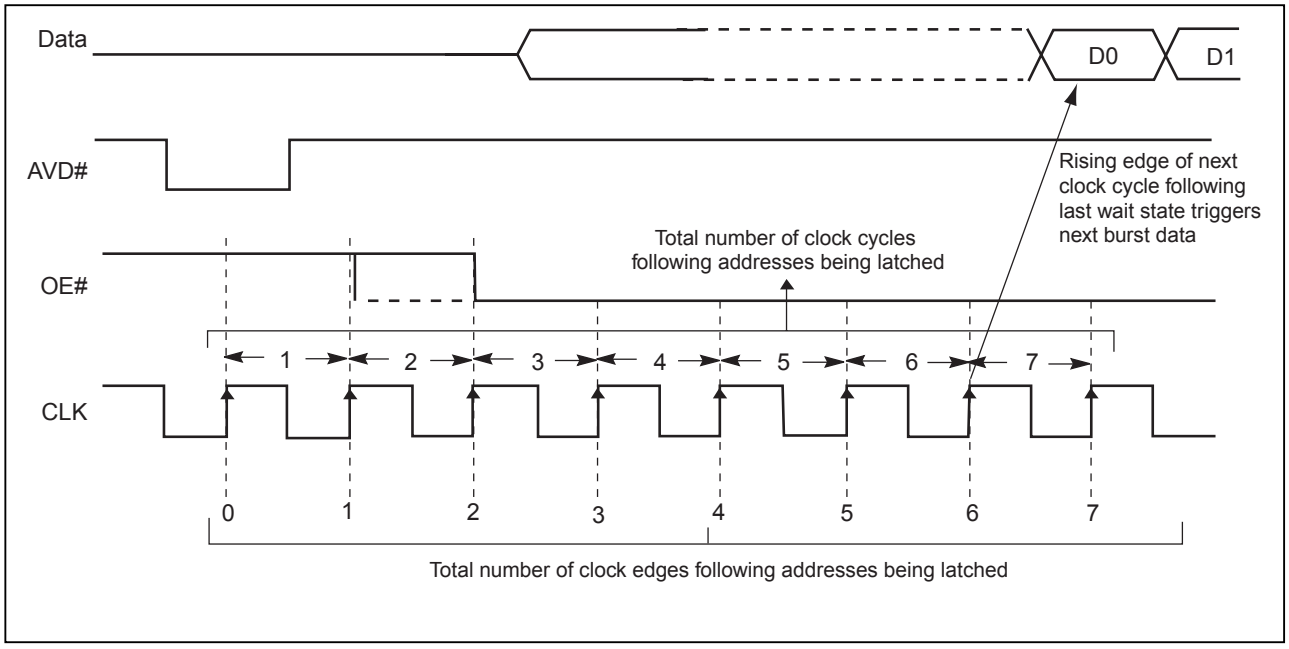
5-8-4. Output Drive Strength

User may tune the strength of output driver from full strength to half strength depends on the configuration bit CR7.

The default setting is CR7=1; with full strength.

If CR7=0, the strength of output buffer will be reduced to half strength.

Figure 4. Example of Programmable Dummy Cycles



5-9. Enter/Exit Secured Silicon Sector Command Sequence

A 8-word, random ESN (Electronic Serial Number) is in the Secured Silicon Sector region. The operation of Secured Silicon Sector region is thus: 1-cycle command to enter the region --> Access of the region --> 1-cycle command to exit the region --> Return to normal operation

The "Enter Secured Silicon Region" enables user to conduct the following:

- Read the Region
- Program the user Region
- Read non re-mapped area
- Issuing "Exit Secured Silicon Region" command

The Secured Silicon Sector Region cannot be accessed when program/erase is in operation.

In the Secured Silicon Sector region, 128-word region is factory locked, while the other 128-word region is customer locked.

5-9-1. Program Secured Silicon Sector Command Sequence

Programming Secured Silicon Sector starts by entering Secured Silicon Sector region. After entering the region the sequence is as the **Table 6. Write Buffer Programming Command Sequence**.

The system can monitor Bit 7, Bit 4 and Bit 0 in Status Register to check the status of the embedded operation as the system does when programming the normal array.

Programming the Secured Silicon Sector will only change the bit status from “1” to “0”. It is not possible to change the bit status from “0” to “1” by programming. Furthermore, the internal write verification only checks and detects errors in case where a ”1” is not successfully programmed to “0”.

When program is complete, the device then returns to Read Secured Silicon Sector mode.

If embedded program exceeds max. time limit (a failure occurs), Bit 4 in Status Register changes to 1. Under this condition, users may input a "Clear Status Register" command. Also, hardware reset can return to idle state.

5-10. Handshaking Feature

By conducting the host to detect the Ready (RDY) signal, the handshaking feature enables the system to decide when the initial burst data is ready, which controls by CE#.

RDY is active when CE# is low. RDY is floating when both CE# are high. A/Q15 - A/Q0 are active when CE# & OE# are low. A/Q15-A/Q0 are floating when both CE# high and OE# are high.

The synchronous mode operation is as thus: Configure the number of dummy cycle by Configuration Register(CR14-CR11) --> AVD# and OE# goes low --> Rising edge of RDY indicates the initial burst word data indicated.

The Burst read may be optimized by configuring the setting the number of dummy cycle per clock frequency.

In Asynchronous mode, CE# is low and RDY is high.

6. SECURITY FEATURES

6-1. Sector Protect/Un-protect

The device is capable of protect all sectors from program/erase operation. Upon power-up, all sectors are unprotected by default.

Protected/Un-protected sector operation is as thus: Issue first two cycles Sector Protected/Un-protected command (x555h & x2AAh) Address & data 60h. 3rd cycle address (SLA) & command (60h) to unlock and indicate Address A6 for the sector to be protected (VIL) or un-protected (VIH). When A6= VIL, all sectors protected. One sector at a time can then be un-protected.

Prior to program/erase operation, un-protected Sector address needs to be checked. Un-protection status of a sector can be altered after program/ erase operations are suspended. During Program Suspend/Resume and Erase Suspend/Resume, the sector protection status is not checked.

When sector protect/un-protect command issued to a "Sector protect Range" area, all sectors in it will not be un-protected. If a program/erase operation occurs in a protected sector, the operation will not start and Bit 1 in Status Register will become 1. Users may input a "Clear Status Register" command or "Hardware Reset" command to return it to default value.

6-2. Sector Protect Range

A range of sectors can be protected from write operation with the Sector Protect Range command till power off or hardware reset. The Sector Protect Range command overrides the sector protect/ un-protect command.

The sequence is as follows: 2 cycles of addresses (x555h & x2AAh) & data (60h)--> 1 cycle (3rd) load sector address & issue sector address command (61h) (setting lower sector of range) --> 1 cycle (4th), Write sector address & load sector address command (61h) (setting upper sector of the range).

The range is 128KB. If the sector address meets the locations of the 4 boot sectors in range, all sectors will be protected.

Before power cycle or hardware reset, the selected sectors are protected.

Address input need to start from lower address to higher address, otherwise the Sector Lock Range command will be invalid. In addition, the Sector Lock Range command would only be valid when A6=VIL.

The Sector Lock Range command is only valid once after a power cycle or hardware reset.

Sector Lock Range command is superior to the sector protect command.

6-3. Hardware Protect

When WP#/ACC = VIL, no program/erase operation then allowed for all sectors.

No program / erase operation is allowed until Vcc > VLKO. If Vcc > VLKO, user needs to avoid unintended write to the device.

For OE#, WE# or CE#'s glitch less than 3ns, the program/erase cycle will not be triggered.

Power-up write inhibit is supported, thus during power up, CE#=RESET#=VIL and OE#=VIH, no program/erase operation is allowed.

6-4. SSS Lock Bits

There are two bits in SSS Lock Bits: Secured Silicon Sector Protection Bit in Customer region is Bit 0. Secured Silicon Sector Protection Bit in Factory region is Bit 1. All other bits in this register are 1 in default. If Bit 0 is 1, the Secured Silicon Sector in Customer region is programmable. If Bit 0 is 0, that region will be un-programmable. As soon as Secured Silicon Sector region has been programmed, SSS Lock Bits should be 0.

6-5. Secured Silicon Sector Flash Memory Region

The Secured Silicon Sector region is an extra OTP memory space of 256 words in length. There are two regions in this memory space: Factory Locked Region(0-7Fh) and Customer Lockable Region(80-FFh). Customer can issue SSS Lock Entry command and then SSS Lock Read command to query the lock status of the device.

In factory-locked device, Secured Silicon Sector region is protected when shipped from factory and the SSS Lock Bit (Bit 1) is set to "1". In customer lockable device, security sector region is unprotected when shipped from factory and the SSS Lock Bit (Bit 0) is set to "0".

Following attributes applies for this Region:

- The region is not available during PE mode or other region in AM mode
- Sector address will be supplied when the SSS entry command choose memory array sector which is overlaid by the SSS Region address map
- Continuous burst read in this region wraps from FFh to 00h
- Read to be performed in Async & Sync mode

6-5-1. Factory Locked Region: Secured Silicon Sector Programmed and Protected at the Factory

In the factory-locked region, the Secured Silicon Sector is permanently locked before shipping from the factory. This region will have a 8-word ESN in the security region. The ESN occupies 00000h to 00007h in word mode.

The following attributes applie for this Region:

Secured Silicon Sector Address Range	Standard Factory Locked	Express Flash Factory Locked
000000h-00007Fh	ESN	Factory lock
000080h-0000FFh	Unavailable	Determined by Customer

6-5-2. Customer Lockable Region: Secured Silicon Sector NOT Programmed or Protected at the Factory

When the security feature is not required, the Customer Lockable region in secured silicon sector can act as an extra memory space.

Secured silicon sector is protected by SSS Lock bit (Bit1 and Bit0). Note that once the secured silicon sector is protected, there is no way to unprotect the secured silicon sector and the content of it can no longer be altered.

After the secured silicon is locked and verified, system must write Exit Security Sector Region, go through a power cycle, or issue a hardware reset to return the device to read normal array mode.

7. COMMAND DEFINITIONS

Command Definitions Table shows the address and data requirements for both command sequences.

Command		Asyn. Read	Program to Buffer	Program Buffer to Flash	Sector Erase	Chip Erase
Cycles		1	3-34(Note1)	1	2	2
1st Bus Cycle	Addr	RA	SA+555	SA+555	SA+555	SA+555
	Data	RD	25	29	80	80
2nd Bus Cycle	Addr		SA+2AA		SA+2AA	SA+2AA
	Data		WC		30	10
3rd Bus Cycle	Addr		SA+PA			
	Data		PD			
4th Bus Cycle	Addr		SA+PA			
	Data		PD			

Command		Reset	Read Status Register	Clear Status Register	Program Suspend	Program Resume
Cycles		1	1	1	1	1
1st Bus Cycle	Addr	X	SA+555	SA+555	XXX	SA+000
	Data	F0	70	71	51	50
2nd Bus Cycle	Addr		SA			
	Data		RR			
3rd Bus Cycle	Addr					
	Data					
4th Bus Cycle	Addr					
	Data					

Command		Erase Suspend	Erase Resume	Blank Check	Sector Protected /Un-protected	Sector Lock Range
Cycles		1	1	1	3	4
1st Bus Cycle	Addr	XXX	SA+000	SA+555	555	555
	Data	B0	30	33	60	60
2nd Bus Cycle	Addr				2AA	2AA
	Data				60	60
3rd Bus Cycle	Addr				SLA	SLA
	Data				60	61
4th Bus Cycle	Addr					SLA
	Data					61

Command		ID/CFI Mode			Deep Power Down	
		Enter	Read	Exit	Enter	Exit
Cycles		1	1	1	**3**	**1**
1st Bus Cycle	Addr	SA+X55	SA+RA	XXX	555	XXX
	Data	90[1] / 98[2]	data	F0	AA	AB
2nd Bus Cycle	Addr				2AA	
	Data				55	
3rd Bus Cycle	Addr				XXX	
	Data				B9	
4thBus Cycle	Addr					
	Data					

Command		Configuration Register				
		Enter	Program to Buffer	Program Buffer to Flash	Read	Exit
Cycles		1	3	1	**1**	**1**
1st Bus Cycle	Addr	SA+555	SA+555	SA+555	SA+X00	XXX
	Data	D0	25	29	RR	F0
2nd Bus Cycle	Addr		SA+2AA			
	Data		0			
3rd Bus Cycle	Addr		SA+X00			
	Data		PD			
4thBus Cycle	Addr					
	Data					

Command		SSS Lock				
		Enter	Program to Buffer	Program Buffer to Flash	Read	Exit
Cycles		1	3	1	**1**	**1**
1st Bus Cycle	Addr	SA+555	SA+555	SA+555	SA+XXX	XXX
	Data	40	25	29	RR	F0
2nd Bus Cycle	Addr		SA+2AA			
	Data		0			
3rd Bus Cycle	Addr		SA+00			
	Data		PD			
4thBus Cycle	Addr					
	Data					

***Note** 1 = ID*

***Note** 2 = CFI*

Command		Secured Silicon Sector Region				
		Enter	Program to Buffer	Program Buffer to Flash	Read	Exit
Cycles		1	3-34 (Note1)	1	1	1
1st Bus Cycle	Addr	SA+555	SA+555	SA+555	SA+RA	XXX
	Data	88	25	29	RD	F0
2nd Bus Cycle	Addr		SA+2AA			
	Data		WC			
3rd Bus Cycle	Addr		SA+PA			
	Data		PD			
4thBus Cycle	Addr		SA+PA			
	Data		PD			

X = Don't care

RA = Address of the memory location to be read.

RD = Data read from location RA during read operation.

PA = Address of the memory location to be programmed. Addresses latch on the falling edge of the WE# or CE# pulse, whichever happens later.

PD = Data to be programmed at location PA. Data latches on the rising edge of WE# or CE# pulse, whichever happens first.

SA = Address of the sector to be verified or erased. Address bits Amax - A13 uniquely select any sector.

WC = Word Count. Number of write buffer locations to load minus 1

SLA= Sector Lock Address

RR= Read Register value

NOTE 1:

The minimum cycles are 3 and the maximum cycles are 34. The number depends on the data which need to be programmed at location PA.

8. ENERGY SAVING MODE

8-1. Standby Mode

The device enters Standby mode whenever the RESET# and CE# pins are both held High except in the embedded mode. While in this mode, WE# and OE# will be ignored, all Data Output pins will be in a high impedance state, and the device will draw minimal (ICC3) current.

8-2. Automatic Sleep Mode

Automatic Sleep mode is able to minimize power consumption of flash device. The device automatically enters this mode when the addresses and clock stays stable. The automatic sleep mode will not be influenced by the CE#, WE#, and OE# control signals. Standard address access timings are responsible for offering new data when addresses are changed.

Output data will be always available to the system and latched in sleep mode.

ICC6 in the **Table 9. DC Characteristics** indicates the current specifications for Automatic Sleep mode. Automatic Sleep mode is not allowed while in sync read mode.

8-3. Output Disable

Output (A/Q15-A/Q0) is disabled and in tri-state when OE#=VIH. OE# doesn't control the RDY.

Table 9. DC Characteristics

Parameter	Description	Test Conditions		Min	Typ	Max	Unit
ICCB	VCC Active Burst Read Current	CE# = VIL, OE# = VIH, WE#=VIH, burst length = 8	108 MHz		15	33	mA
		CE# = VIL, OE# = VIH, WE#=VIH, burst length = 16	108 MHz		15	35	mA
		CE# = VIL, OE# = VIH, WE#=VIH, burst length = continuous	108 MHz		20	39	mA
ICC1	VCC Active Asynchronous Read Current	CE# = VIL, OE# = VIH, WE#=VIH,	5 MHz		10	18	mA
			1 MHz		3	4	mA
ICC2	VCC Active Write Current	CE# = VIL, OE# = VIH, WP#/ACC = VIH			20	60	mA
ICC3	VCC Standby Current	CE# = Vcc+/-0.2V, RESET# = Vcc+/-0.2V			30	115	uA
ICC4	VCC Reset Current	RESET# = VIL, CLK = VIL			30	150	uA
ICC5	VCC Read While Write Current	CE#=VIL, OE#=VIH, WP#/ACC=VIH			71	76	mA
ICC6	VCC Sleep Current	CE# = VIL, OE# = VIH			30	115	uA
IDPD	Vcc Deep Power Down Current	CE# = Vcc+/-0.2V, RESET# = Vcc+/-0.2V			5	50	uA
ILO	Output Leakage Current	VOUT = VSS to VCC, VCC = VCC max				±1	uA
ILHV	High Voltage Pin Leakage Current	VIN=Vhv, VCC=VCC max				35	uA
ILI	Input Leakage Current	VIN = VSS to VCC, VCC = VCC max				±1	uA
IPPE	Accelerated Erase Current	WP#/ACC = Vhv			10	30	mA
IPPW	Accelerated Program Current	WP#/ACC = Vhv			5	30	mA
Vhv	Very High Voltage for Accelerated Program			8.5		9.5	V
VIH	Input High Voltage			VI/O-0.4		VI/O+0.4	V
VIL	Input Low Voltage			-0.2		0.4	V
VLKO	Low VCC Lock-out Voltage			1.0		1.4	V
VOH	Output High Voltage	IOH = –100 uA, VCC = VCC min		0.85x VI/O			V
VOL	Output Low Voltage	IOL = 100 uA, VCC = VCC min				0.45	V

8-3-1. Hardware Reset

Driving the RESET# pin LOW for a period of tRP or more will return the device to Read mode. If the device is in the process of a program or erase operation, the reset operation will take at most a period of tRH before the device returns to Read mode.

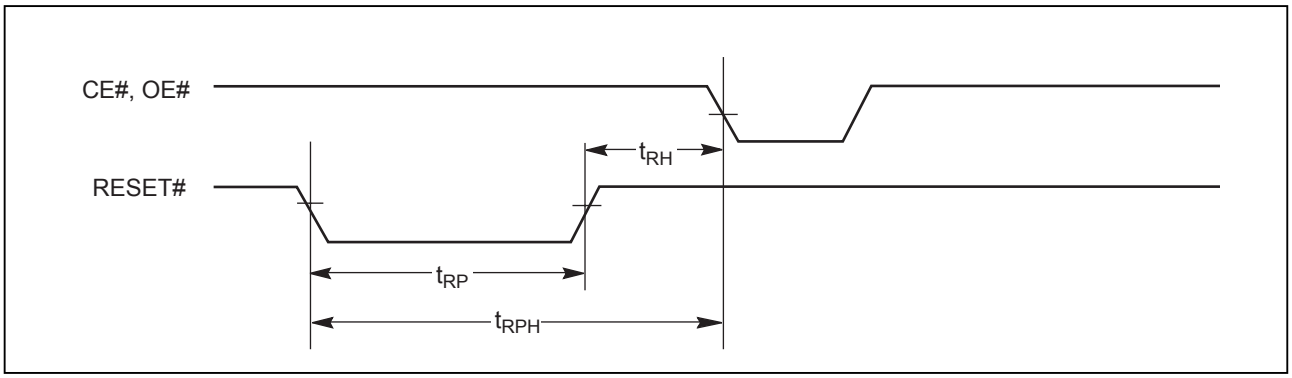
When the RESET# pin is held at GND±0.3V, the device only consumes standby (Isbr) current. However, the device draws larger current if the RESET# pin is held at a voltage greater than GND+0.3V and less than or equal to Vil.

It is recommended to tie the system reset signal to the RESET# pin of the flash memory. This allows the device to be reset with the system and puts it in a state where the system can immediately begin reading boot code from it.

Table 10. Hardware Reset

Parameter	Description		Speed	Unit
tRP	RESET# Waveform Width	RESET at Embedded Program / Erase Operation	25	us
		RESET at Read Operation	5	us
tRH	Reset High Time Before Read		200	ns

Figure 5. Reset Timings



8-3-2. Software Reset

Software reset is one of reset commands in the command set **(See Chapter 7. Command Definitions**) that is able to return the device to read array memory after reset. It must be used under the following conditions:

1. Exit SSS Lock.
2. Exit Secured Silicon Sector region.
3. Exit Configuration Register Region.
4. Exit ID/CFI mode.

9. Device ID and COMMON FLASH MEMORY INTERFACE (CFI) MODE

The device features CFI mode. Host system can retrieve the operating characteristics, structure and vendor-specified information such as identifying information, memory size, byte/word configuration, operating voltages and timing information of this device by CFI mode. If the system writes the CFI Query command "98h", to address "55h", the device will enter the CFI Query Mode. The system can read CFI information at the addresses given in **Table 13.**

Once user enters CFI query mode, users are allowed to issue reset command to exit CFI mode and return to read array mode.

Table 11-1. ID/CFI Mode: Device ID

Description	Address (h) (Word Mode)	Data (h)
Macronix Manufacture ID	00	C2h
Device ID	01	007E
Revision ID	03	00h
ID Version	06	10h
Security Silicon	07	Q5-Q0=Reserved Q6 - Customer Lock Bit 0 = Un-Locked, 1 = Locked, Q7 - Factory Lock Bit 0 = Un-Locked, 1 = Locked Q8 - Q15 = Reserved
Lower Software Bites	0C	05h Bit 0 - Status Register Support 1 = Status Register Supported 0 = Status register not Supported Bit 1 - DQ Polling Support 1 = DQ bits polling supported 0 = DQ bits polling not supported Bit 3-2 - Command Set Support 11 = Reserved 10 = Reserved 01 = Reduced Command Set 0 = Old Command Set Bit 4- F - Reserved
High Order Device ID, Word 2	0E	0063h/Top; 0065h/Bottom
Low Order Device ID, Word 3	0F	0001h (Top/Bottom)

Table 11-2. ID/CFI Mode: Identification Data Values

Description	Address (h) (Word Mode)	Data (h)
Query-unique ASCII string "QRY"	10	0051h
	11	0052h
	12	0059h
Primary vendor command set and control interface ID code	13	0002h
	14	0000h
Address for primary algorithm extended query table	15	0040h
	16	0000h
Alternate vendor command set and control interface ID code	17	0000h
	18	0000h
Address for alternate algorithm extended query table	19	0000h
	1A	0000h

Table 11-3. ID/CFI Mode: System Interface Data Values

Description	Address (h) (Word Mode)	Data (h)
VCC Min. (program/erase) D7–D4: volt, D3–D0: 100 millivolt	1Bh	0017h
VCC Max. (program/erase) D7–D4: volt, D3–D0: 100 millivolt	1Ch	0019h
ACC Min. voltage (00h = no ACC pin present) Refer to 4Dh	1Dh	0000h
ACC Max. voltage (00h = no ACC pin present) Refer to 4Eh	1Eh	0000h
Typical timeout per single word write 2^N us	1Fh	0004h
Typical timeout for Min. size buffer write 2^N us (00h = not supported)	20h	0009h
Typical timeout per individual block erase 2^N ms	21h	000Ah
Typical timeout for full chip erase 2^N ms (00h = not supported)	22h	0011h
Max. timeout for word write 2^N times typical	23h	0004h
Max. timeout for buffer write 2^N times typical	24h	0002h
Max. timeout for sector erase 2^N times typical	25h	0003h
Max. timeout for full chip erase 2^N times typical (00h = not supported)	26h	0002h

Table 11-4. CFI Mode: Device Geometry Data Values

Description	Address	Data
		128E
Device Size = 2^N byte	27h	0018h
Flash Device Interface description (refer to CFI publication 100)	28h	0001h
	29h	0000h
Max. number of bytes in multi-byte write = 2^N (00h = not supported)	2Ah	0006h
	2Bh	0000h
Number of Erase Block Regions within device	2Ch	0002h
Erase Block Region 1 Information (refer to the CFI specification or CFI publication 100)	2Dh	007Eh (Top Boot)
		0003h (Bottom Boot)
	2Eh	0000h
	2Fh	0000h (Top Boot)
		0080h (Bottom Boot)
	30h	0002h (Top Boot)
		0000h (Bottom Boot)
Erase Block Region 2 Information	31h	0003h (Top Boot)
		007Eh (Bottm Boot)
	32h	0000h
	33h	0080h (Top Boot)
		0000h (Bottom Boot)
	34h	0000h (Top Boot)
		0002h (Bottom Boot)

Table 11-5. CFI Mode: Primary Vendor-Specific Extended Query Data Values

Description	Address (h) (Word Mode)	Data (h)
Query - Primary extended table, unique ASCII string, PRI	40h	0050h
	41h	0052h
	42h	0049h
Major version number, ASCII	43h	0031h
Minor version number, ASCII	44h	0033h
Unlock recognizes address (Bits 1-0) 0= recognize, 1= don't recognize	45h	0000h
Erase suspend (2= to both read and program)	46h	0002h
Sector protect (N= # of sectors/group)	47h	0001h
Temporary sector unprotect (1=supported)	48h	0000h
Sector protect/Chip unprotect scheme	49h	0008h
Simultaneous R/W operation (0=not supported)	4Ah	0000h
Burst mode (0=not supported)	4Bh	0001h
Page mode (0=not supported, 01 = 4 word page, 02 = 8 word page)	4Ch	0000h
Minimum ACC(acceleration) supply (0= not supported), [D7:D4] for volt, [D3:D0] for 100mV	4Dh	0085h
Maximum ACC(acceleration) supply (0= not supported), [D7:D4] for volt, [D3:D0] for 100mV	4Eh	0095h
Top/Bottom Sector Flags 00h: Uniform 02h: Bottom Boot 03h: Top Boot	4Fh	02h (Bottom Boot)
		03h (Top Boot)
Program Suspend (0=not supported, 1=supported)	50h	0001h

Table 11-6. CFI Mode: ID/CFI Data

Description	Address (h) (Word Mode)	Data (h)
Unlock Bypass 00h = Not Supported 01h = Supported	51h	0000h
Secure Silicon Region (Customer Lockable Region) Size 2N bytes	52h	0008h
Hardware Reset Low Time-out until reset is completed during an embedded algorithm - Maximum 2^N ns (e.g. 10 µs => n = E)	53h	000Eh
Hardware Reset Low Time-out until reset is completed not during an embedded algorithm - Maximum 2^N ns (e.g. 10 µs => n = E)	54h	0008h
Erase Suspend Time-out Maximum 2^N us	55h	0005h
Program Suspend Time-out Maximum 2^N us	56h	0005h
Bank Organization: X= Number of banks	57h	0008h
Bank 0 Region Information X= Number of sectors in bank	58h	0010h (Top Boot)
		0013h (Bottom Boot)
Bank 1 Region Information X= Number of sectors in bank	59h	0010h
Bank 2 Region Information X= Number of sectors in bank	5Ah	0010h
Bank 3 Region Information X= Number of sectors in bank	5Bh	0010h
Bank 4 Region Information X= Number of sectors in bank	5Ch	0010h
Bank 5 Region Information. X= Number of sectors in bank	5Dh	0010h
Bank 6 Region Information X= Number of sectors in bank	5Eh	0010h
Bank 7 Region Information X= Number of sectors in bank	5Fh	0010h (Bottom Boot)
		0013h (Top Boot)

10. ELECTRICAL CHARACTERISTICS

10-1. Absolute Maximum Stress Ratings

Surrounding Temperature with Bias		-65°C to +125°C
Storage Temperature		-65°C to +150°C
Voltage Range	VCC	-0.5V to VCC+0.5V
	VI/O	-0.5V to VCC+0.5V
	ACC	-0.5V to +10.5V
	The other pins.	-0.5V to Vcc +0.5V
Output Short Circuit Current (less than one second)		200 mA

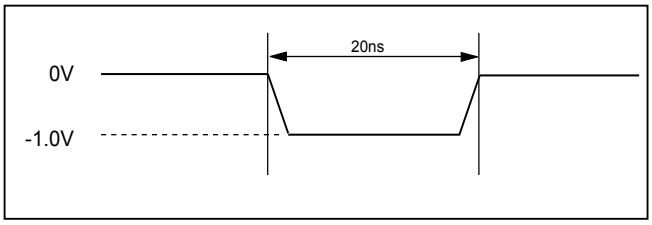
10-2. Operating Temperatures and Voltages

Commercial (C) Grade	Surrounding Temperature (T_A)	0°C to +70°C
Industrial (I) Grade	Surrounding Temperature (T_A)	-40°C to +85°C
VCC Supply Voltages	Full VCC range	1.7-1.95V
	VI/O range	= VCC

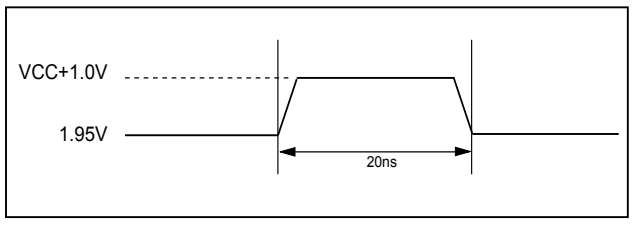
NOTES:

1. *Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and functional operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.*
2. *Specifications contained within the following tables are subject to change.*
3. *During voltage transitions, all pins may overshoot to VCC+1.0V or -1.0V for period up to 20ns.*

Maximum Positive Overshoot Waveform



Maximum Negative Overshoot Waveform



10-3. Test Conditions

Testing Conditions:

- Output Load Capacitance, CL : 1TTL gate, 10pF
- Rise/Fall Times : 2ns
- Input Pulse levels :0.0 - VI/O
- In/Out reference levels :0.5VI/O

Figure 6. Test Setup

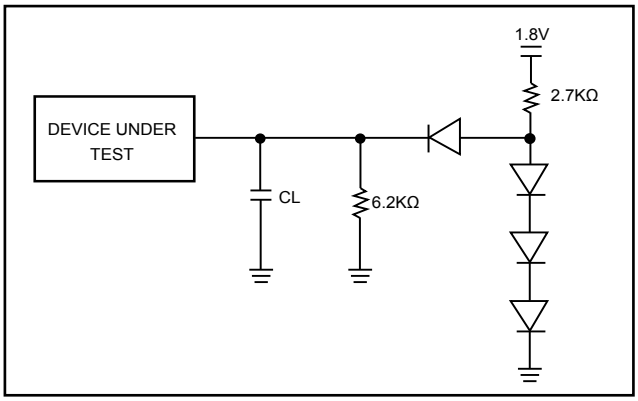
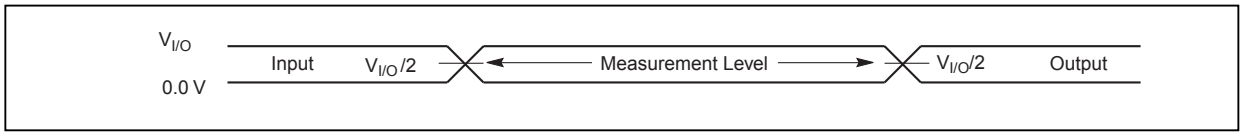


Figure 7. Input Waveforms and Measurement Levels



10-4. AC Characteristics

VCC Power-up and Power-down Sequencing

Once VCC attains its operating voltage, de-assertion of RESET# to VIH is permitted. VCC power-up and power-down sequencing are not restricted. During the entire VCC power sequence, RESET# needs to be asserted to VIL until the respective supplies reach their operating voltages. Once VCC operating voltage has been achieved, RESET# to VIH is allowed to be de-asserted.

Output Disable Mode

Once OE# is input is at VIH, output from the device is disabled and placed in the state of high impedance.

VCC Power-up

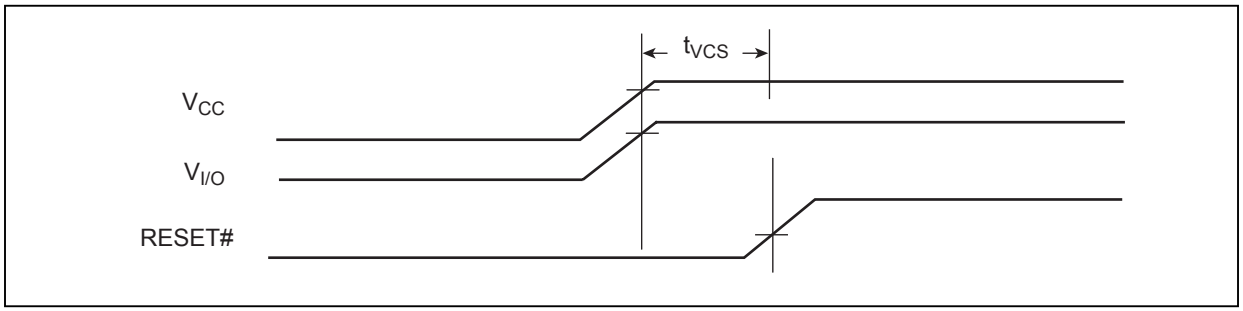
Parameter	Description	Test Setup	Speed	Unit
tVCS	VCC Setup Time	Min	1	ms

NOTES:

1. VCC >+ VI/O - 100 mV

2. VCC ramp rate is > 100 us/V

Figure 8. VCC Power-up Diagram



CLK CHARACTERISTICS

Parameter	Description		Frequency			Unit
			66	83	108	
tCLK	**CLK Cycle**	Min	15	12	9.26	ns
tCLKR	**CLK Rise Time**	Max	3	2.5	1.9	ns
tCLKF	**CLK Fall Time**					
tCLKH/L	**CLK High or Low Time**	Min	7	5.5	4.2	ns

NOTES:

1. Clock jitter of +/- 5% permitted.

2. Not 100% tested.

AC CHARACTERISTICS

ITEM		TYP	MAX
WEB high to release from deep power down mode	tRDP	100us	200us
WEB high to deep power down mode	tDP	10us	20us

Figure 9. Deep Power Down Mode Waveform

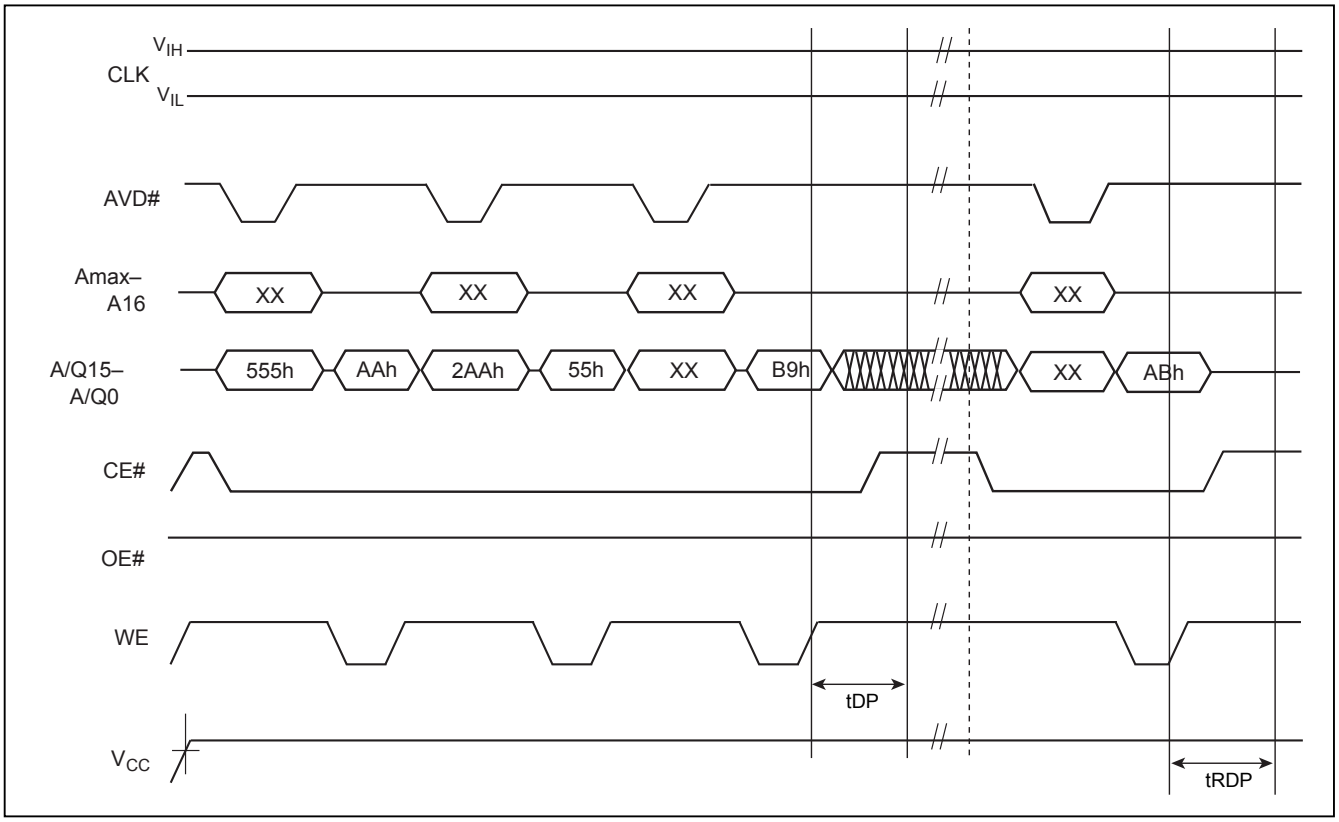


Figure 10. CLK Characterization

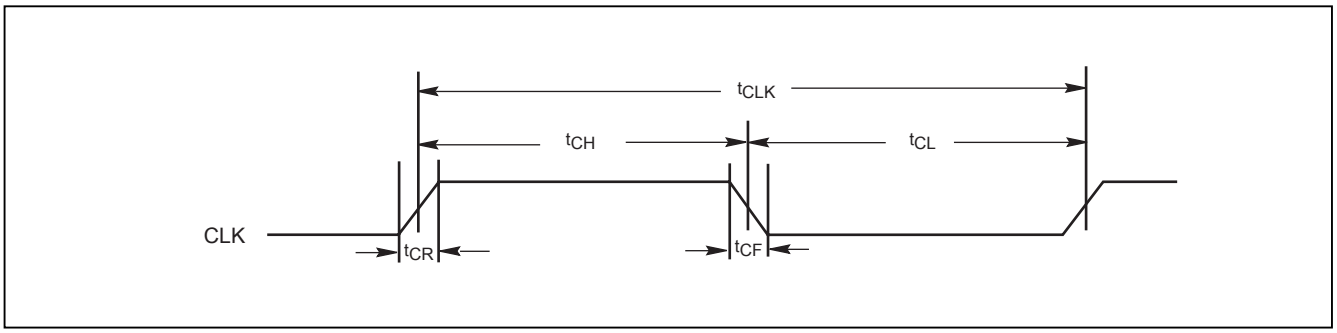


Table 12. Synchronous / Burst Read

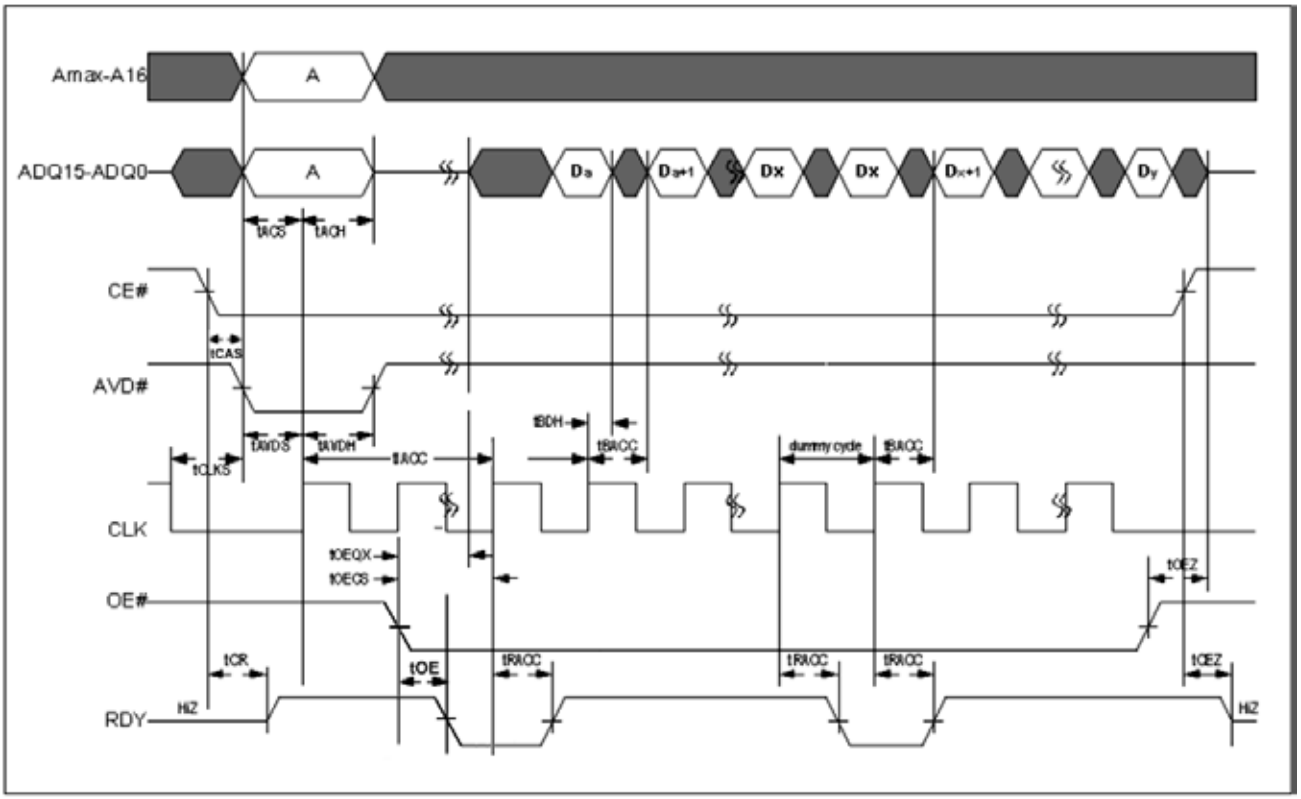
Parameter	Description		Speed	Unit
tIACC	Initial Access Time	Max	75	ns
tBACC	Burst Access Time Valid Clock to Output Delay	Max	7	ns
tAVDS	AVD# Setup Time to CLK	Min	4	ns
tAVDH	AVD# Hold Time from CLK	Min	5	ns
tAVDO	AVD# High to OE# Low	Min	4	ns
tACS	Address Setup Time to CLK	Min	4	ns
tACH	Address Hold Time from CLK	Min	5	ns
tBDH	Data Hold Time from Next Clock Cycle	Min	0	ns
tCEZ	Chip Enable to High Z (Note)	Max	10	ns
tOEZ	Output Enable to High Z (Note)	Max	10	ns
tCES	CE# Setup Time to CLK	Min	4	ns
tRACC	Ready access time from CLK	Max	7	ns
tCLKS	CLK low to AVD# low	Min	5	ns
tOECS	OE# Enable to First Output CLK Setup Time	Min	8	ns
tOE	Output Enable to Valid Data	Max	15	ns
tCAS	CE# Setup Time to Falling Edged of AVD#	Min	0	ns

NOTES:

1. Not 100% tested.

2. AVD# cannot be VIL for 2 subsequent clock cycles.

Figure 11. Burst Mode Read



NOTE: *Chip enters burst mode once 1st CLK rises and AVD# equals to VIL.*

Table 13. Asynchronous Read

Parameter	Description		Speed	Unit
tCE	Access Time from CE# Low	Max	80	ns
tACC	Asynchronous Access Time	Max	80	ns
tAVDP	AVD# Low Time	Min	7	ns
tAAVDS	Address Setup Time to Rising Edge of AVD#	Min	3.5	ns
tAAVDH	Address Hold Time from Rising Edge of AVD#	Min	3.2	ns
tOE	Output Enable to Output Valid	Max	15	ns
tOEH	WE# disable to OE# enable	Min	4	ns
tOEZ	Output disable to High Z (See Note)	Max	10	ns
tOAVD	AVD# disable to OEB enable	Min	10	ns
tAVDO	OE# disable to AVD# enable	Min	10	ns
tOEQX	Output Enable to Data Low Z	Min	0	ns
tCR	CE# enable to RDY ready	Max	10	ns
tCEZ	CE# disable to RDY HiZ	Max	10	ns
tCAS	CE# Setup Time to Falling Edged of AVD#	Min	0	ns

NOTE: *Not 100% tested.*

Figure 12. Asynchronous Mode Read

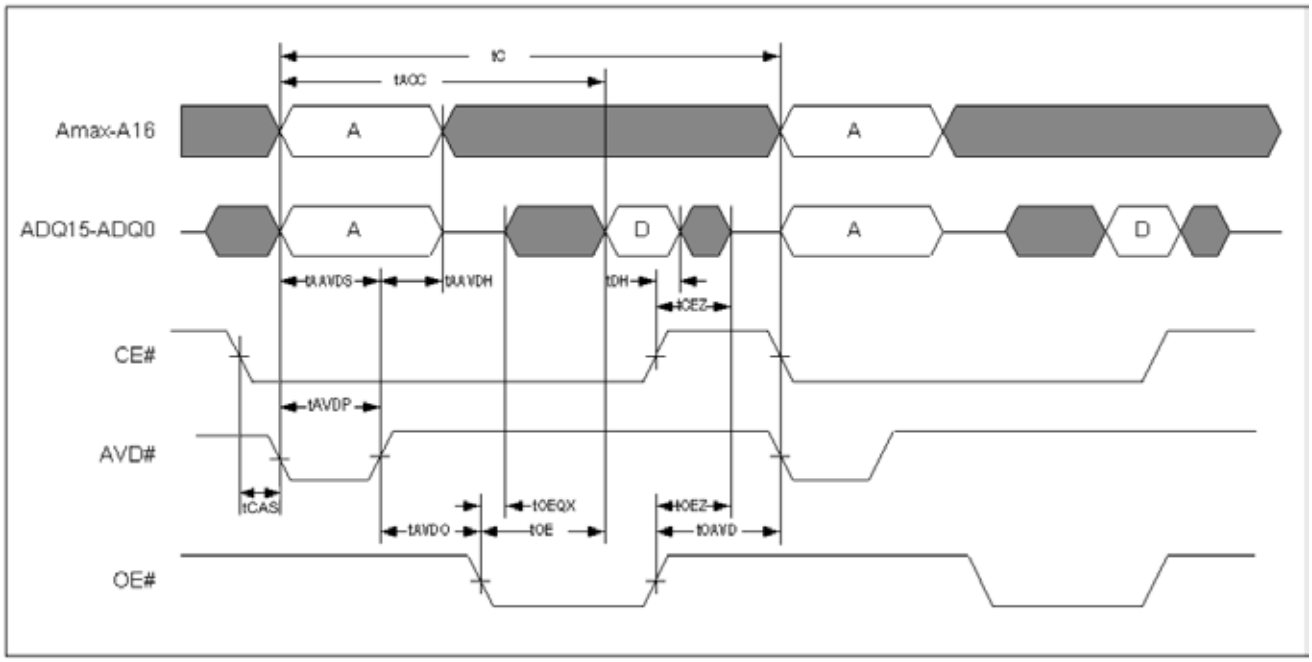


Table 14. Erase/Program Operations

Parameter	Description		Speed	Unit
tWC	Write Cycle Time (Note 1)	Min	45	ns
tAS	Address Setup Time	Min	4	ns
tAH	Address Hold Time	Min	6	ns
tAVDP	AVD# Low Time	Min	7	ns
tDS	Data Setup Time	Min	25	ns
tDH	Data Hold Time	Min	0	ns
tGHWL	Read Recovery Time Before Write	Min	0	ns
tCS	CE# Setup Time to WE#	Min	8	ns
tCH	CE# Hold Time	Min	0	ns
tWP/tWRL	Write Pulse Width	Min	30	ns
tWPH	Write Pulse Width High	Min	20	ns
tSR/W	Latency Between Read and Write Operations	Min	0	ns
tACC	ACC Rise and Fall Time	Min	500	ns
tVPS	ACC Setup Time (During Accelerated Programming)	Min	1	us
tVCS	VCC Setup Time	Min	1	ms
tESL	Erase Suspend Latency	Max	25	us
tPSL	Program Suspend Latency	Max	25	us
tERS	Erase Resume to Erase Suspend	Min	400	us
tPRS	Program Resume to Program Suspend	Min	25	us
tWEA	WEB disable to AVD# enable	Min	9.2	ns
tVLWH	AVD# disable to WEB# disable	Min	23.5	ns
tCAS	CE# Setup Time to Falling Edged of AVD#	Min	0	ns
tWEH	OE# Disable to WE# Enable Time	Min	4	ns

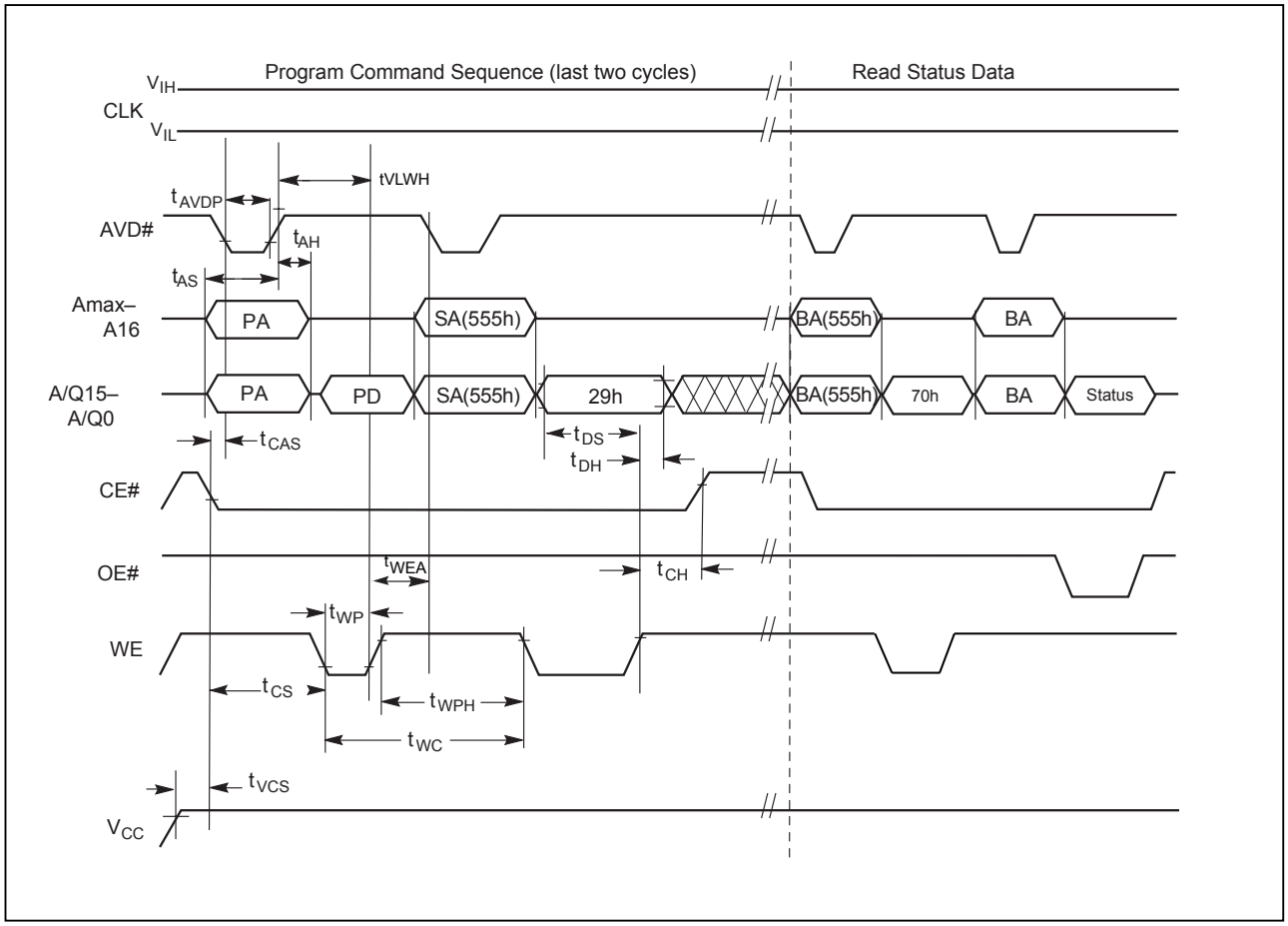
NOTES:

1. Not 100% tested.

2. See the Erase and Programming Performance section for more information.

3. Preprogramming time is not included.

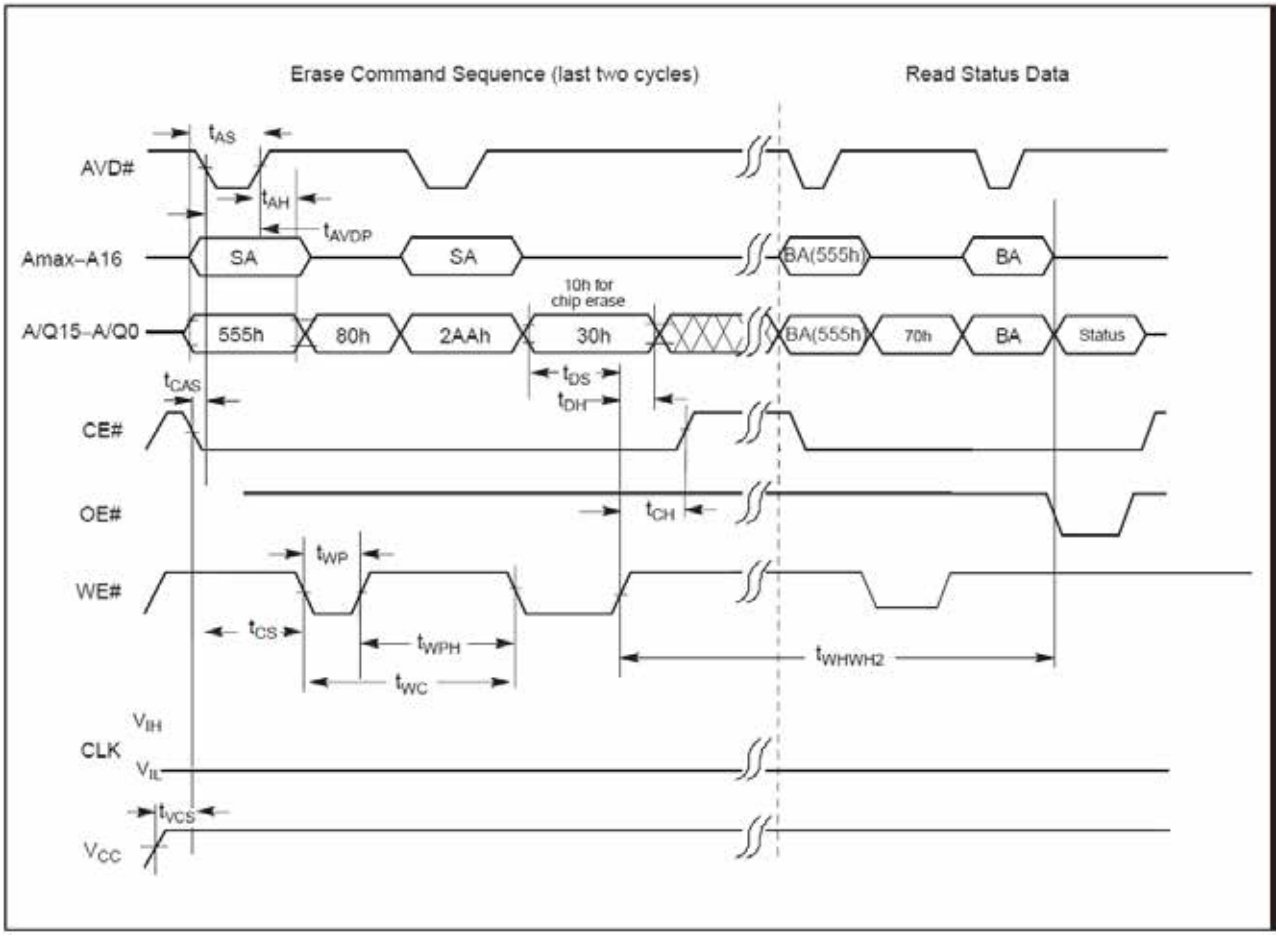
Figure 13. Program Operation Timings



NOTES:

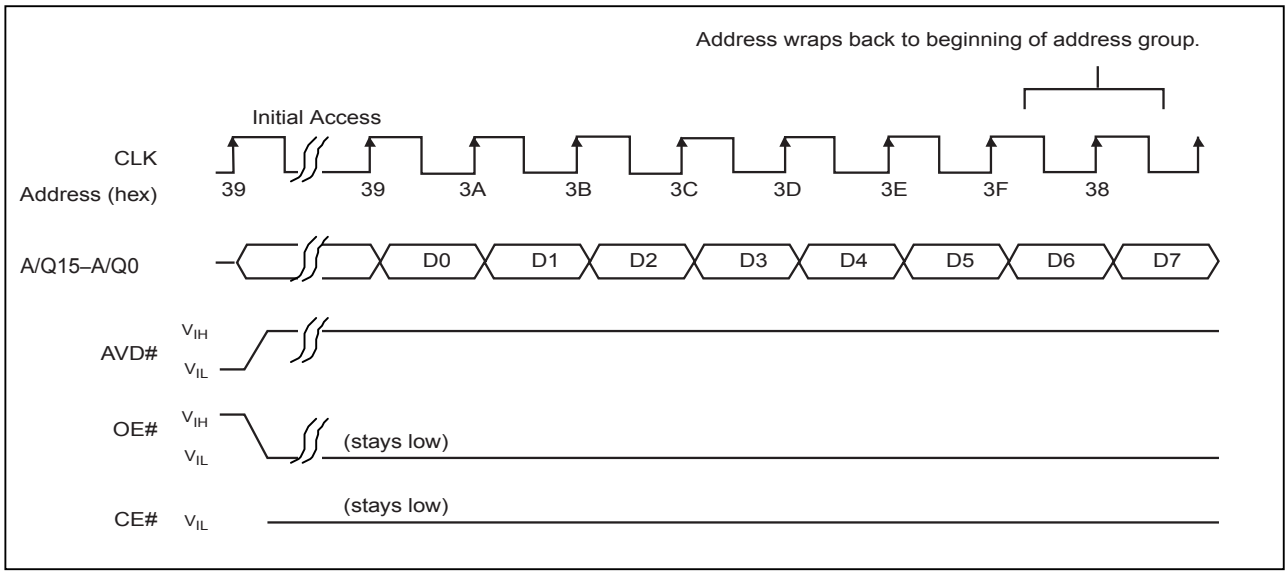
1. *PA = Program Address, PD = Program Data, VA = Valid Address for reading status bits.*
2. *"In progress" and "complete" refer to status of program operation.*
3. *BA = Address bits are sufficient to select a bank.*

Figure 14. Chip/Sector Erase Operations



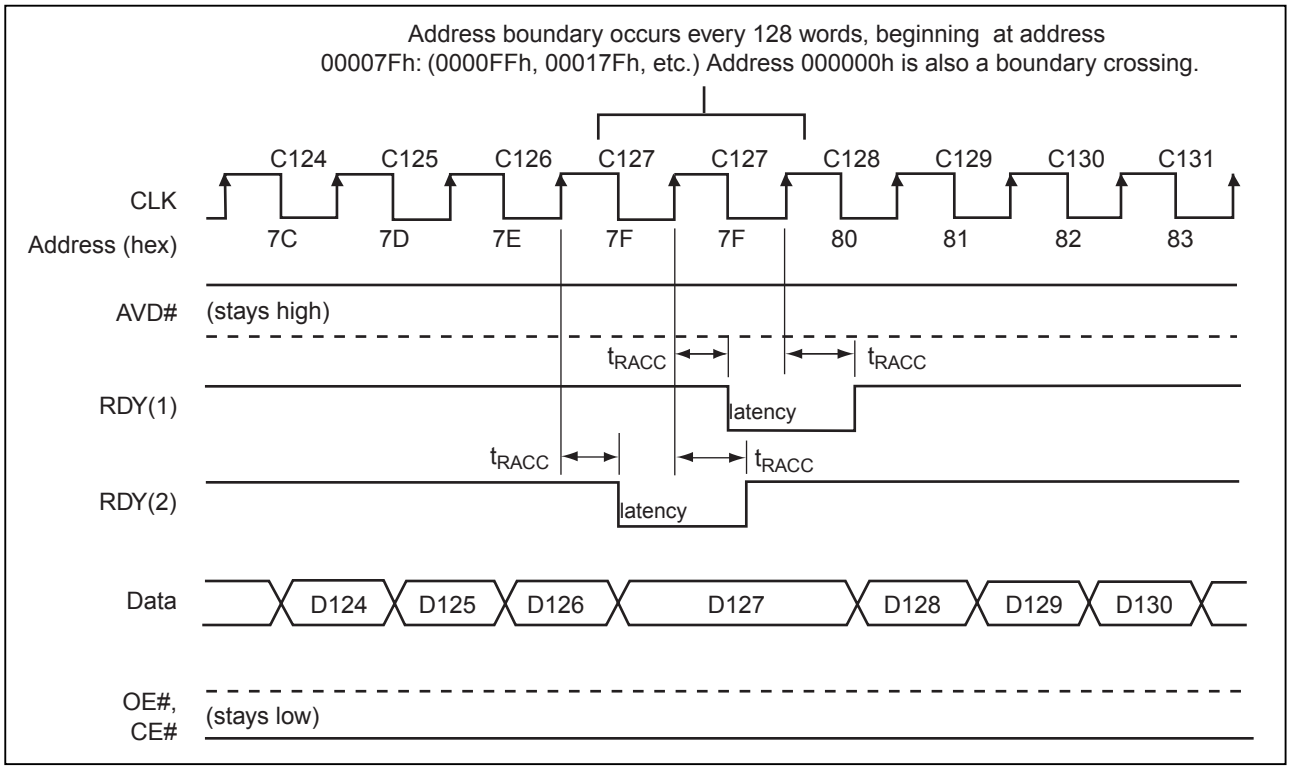
NOTE: *SA is the sector address for Sector Erase.*

Figure 15. 8-, 16-Word Linear Burst Address Wrap Around



NOTE: *8-word linear burst mode shown. 16-word linear burst read modes behave similarly. D0 represents the first word of the linear burst.*

Figure 16. Latency with Boundary Crossing



NOTES:

1. *Cxx indicates the clock that triggers data Dxx on the outputs; for example, C60 triggers D60.*
2. *Please reference burst read related tables for details.*

10-5. Erase and Programming Performance

PARAMETER	LIMITS			UNITS
	MIN.	TYP. (1)	MAX. (2)	
Chip Programming Time (128Mb)		70		sec
Chip Erase Time (128Mb)		80	300	sec
Sector Erase Time (16KW)		0.5	5	sec
Sector Erase Time (64KW)		1	7	sec
Word Program Time		30	360	us
Total Write Buffer Time		240		us
ACC Total Write Buffer Time		80		us
Erase/Program Cycles		100,000		cycles
Effective Word Programming Time		7.5		us
Blank Check Time			10	ms

NOTES:

1. *Typical program and erase times assume the following conditions: 25°C, 1.8V VCC. Programming specifications assume checkboard data pattern.*
2. *Maximum values are measured at VCC = 1.8 V, worst case temperature. Maximum values are valid up to and including 100,000 program/erase cycles.*
3. *Erase/Program cycles comply with JEDEC JESD-47E & A117A standard.*
4. *Exclude 00h program before erase operation.*

Data Retention

PARAMETER	Condition	Min.	Max.	UNIT
Data retention	55˚C	20		years

Latch-up Characteristics

	MIN.	MAX.
Input Voltage voltage difference with GND on WP#/ACC pins	-1.0V	10.5V
Input Voltage voltage difference with GND on all normal pins input	-1.0V	1.5Vcc
Vcc Current	-100mA	+100mA
All pins included except Vcc. Test conditions: Vcc = 1.8V, one pin per testing		

Pin Capacitance

Parameter Symbol	Parameter Description	Test Setup	TYP	MAX	UNIT
CIN2	Control Pin Capacitance	VIN=0	7.5	9	pF
COUT	Output Capacitance	VOUT=0	8.5	12	pF
CIN	Input Capacitance	VIN=0	6	7.5	pF

10-5-1. BGA Ball Capacitance

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
CIN	Input Capacitance	VIN = 0	4.2	5.0	pF
COUT	Output Capacitance	VOUT = 0	5.4	6.5	pF
CIN2	Control Pin Capacitance	VIN = 0	3.9	4.7	pF

NOTES:

1. *Sampled, not 100% tested.*
2. *Test conditions TA = 25°C, f = 1.0 MHz.*

10-6. Low VCC Write Prohibit

The device refuses to accept any write command when Vcc is less than VLKO. This prevents data from spuriously being altered during power-up, power-down, or temporary power interruptions. The device automatically resets itself when Vcc is lower than VLKO and write cycles are ignored until Vcc is greater than VLKO. The system must provide proper signals on control pins after Vcc rises above VLKO to avoid unintentional program or erase operations.

10-6-1. Write Pulse "Glitch" Protection

CE#, WE#, OE# pulses shorter than 5ns are treated as glitches and will not be regarded as an effective write cycle. On WE#, noise pulses of less than 5ns do not initiate a write cycle.

10-6-2. Logical Prohibit

A valid write cycle requires both CE# and WE# at Vil with OE# at Vih. While initiating a write cycle, CE# and WE# must be a logical "0" while OE# is a logical "1". Write cycle is ignored when either CE# at Vih, WE# at Vih, or OE# at Vil.

10-6-3. Power-up Sequence

Upon power-up, the device is placed in Read mode. Furthermore, program or erase operation will begin only after successful completion of specified command sequences.

10-6-4. Power-up Write Prohibit

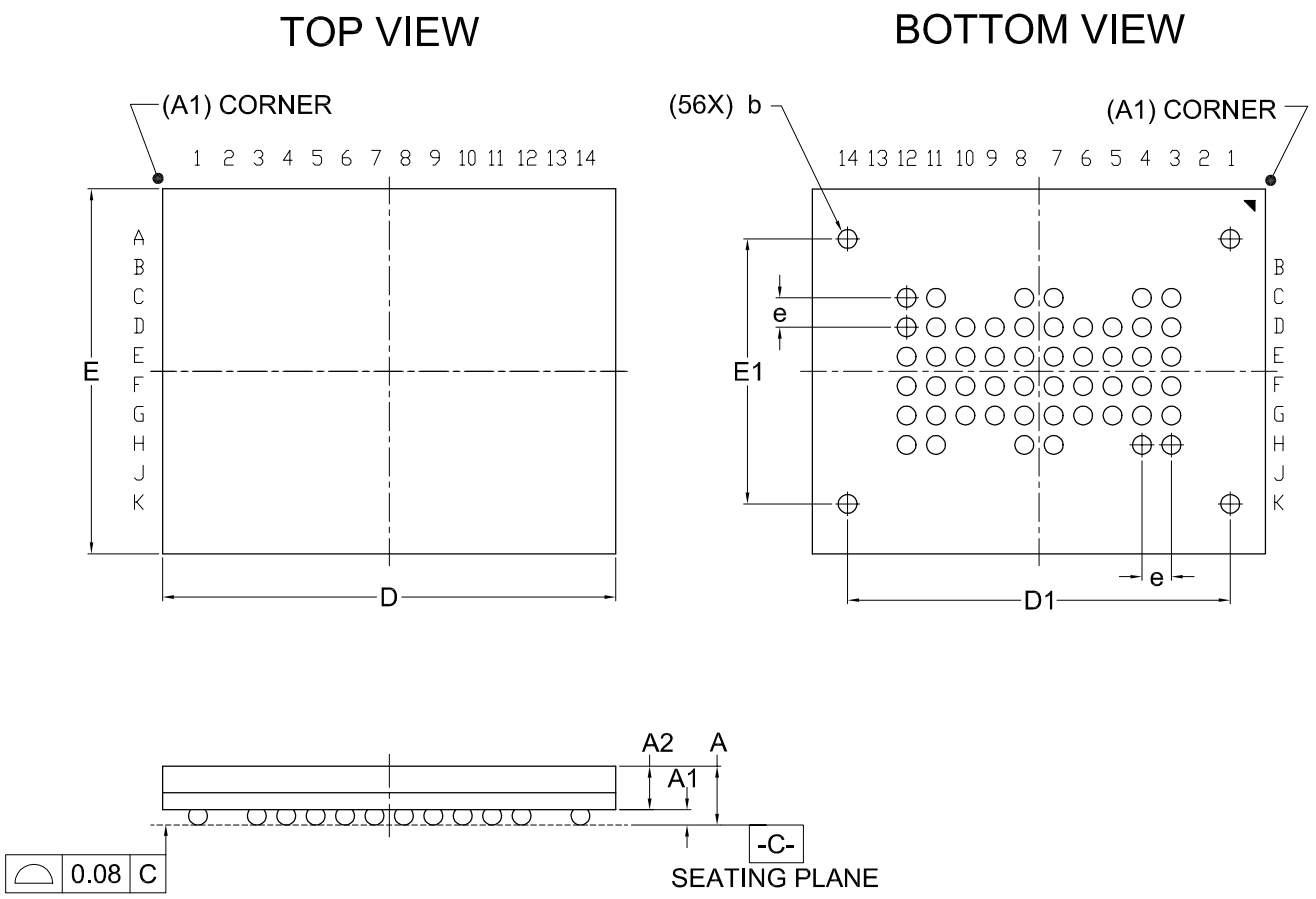
When WE#, CE# is held at Vil and OE# is held at Vih during power up, the device ignores the first command on the rising edge of WE#.

10-6-5. Power Supply Decoupling

A 0.1uF capacitor should be connected between the Vcc and GND to reduce the noise effect.

11. PACKAGE INFORMATION

Title: Package Outline for CSP 56BALL(7.7X6.2X1.2MM,BALL PITCH 0.5MM,BALL DIAMETER 0.3MM)



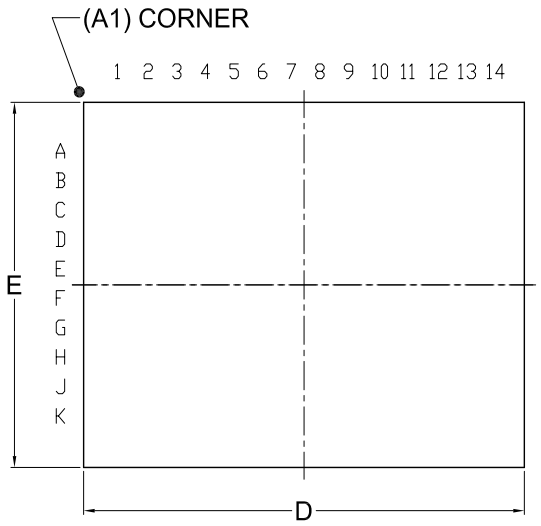
Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	D	D1	E	E1	e
mm	Min.	---	0.16	0.65	0.25	7.6	---	6.1	—	---
	Nom.	---	0.21	---	0.30	7.7	6.5	6.2	4.5	0.50
	Max.	1.20	0.26	---	0.35	7.8	---	6.3	—	---
Inch	Min.	---	0.006	0.026	0.010	0.299	—	0.240	—	---
	Nom.	---	0.008	—	0.012	0.303	0.256	0.244	0.177	0.0197
	Max.	0.047	0.010	—	0.014	0.307	—	0.248	—	---

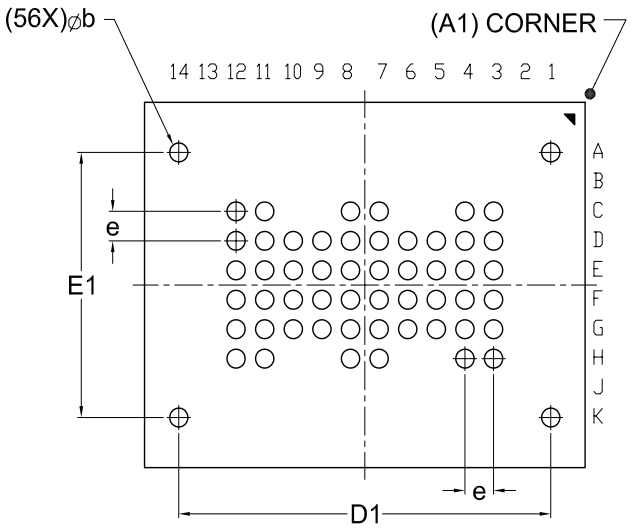
Dwg. No.	Revision	Reference			
		JEDEC	EIAJ		
6110-4264	0				

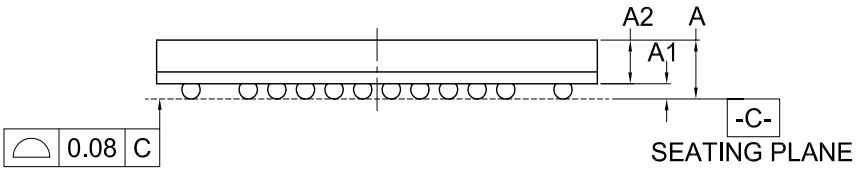
Doc. Title: Package Outline for CSP 56BALL(7.7X6.2X1.05MM,BALL PITCH 0.5MM,BALL DIAMETER 0.3MM)

TOP VIEW



BOTTOM VIEW





Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	D	D1	E	E1	e
mm	Min.	---	0.16	0.65	0.25	7.6	---	6.1	---	---
	Nom.	---	0.21	---	0.30	7.7	6.5	6.2	4.5	0.50
	Max.	1.05	0.26	---	0.35	7.8	---	6.3	---	---
Inch	Min.	---	0.006	0.026	0.010	0.299	---	0.240	---	---
	Nom.	---	0.008	---	0.012	0.303	0.256	0.244	0.177	0.0197
	Max.	0.041	0.010	---	0.014	0.307	---	0.248	---	---

Dwg. No.	Revision	Reference			
		JEDEC	EIAJ		
6110-4269	0	MO-225			

12. REVISION HISTORY

Rev. No.	Description	Page	Date
1.0	1. Removed "Advanced Information" from Features page	P5	FEB/22/2012
1.1	1. Modified Table 10-1. Voltage range (For VCC & VI/O) to VCC+0.5V	P49	AUG/05/2013
1.2	1. Updated D9 and DNU pin descriptions	P9,10	FEB/13/2014
	2. Modified the address and cycles of Program to buffer command.	P38,40	
	3. Added notes for ID/CFI mode enter data	P39	
	4. Modified VCC ramp up rate unit	P51	
	5. Updated pin descriptions for Write Protection	P6,10,18,26, 27,35,42,59	
	6. Modified Set Configuration Register Command Sequence	P32	
1.3	1. Modified waveform/descriptions for Asynchronous Read/ Erase/Program Operations	P54,55,56	MAR/21/2014
1.4	1. Added ordering information and package outline for 56-Ball TFBGA,	P7,8,62	OCT/21/2015

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