

## GENERAL DESCRIPTION

The 843251I-12 is a 10Gb Ethernet Clock Generator. The 843251I-12 uses an 18pF parallel resonant crystal over the range of 23.2MHz - 30MHz. For Ethernet applications, a 25MHz crystal is used. The 843251I-12 uses IDT's 3<sup>rd</sup> generation low phase noise VCO technology, and can achieve <1ps rms phase jitter performance over the 1.875MHz - 20MHz integration range. The 843251I-12 is packaged in a small 8-pin TSSOP, making it ideal for use in systems with limited board space.

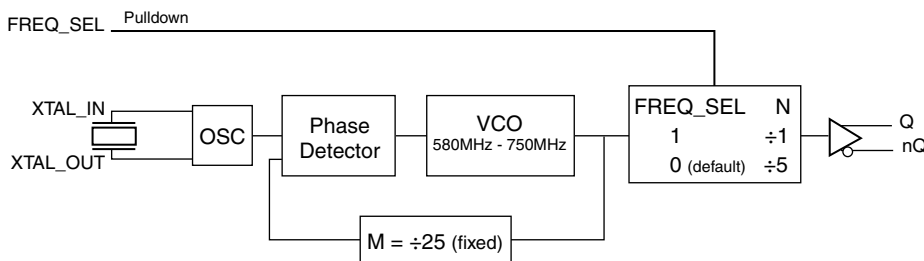
## FEATURES

- One Differential LVPECL output
- Crystal oscillator interface, 18pF parallel resonant crystal (23.2MHz - 30MHz)
- Output frequency range: 290MHz - 750MHz
- VCO range: 580MHz - 750MHz
- RMS phase jitter @ 312.5MHz, using a 25MHz crystal (1.875MHz - 20MHz): 0.36ps (typical)
- 3.3V or 2.5V operating supply
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

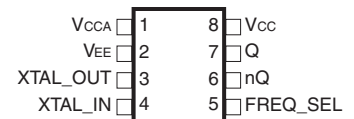
COMMON CONFIGURATION TABLE

Crystal Frequency (MHz)	Inputs				Output Frequency (MHz)
	FREQ_SEL	M	N	Multiplication Value M/N	
25	1	25	1	25	625
25	0	25	2	12.5	312.5

## BLOCK DIAGRAM



## PIN ASSIGNMENT



### 843251I-12

#### 8-Lead TSSOP

4.4mm x 3.0mm x 0.925mm package body

#### G Package

Top View

**TABLE 1. PIN DESCRIPTIONS**

Number	Name	Type		Description
1	V <sub>CCA</sub>	Power		Analog supply pin.
2	V <sub>EE</sub>	Power		Negative supply pin.
3, 4	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
5	FREQ_SEL	Input	Pulldown	Frequency select pin. LVCMOS/LVTTL interface levels.
6, 7	nQ, Q	Output		Differential clock outputs. LVPECL interface levels.
8	V <sub>CC</sub>	Power		Core supply pin.

NOTE: *Pulldown* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

**TABLE 2. PIN CHARACTERISTICS**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			4		pF
R <sub>PULLDOWN</sub>	Input Pulldown Resistor			51		kΩ

**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage, $V_{CC}$	4.6V
Inputs, $V_I$	-0.5V to $V_{CC} + 0.5V$
Outputs, $I_O$	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, $\theta_{JA}$	129.5°C/W (0 mps)
Storage Temperature, $T_{STG}$	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 3A. POWER SUPPLY DC CHARACTERISTICS,  $V_{CC} = 3.3V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  TO  $85^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{CC}$	Core Supply Voltage		3.135	3.3	3.465	V
$V_{CCA}$	Analog Supply Voltage		$V_{CC} - 0.10$	3.3	$V_{CC}$	V
$I_{EE}$	Power Supply Current				83	mA
$I_{CCA}$	Analog Supply Current				10	mA

**TABLE 3B. POWER SUPPLY DC CHARACTERISTICS,  $V_{CC} = 2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  TO  $85^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{CC}$	Core Supply Voltage		2.375	2.5	2.625	V
$V_{CCA}$	Analog Supply Voltage		$V_{CC} - 0.08$	2.5	$V_{CC}$	V
$I_{EE}$	Power Supply Current				78	mA
$I_{CCA}$	Analog Supply Current				8	mA

**TABLE 3C. LVCMOS/LVTTL DC CHARACTERISTICS,  $V_{CC} = 3.3V \pm 5\%$  OR  $2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  TO  $85^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage	$V_{CC} = 3.3V$	2		$V_{CC} + 0.3$	V
		$V_{CC} = 2.5V$	1.7		$V_{CC} + 0.3$	V
$V_{IL}$	Input Low Voltage	$V_{CC} = 3.3V$	-0.3		0.8	V
		$V_{CC} = 2.5V$	-0.3		0.7	V
$I_{IH}$	Input High Current	$V_{CC} = V_{IN} = 3.465V$ or $2.625V$			150	$\mu A$
$I_{IL}$	Input Low Current	$V_{CC} = 3.465V$ or $2.625V$ , $V_{IN} = 0V$	-5			$\mu A$

**TABLE 3D. LVPECL DC CHARACTERISTICS,  $V_{CC} = 3.3V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  TO  $85^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OH}$	Output High Voltage; NOTE 1		$V_{CC} - 1.4$		$V_{CC} - 0.9$	V
$V_{OL}$	Output Low Voltage; NOTE 1		$V_{CC} - 2.0$		$V_{CC} - 1.7$	V
$V_{SWING}$	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

 NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{CC} - 2V$ .

**TABLE 3E. LVPECL DC CHARACTERISTICS,  $V_{CC} = 2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  TO  $85^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OH}$	Output High Voltage; NOTE 1		$V_{CC} - 1.4$		$V_{CC} - 0.9$	V
$V_{OL}$	Output Low Voltage; NOTE 1		$V_{CC} - 2.0$		$V_{CC} - 1.5$	V
$V_{SWING}$	Peak-to-Peak Output Voltage Swing		0.4		1.0	V

 NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{CC} - 2V$ .

**TABLE 4. CRYSTAL CHARACTERISTICS**

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		23.2		30	MHz
Equivalent Series Resistance (ESR)				40	$\Omega$
Shunt Capacitance				7	pF

NOTE: It is not recommended to overdrive the crystal input with an external clock.

**TABLE 5A. AC CHARACTERISTICS,  $V_{CC} = 3.3V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  TO  $85^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{OUT}$	Output Frequency	FREQ_SEL = 0		312.5		MHz
		FREQ_SEL = 1		625		MHz
$f_{jit}(\emptyset)$	RMS Phase Jitter ( Random); NOTE 1	312.5MHz @ Integration Range: 1.875MHz - 20MHz		0.36		ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	100		600	ps
odc	Output Duty Cycle		47		53	%

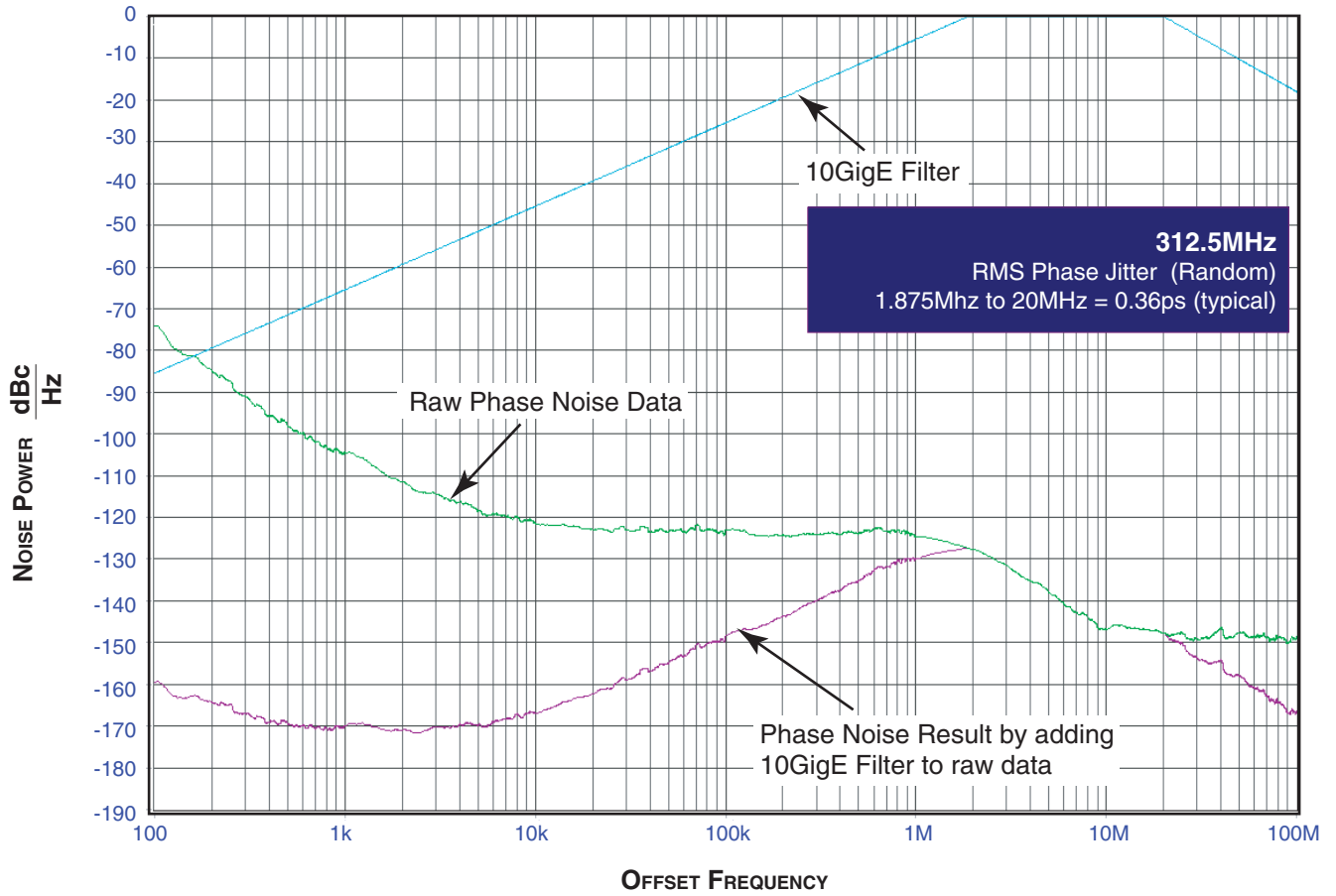
NOTE 1: Refer to the Phase Noise Plots following this section.

**TABLE 5B. AC CHARACTERISTICS,  $V_{CC} = 2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  TO  $85^\circ C$** 

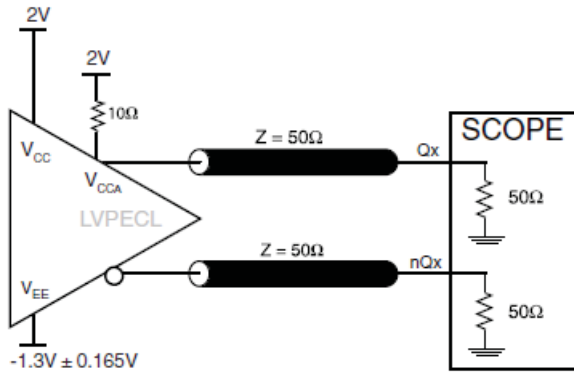
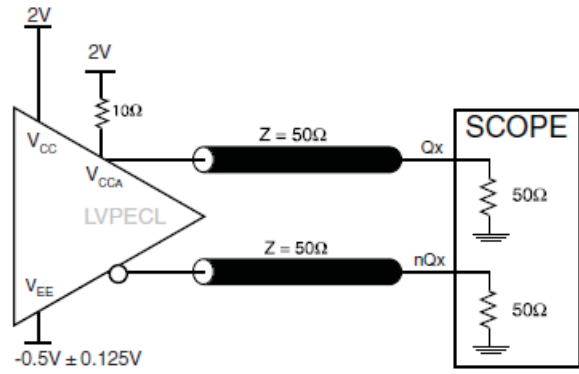
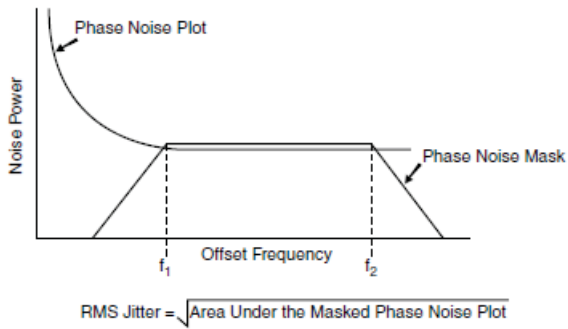
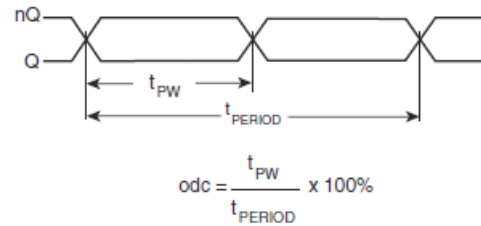
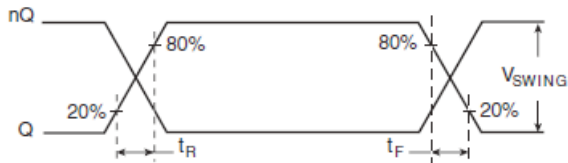
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{OUT}$	Output Frequency	FREQ_SEL = 0		312.5		MHz
		FREQ_SEL = 1		625		MHz
$f_{jit}(\emptyset)$	RMS Phase Jitter ( Random); NOTE 1	312.5MHz @ Integration Range: 1.875MHz - 20MHz		0.38		ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	100		600	ps
odc	Output Duty Cycle		45		55	%

NOTE 1: Refer to the Phase Noise Plots following this section.

TYPICAL PHASE NOISE AT 312.5MHz (3.3V)



## PARAMETER MEASUREMENT INFORMATION


**LVPECL 3.3V OUTPUT LOAD AC TEST CIRCUIT**

**LVPECL 2.5V OUTPUT LOAD AC TEST CIRCUIT**

**RMS PHASE JITTER**

**OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD**

**OUTPUT RISE/FALL TIME**

## APPLICATION INFORMATION

### POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 8432511-12 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL.  $V_{CC}$  and  $V_{CCA}$  should be individually connected to the power supply plane through vias, and  $0.01\mu\text{F}$  bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic  $V_{CC}$  pin and also shows that  $V_{CCA}$  requires that an additional  $10\Omega$  resistor along with a  $10\mu\text{F}$  bypass capacitor be connected to the  $V_{CCA}$  pin.

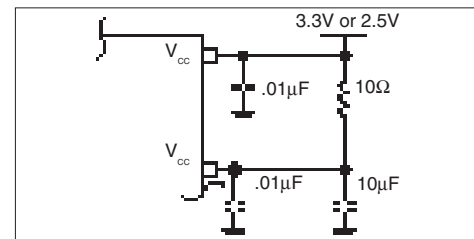


FIGURE 1. POWER SUPPLY FILTERING

### CRYSTAL INPUT INTERFACE

The 8432511-12 has been characterized with  $18\text{pF}$  parallel resonant crystals. The capacitor values,  $C1$  and  $C2$ , shown in *Figure 2* below were determined using a  $25\text{MHz}$ ,  $18\text{pF}$  parallel resonant crystal and

were chosen to minimize the ppm error. The optimum  $C1$  and  $C2$  values can be slightly adjusted for different board layouts.

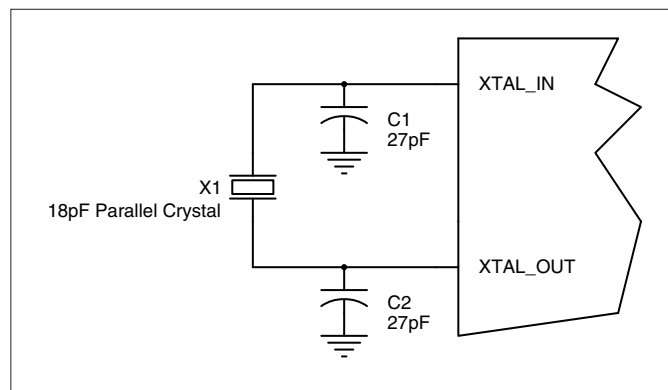


FIGURE 2. CRYSTAL INPUT INTERFACE

### TERMINATION FOR 3.3V LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission

lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

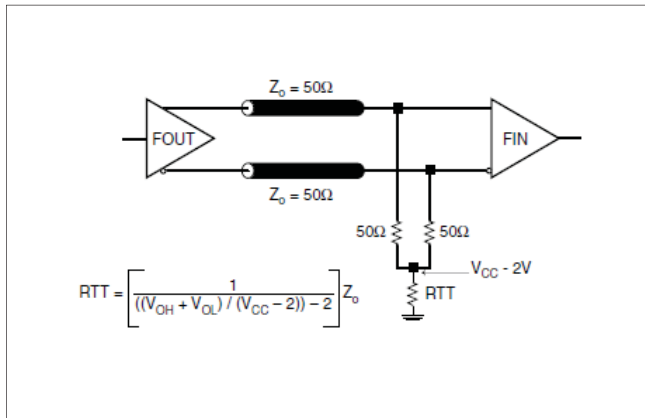


FIGURE 4A. LVPECL OUTPUT TERMINATION

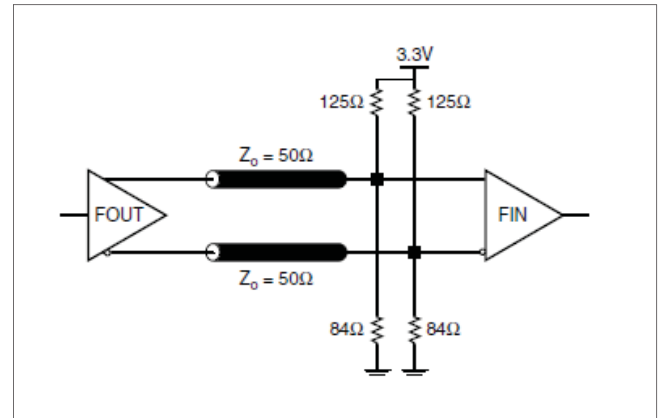


FIGURE 4B. LVPECL OUTPUT TERMINATION



## TERMINATION FOR 2.5V LVPECL OUTPUTS

Figure 5A and Figure 5B show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating  $50\Omega$  to  $V_{cc} - 2V$ . For  $V_{cc} = 2.5V$ , the  $V_{cc} - 2V$  is very close to ground

level. The R3 in Figure 5B can be eliminated and the termination is shown in Figure 5C.

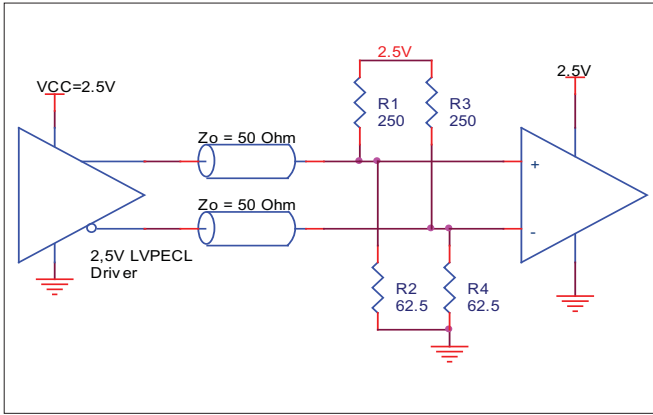


FIGURE 5A. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

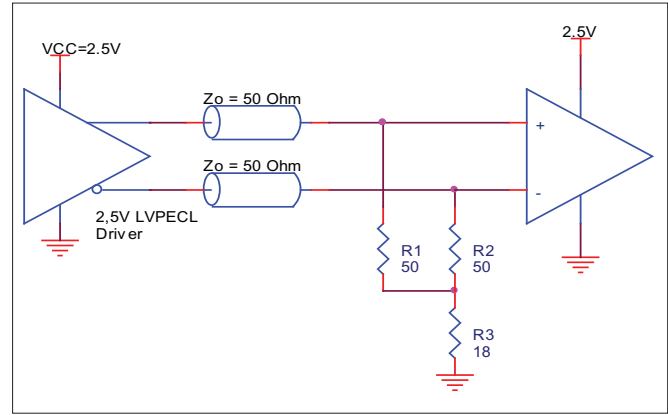


FIGURE 5B. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

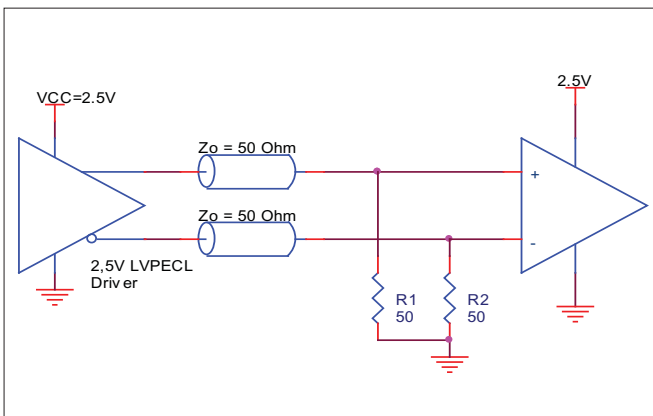


FIGURE 5C. 2.5V LVPECL TERMINATION EXAMPLE

## SCHEMATIC EXAMPLE

Figure 6 shows an example of 8432511-12 application schematic. In this example, the device is operated at  $V_{CC} = 3.3V$ . The 18pF parallel resonant 25MHz crystal is used. The  $C1 = 27pF$  and  $C2 = 27pF$  are recommended for frequency accuracy. For different board layout,

the  $C1$  and  $C2$  may be slightly adjusted for optimizing frequency accuracy. Two examples of LVPECL terminations are shown in this schematic. Additional termination approaches are shown in the LVPECL Termination Application Note.

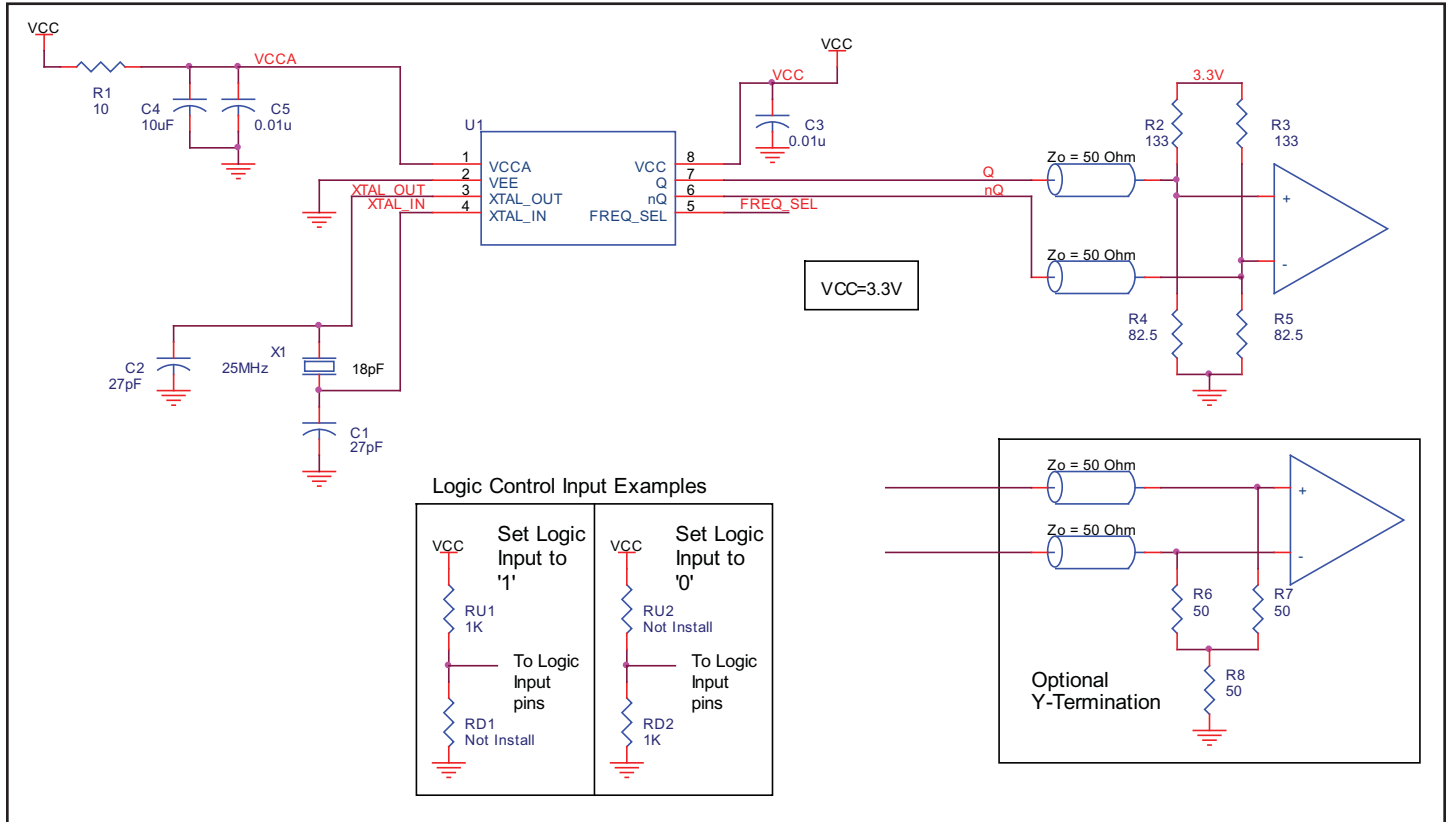


FIGURE 6. 8432511-12 SCHEMATIC EXAMPLE

## POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the 8432511-12. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the 8432511-12 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{CC} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

**NOTE:** Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{CC,MAX} * I_{EE,MAX} = 3.465V * 83mA = 287.60mW$
- Power (outputs)<sub>MAX</sub> = **30mW/Loaded Output pair**

**Total Power**<sub>MAX</sub> (3.465V, with all outputs switching) =  $287.60mW + 30mW = 317.60mW$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd_{total} + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd_{total}$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming a moderate air flow of 1 meter per second and a multi-layer board, the appropriate value is 125.5°C/W per Table 6 below.

Therefore,  $T_j$  for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ C + 0.318W * 125.5^\circ C/W = 124.9^\circ C. \text{ This is below the limit of } 125^\circ C.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (multi-layer).

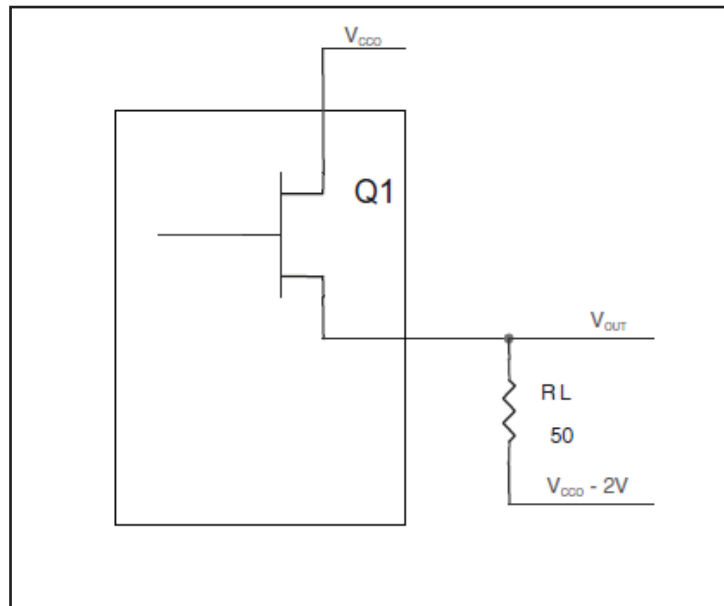
**TABLE 6. THERMAL RESISTANCE  $\theta_{JA}$  FOR 8-PIN TSSOP, FORCED CONVECTION**

$\theta_{JA}$ by Velocity (Meters per Second)			
	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	129.5°C/W	125.5°C/W	123.5°C/W

### 3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 7*.



**FIGURE 7. LVPECL DRIVER CIRCUIT AND TERMINATION**

To calculate worst case power dissipation into the load, use the following equations which assume a  $50\Omega$  load, and a termination voltage of  $V_{CC} - 2V$ .

- For logic high,  $V_{OUT} = V_{OH\_MAX} = V_{CC\_MAX} - 0.9V$

$$(V_{CC\_MAX} - V_{OH\_MAX}) = 0.9V$$

- For logic low,  $V_{OUT} = V_{OL\_MAX} = V_{CC\_MAX} - 1.7V$

$$(V_{CC\_MAX} - V_{OL\_MAX}) = 1.7V$$

$Pd\_H$  is power dissipation when the output drives high.

$Pd\_L$  is the power dissipation when the output drives low.

$$Pd\_H = [(V_{OH\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - 0.9V)/50\Omega] * 0.9V = 19.8mW$$

$$Pd\_L = [(V_{OL\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - 1.7V)/50\Omega] * 1.7V = 10.2mW$$

$$\text{Total Power Dissipation per output pair} = Pd\_H + Pd\_L = 30mW$$

## RELIABILITY INFORMATION

TABLE 7.  $\theta_{JA}$  VS. AIR FLOW TABLE FOR 8 LEAD TSSOP

$\theta_{JA}$ by Velocity (Meters per Second)			
	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	129.5°C/W	125.5°C/W	123.5°C/W

### TRANSISTOR COUNT

The transistor count for 8432511-12 is: 2395

## PACKAGE OUTLINE AND DIMENSIONS

PACKAGE OUTLINE - G SUFFIX FOR 8 LEAD TSSOP

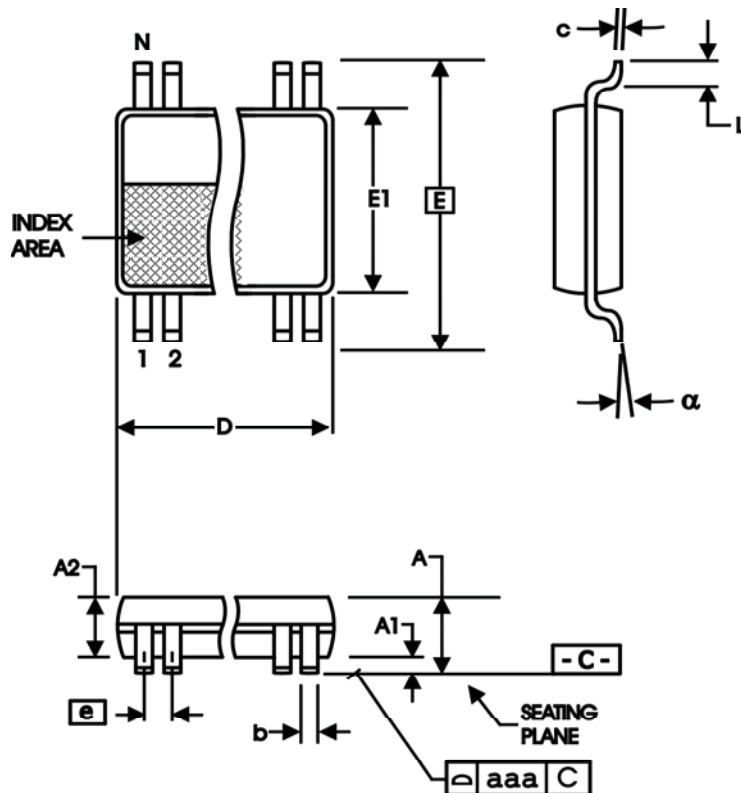


TABLE 8. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	8	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	2.90	3.10
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
$\alpha$	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

**TABLE 9. ORDERING INFORMATION**

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
843251BGI-12LF	BI12L	8 Lead "Lead-Free" TSSOP	tube	-40°C to 85°C
843251BGI-12LFT	BI12L	8 Lead "Lead-Free" TSSOP	tape & reel	-40°C to 85°C

REVISION HISTORY SHEET				
Rev	Table	Page	Description of Change	Date
A	T4	1	Deleted HiPerClockS references.	11/2/12
		4	Crystal Characteristics Table - added note.	
	8	Deleted application note, LVCMOS to XTAL Interface.		
	14	Deleted quantity from tape and reel.		
A	T9	14	Remove ICS from part numbers where needed. Ordering Information - Deleted LF note below the table. Updated data sheet header and footer.	1/19/16



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