IMPACT CONNECTOR ROUTING GUIDE

Impact™ Backplane System
Connector Routing Guide

REVISION:	ECR/ECN INFORMATION:	TITLE:	SHEET No.
C	EC No: **UCP2014-4273** DATE: **2014/04/15**	**IMPACT BACKPLANE SYSTEM CONNECTOR ROUTING GUIDE**	**1** of **12**

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FILENAME: PS74031C.DOC

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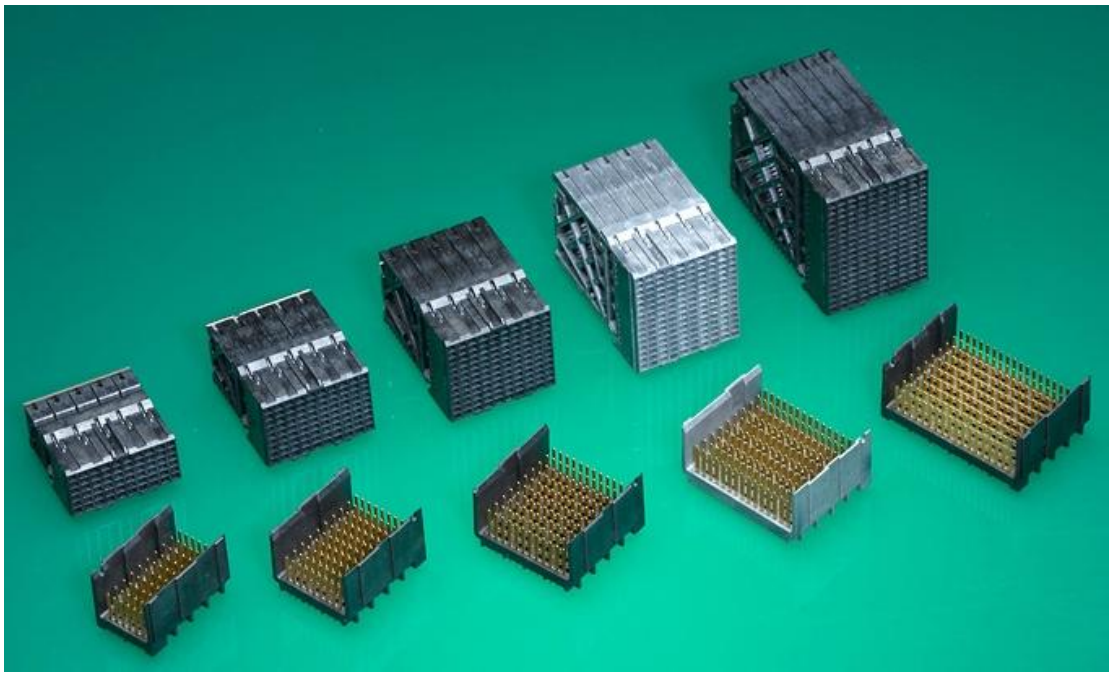
I. OVERVIEW OF THE CONNECTOR

The Impact backplane connector system provides data rates up to 25 Gbps and superior signal density up to 80 differential pairs per inch. The Impact System's broad-edge-coupled technology enables low cross-talk and high signal bandwidth while minimizing channel performance variation across every differential pair within the system.

Molex's Impact System offers multiple compliant-pin design options on both the daughter card and backplane connectors, providing customers ultimate flexibility to optimize their designs for superior mechanical and electrical performance.

The Impact backplane connector system is designed for traditional backplane and/or midplane architectures to meet the growing demands of next-generation telecommunication and data networking equipment manufacturers. The Impact backplane connector system is offered in 2 pair, 3 pair, 4 pair, 5 pair, and 6 pair traditional BP header and DC connector versions, with a complete range of guidance, power, coplanar, mezzanine, and high performance cable solutions.



II. ROUTING STRATEGIES

A) Compliant Pin Via Constructions

The Impact connector system is available in two distinct compliant pin sizes, designed for 0.39mm diameter and 0.46mm diameter plated-thru-holes. The pcb hole pattern is identical between the backplane and daughter card. A simple 1.90 by 1.35mm (.075 by .053") compliant pin grid, as shown in Figure 1, on both backplane and daughter card, reduces PCB routing complexity.

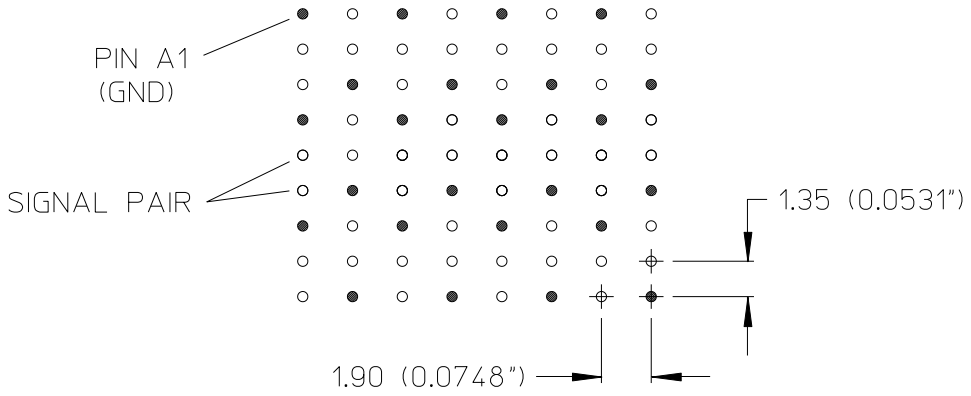


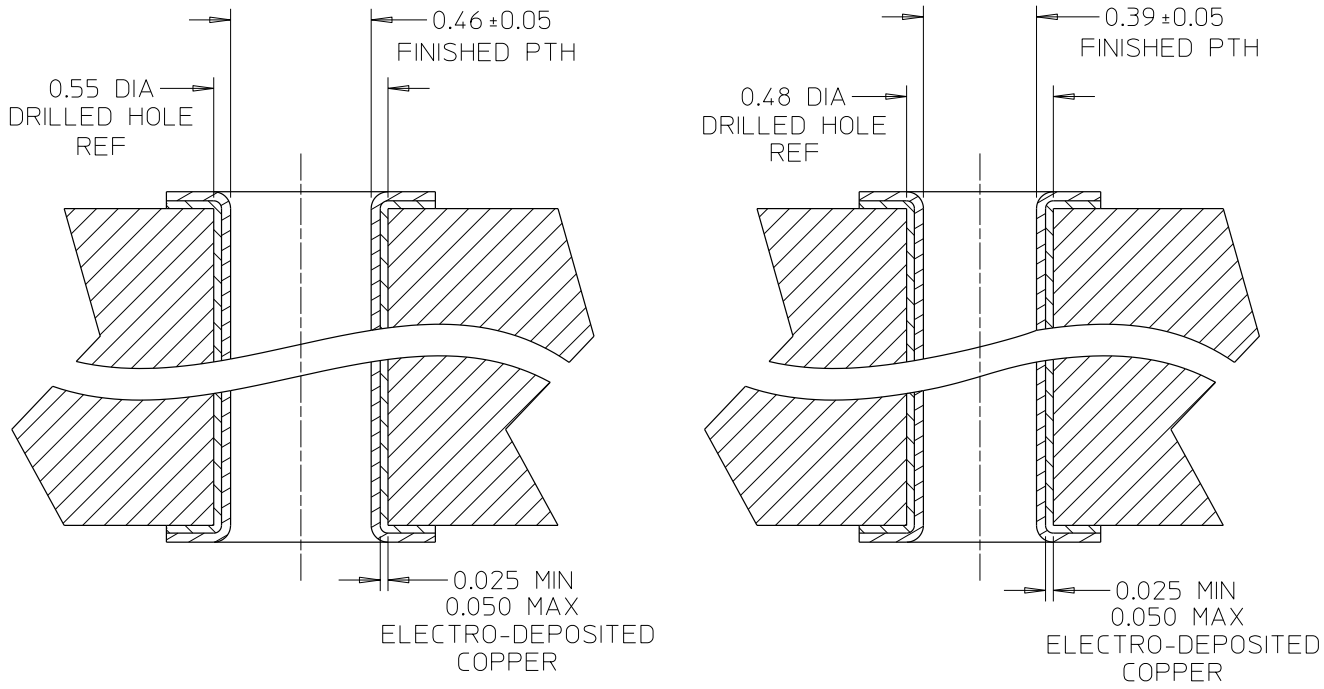
Figure 1
Connector Hole Pattern (BP)

The recommended pad stack for the two hole sizes are contained in Table A. All non-functional pads are to be removed for high speed applications.

FEATURE	0.39mm PTH NOMINAL DIA	0.46mm PTH NOMINAL DIA
Finished hole	0.39mm (15.3 mil)	0.46mm (18 mil)
Drill	0.48mm (18.9 mil)	0.55mm (21.7 mil)
Interior Pad	0.71mm (28 mil)	0.80mm (31.5 mil)
Top Layer Pad	0.80mm (31.5 mil)	0.80mm (31.5mil)
Bottom Layer Pad	0.71mm (28 mil)	0.80mm (31.5 mil)
Anti-pad	See Figure 2 (page 6)	See Figure 2 (page 6)

Table A
Pad Stack Dimensions

Refer to the appropriate Sales Drawing for the recommended PCB thickness.



Notes:

1. The finished PTH size is the critical feature for proper performance of the compliant pin terminal. It is important to maintain a reasonable Cpk to this feature.
2. The reference drill sizes listed are recommended based on Molex's qualification to achieve the finished PTH size. Depending upon the specific manufacturer's plating process, a different drill size can be used to achieve the required finished PTH size.
3. The typical drill hole tolerance is +/-0.013mm.

PLATING VALIDATION

The requirements of finish hole size and copper barrel thickness must be maintained in the via from the board surface (applied connector side) through 1.00 mm depth to guarantee the mechanical performance of the compliant pin (see Figure 2).

Validation of the plated through hole must be achieved through cross-sectioning. Sectioning radially (Figure 4) provides information regarding the drill size, copper barrel thickness, and finish plating barrel thickness. Molex recommends cross-sectioning radially to the depths of 0.15 mm and 1.00 mm to ensure a uniform plated hole meets the requirements provided in this document.

Longitudinal sectioning (Figure 5) will confirm plating uniformity, which must be held to the depths given for proper compliant pin performance. Non-uniformity beyond the 1.00 mm depth requirement will not affect the compliant pin mechanical performance (see Figure 3). Please see the next page for cross section examples.

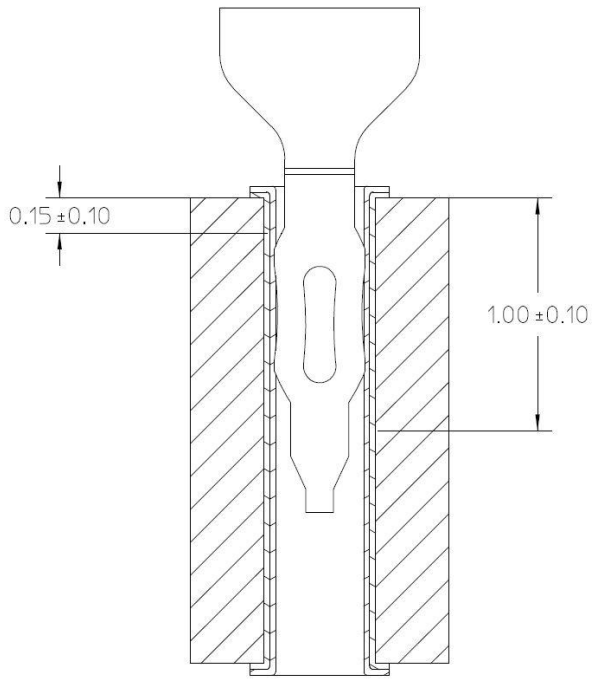


Figure 2. Cross-section depth reference

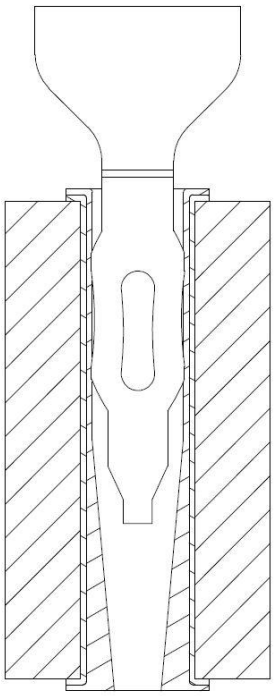


Figure 3. Non-Uniform Plating

CROSS-SECTION EXAMPLES

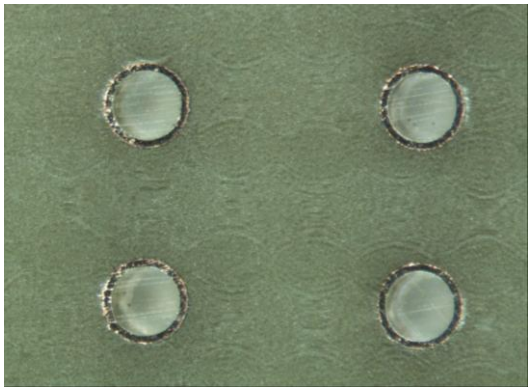


Figure 4. Radial Cross-section of PC Board to validate dimensions.

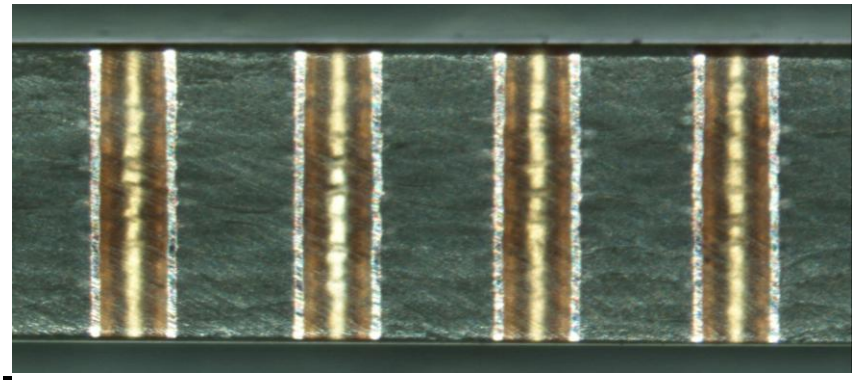


Figure 5. Longitudinal Section verifying plating uniformity of hole.

It is Molex's recommendation that the PCB supplier provide board cross-sections confirming dimensional conformity to the requirements established in this document. A dimensional report and associated IPC compliance requirements should be provided with every lot of board material provided to the customer. The board supplier should target an average finish plated hole size (of 0.39 mm or 0.46 mm) to optimize the performance of the connector at board installation.

B) Transmission Line Configuration

Coupled differential strip lines are the recommended transmission lines for high speed applications. For a specific system differential impedance (i.e., 100 or 85 ohms), different trace width and spacing can be accommodated for any preferred pcb stack up configuration. Designers often consider particular common mode impedance based on factors such as skew, fabrication consistency, and density. Any particular choice of trace width and spacing ultimately affects the routing configuration within the routing channel. In high speed applications, the routing channel is a defined channel between the connector column pins.

C) Anti-pad Size

For most high-speed applications, one needs to maximize the anti-pad width (between columns) and length (between rows). The width of the anti-pad is affected by the following:

1) Trace width and spacing
2) Pair to pair spacing
3) Top and bottom ground strips to trace edge spacing

The length of the anti-pad is limited by the distance and the construction of ground pin vias. The anti-pads shown in Figure 6 are based on a 7 mil trace width and spacing and a 4 mil registration buffer (top and bottom ground strips edge to trace outer edge).

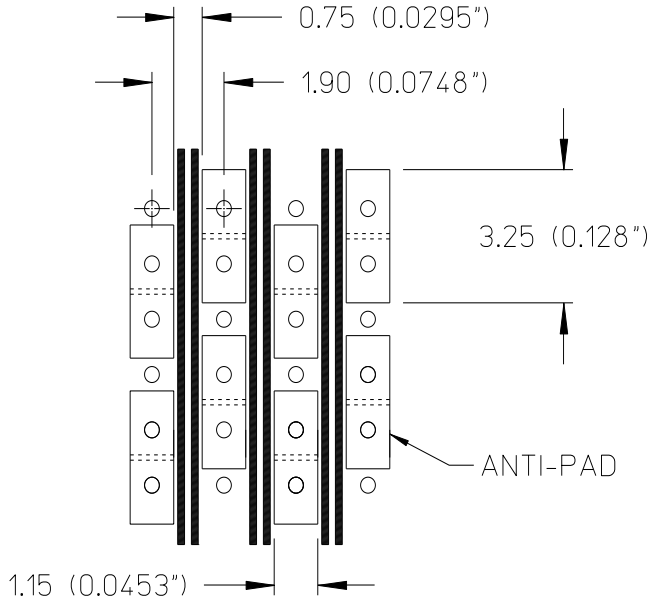


Figure 6
Trace Routing

D) Differential Trace to Signal Pad Attachment

There are several ways to connect the differential traces to their corresponding signal pads. Two possible methods are illustrated in Figures 7 and 8.

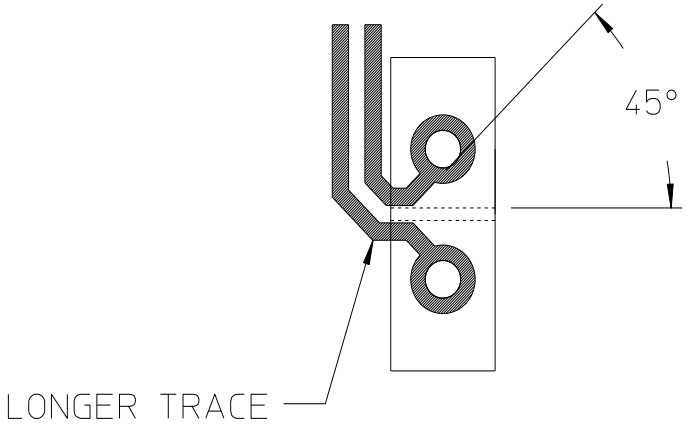


Figure 7
Standard Escape Detail

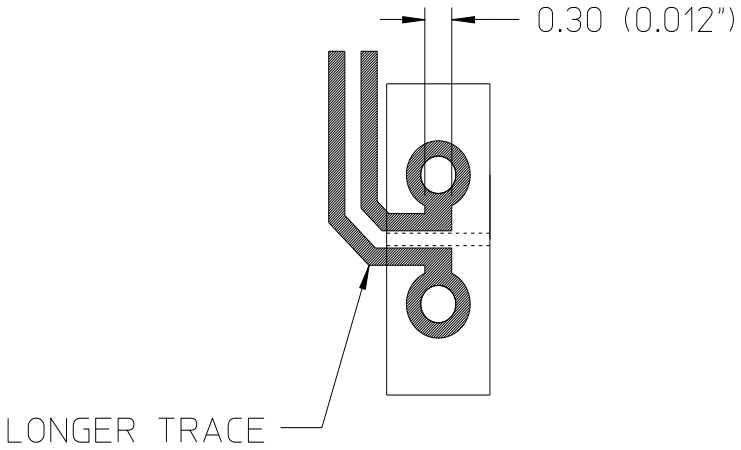


Figure 8
Flag Escape Detail

As seen in Figures 7 and 8, one of the traces has a longer length than the other one. This natural uneven length can be used to reduce the skew within the connector by connecting the longer trace to the shorter conductor within each differential pair of the connector. For high speed applications, it is important to design the trace configuration to compensate for the connector internal skew.

E) Routing Examples

It is recommended to use ground pinning vias to improve the crosstalk performance of the board.
Figure 9 shows the recommended pinning vias and routing example for the Impact 2 Pair backplane connector. Typically, the size of the pinning vias is the same size as the connector vias. Figure 10 shows the recommended pinning vias for the Impact 2 Pair daughtercard.

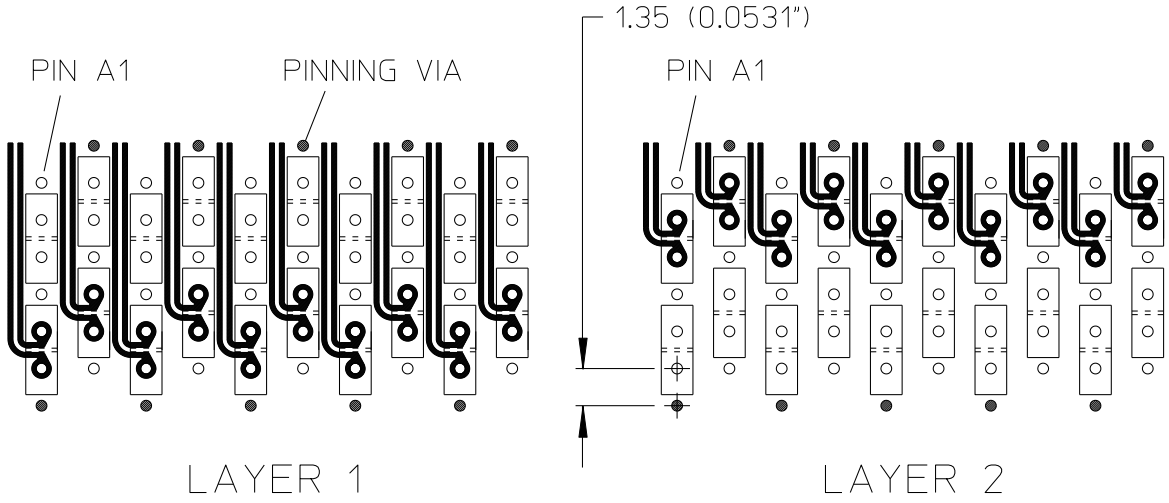


Figure 9
2 Pair x 10 Column BP Routing with recommended pinning vias

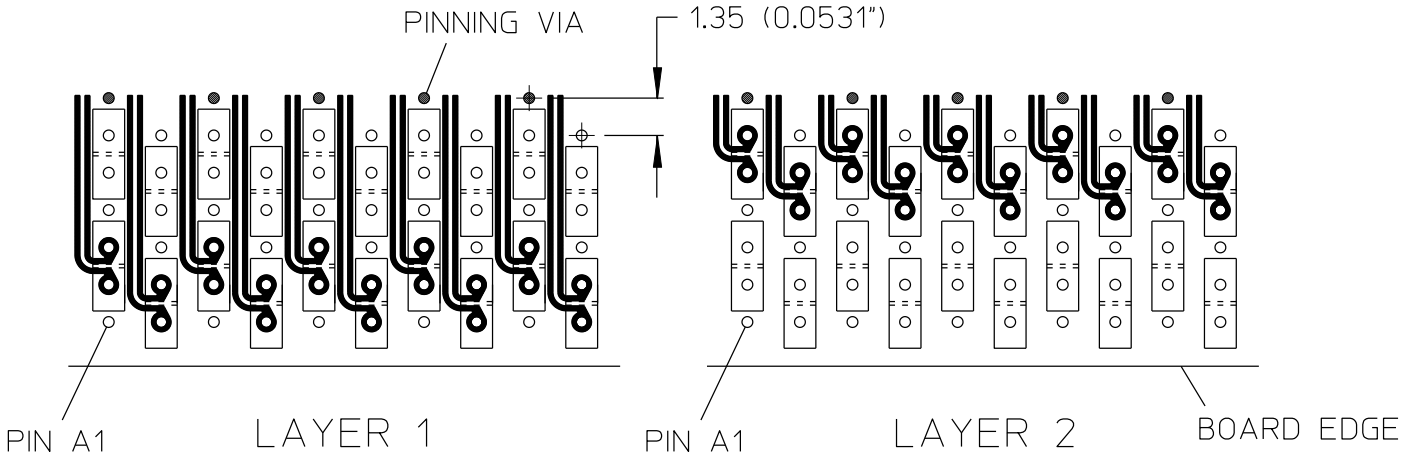


Figure 10
2 Pair x 10 Column DC Routing with recommended pinning vias

III. CROSSTALK

Crosstalk mitigation is a critical element of high speed system design. There are some simple considerations to reduce crosstalk in many systems. These include the following:

1. Separate transmit and receive transmission lines. If transmit and receive transmission lines need to be placed on the same layer, separate them with extra space. It is recommended to place them on separate routing layers.
2. Separate transmit and receive vias. Group the TX and RX differential vias in blocks in rows or columns and, if possible, separate them with slow or DC signal lines.

Tables C and D show two examples of TX and RX grouping.

	1	2	3	4	5	6	7	8	9	10
A	G	TX	G	TX	G	LS	G	RX	G	RX
B	TX	TX	TX	TX	LS	LS	RX	RX	RX	RX
C	TX	G	TX	G	LS	G	RX	G	RX	G
D	G	TX	G	TX	G	LS	G	RX	G	RX
E	TX	TX	TX	TX	LS	LS	RX	RX	RX	RX
F	TX	G	TX	G	LS	G	RX	G	RX	G
G	G	TX	G	TX	G	LS	G	RX	G	RX
H	TX	TX	TX	TX	LS	LS	RX	RX	RX	RX
J	TX	G	TX	G	LS	G	RX	G	RX	G
K	G	TX	G	TX	G	LS	G	RX	G	RX
L	TX	TX	TX	TX	LS	LS	RX	RX	RX	RX
M	TX	G	TX	G	LS	G	RX	G	RX	G

Table C

TX RX grouping separated by low speed (LS) signal columns

	1	2	3	4	5	6	7	8	9	10
A	G	TX	G	TX	G	TX	G	TX	G	TX
B	TX	TX	TX	TX	TX	TX	TX	TX	TX	TX
C	TX	G	TX	G	TX	G	TX	G	TX	G
D	G	TX	G	TX	G	TX	G	TX	G	TX
E	TX	TX	TX	TX	TX	TX	TX	TX	TX	TX
F	TX	G	TX	G	TX	G	TX	G	TX	G
G	G	RX	G	RX	G	RX	G	RX	G	RX
H	RX	RX	RX	RX	RX	RX	RX	RX	RX	RX
J	RX	G	RX	G	RX	G	RX	G	RX	G
K	G	RX	G	RX	G	RX	G	RX	G	RX
L	RX	RX	RX	RX	RX	RX	RX	RX	RX	RX
M	RX	G	RX	G	RX	G	RX	G	RX	G

Table D

TX RX grouping by rows (separated by defined grounds)

IV. BACKDRILLING

For high speed signals, it may be necessary to remove excess via stub below the pcb signal layer. This is accomplished by backdrilling the plated via with a larger diameter drill to remove the undesirable excess via. The Impact compliant pin design allows for backdrilling to within 1mm of the top surface of the PCB.

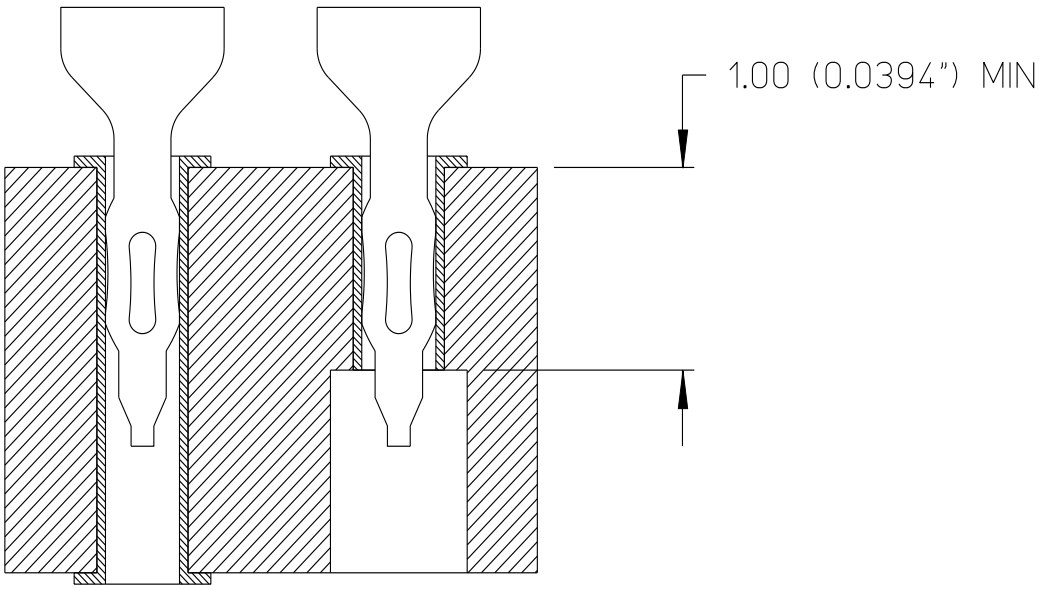


Figure 11
Backdrill Specification