xCORE XA Module Board Hardware Manual

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XMOS

SYNOPSIS

This document pertains to the REV 2 revision of the xCORE XA Module Board.

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1 Overview

IN THIS CHAPTER

- Introduction
- Module Board Layout

1.1 Introduction

This document covers the hardware design of the xCORE XA Module Board.

The Core Board contains a fully pinned out 8-core xCORE-XA Processor, with its GPIOs connected to header connectors to interface with expansion cards, interposer boards and other external hardware. The Module Board also contains on board debugger hardware for interfacing with the xCORE and ARM processors on the xCORE XA device.

1.2 Module Board Layout

The diagram below shows an overview of the layout of the xCORE-XA Module Board.

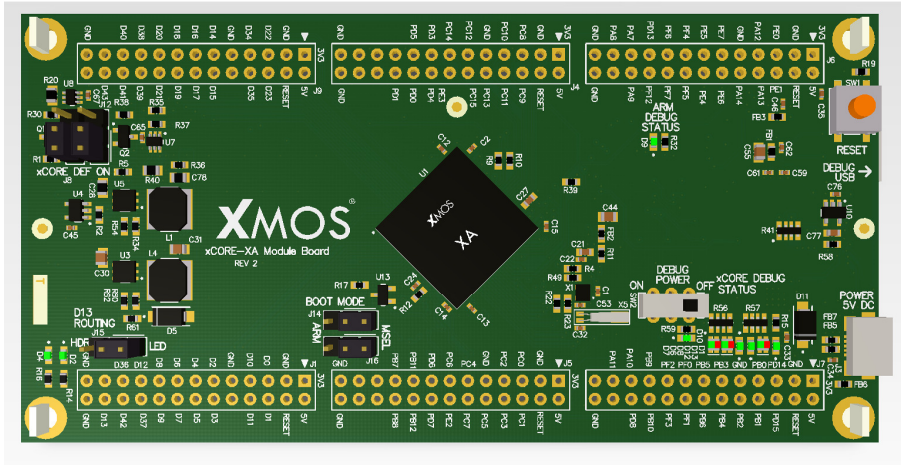

Figure 1: Module Board diagram

2 Module Board

IN THIS CHAPTER

- Setup
- Power Supply
- Debug
- xCORE-XA Boot
- XMOS Links
- Reset
- Clocking
- I/O
- LEDs
- ARM Peripherals

The Module Board contains the XMOS device plus support and debug circuitry.

A single XS1-XA8A-10-FB265 device has its GPIO connected to the headers.

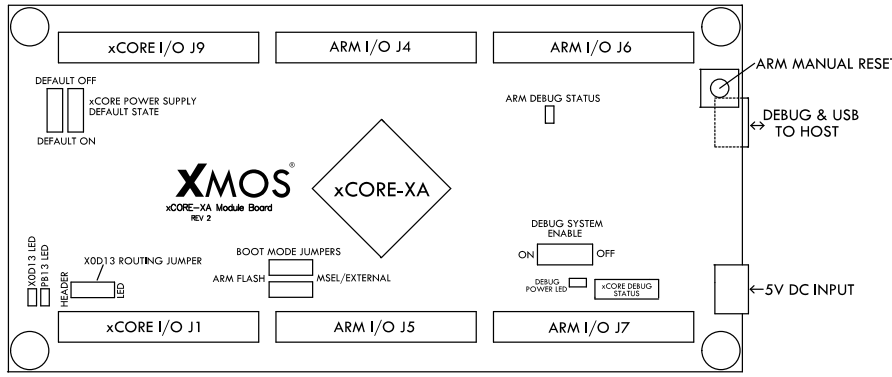

Figure 2: xCORE-XA Module Board

2.1 Setup

The Module Board is powered by a 5V external power supply.

For debugging, an on board XTAG device is available for debugging the xCOREs and a JLINK-OB device is available for debugging the ARM core.

2.1.1 Default Jumper Settings

- Power up : Jumpers J8 and J12 should be connected to “xCORE DEF ON” to have the xCORE power default to on.
- Boot mode: Jumpers J14 and J16 should be connected to “MSEL” for initial xCORE debugging.
- D13 Routing: There is another jumper J15 that selects on board LED or GPIO (X0D13) in one of the I/O header. It should be connected in “LED” position.

2.2 Power Supply

Power input can be fed either via a USB micro B connector (J3), or to pin 2 any of the I/O headers. The 5V input supply is used to generate the 3.3V and 1.0V supplies required by the xCORE-XA device.

The 5V and 3.3V supplies are connected to the I/O headers, and can be supplied to or by the Module Board. The on board 3.3V supply is capable of supplying 1.25A to external circuits connected to the I/O headers, as long as a suitable 5V adapter is used to provide the system power.

2.2.1 xCORE Power Control

The xCORE power is controlled by two jumpers(J8,J9). The jumpers selects xCORE power default to on (XCORE DEF ON) or off. It is also controlled by ARM via GPIO’s PD2 and PD10 to powering it down during low energy mode applications.

2.2.2 Power Supply Monitoring

The xCORE-XA power supply can be monitored via low power mode and sleep mode etc. Four ADC signals including two shunt signals with 100:1 gain are used for power monitoring.

2.3 Debug

Debug of the system is via the micro USB connector J2, on the bottom side of the Module Board. This should be connected to a host computer for debugging and programming.

2.3.1 Debug LEDs

The LEDs indicate the status of the device as shown in the below table.

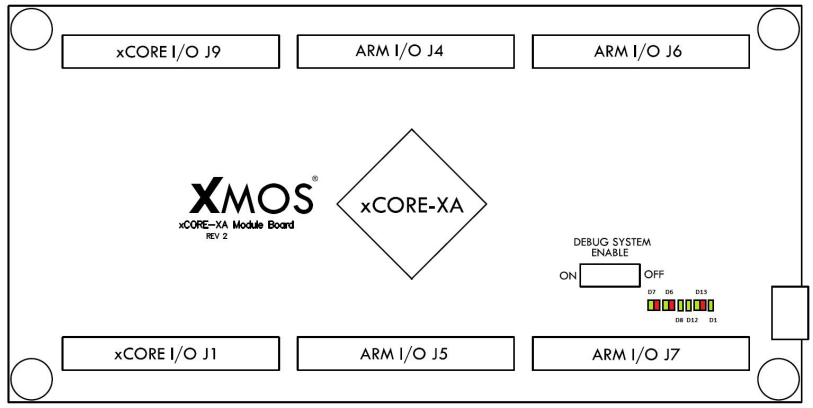

Figure 3: Debug LEDs

LED	Status	Description
D1	Green	The xTAG is powered on
D7	Green	Target is running
	Red	Target is in debug mode and stopped
D13	Green	Target stop reason is expected e.g. breakpoint,print message
	Red	Target stop reason is unexpected e.g.exception
D12	Green	There is JTAG activity with the target happening
	Off	No JTAG
D8	Green Flashing	xSCOPE is enabled
	Off	No xSCOPE
D6	Green	Target device is detected after a Run Configuration or Debug Configuration is used (xrun or xgdb command)
	Red	Target device is not detected after a Run Configuration or Debug Configuration is used (xrun or xgdb command)

2.3.2 Debug System Disable

The debug system could be powered down(OFF) or enabled (ON) by setting the jumper J13. This allows the board in a standalone mode with typical power usage.

2.4 xCORE-XA Boot

The boot mode jumpers J14 & J16 can be selected to boot from ARM flash using LINKS or through external Flash or from xTAG(MSEL). This allows to develop xCORE code independent of ARM code and experiment with xCORE.

2.5 XMOS Links

This board contains two 5-bit xCONNECT links XLA and XLB which can be used for connecting more xCORES together. The 2-bit xCONNECT link XLC is used for xSCOPE.

2.6 Reset

The reset can be applied to the board in two ways. Manual reset can be generated using push button SW1. In debug mode the reset from xTAG resets the whole system. The reset is connected to all I/O headers so any circuitry on them can be reset.

2.7 Clocking

There are two clock sources available in the board. One provides a 48MHZ system clock to both ARM and xCORE. The other is a 32.768 KHZ clock connected to ARM to allow low energy mode applications.

2.8 I/O

2.8.1 xCORE Headers

The xCORE signals are identified on the silkscreen layer of the Module Board, the table below lists their relationship to the internal ports.

J1 Pin	Designator	Function					
1	3V3	Power supply 3.3V in/out					
2	5V	Power supply 5.0V in/out					
3	GND	Power supply ground					
4	RESET	xCORE reset signal (active low)					
5	D0	X0D00	P1A0				
6	D1	X0D01	P1B0				
7	D10	X0D10	P1C0				
8	D11	X0D11	P1D0				
9	GND	Power supply ground					
10		Not Connected					
11	D2	X0D02		P4A0	P8A0	P16A0	P32A20
12	D3	X0D03		P4A1	P8A1	P16A1	P32A21
13	D4	X0D04		P4B0	P8A2	P16A2	P32A22
14	D5	X0D05		P4B1	P8A3	P16A3	P32A23
15	D6	X0D06		P4B2	P8A4	P16A4	P32A24
16	D7	X0D07		P4B3	P8A5	P16A5	P32A25
17	D8	X0D08		P4A2	P8A6	P16A6	P32A26
18	D9	X0D09		P4A3	P8A7	P16A7	P32A27
19	D12	X0D12	P1E0				
20	D37	X0D37	P1N0		P8D1	P16B9	
21	D36	X0D36	P1M0		P8D0	P16B8	
22	D42	X0D42			P8D6	P16B14	
23		Not Connected					
24	D13	X0D13	P1F0				
25	GND	Power supply ground					
26	GND	Power supply ground					

J9 Pin	Designator	Function					
1	3V3	Power supply 3.3V in/out					
2	5V	Power supply 5.0V in/out					
3	GND	Power supply ground					
4	RESET	xCORE reset signal (active low)					
5	D22	X0D22	P1G0				
6	D23	X0D23	P1H0				
7	D34	X0D34	P1K0				
8	D35	X0D35	P1L0				
9	GND	Power supply ground					
10		Not Connected					
11	D14	X0D14		P4C0	P8B0	P16A8	P32A28
12	D15	X0D15		P4C1	P8B1	P16A9	P32A29
13	D16	X0D16		P4D0	P8B2	P16A10	
14	D17	X0D17		P4D1	P8B3	P16A11	
15	D18	X0D18		P4D2	P8B4	P16A12	
16	D19	X0D19		P4D3	P8B5	P16A13	
17	D20	X0D20		P4C2	P8B6	P16A14	P32A30
18	D21	X0D21		P4C3	P8B7	P16A15	P32A31
19	D38	X0D38	P1O0		P8D2	P16B10	
20	D39	X0D39	P1P0		P8D3	P16B11	
21	D40	X0D40			P8D4	P16B12	
22	D41	X0D41			P8D5	P16B13	
23		Not Connected					
24	D43	X0D43			P8D7	P16B15	
25	GND	Power supply ground					
26	GND	Power supply ground					

2.8.2 ARM Headers

The ARM signals are identified on the silkscreen layer of the Module Board. All of the signals can be used as GPIO as well as being multiplexed to the internal peripherals, the table below lists their relationship to the peripherals.

J6 Pin	Designator	Function
1	3V3	Power supply 3.3V in/out
2	5V	Power supply 5.0V in/out
3	GND	Power supply ground
4	RESET	ARM reset signal (active low)
5	PE0	PCNT0 S0IN UART0 TX I2C1 SDA
6	PE1	PCNT0 S1IN UART0 RX I2C1 SCL
7	PA12	TIMER2 CC0
8	PA13	TIMER2 CC1
9	GND	Power supply ground
10	PA14	TIMER2 CC2
11	PE7	USART0 TX
12	PE6	USART0 RX
13	PE5	USART0 CLK
14	PE4	USART0 CS
15	PF4	GPIO
16	PF5	GPIO
17	PF6	GPIO
18	PF7	GPIO
19	PD13	GPIO
20	PF12	GPIO
21	PA7	GPIO
22	PA9	GPIO
23	PA8	GPIO
24		Not Connected
25	GND	Power supply ground
26	GND	Power supply ground

J4 Pin	Designator	Function		
1	3V3	Power supply 3.3V in/out		
2	5V	Power supply 5.0V in/out		
3	GND	Power supply ground		
4	RESET	ARM reset signal (active low)		
5	PC8	ACMP1 CH0		
6	PC9	ACMP1 CH1		
7	PC10	ACMP1 CH2		
8	PC11	ACMP1 CH3		
9	GND	Power supply ground		
10	PC13	ACMP1 CH5	OPAMP1 OUTALT1	
11	PC12	ACMP1 CH4	OPAMP1 OUTALT0	
12	PC15	ACMP1 CH7	OPAMP1 OUTALT3	
13	PC14	ACMP1 CH6	OPAMP1 OUTALT2	
14	PE3	ACMP1 OUT		
15	PD3	ADC0 CH3	OPAMP2 N2	
16	PD4	ADC0 CH4	OPAMP2 P2	
17	PD5	ADC0 CH5	OPAMP2 OUT0	
18	PD0	ADC0 CH0	OPAMP2 OUT1	OPAMP0 OUTALT4
19		Not Connected		
20	PD1	ADC0 CH1	OPAMP1 OUTALT4	
21		Not Connected		
22		Not Connected		
23		Not Connected		
24		Not Connected		
25	GND	Power supply ground		
26	GND	Power supply ground		

J7 Pin	Designator	Function
1	3V3	Power supply 3.3V in/out
2	5V	Power supply 5.0V in/out
3	GND	Power supply ground
4	RESET	ARM reset signal (active low)
5	PD14	I2C0 SDA
6	PD15	I2C0 SCL
7	PB0	TIMER1 CC0
8	PB1	TIMER1 CC1
9	GND	Power supply ground
10	PB2	TIMER1 CC2
11	PB3	USART2 TX
12	PB4	USART2 RX
13	PB5	USART2 CLK
14	PB6	USART2 CS
15	PF0	GPIO
16	PF1	GPIO
17	PF2	GPIO
18	PF3	GPIO
19	PB9	UART1 TX
20	PB10	UART1 RX
21	PA10	GPIO
22	PD8	CMU CLK1
23	PA11	GPIO
24		Not Connected
25	GND	Power supply ground
26	GND	Power supply ground

J5 Pin	Designator	Function		
1	3V3	Power supply 3.3V in/out		
2	5V	Power supply 5.0V in/out		
3	GND	Power supply ground		
4	RESET	ARM reset signal (active low)		
5	PC0	ACMP0 CH0	OPAMP0 OUTALT0	USART1 TX
6	PC1	ACMP0 CH1	OPAMP0 OUTALT1	USART1 RX
7	PC2	ACMP0 CH2	OPAMP0 OUTALT2	
8	PC3	ACMP0 CH3	OPAMP0 OUTALT3	
9	GND	Power supply ground		
10	PC5	ACMP0 CH5	OPAMP0 N0	
11	PC4	ACMP0 CH4	OPAMP0 P0	
12	PC7	ACMP0 CH7		
13	PC6	ACMP0 CH6		
14	PE2	ACMP0 OUT		
15	PD6	ADC0 CH6	OPAMP1 P1	
16	PD7	ADC0 CH7	OPAMP1 N1	
17	PB11	OPAMP0 OUT0		
18	PB12	OPAMP0 OUT1		
19	PB7	USART1 CLK	LFXO P	
20	PB8	USART1 CS	LFXO N	
21		Not Connected		
22		Not Connected		
23		Not Connected		
24		Not Connected		
25	GND	Power supply ground		
26	GND	Power supply ground		

2.9 LEDs

Access to two gpio leds. D2 is connected to PB13 and D4 is connected X0D13. Jumper J15 should be connected to “LED” position to access D4.

2.10 ARM Peripherals

xCORE-XA ARM includes dedicated low energy peripherals,low energy sensor interfaces and a full speed USB. ARM I/O header includes peripherals like I2C,UART,USART,PWM and ADC. The I/O from the ARM core in the xCORE-XA is bought out to four headers. The I/O is laid out to give two pairs of similar layout (J6 & J4, J7 & J5) one containing GPIO linked to analogue I/O and the other containing GPIOs linked to digital peripherals.

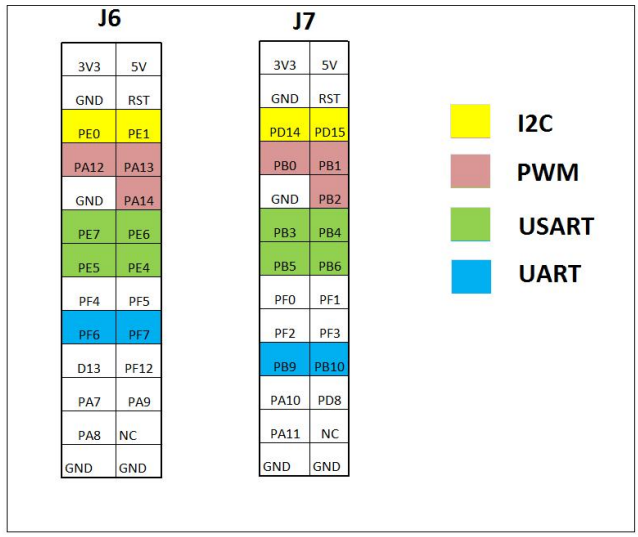

Figure 4: ARM I/O Header with peripheral locations

3 Add On Board Design

The module board can be plug down into a application specific larger motherboard, or have smaller daughter boards plugged into it from above.

Each set of I/O headers includes power, ground and reset for maximum flexibility. Flexible power supply options allow this board to be powered from a microUSB supply, supplying the add on board, or from the add on board, via the headers.

This board plugs into top of the xCORE-XA industrial board. Custom daughter cards, such as the xCORE-XA vision module and click board interposer can be attached this board.

4 New Designs Based on Module Board

IN THIS CHAPTER

- Power Supply
- Debug
- I/O

There are a number of sections of the design of the xCORE-XA Module Board that have been optimized for flexibility to cover as many use cases as possible. Therefore some consideration may be required in what to leave out or change in a custom design. Some of the important points to consider are dealt with in this section.

Some general points to consider when implementing your own design are:

- Always check the datasheet of the xCORE device. In the case where the reference design and datasheet conflict, the datasheet presides.
- XMOS datasheets contain additional hardware design requirements and guidelines that are not covered in this document, which users of XMOS hardware reference designs must ensure are followed.
- The presence of a third party device in an XMOS hardware reference design does not make any statement about its general availability. You must make your own arrangements to ensure that all components can be sourced in the required volumes.

4.1 Power Supply

For custom designs the minimum power supply requirements for the xCORE-XA device should be met. A 1.0V supply, capable of supplying at least 500mA is required for the xCORE-XA core, and a 3.3V supply, capable of supplying at least 100mA is required for the xCORE-XA I/O and ARM core supply. The required capability of the 3.3V supply will vary depending on the I/O usage and may need to be higher to supply peripheral devices. The 1.0V, 3.3V supplies and reset should all be sequenced in accordance with the requirements stated in the datasheet.

4.2 Debug

In a custom design debug and programming interfaces for both the xCORE cores and the ARM core will be required. A standard XSYS connection should be added to debug and program the xCORE cores by way of an XTAG debug adapter. A standard SWD interface should be implemented, for connection to an external debug adapter.

4.3 I/O

Attention should be paid to the I/O planning for both the xCORE and ARM cores. The peripherals provided by the ARM core can be multiplexed to a variety of different pin groups, care should be taken to ensure there is no overlap. the xCORE I/O should be mapped, with care taken to ensure that port types are used appropriately, and that bi-directional usage for wide ports is avoided.

5 Errata