MLX72013

433MHz
FSK/ASK Transmitter

1. Features

- Drop-in replacement of TH72011 with reduced phase noise
- Frequency range from 425 MHz to 445 MHz
- Fully integrated PLL-stabilized VCO
- Single-ended RF output
- FSK via crystal pulling
- Wideband FSK deviation possible
- ASK/OOK via power amplifier modulation
- Wide power supply range from 1.95 V to 5.5 V
- Very low standby current
- Low voltage detector
- High over-all frequency accuracy
- FSK deviation and center frequency independently adjustable
- Data rates from DC to 40 kbps
- Adjustable output power range from -10 dBm to +12 dBm
- Adjustable current consumption from 2.9 mA to 16.8 mA
- Conforms to EN 300 220 and similar standards
- 8-pin Small Outline Integrated Circuit (SOIC)

2. Ordering Code

Product Code	Temperature Code	Package Code	Option Code	Packing Form Code
MLX72013	K	DC	AAA-000	RE
MLX72013	K	DC	AAA-000	TU

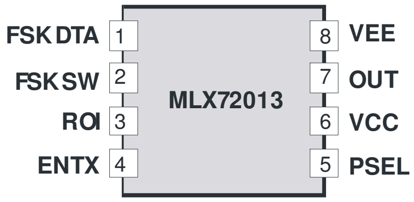
Legend:
Temperature Code: K for Temperature Range -40°C to 125°C
Package Code: DC for SOIC150Mil
Packing Form: RE for Reel, TU for Tube

Ordering example: MLX72013KDC-AAA-000-RE

3. Application Examples

- RF remote controls
- Automatic meter reading (AMR)
- Tire pressure monitoring systems (TPMS)
- Remote keyless entry (RKE)
- Alarm and security systems
- Garage door openers
- Home automation

4. Pin Description



5. General Description

The MLX72013 transmitter IC is designed for applications in the European 433 MHz industrial-scientific-medical (ISM) band, according to the EN 300 220 telecommunications standard; but it can also be used in any other country with similar frequency bands.
The transmitter's carrier frequency f_c is determined by the frequency of the reference crystal f_{ref}. The integrated PLL synthesizer ensures that each RF value, ranging from 425 MHz to 445 MHz, can be achieved by using a crystal with a reference frequency according to: $f_{ref} = f_c/N$, where N = 16 is the PLL feedback divider ratio.

6. Theory of Operation

6.1 General

As depicted in Fig.1, the MLX72013 transmitter consists of a fully integrated voltage-controlled oscillator (VCO), a divide-by-16 divider (div16), a phase-frequency detector (PFD) and a charge pump (CP). An internal loop filter determines the dynamic behavior of the PLL and suppresses reference spurious signals. A Colpitts crystal oscillator (XOSC) is used as the reference oscillator of a phase-locked loop (PLL) synthesizer. The VCO's output signal feeds the power amplifier (PA). The RF signal power P_{out} can be adjusted in four steps from P_{out} = –14 dBm to +11 dBm, either by changing the value of resistor RPS or by varying the voltage V_{PS} at pin PSEL. The open-collector output (OUT) can be used either to directly drive a loop antenna or to be matched to a 50Ohm load. Bandgap biasing ensures stable operation of the IC at a power supply range of 1.95 V to 5.5 V.

6.2 Block Diagram

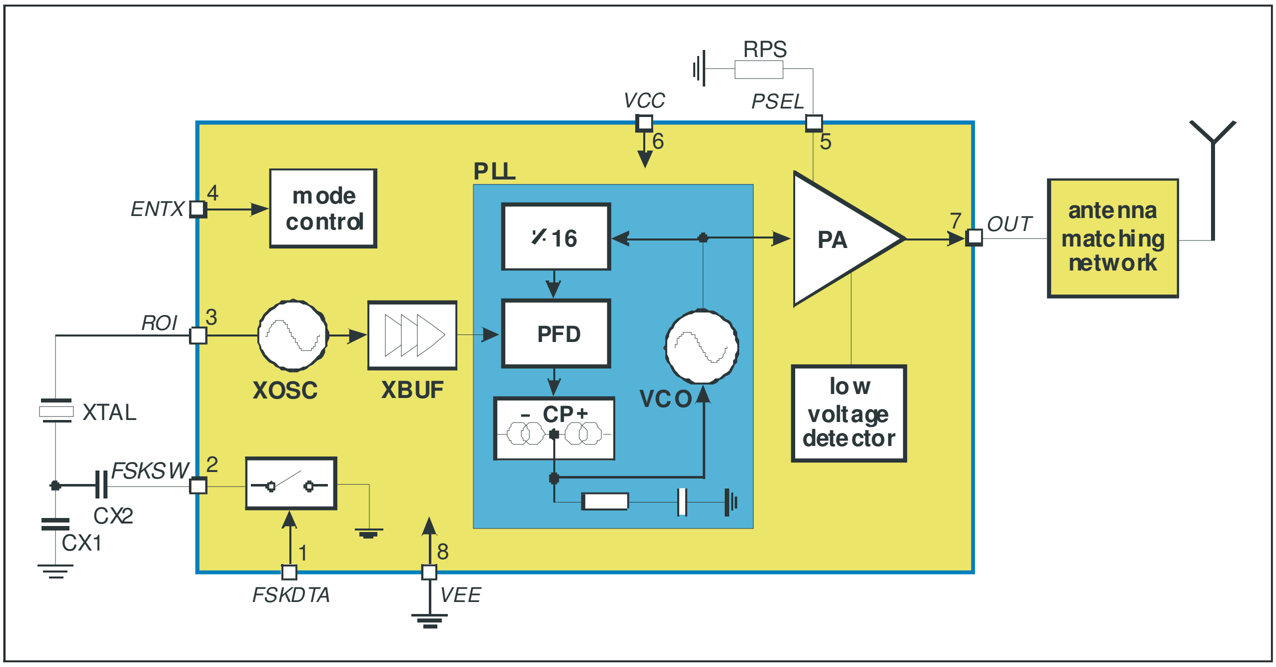


Fig. 1: Block diagram with external components

7. Functional Description

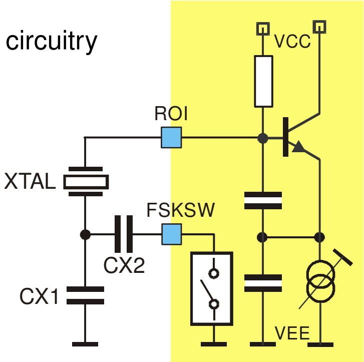
7.1 Crystal Oscillator

A Colpitts crystal oscillator with integrated functional capacitors is used as the reference oscillator for the PLL synthesizer. The equivalent input capacitance CRO offered by the crystal oscillator input pin ROI is about 18pF. The crystal oscillator is provided with an amplitude control loop in order to have a very stable frequency over the specified supply voltage and temperature range in combination with a short start-up time.

7.2 FSK Modulation

FSK modulation can be achieved by pulling the crystal oscillator frequency. A CMOS-compatible data stream applied at the pin FSKDTA digitally modulates the XOSC via an integrated NMOS switch. Two external pulling capacitors CX1 and CX2 allow the FSK deviation Δf and the center frequency f_c to be adjusted independently. At FSKDTA = 0, CX2 is connected in parallel to CX1 leading to the low-frequency component of the FSK spectrum (f_{min}); while at FSKDTA = 1, CX2 is deactivated and the XOSC is set to its high frequency f_{max}.
An external reference signal can be directly AC-coupled to the reference oscillator input pin ROI. Then the transmitter is used without a crystal. Now the reference signal sets the carrier frequency and may also contain the FSK (or FM) modulation.

Fig. 2: Crystal pulling circuitry



FSKDTA	Description
0	$f_{min} = f_c - \Delta f$ (FSK switch is closed)
1	$f_{max} = f_c + \Delta f$ (FSK switch is open)

7.3 Crystal Pulling

A crystal is tuned by the manufacturer to the required oscillation frequency f_0 at a given load capacitance CL and within the specified calibration tolerance. The only way to pull the oscillation frequency is to vary the effective load capacitance CL_{eff} seen by the crystal.
Figure 3 shows the oscillation frequency of a crystal as a function of the effective load capacitance. This capacitance changes in accordance with the logic level of FSKDTA around the specified load capacitance. The figure illustrates the relationship between the external pulling capacitors and the frequency deviation.
It can also be seen that the pulling sensitivity increases with the reduction of CL. Therefore, applications with a high frequency deviation require a low load capacitance. For narrow band FSK applications, a higher load capacitance could be chosen in order to reduce the frequency drift caused by the tolerances of the chip and the external pulling capacitors.

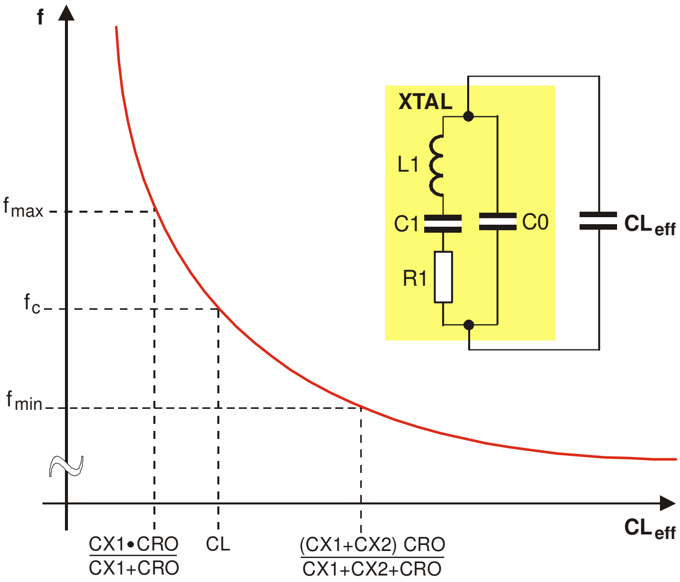


Fig. 3: Crystal pulling characteristic

7.4 ASK Modulation

The MLX72013 can be ASK-modulated by applying data directly at pin PSEL. This turns the PA on and off and therefore leads to an ASK signal at the output.

7.5 Output Power Selection

The transmitter is provided with an output power selection feature. There are four predefined output power steps and one off-step accessible via the power selection pin PSEL. A digital power step adjustment was chosen because of its high accuracy and stability. The number of steps and the step sizes as well as the corresponding power levels are selected to cover a wide spectrum of different applications.

The implementation of the output power control logic is shown in figure 4. There are two matched current sources with an amount of about 8 µA. One current source is directly applied to the PSEL pin. The other current source is used for the generation of reference voltages with a resistor ladder. These reference voltages are defining the thresholds between the power steps. The four comparators deliver thermometer-coded control signals depending on the voltage level at the pin PSEL. In order to have a certain amount of ripple tolerance in a noisy environment the comparators are provided with a little hysteresis of about 20 mV. With these control signals, weighted current sources of the power amplifier are switched on or off to set the desired output power level (Digitally Controlled Current Source). The LOCK signal and the output of the low voltage detector are gating this current source.

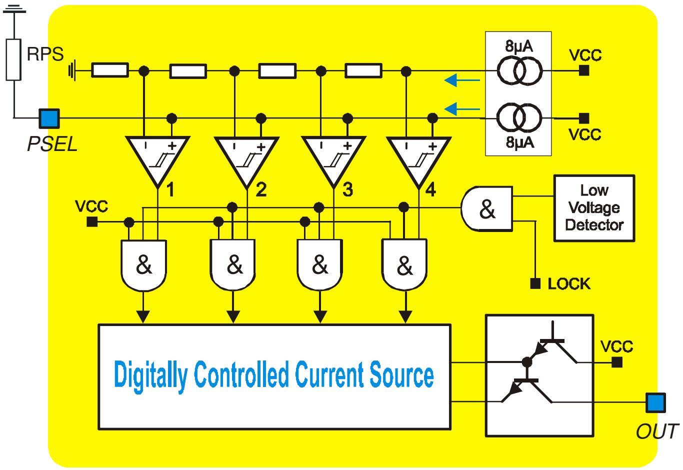


Fig. 4: Block diagram of output power control circuitry

There are two ways to select the desired output power step. First by applying a DC voltage at the pin PSEL, then this voltage directly selects the desired output power step. This kind of power selection can be used if the transmission power must be changed during operation. For a fixed-power application a resistor can be used which is connected from the PSEL pin to ground. The voltage drop across this resistor selects the desired output power level. For fixed-power applications at the highest power step this resistor can be omitted. The pin PSEL is in a high impedance state during the “TX standby” mode.

7.6 Lock Detection

The lock detection circuitry turns on the power amplifier only after PLL lock. This prevents from unwanted emission of the transmitter if the PLL is unlocked.

7.7 Low Voltage Detection

The supply voltage is sensed by a low voltage detect circuitry. The power amplifier is turned off if the supply voltage drops below a value of about 1.85 V. This is done in order to prevent unwanted emission of the transmitter if the supply voltage is too low.

7.8 Mode Control Logic

The mode control logic allows two different modes of operation as listed in the following table. The mode control pin ENTX is pulled-down internally. This guarantees that the whole circuit is shut down if this pin is left floating.

ENTX	Mode	Description
0	TX standby	TX disabled
1	TX active	TX enable

7.9 Timing Diagrams

After enabling the transmitter by the ENTX signal, the power amplifier remains inactive for the time t_{on}, the transmitter start-up time. The crystal oscillator starts oscillation and the PLL locks to the desired output frequency within the time duration t_{on}. After successful PLL lock, the LOCK signal turns on the power amplifier, and then the RF carrier can be FSK or ASK modulated.

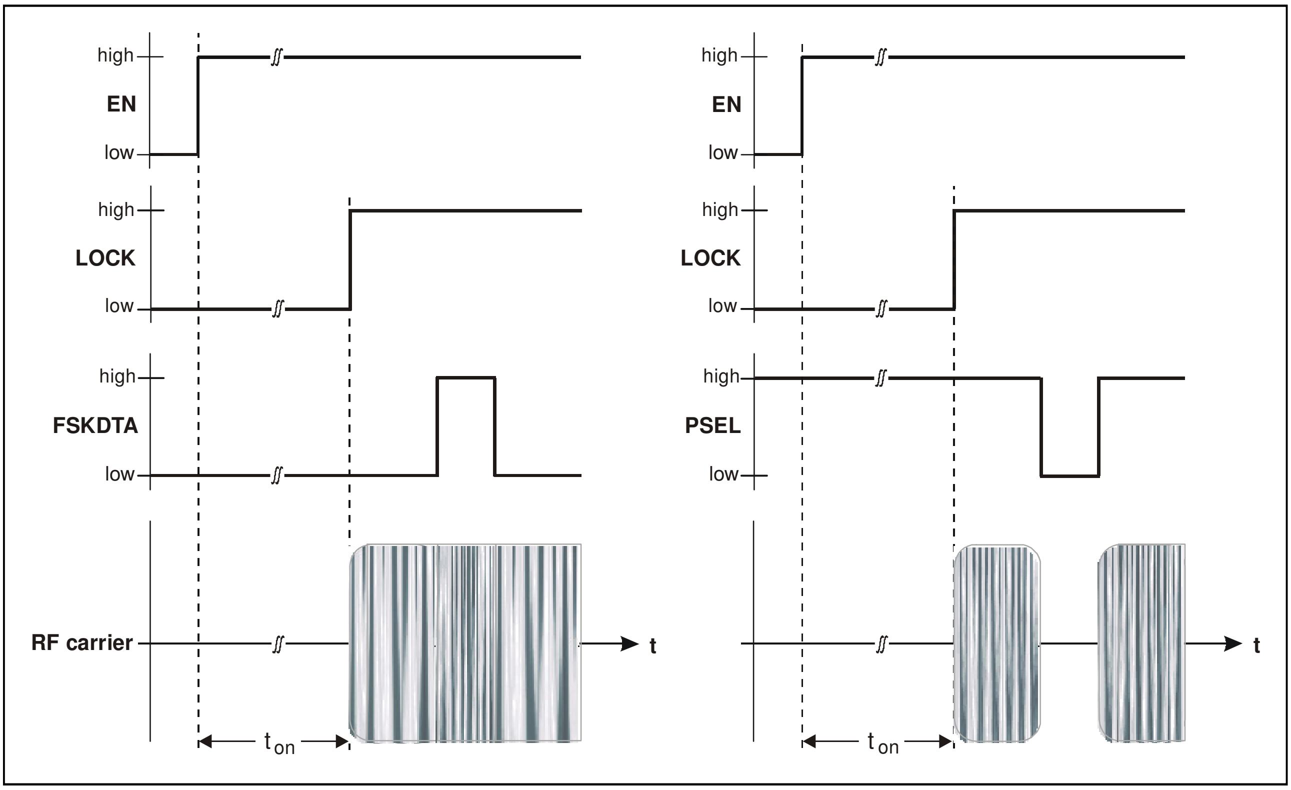
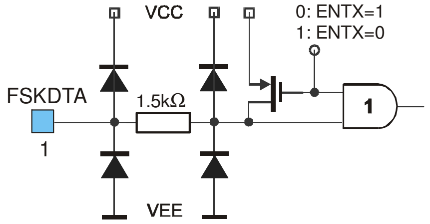
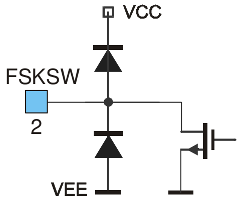
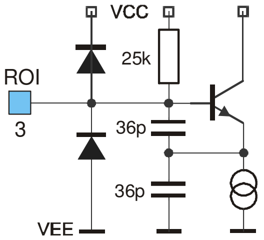
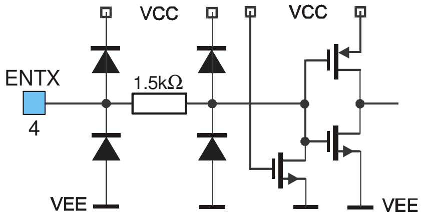
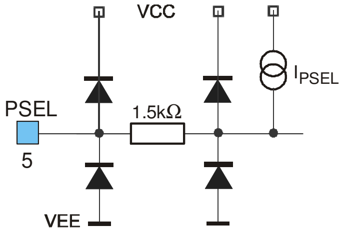
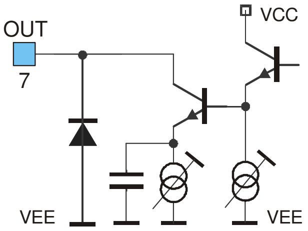


Fig. 5: Timing diagram for FSK and ASK modulation

7.10 Pin Definition and Description

Pin No.	Name	I/O Type	Functional Schematic	Description
1	FSKDTA	input		FSK data input, CMOS compatible with operation mode dependent pull-up circuit TX standby: no pull-up TX active: pull-up
2	FSKSW	analog I/O		XOSC FSK pulling pin, MOS switch
3	ROI	analog I/O		XOSC connection to XTAL, Colpitts type crystal oscillator
4	ENTX	input		mode control input, CMOS-compatible with internal pull-down circuit
5	PSEL	analog I/O		power select input, high-impedance comparator logic TX standby: I_{PSEL} = 0 TX active: I_{PSEL} = 8µA
6	VCC	supply		positive power supply
7	OUT	output		power amplifier output, open collector
8	VEE	ground		negative power supply

8. Electrical Characteristics

8.1 Absolute Maximum Ratings

Parameter	Symbol	Condition	Min	Max	Unit
Supply voltage	V_{CC}		0	7.0	V
Input voltage	V_{IN}		-0.3	V_{CC}+0.3	V
Storage temperature	T_{STG}		-65	150	°C
Junction temperature	T_J			150	°C
Thermal Resistance	R_{thJA}			163	K/W
Power dissipation	P_{diss}			0.15	W
Electrostatic discharge	V_{ESD}	human body model (HBM) according to CDF-AEC-Q100-002	±2.0		kV

8.2 Normal Operating Conditions

Parameter	Symbol	Condition	Min	Max	Unit
Supply voltage	V_{CC}		1.95	5.5	V
Operating temperature	T_A	MLX72013 K	-40	125	°C
Input low voltage CMOS	V_{IL}	ENTX, FSKDTA pins		0.3*V_{CC}	V
Input high voltage CMOS	V_{IH}	ENTX, FSKDTA pins	0.7*V_{CC}		V
XOSC frequency	f_{ref}	set by the crystal	26.5	27.8	MHz
VCO frequency	f_c	$f_c = 16 \bullet f_{ref}$	425	445	MHz
FSK deviation	Δf	depending on CX1, CX2 and crystal parameters	±5	±25	kHz
Data rate	R	NRZ code		40	kbit/s

8.3 Crystal Parameters

Parameter	Symbol	Condition	Min	Max	Unit
Crystal frequency	f_0	fundamental mode, AT	26.5	27.8	MHz
Load capacitance	C_L		10	15	pF
Static capacitance	C_0			7	pF
Series resistance	R_1			50	Ω
Spurious response	a_{spur}			-10	dB

8.4 DC Characteristics

All parameters under normal operating conditions, unless otherwise stated;
typical values at T_A = 23 °C and V_{CC} = 3.3 V

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Operating Currents						
Standby current	I_{SBY}	ENTX=0		10	4000	nA
Supply current in power step 0	I_{CC0}	ENTX=1		2.9	4.6	mA
Supply current in power step 1	I_{CC1}	ENTX=1		3.8	5.8	mA
Supply current in power step 2	I_{CC2}	ENTX=1		6.6	8.8	mA
Supply current in power step 3	I_{CC3}	ENTX=1		10.7	13.4	mA
Supply current in power step 4	I_{CC4}	ENTX=1		16.8	20.0	mA
Digital Pin Characteristics						
Input low voltage CMOS	V_{IL}	ENTX, FSKDTA pins	-0.3		$0.3*V_{cc}$	V
Input high voltage CMOS	V_{IH}	ENTX, FSKDTA pins	$0.7*V_{CC}$		$V_{CC}+0.3$	V
Pull down current ENTX pin	I_{PDEN}	ENTX=1	0.2	2.0	20	µA
Low level input current ENTX	I_{INLEN}	ENTX=0			0.02	µA
High level input current FSKDTA	I_{INHDTA}	FSKDTA=1			0.02	µA
Pull up current FSKDTA active	I_{PUDTAa}	FSKDTA=0, ENTX=1	0.1	1.5	12	µA
Pull up current FSKDTA standby	I_{PUDTAs}	FSKDTA=0, ENTX=0			0.02	µA
FSK Switch Resistance						
MOS switch On resistance	R_{ON}	FSKDTA=0, ENTX=1		20	70	Ω
MOS switch Off resistance	R_{OFF}	FSKDTA=1, ENTX=1	1			MΩ
Power Select Characteristics						
Power select current	I_{PSEL}	ENTX=1	7.0	8.6	9.9	µA
Power select voltage step 0	V_{PS0}	ENTX=1			0.035	V
Power select voltage step 1	V_{PS1}	ENTX=1	0.14		0.24	V
Power select voltage step 2	V_{PS2}	ENTX=1	0.37		0.60	V
Power select voltage step 3	V_{PS3}	ENTX=1	0.78		1.29	V
Power select voltage step 4	V_{PS4}	ENTX=1	1.55			V
Low Voltage Detection Characteristic						
Low voltage detect threshold	V_{LVD}	ENTX=1	1.75	1.85	1.95	V

8.5 AC Characteristics

All parameters under normal operating conditions, unless otherwise stated;
typical values at T_A = 23 °C and V_{CC} = 3.3 V; test circuit shown in Fig. 12, f_c = 433.92 MHz

Parameter	Symbol	Condition	Min	Typ	Max	Unit
CW Spectrum Characteristics						
Output power in step 0 (Isolation in off-state)	P_{off}	ENTX=1			-70	dBm
Output power in step 1	P_1	ENTX=1	-10	-9	-8	dBm
Output power in step 2	P_2	ENTX=1	2.5	3	4	dBm
Output power in step 3	P_3	ENTX=1	6	7	8	dBm
Output power in step 4	P_4	ENTX=1	10	11	12	dBm
Phase noise at 5kHz offset	$L(f_m)_5$	@ 5kHz offset		-98		dBc/Hz
Phase noise at 200kHz offset	$L(f_m)_{200}$	@ 200kHz offset		-97		dBc/Hz
Spurious emissions according to EN 300 220-1 (2000.09) table 13	P_{spur}	47MHz< f <74MHz 87.5MHz< f <118MHz 174MHz< f <230MHz 470MHz< f <862MHz B=100kHz			-54	dBm
		f < 1GHz, B=100kHz			-36	dBm
		f > 1GHz, B=1MHz			-30	dBm
Start-up Parameters						
Start-up time	t_{on}	from standby to transmit mode		0.6	1.0	ms
Frequency Stability						
Frequency stability vs. supply voltage	df_{VCC}				±3	ppm
Frequency stability vs. temperature	df_{TA}	crystal at constant temperature			±10	ppm
Frequency stability vs. variation range of C_{RO}	df_{CRO}				±20	ppm

8.6 Output Power Steps – FSK Mode

typical values at Ta = 23 °C

Power step	0	1	2	3	4
RPS / kΩ	< 3	22	56	120	not connected

8.7 Output Power Steps – ASK Mode

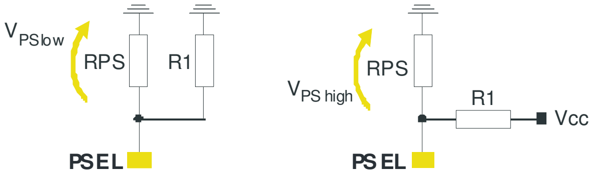
If the transmitter IC is operated in ASK mode and at a power step lower than 4 then the ASK data signal should be applied to pin PSEL via an additional resistor R1. Below table shows recommended component values for resistors RPS and R1 for all power steps.

typical values at Ta = 23 °C and VCC = 3.3 V

Power step - PS	1	2	3	4
RPS / **kΩ**	2.4	2.8	3.5	not connected
R1 / **kΩ**	36	14	7	0

V_{PSlow} = voltage across RPS if ASK_DTA at 0V

V_{PShigh} = voltage across RPS if ASK_DTA at Vcc



If the transmitter is operated at any supply voltage V_{cc}, the values for R1 and RPS can be calculated as follows:

$$R_1 = \frac{V_{CC} \cdot V_{PSlow}}{I_{PSEL} \cdot V_{PShigh}} \qquad R_{PS} = R_1 \frac{V_{PShigh}}{V_{CC} - V_{PShigh}}$$

9. Operating Characteristics vs Temperature

9.1 General

The following curves are based on the application circuit of Fig. 12.

9.2 DC Characteristics

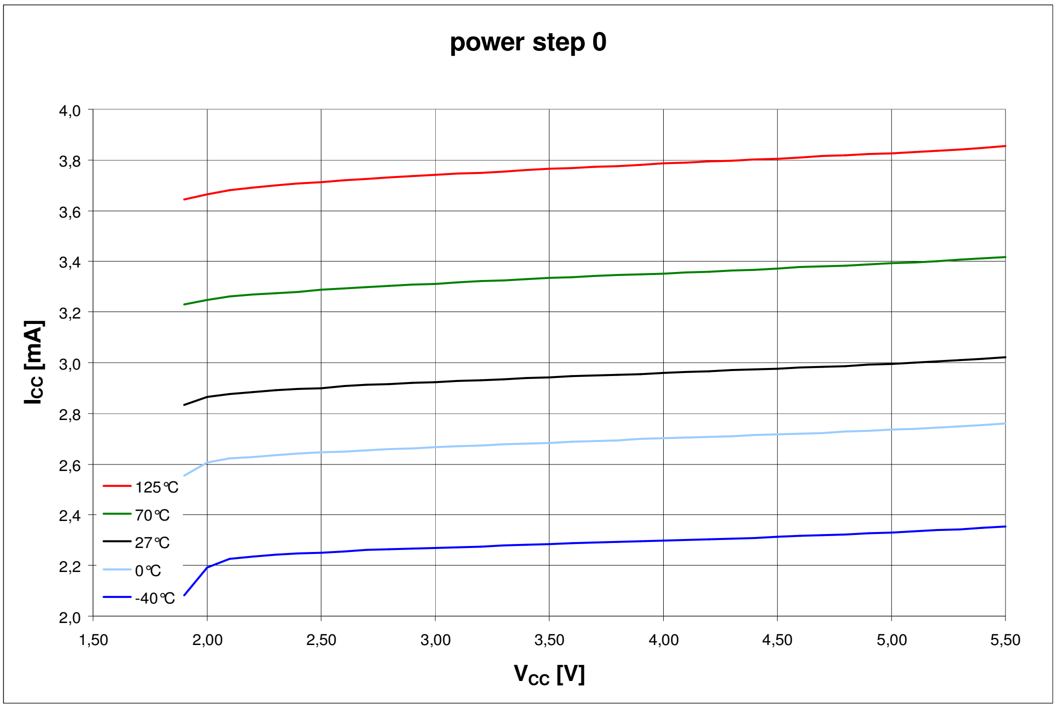


Fig. 6: Supply current in power step 0

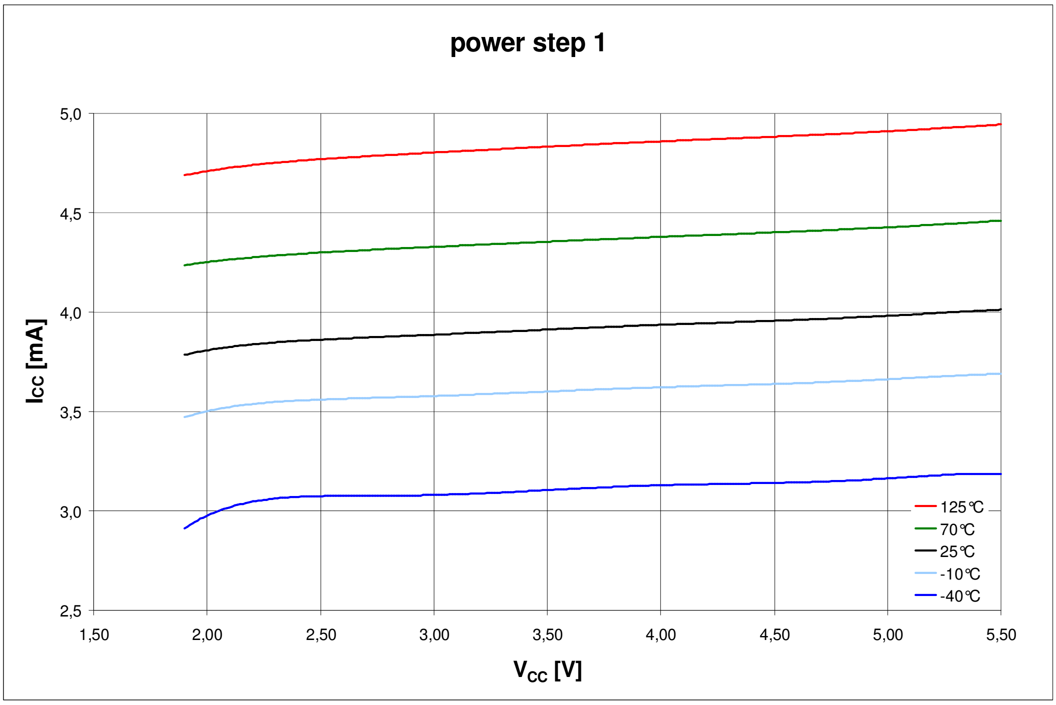


Fig. 7: Supply current in power step 1

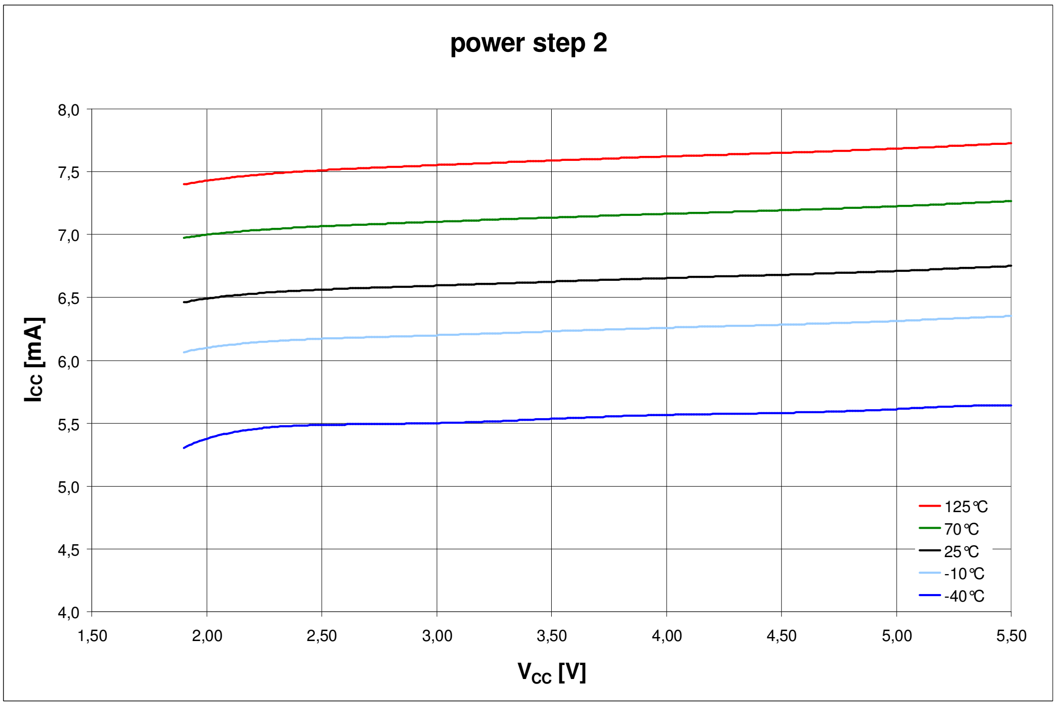


Fig. 8: Supply current in power step 2

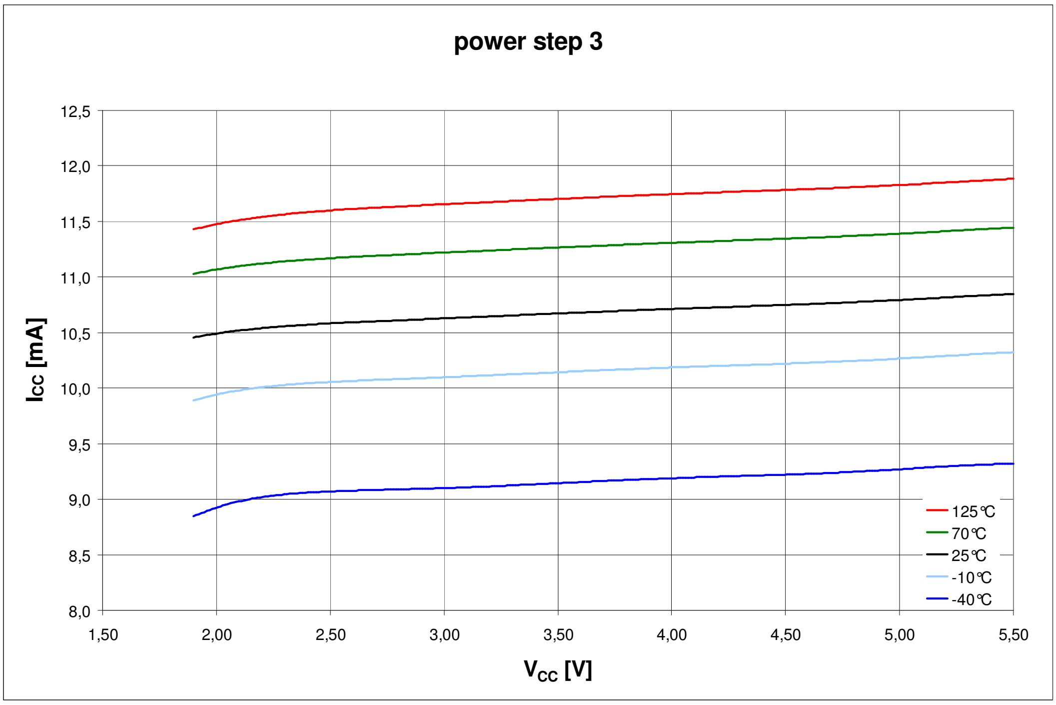


Fig. 9: Supply current in power step 3

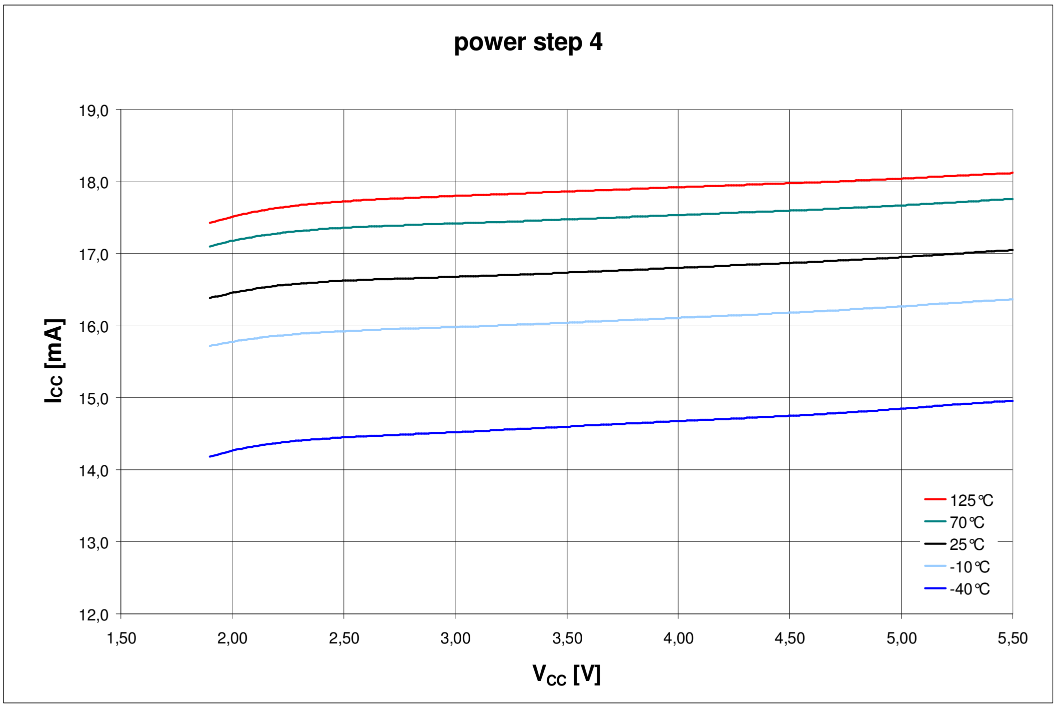


Fig. 10: Supply current in power step 4

9.3 AC Characteristics

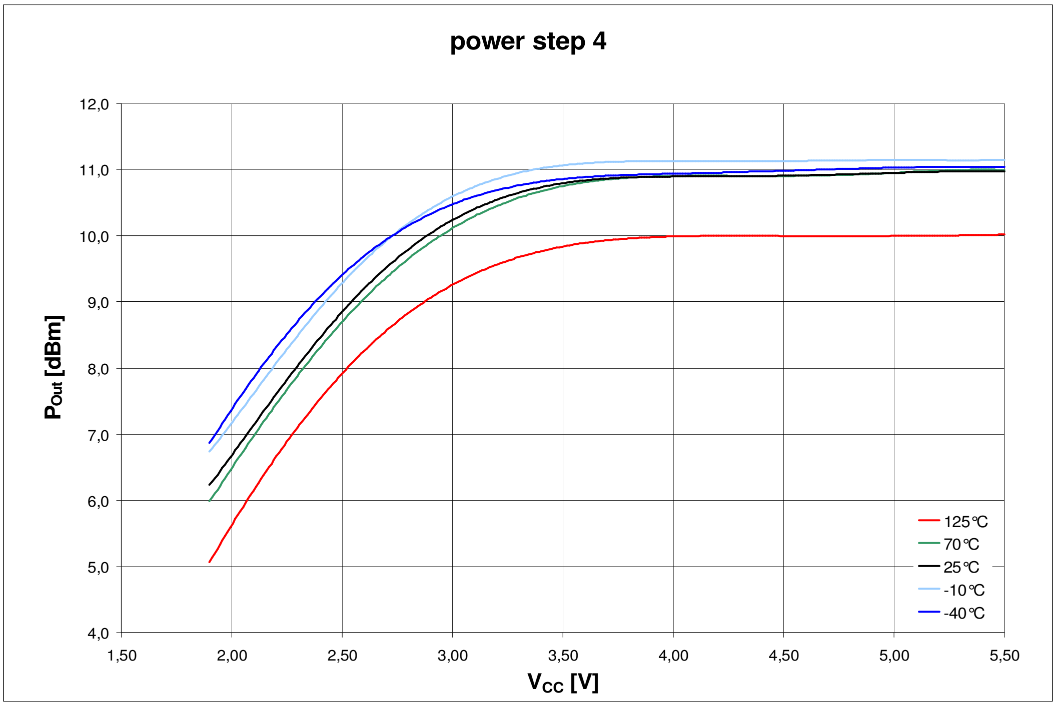


Fig. 11: Output power in step 4

10. Test Circuit for 433.92MHz

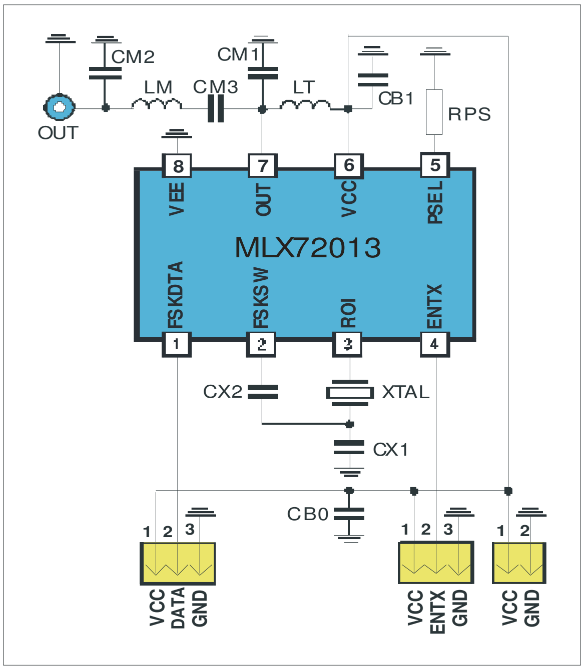


Fig. 12: 433.92MHz test circuit for FSK with 50 Ω matching network

10.1 433.92 MHz test circuit components

Part	Size	PS1	PS2	PS3	PS4	Tolerance	Description
CM1	0805	1 pF	2.7 pF	4.7 pF	8.2 pF	±2%	impedance matching capacitor
CM2	0805	N/C	5.6 pF	6.8 pF	12 pF	±2%	impedance matching capacitor
CM3	0805	82 pF				±2%	impedance matching capacitor
LM	0805	100 nH	56 nH	39 nH	22 nH	±5%	impedance matching inductor, **note 2**
LT	0805	47 nH	47 nH	33 nH	27 nH	±5%	output tank inductor, **note 2**
CX1	0805	10 pF				±2%	XOSC capacitor, **note 1**
CX2	0805	12 pF				±2%	XOSC capacitor, **note 1**
RPS	0805	22 kΩ	56 kΩ	120 kΩ	N/C	±5%	power-select resistor
CB0	1206	220 nF				±20%	blocking capacitor
CB1	0805	330 pF				±10%	blocking capacitor
XTAL	SMD 6x3.5	27.1200 MHz				±20ppm calibr. ±20ppm temp.	fundamental wave crystal, C_L = 10 pF, $C_{0,\,max}$ = 7 pF, R_1 = 40 Ω

Note 1: value depending on crystal parameters
Note 2: for high-power applications high-Q wire-wound inductors should be used

11. Package Information

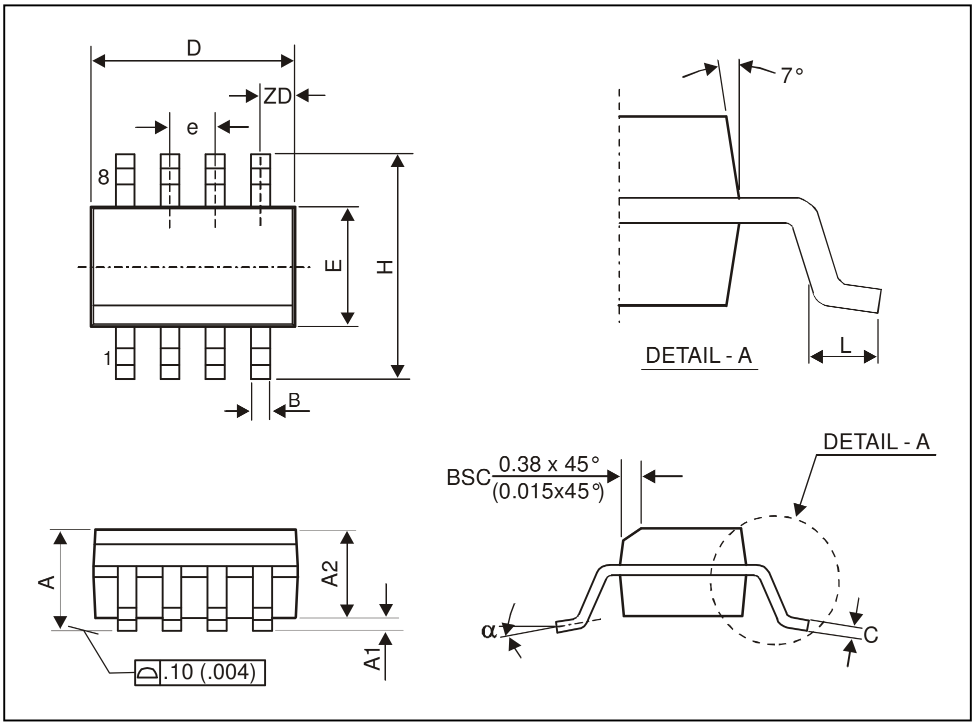


Fig. 13: SOIC8 (Small Outline Integrated Circuit)

All Dimensions in mm, coplanarity < 0.1mm												
min	4.80	3.81	5.80	1.52	0.10	1.37	1.27	0.36	0.53	0.19	0.41	0°
max	4.98	3.99	6.20	1.72	0.25	1.57		0.46		0.25	1.27	8°
all Dimension in inch, coplanarity < 0.004”												
min	0.189	0.150	0.2284	0.060	0.0040	0.054	0.050	0.014	0.021	0.075	0.016	0°
max	0.196	0.157	0.2440	0.068	0.0098	0.062		0.018		0.098	0.050	8°

11.1 Soldering Information

- The device MLX72013 is qualified for MSL1 with soldering peak temperature 260 deg C according to JEDEC J-STD-20.

12. Standard information regarding manufacturability of Melexis products with different soldering processes

Our products are classified and qualified regarding soldering technology, solderability and moisture sensitivity level according to following test methods:

Reflow Soldering SMD's (Surface Mount Devices)
- IPC/JEDEC J-STD-020
  Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices (classification reflow profiles according to table 5-2)
- EIA/JEDEC JESD22-A113
  Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing (reflow profiles according to table 2)

Wave Soldering SMD's (Surface Mount Devices) and THD's (Through Hole Devices)
- EN60749-20
  Resistance of plastic- encapsulated SMD's to combined effect of moisture and soldering heat
- EIA/JEDEC JESD22-B106 and EN60749-15
  Resistance to soldering temperature for through-hole mounted devices

Iron Soldering THD's (Through Hole Devices)
- EN60749-15
  Resistance to soldering temperature for through-hole mounted devices

Solderability SMD's (Surface Mount Devices) and THD's (Through Hole Devices)
- EIA/JEDEC JESD22-B102 and EN60749-21
  Solderability

For all soldering technologies deviating from above mentioned standard conditions (regarding peak temperature, temperature gradient, temperature profile etc) additional classification and qualification tests have to be agreed upon with Melexis.

The application of Wave Soldering for SMD's is allowed only after consulting Melexis regarding assurance of adhesive strength between device and board.

Melexis recommends reviewing on our web site the General Guidelines soldering recommendation (http://www.melexis.com/Quality_soldering.aspx) as well as trim&form recommendations (http://www.melexis.com/Assets/Trim-and-form-recommendations-5565.aspx).

Melexis is contributing to global environmental conservation by promoting **lead free** solutions. For more information on qualifications of **RoHS** compliant products (RoHS = European directive on the Restriction Of the use of certain Hazardous Substances) please visit the quality page on our website: http://www.melexis.com/quality.aspx

13. ESD Precautions

Electronic semiconductor products are sensitive to Electro Static Discharge (ESD).
Always observe Electro Static Discharge control procedures whenever handling semiconductor products.

14. Disclaimer

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