IDT™ 89HPES12NT3 PCI Express® Switch

User Manual

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About This Manual

Notes

Introduction

This user manual includes hardware and software information on the 89HPES12NT3, a member of IDT's PRECISE™ family of PCI Express® switching solutions offering the next-generation I/O interconnect standard.

Finding Additional Information

Information not included in this manual such as mechanicals, package pin-outs, and electrical characteristics can be found in the data sheet for this device, which is available from the IDT website (www.idt.com) as well as through your local IDT sales representative.

Content Summary

Chapter 1, "PES12NT3 Device Overview," provides a complete introduction to the performance capabilities of the 89HPES12NT3. Included in this chapter is a summary of features for the device as well as a system block diagram and pin description.

Chapter 2, "Clocking, Reset, and Initialization," provides a description of the two differential reference clock inputs that are used internally to generate all of the clocks required by the internal switch logic and the SerDes.

Chapter 3, "Link Operation," describes the operation of the link feature including polarity inversion, link width negotiation, and lane reversal.

Chapter 4, "Switch Operation," discusses the procedure for forwarding PCIe® TLPs between switch ports.

Chapter 5, "Power Management," describes the power management capability structure located in the configuration space of each PCI-PCI bridge in the PES12NT3.

Chapter 6, "SMBus Interfaces," describes the operation of the 2 SMBus interfaces on the PES12NT3.

Chapter 7, "NTB Upstream Port Failover," describes the NTB upstream port failover mechanism that enables the construction of fault tolerant systems.

Chapter 8, "General Purpose I/O," describes how the eight General Purpose I/O (GPIO) pins may be individually configured as general purpose inputs, general purpose outputs, or alternate functions

Chapter 9, "Non-Transparent Mode Operation," describes how the PES12NT3 can be configured during a fundamental reset to operate in non-transparent mode or non-transparent mode with serial EEPROM initialization.

Chapter 10, "JTAG Boundary Scan," discusses an enhanced JTAG interface, including a system logic TAP controller, signal definitions, a test data register, an instruction register, and usage considerations.

Signal Nomenclature

To avoid confusion when dealing with a mixture of "active-low" and "active-high" signals, the terms assertion and negation are used. The term assert or assertion is used to indicate that a signal is active or true, independent of whether that level is represented by a high or low voltage. The term negate or negation is used to indicate that a signal is inactive or false.

Notes

To define the active polarity of a signal, a suffix will be used. Signals ending with an 'N' should be interpreted as being active, or asserted, when at a logic zero (low) level. All other signals (including clocks, buses and select lines) will be interpreted as being active, or asserted when at a logic one (high) level. To define buses, the most significant bit (MSB) will be on the left and least significant bit (LSB) will be on the right. No leading zeros will be included.

Throughout this manual, when describing signal transitions, the following terminology is used. Rising edge indicates a low-to-high (0 to 1) transition. Falling edge indicates a high-to-low (1 to 0) transition. These terms are illustrated in Figure 1.

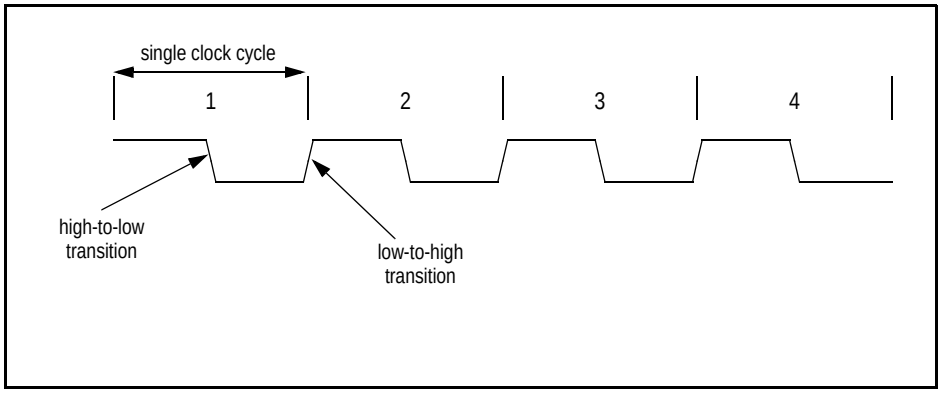

Figure 1 Signal Transitions

Numeric Representations

To represent numerical values, either decimal, binary, or hexadecimal formats will be used. The binary format is as follows: 0bDDD, where "D" represents either 0 or 1; the hexadecimal format is as follows: 0xDD, where "D" represents the hexadecimal digit(s); otherwise, it is decimal.

The compressed notation ABC[x|y|z]D refers to ABCxD, ABCyD, and ABCzD.

The compressed notation ABC[x..y]D refers to ABCxD, ABC(x+1)D, ABC(x+2)D,... ABCyD.

Data Units

The following data unit terminology is used in this document.

Term	Words	Bytes	Bits
Byte	1/2	1	8
Word	1	2	16
Doubleword (Dword)	2	4	32
Quadword (Qword)	4	8	64

Table 1 Data Unit Terminology

In quadwords, bit 63 is always the most significant bit and bit 0 is the least significant bit. In doublewords, bit 31 is always the most significant bit and bit 0 is the least significant bit. In words, bit 15 is always the most significant bit and bit 0 is the least significant bit. In bytes, bit 7 is always the most significant bit and bit 0 is the least significant bit.

The ordering of bytes within words is referred to as either "big endian" or "little endian." Big endian systems label byte zero as the most significant (leftmost) byte of a word. Little endian systems label byte zero as the least significant (rightmost) byte of a word. See Figure 2.

Notes

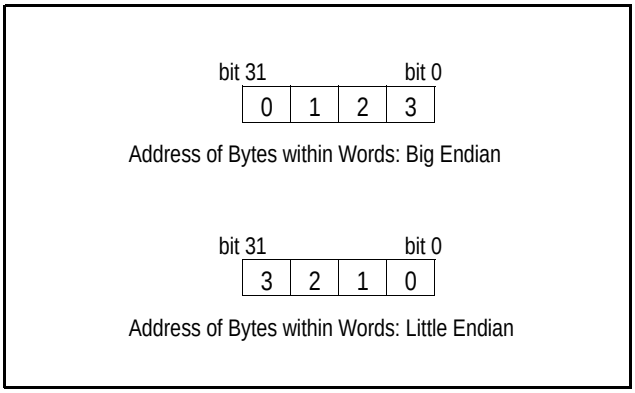

Figure 2 Example of Byte Ordering for “Big Endian” or “Little Endian” System Definition

Register Terminology

Software in the context of this register terminology refers to modifications made by PCIe root configuration writes, writes to registers made through the slave SMBus interface, or serial EEPROM register initialization. See Table 2.

Type	Abbreviation	Description
Hardware Initialized	HWINIT	Register bits are initialized by firmware or hardware mechanisms such as pin strapping or serial EEPROM. (System firmware hardware initialization is only allowed for system integrated devices.) Bits are read-only after initialization and can only be reset (for write-once by firmware) with reset.
Read Only and Clear	RC	Software can read the register/bits with this attribute. Reading the value will automatically cause the register/bit to be reset to zero. Writing to a RC location has no effect.
Read Clear and Write	RCW	Software can read the register/bits with this attribute. Reading the value will automatically cause the register/bits to be reset to zero. Writes cause the register/bits to be modified.
Reserved	Reserved	The value read from a reserved register/bit is undefined. Thus, software must deal correctly with fields that are reserved. On reads, software must use appropriate masks to extract the defined bits and not rely on reserved bits being any particular value. On writes, software must ensure that the values of reserved bit positions are preserved. That is, the values of reserved bit positions must first be read, merged with the new values for other bit positions and then written back.
Read Only	RO	Software can only read registers/bits with this attribute. Contents are hardwired. Writing to a RO location has no effect.
Read Only and set by Hardware	ROS	Software can only read registers/bits with this attribute. Contents are set by hardware and may change. Writing to a ROS location has no effect.
Read and Write	RW	Software can both read and write bits with this attribute.

Table 2 Register Terminology (Sheet 1 of 2)

Notes

Type	Abbreviation	Description
Read and Write Clear	RW1C	Software can read and write to registers/bits with this attribute. However, writing a value of zero to a bit with this attribute has no effect. A RW1C bit can only be set to a value of 1 by a hardware event. To clear a RW1C bit (i.e., change its value to zero) a value of one must be written to the location. An RW1C bit is never cleared by hardware.
Read and Write when Unlocked	RWL	Software can read the register/bits with this attribute. Writing to register/bits with this attribute will only cause the value to be modified if the REGUNLOCK bit in the SWCNTL register is set. When the REGUNLOCK bit is cleared, writes are ignored and the register/bits are effectively read-only
Zero	Zero	A zero register or bit must be written with a value of zero and returns a value of zero when read.

Table 2 Register Terminology (Sheet 2 of 2)

Use of Hypertext

In Chapter 9 there are tables which contain register names and page numbers highlighted in blue under the Register Definition column. In pdf files, users can jump from the source table directly to the registers by clicking on the register name in the source table. Each register name in the table is linked directly to the appropriate register in the register section of the chapter. To return to the source table after having jumped to the register section, click on the same register name (in blue) in the register section.

Revision History

April 15, 2008: Initial publication of user manual.

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PES12NT3 Device Overview

Notes

Introduction

The 89HPES12NT3 is a member of the IDT PRECISE™ family of PCI Express® switching solutions offering the next-generation I/O interconnect standard. The PES12NT3 is a 12-lane, 3-port peripheral chip that performs PCI Express Base switching with a feature set optimized for high performance applications such as servers, storage, and communications/networking. It provides high-performance I/O connectivity and switching functions between a PCIe® upstream port, a transparent downstream port, and a non-transparent downstream port.

With non-transparent bridging (NTB) functionality, the PES12NT3 can be used standalone or as a chipset with IDT PCIe System Interconnect Switches in multi-host and intelligent I/O applications such as communications, storage, and blade servers where inter-domain communication is required.

Utilizing standard PCI Express interconnect, the PES12NT3 provides the most efficient high-performance I/O connectivity solution for applications requiring high throughput, low latency, and simple board layout with a minimum number of board layers. With support for non-transparent bridging, the PES12NT3, as a standalone switch or as a chipset with IDT PCIe System Interconnect Switches, enables multi-host and intelligent I/O applications requiring inter-domain communication. The PES12NT3 provides 48 Gbps (6 GBps) of aggregated, full-duplex switching capacity through 12 integrated serial lanes, using proven and robust IDT technology. Each lane provides 2.5 Gbps of bandwidth in both directions and is fully compliant with PCI Express Base specification 1.0a.

The PES12NT3 is based on a flexible and efficient layered architecture. The PCI Express layer consists of SerDes, Physical, Data Link and Transaction layers in compliance with PCI Express Base specification Revision 1.0a. The PES12NT3 can operate either as a store and forward or cut-through switch depending on the packet size and is designed to switch memory and I/O transactions. It supports eight Traffic Classes (TCs) and one Virtual Channel (VC) with sophisticated resource management. This includes round robin port arbitration, guaranteeing bandwidth allocation and/or latency for critical traffic classes in applications such as high throughput 10 GbE I/Os, SATA controllers, and Fibre Channel HBAs.

Figure 1.1 provides a functional block diagram while Figure 1.2 illustrates the architecture of the device.

Notes

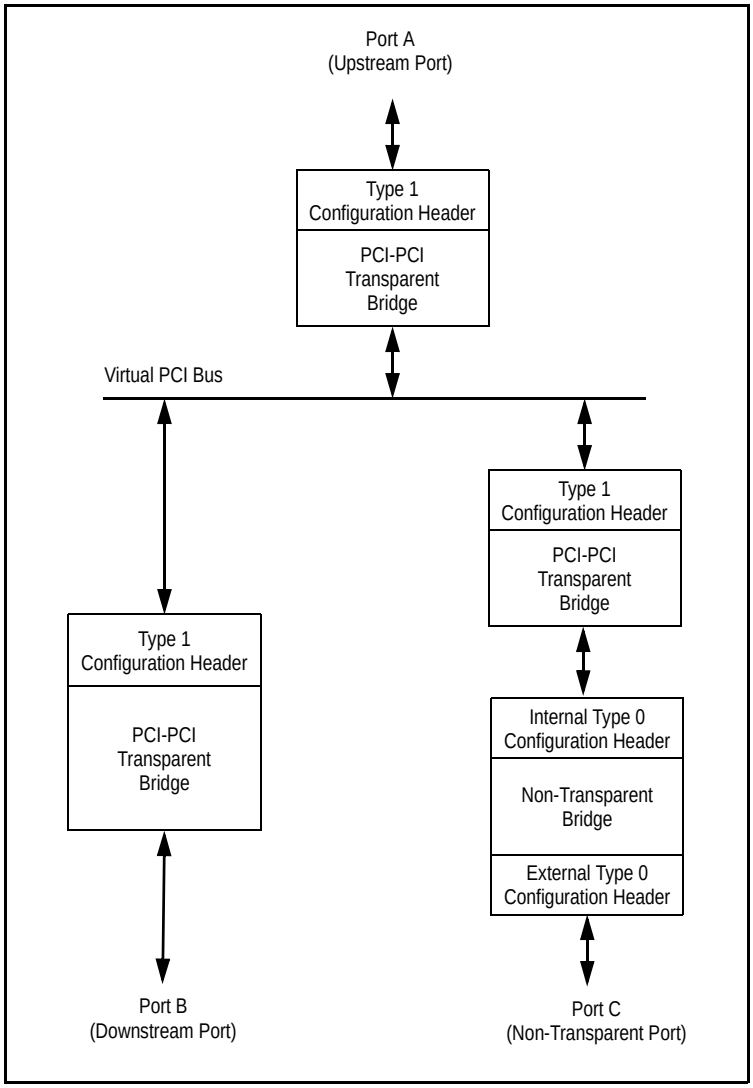

Figure 1.1 PES12NT3 Functional Block Diagram

As shown in Figure 1.1, port A is configured as the upstream port and ports B and C as the downstream ports. Port B resides on the internal PCI Bus at Device 0, Function 0. Port C resides on the internal PCI Bus at Device 1, Function 0.

Notes

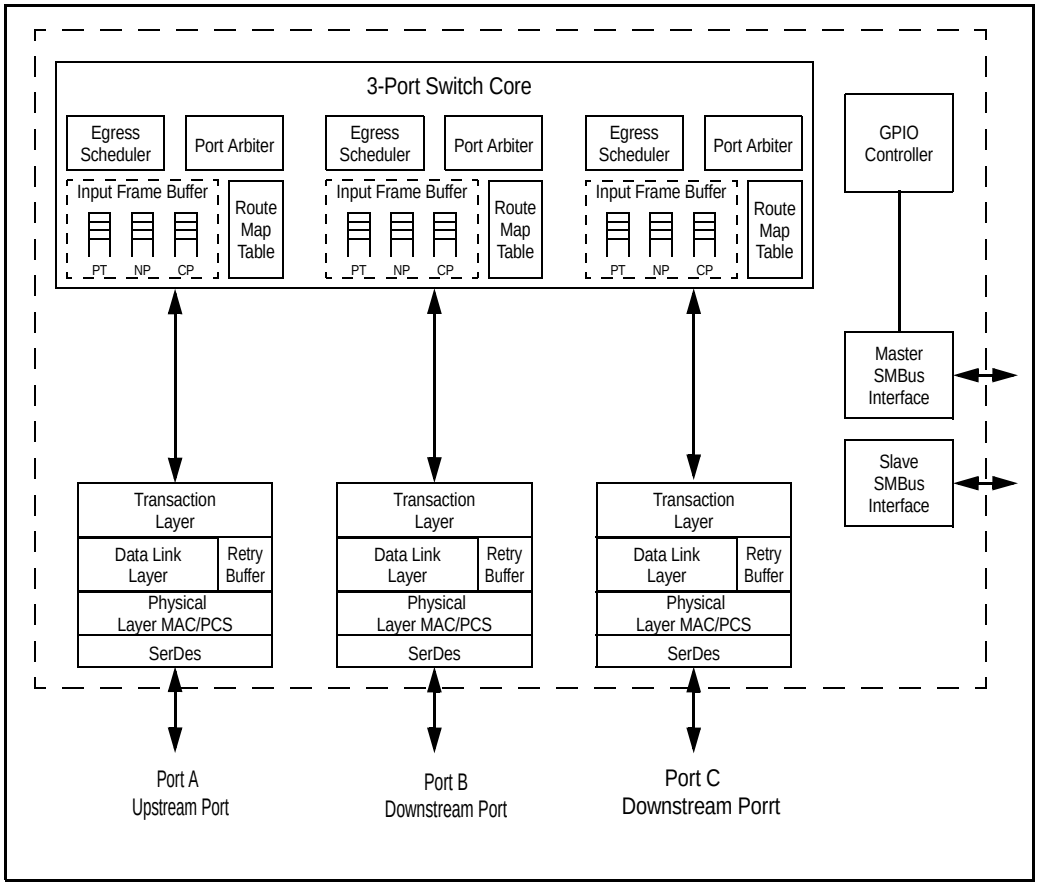

Figure 1.2 PES12NT3 Architectural Block Diagram

Features

- High Performance PCI Express Switch
  - *Twelve PCI Express lanes (2.5Gbps), three switch ports*
  - *Delivers 48 Gbps (6 GBps) of aggregate switching capacity*
  - *Low latency cut-through switch architecture*
  - *Support for Max Payload size up to 2048 bytes*
  - *Supports one virtual channel and eight traffic classes*
  - *PCI Express Base specification Revision 1.0a compliant*
- Flexible Architecture with Numerous Configuration Options
  - *Port arbitration schemes utilizing round robin*
  - *Supports automatic per port link width negotiation (x4, x2, or x1)*
  - *Static lane reversal on all ports*
  - *Automatic polarity inversion on all lanes*
  - *Supports locked transactions, allowing use with legacy software*
  - *Ability to load device configuration from serial EEPROM*
  - *Ability to control device via SMBus*
- Non-Transparent Port
  - *Crosslink support on NTB port*
  - *Four mapping windows supported*

Notes

- Each may be configured as a 32-bit memory or I/O window
- May be paired to form a 64-bit memory window

– *Interprocessor communication*
- Thirty-two inbound and outbound doorbells
- Four inbound and outbound message registers
- Two shared scratchpad registers

– *Allows up to sixteen masters to communicate through the non-transparent port*
– *No limit on the number of supported outstanding transactions through the non-transparent bridge*
– *Completely symmetric non-transparent bridge operation allows similar/same configuration software to be run*
– *Supports direct connection to a transparent or non-transparent port of another switch*

◆ Highly Integrated Solution
– *Requires no external components*
– *Incorporates on-chip internal memory for packet buffering and queueing*
– *Integrates twelve 2.5 Gbps embedded full duplex SerDes, 8B/10B encoder/decoder (no separate transceivers needed)*

◆ Reliability, Availability, and Serviceability (RAS) Features
– *Upstream port can be dynamically swapped with non-transparent downstream port to support failover applications*
– *Internal end-to-end parity protection on all TLPs ensures data integrity even in systems that do not implement end-to-end CRC (ECRC)*
– *Supports ECRC pass-through in transparent and non-transparent ports*
– *Supports Hot-Swap*

◆ Power Management
– *Supports PCI Power Management Interface specification, Revision 1.1 (PCI-PM)*
– *Unused SerDes are disabled*

◆ Testability and Debug Features
– *Built in SerDes Pseudo-Random Bit Stream (PRBS) generator*
– *Ability to read and write any internal register via the SMBus*
– *Ability to bypass link training and force any link into any mode*
– *Provides statistics and performance counters*

◆ Two SMBus Interfaces
– *Slave interface provides full access to all software-visible registers by an external SMBus master*
– *Master interface provides connection for an optional serial EEPROM used for initialization*
– *Master and slave interfaces may be tied together so the switch can act as both master and slave*

◆ Eight General Purpose Input/Output pins

◆ Packaged in 19x19mm 324-ball BGA with 1mm ball spacing

System Identification

Vendor ID

All vendor IDs in the device are hardwired to 0x111D which corresponds to Integrated Device Technology, Inc.

Notes

Device ID

The device IDs for the PES12NT3 are shown in Table 1.1.

PCI Device	Offset Device ID
Transparent bridge associated with Ports A and B	0x8058
Transparent bridge associated with Port C	0x8059
Internal NTB Endpoint associated with Port C	0x805A
External NTB Endpoint associated with Port C	0x805B

Table 1.1 PES12NT3 Offset Device IDs

Revision ID

All revision IDs in the PES12NT3 are set to the same value. The value of the revision ID is determined in one place and is easily modified during a metal mask change. The revision ID shall be incremented with each all layer or metal mask change.

Revision ID	Description
0x1	Corresponds to YA silicon
0x2	Corresponds to YB silicon
0x4	Corresponds to YC silicon

Table 1.2 PES12NT3 Revision IDs

JTAG ID

The JTAG ID is:

- Version: Same value as Revision ID. See the Revision ID section above.
- Part number: Same value as base Device ID. See the Device ID section above.
- Manufacture ID: 0x33
- LSB: 0x1

Notes

Logic Diagram

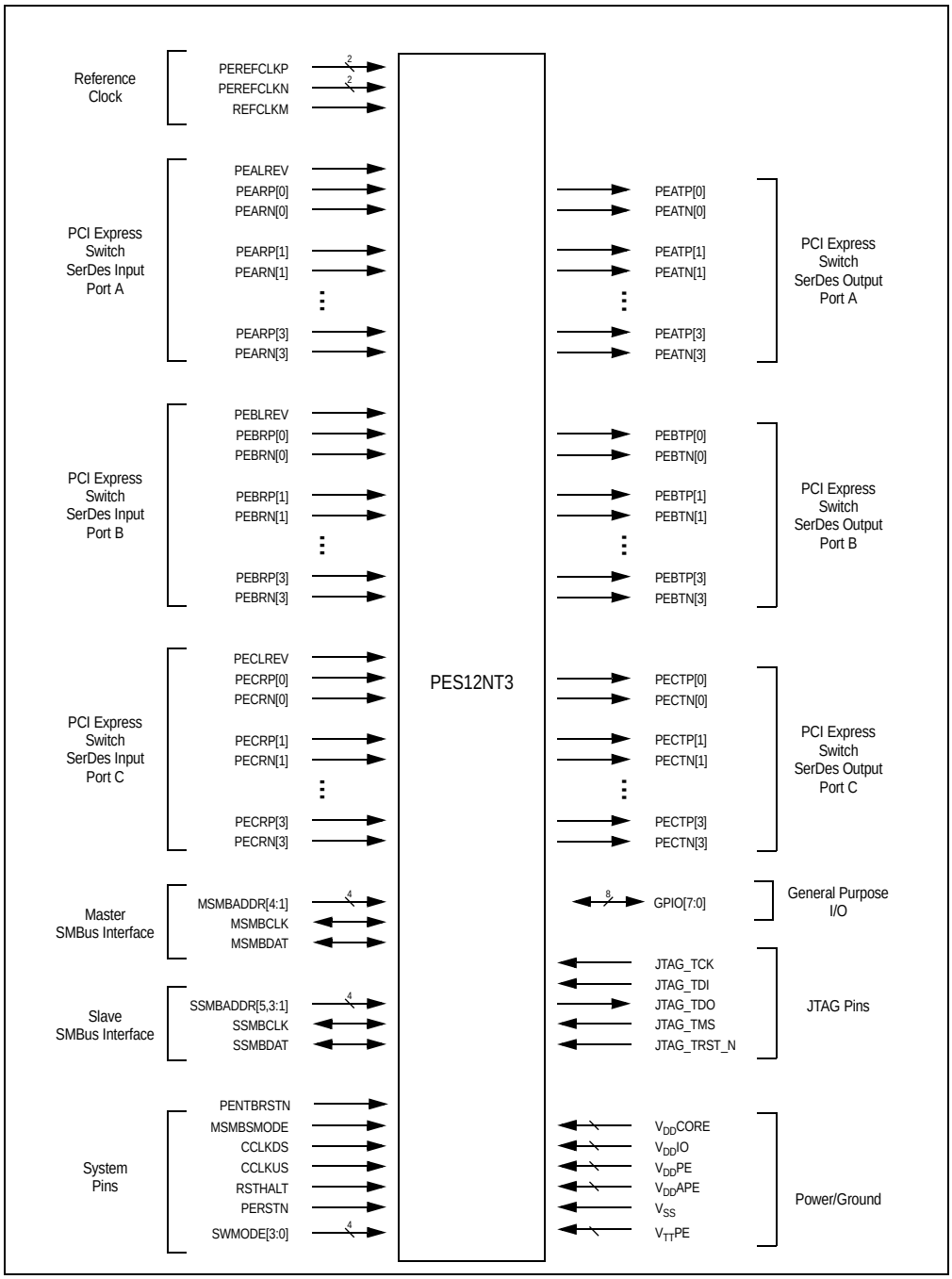

Figure 1.3 PES12NT3 Logic Diagram

Pin Description

The following tables list the functions of the pins provided on the PES12NT3. Some of the functions listed may be multiplexed onto the same pin. The active polarity of a signal is defined using a suffix. Signals ending with an “N” are defined as being active, or asserted, when at a logic zero (low) level. All other signals (including clocks, buses, and select lines) will be interpreted as being active, or asserted, when at a logic one (high) level.

Notes

Signal	Type	Name/Description
PEALREV	I	PCI Express Port A Lane Reverse. When this bit is asserted, the lanes of PCI Express Port A are reversed. This value may be overridden by modifying the value of the PALREV bit in the PA_SWCTL register.
PEARP[3:0] PEARN[3:0]	I	PCI Express Port A Serial Data Receive. Differential PCI Express receive pairs for port A.
PEATP[3:0] PEATN[3:0]	O	PCI Express Port A Serial Data Transmit. Differential PCI Express transmit pairs for port A
PEBLREV	I	PCI Express Port B Lane Reverse. When this bit is asserted, the lanes of PCI Express Port B are reversed. This value may be overridden by modifying the value of the PBLREV bit in the PA_SWCTL register.
PEBRP[3:0] PEBRN[3:0]	I	PCI Express Port B Serial Data Receive. Differential PCI Express receive pairs for port B.
PEBTP[3:0] PEBTN[3:0]	O	PCI Express Port B Serial Data Transmit. Differential PCI Express transmit pairs for port B
PECLREV	I	PCI Express Port C Lane Reverse. When this bit is asserted, the lanes of PCI Express Port C are reversed. This value may be overridden by modifying the value of the PCLREV bit in the PA_SWCTL register.
PECRP[3:0] PECRN[3:0]	I	PCI Express Port C Serial Data Receive. Differential PCI Express receive pairs for port C.
PECTP[3:0] PECTN[3:0]	O	PCI Express Port C Serial Data Transmit. Differential PCI Express transmit pairs for port C
PEREFCLKP[1:0] PEREFCLKN[1:0]	I	PCI Express Reference Clock. Differential reference clock pair input. This clock is used as the reference clock by on-chip PLLs to generate the clocks required for the system logic and on-chip SerDes. The frequency of the differential reference clock is determined by the REFCLKM signal.
REFCLKM	I	PCI Express Reference Clock Mode Select. These signals select the frequency of the reference clock input. 0x0 - 100 MHz 0x1 - 125 MHz

Table 1.3 PCI Express Interface Pins

Signal	Type	Name/Description
MSMBADDR[4:1]	I	Master SMBus Address. These pins determine the SMBus address of the serial EEPROM from which configuration information is loaded.
MSMBCLK	I/O	Master SMBus Clock. This bidirectional signal is used to synchronize transfers on the master SMBus. It is active and generating the clock only when the EEPROM or I/O Expanders are being accessed.
MSMBDAT	I/O	Master SMBus Data. This bidirectional signal is used for data on the master SMBus.

Table 1.4 SMBus Interface Pins (Part 1 of 2)

Notes

Signal	Type	Name/Description
SSMBADDR[5,3:1]	I	Slave SMBus Address. These pins determine the SMBus address to which the slave SMBus interface responds.
SSMBCLK	I/O	Slave SMBus Clock. This bidirectional signal is used to synchronize transfers on the slave SMBus.
SSMBDAT	I/O	Slave SMBus Data. This bidirectional signal is used for data on the slave SMBus.

Table 1.4 SMBus Interface Pins (Part 2 of 2)

Signal	Type	Name/Description
GPIO[0]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: PEBRSTN Alternate function pin type: Output Alternate function: Reset output for downstream port B
GPIO[1]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: PECRSTN Alternate function pin type: Output Alternate function: Reset output for downstream port C
GPIO[2]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: PALINKUPN Alternate function pin type: Output Alternate function: Port A link up status output
GPIO[3]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: PBLINKUPN Alternate function pin type: Output Alternate function: Port B link up status output
GPIO[4]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: PCLINKUPN Alternate function pin type: Output Alternate function: Port C link up status output
GPIO[5]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: FAILOVERP Alternate function pin type: Input Alternate function: NTB upstream port failover
GPIO[6]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin.
GPIO[7]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin.

Table 1.5 General Purpose I/O Pins

Notes

Signal	Type	Name/Description
CCLKDS	I	Common Clock Downstream. When the CCLKDS pin is asserted, it indicates that a common clock is being used between the downstream device and the downstream port.
CCLKUS	I	Common Clock Upstream. When the CCLKUS pin is asserted, it indicates that a common clock is being used between the upstream device and the upstream port.
MSMBSMODE	I	Master SMBus Slow Mode. The assertion of this pin indicates that the master SMBus should operate at 100 KHz instead of 400 KHz. This value may not be overridden.
PENTBRSTN	I	Non-Transparent Bridge Reset. Assertion of this signal indicates a reset on the external side of the non-transparent bridge. This signal is only used when the switch mode selects a non-transparent mode and has no effect otherwise.
PERSTN	I	Fundamental Reset. Assertion of this signal resets all logic inside the PES12NT3 and initiates a PCI Express fundamental reset.
RSTHALT	I	Reset Halt. When this signal is asserted during a PCI Express fundamental reset, the PES12NT3 executes the reset procedure and remains in a reset state with the Master and Slave SMBuses active. This allows software to read and write registers internal to the device before normal device operation begins. The device exits the reset state when the RSTHALT bit is cleared in the PA_SWCTL register by an SMBus master.
SWMODE[3:0]	I	Switch Mode. These configuration pins determine the PES12NT3 switch operating mode. 0x0 - Reserved 0x1 - Reserved 0x2 - Non-transparent mode 0x3 - Non-transparent mode with serial EEPROM initialization 0x4 - Non-transparent failover mode 0x5 - Non-transparent failover mode with serial EEPROM initialization 0x6 through 0xF - Reserved

Table 1.6 System Pins

Signal	Type	Name/Description
JTAG_TCK	I	JTAG Clock. This is an input test clock used to clock the shifting of data into or out of the boundary scan logic or JTAG Controller. JTAG_TCK is independent of the system clock with a nominal 50% duty cycle.
JTAG_TDI	I	JTAG Data Input. This is the serial data input to the boundary scan logic or JTAG Controller.
JTAG_TDO	O	JTAG Data Output. This is the serial data shifted out from the boundary scan logic or JTAG Controller. When no data is being shifted out, this signal is tri-stated.
JTAG_TMS	I	JTAG Mode. The value on this signal controls the test mode select of the boundary scan logic or JTAG Controller.

Table 1.7 Test Pins (Part 1 of 2)

Notes

Signal	Type	Name/Description
JTAG_TRST_N	I	JTAG Reset. This active low signal asynchronously resets the boundary scan logic and JTAG TAP Controller. An external pull-up on the board is recommended to meet the JTAG specification in cases where the tester can access this signal. However, for systems running in functional mode, one of the following should occur: 1) actively drive this signal low with control logic 2) statically drive this signal low with an external pull-down on the board

Table 1.7 Test Pins (Part 2 of 2)

Signal	Type	Name/Description
V_{DD}CORE	I	Core V_{DD}. Power supply for core logic.
V_{DD}IO	I	I/O V_{DD}. LVTTL I/O buffer power supply.
V_{DD}PE	I	PCI Express Digital Power. PCI Express digital power used by the digital power of the SerDes.
V_{DD}APE	I	PCI Express Analog Power. PCI Express analog power used by the PLL and bias generator.
V_{TT}PE	I	PCI Express Termination Power.
V_{SS}	I	Ground.

Table 1.8 Power and Ground Pins

Pin Characteristics

Note: Some input pads of the PES12NT3 do not contain internal pull-ups or pull-downs. Unused inputs should be tied off to appropriate levels. This is especially critical for unused control signal inputs which, if left floating, could adversely affect operation. Also, any input pin left floating can cause a slight increase in power consumption.

Notes

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor	Notes
PCI Express Interface	PEALREV	I	LVTTL	Input	pull-down	
	PEARN[3:0]	I	CML	Serial link		
	PEARP[3:0]	I				
	PEATN[3:0]	O				
	PEATP[3:0]	O				
	PEBLREV	I	LVTTL	Input	pull-down	
	PEBRN[3:0]	I	CML	Serial link		
	PEBRP[3:0]	I				
	PEBTN[3:0]	O				
	PEBTP[3:0]	O				
	PECLREV	I	LVTTL	Input	pull-down	
	PECRN[3:0]	I	CML	Serial link		
	PECRP[3:0]	I				
	PECTN[3:0]	O				
	PECTP[3:0]	O				
	PEREFCLKN[1:0]	I	LVPECL/ CML	Diff. Clock Input		Refer to Table 8 of the PES12NT3 Data Sheet
	PEREFCLKP[1:0]	I				
	REFCLKM	I	LVTTL	Input	pull-down	
SMBus	MSMBADDR[4:1]	I	LVTTL	Input	pull-up	
	MSMBCLK	I/O		STI		
	MSMBDAT	I/O				
	SSMBADDR[5,3:1]	I		Input	pull-up	
	SSMBCLK	I/O		STI		
	SSMBDAT	I/O				
General Purpose I/O	GPIO[7:0]	I/O	LVTTL	Input, High Drive	pull-up	
System Pins	CCLKDS	I	LVTTL	Input	pull-up	
	CCLKUS	I			pull-up	
	MSMBSMODE	I			pull-down	
	PENTBRSTN	I				
	PERSTN	I				
	RSTHALT	I			pull-down	
	SWMODE[3:0]	I			pull-up	

Table 1.9 Pin Characteristics (Part 1 of 2)

Notes

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor	Notes
JTAG	JTAG_TCK	I	LVTTL	STI	pull-up	
	JTAG_TDI	I			pull-up	
	JTAG_TDO	O		Low Drive		
	JTAG_TMS	I		STI	pull-up	
	JTAG_TRST_N	I			pull-up	External pull-down

Table 1.9 Pin Characteristics (Part 2 of 2)

Clocking, Reset, and Initialization

Notes

Introduction

The PES12NT3 has two differential reference clock inputs that are used internally to generate all of the clocks required by the internal switch logic and the SerDes. While not required, it is recommended that both reference clock input pairs be driven from a common clock source. There are no skew requirements between the reference clock inputs.The frequency of the reference clock inputs may be selected by the Reference Clock Mode Select (REFCLKM) input.

REFCLKM	Description
0	100 MHz reference clock input.
1	125 MHz reference clock input.

Table 2.1 Reference Clock Mode Encoding

Each of the reference clock differential inputs feeds six on-chip PLLs. Each PLL generates a 2.5 GHz clock which is used by four SerDes lanes and produces a 250 MHz core clock.The 250 MHz core clock output from one of the six internal PLLs is used as the system clock for internal switch logic.

Each of the reference clock differential inputs feeds six on-chip PLLs. Each PLL generates a 2.5 GHz clock which is used by four SerDes lanes and produces a 250 MHz core clock. The 250 MHz core clock output from one of the six internal PLLs is used as the system clock for internal switch logic.

Clock Operation

When the CCLKUS and CCLKDS pins are asserted, they indicate that a common clock is being used between the upstream device and the upstream port, as well as between the downstream devices and the downstream ports. The Spread Spectrum Clock (SSC) must be disabled when the non-common clock is used on either the upstream port or downstream port. Figures 2.1 through 2.4 illustrate the operation of the CCLKUS and CCLKDS clocks using a common clock and a non-common clock.

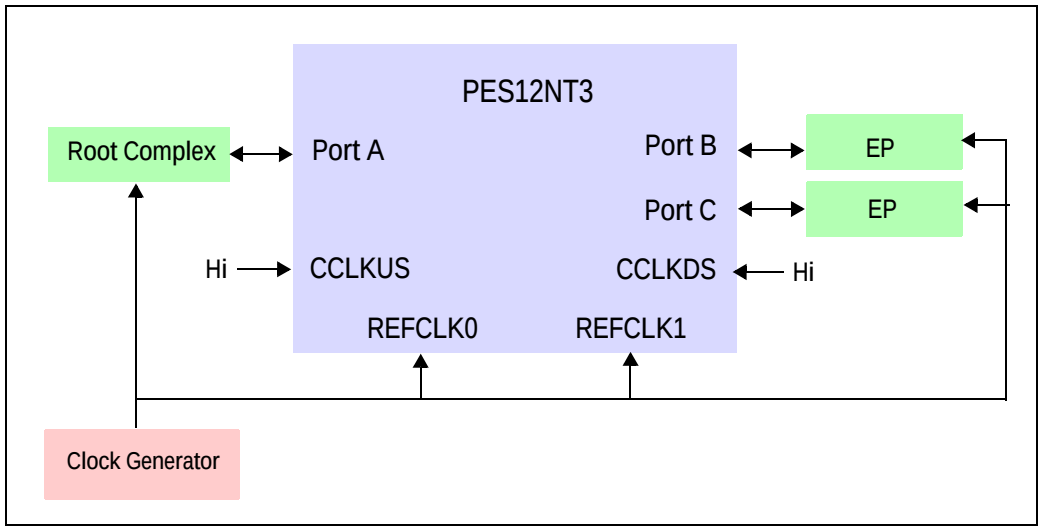

Figure 2.1 Common Clock on Upstream and Downstream (option to enable or disable Spread Spectrum Clock)

Notes

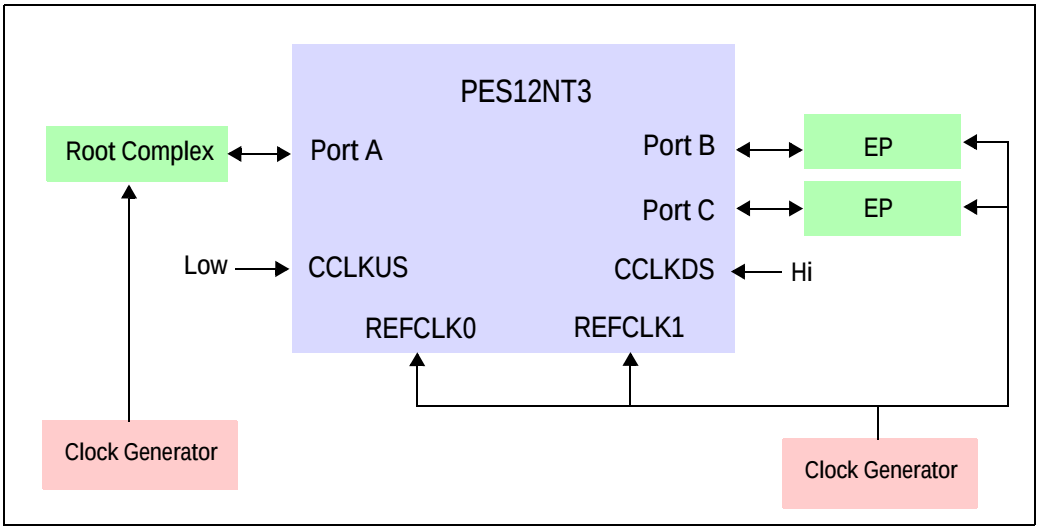

Figure 2.2 Non-Common Clock on Upstream; Common Clock on Downstream (must disable Spread Spectrum Clock)

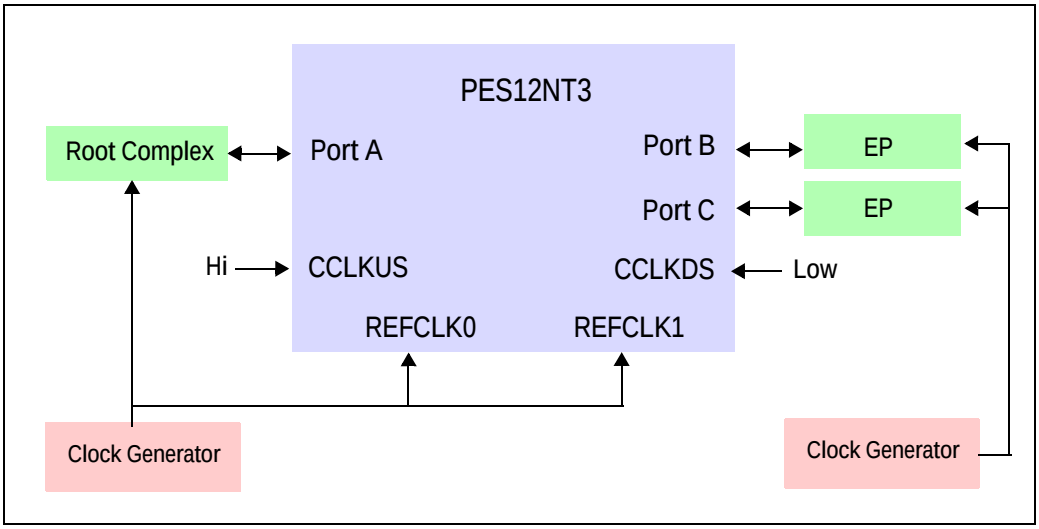

Figure 2.3 Common Clock on Upstream; Non-Common Clock on Downstream (must disable Spread Spectrum Clock)

Notes

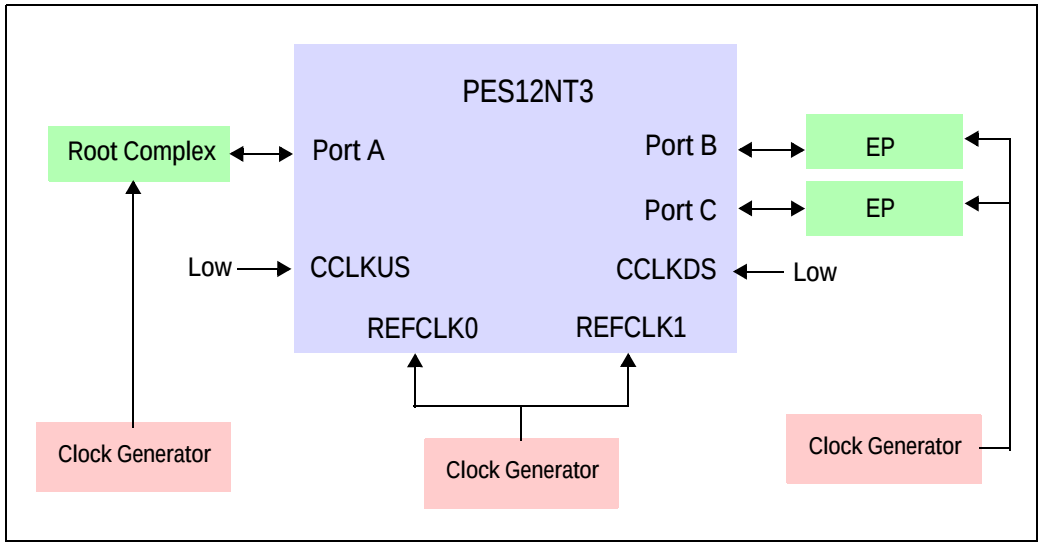

Figure 2.4 Non-Common Clock on Upstream and Downstream (must disable Spread Spectrum Clock)

Initialization

A boot configuration vector consisting of the signals listed in Table 2.2 is sampled by the PES12NT3 during a fundamental reset when PERSTN is negated. The boot configuration vector defines essential parameters for switch operation.

While basic switch operation may be configured using signals in the boot configuration vector, advanced switch features require configuration via an external serial EEPROM. The external serial EEPROM allows modification of any bit in any software visible register. See Chapter 6, SMBus Interfaces, for more information on the serial EEPROM.

The external serial EEPROM and slave SMBus interface may be used to override the function of some of the signals in the boot configuration vector during a fundamental reset. The signals that may be overridden are noted in Table 2.2. The state of all of the boot configuration signals in Table 2.2 sampled during the most recent cold reset may be determined by reading the PA_SWSTS register.

Signal	May Be Overridden	Description
CCLKDS	Y	Common Clock Downstream. When the CCLKDS pin is asserted, it indicates that a common clock is being used between the downstream device and the downstream port. This pin is used as the initial value of the Slot Clock Configuration bit in all of the Link Status Registers for downstream ports. The value may be overridden by modifying the SCLK bit in the PB_PCIELSTS or PC_PCIELSTS register.
CCLKUS	Y	Common Clock Upstream. When the CCLKUS pin is asserted, it indicates that a common clock is being used between the upstream device and the upstream port. This pin is used as the initial value of the Slot Clock Configuration bit in the Link Status Register for the upstream port. The value may be overridden by modifying the SCLK bit in the PA_PCIELSTS register.
MSMBSMODE	N	Master SMBus Slow Mode. The assertion of this pin indicates that the master SMBus should operate at 100 KHz instead of 400 kHz.

Table 2.2 Boot Configuration Vector Signals (Part 1 of 2)

Notes

Signal	May Be Overridden	Description
PEALREV	Y	PCI Express Port A Lane Reverse. When this pin is asserted, the lanes of PCI Express Port A are reversed. This value may be overridden by modifying the value of the PALREV bit in the PA_SWCTL register.
PEBLREV	Y	PCI Express Port B Lane Reverse. When this pin is asserted, the lanes of PCI Express Port B are reversed. This value may be overridden by modifying the value of the PBLREV bit in the PA_SWCTL register.
PECLREV	Y	PCI Express Port C Lane Reverse. When this pin is asserted, the lanes of PCI Express Port C are reversed. This value may be overridden by modifying the value of the PCLREV bit in the PA_SWCTL register.
REFCLKM	N	PCI Express Reference Clock Mode Select. These signals select the frequency of the reference clock input. 0x0 - 100 MHz 0x1 - 125 MHz
RSTHALT	Y	Reset Halt. When this signal is asserted during a PCI Express fundamental reset, the PES12NT3 executes the reset procedure and remains in a reset state with the Master and Slave SMBuses active. This allows software to read and write registers internal to the device before normal device operation begins. The device exits the reset state when the RSTHALT bit is cleared in the PA_SWCTL register through the SMBus. The value may be overridden by modifying the RSTHALT bit in the PA_SWCTL register.
SWMODE[3:0]	N	Switch Mode. These configuration pins determine the PES12NT3 switch operating mode. 0x0 - Reserved 0x1 - Reserved 0x2 - Non-transparent mode 0x3 - Non-transparent mode with serial EEPROM initialization 0x4 - Non-transparent failover mode 0x5 - Non-transparent failover mode with serial EEPROM initialization 0x6 through 0xF - Reserved

Table 2.2 Boot Configuration Vector Signals (Part 2 of 2)

Reset

PCI Express® defines two reset categories: fundamental reset and hot reset. A fundamental reset causes all associated logic to be returned to an initial state. A hot reset causes all associated logic to be returned to an initial state, but does not cause the state of register fields denoted as “sticky” to be modified.

There are two sub-categories of fundamental reset: cold reset and warm reset. A cold reset occurs following a device being powered on and assertion of PERSTN. A warm reset is a fundamental reset that occurs without removal of power.

A summary of reset conditions and their effect is exhibited in Table 2.3.

Notes

	Fund. Reset	Global Hot Reset to Entire Device	Global Hot Reset to Downstream Ports	Local Hot Reset	Ext. NTB Fund. Reset[1]	Ext. NTB Hot Reset
Master SMBus	Y	N	N	N	N	N
Slave SMBus	Y	N	N	N	N	N
Serial EEPROM Initial-ization	Y if mode requires it	N	N	N	N	N
Switch Core	Y	Y	N (flush buffer only)	N	N	N
Port A All Registers	Y	N	N	N	N	N
Port A All Registers Except Those of Type Sticky or RWL	Y	Y	N	N	N	N
Port A Transaction Layer	Y	Y	N	N	N	N
Port A Data Link Layer	Y	Y	N	N	N	N
Port A Phy Layer	Y	Y	N	N	N	N
Port B All Registers	Y	N	N	N	N	N
Port B All Registers Except Those of Type Sticky or RWL	Y	Y	Y	N	N	N
Port B Transaction Layer	Y	Y	Y	N	N	N
Port B Data Link Layer	Y	Y	Y	Y if selected	N	N
Port B Phy Layer	Y	Y	Y	Y if selected	N	N
Port B Downstream Hot Reset Req.	N	Y	Y	Y if selected	N	N
Port C All Registers	Y	N	N	N	N	N
Port C All Registers Except Those of Type Sticky or RWL	Y	Y	Y	N	N	N
Port C Transaction Layer	Y	Y	Y	N	N	N
Port C Data Link Layer	Y	Y (Y in NTB Mode)	Y (Y in NTB Mode)	Y if selected (Y in NTB Mode only if Port C is reset)	Y in NTB mode	Y in NTB mode

Table 2.3 Reset Conditions and Their Effect (Part 1 of 2)

Notes

	Fund. Reset	Global Hot Reset to Entire Device	Global Hot Reset to Downstream Ports	Local Hot Reset	Ext. NTB Fund. Reset[1]	Ext. NTB Hot Reset
Port C Phy Layer	Y	Y	Y	Y if selected (Y in NTB Mode only if Port C is reset)	Y in NTB mode	Y in NTB mode
Port C Downstream Hot Reset Req.	N	Y (N in NTB Mode)	Y (N in NTB Mode)	Y if selected (N in NTB mode)	N	N
NTB Internal Endpoint All Registers	Y	N	N	N	N	N
NTB Internal Endpoint All Registers Except Those of Type Sticky or RWL	Y	Y[2]	Y[2]	Y[2] only if port C reset	N	N
NTB External Endpoint All Registers	Y	N	N	N	Y[2]	N
NTB External Endpoint All Registers Except Those of Type Sticky or RWL	Y	Y[2]	Y[2]	Y[2] only if port C reset	Y[2]	Y[2]
PEBRSTN and/or PECRSTN asserted	N (tri-state)	Y (both) in transparent mode PECRSTN if selected by NTBROS field in NTB mode	Y (both) in transparent mode PECRSTN if selected by NTBROS field in NTB mode	Y (one) in transparent mode PECRSTN if NTB mode and if port C reset	PECRSTN if selected by NTBROS field in NTB mode	PECRSTN if selected by NTBROS field in NTB mode

Table 2.3 Reset Conditions and Their Effect (Part 2 of 2)

1. An External Fundamental reset in non-transparent mode with the PEFR bit set in either NTBCTL register is the same as a fundamental reset. See that column for its behavior.

2. All registers except those in the NTB configuration capability structure.

Notes

Fundamental Reset

A fundamental reset of the entire device may be initiated by one of five conditions:

- A cold reset initiated by a power-on and the assertion of the PCI Express Reset (PERSTN) input pin.
- A warm reset initiated by the assertion of the PCI Express Reset (PERSTN) input pin while power is on.
- A warm reset initiated by the writing of a one to the Reset (RST) bit in the Port A Switch Control (PA_SWCTL) register.
- A warm reset initiated by the writing of a one to the Reset (RST) bit in the Non-Transparent Bridge Control (NTBCTL) register of the internal side of the non-transparent bridge when the switch is in a non-transparent operating mode.
- A warm reset initiated by the writing of a one to the Reset (RST) bit in the Non-Transparent Bridge Control (NTBCTL) register of the external side of the non-transparent bridge when the switch is in a non-transparent operating mode.
- A warm reset initiated by the assertion of the non-transparent bridge fundamental reset (PENTBRSTN) signal when the device is configured to operate in non-transparent mode and the Propagate External Fundamental Reset (PEFR) bit is set in the NTBCTL register of the internal or external side of the non-transparent bridge.

The PCIe® standard specifies that normal operation should begin within 1.0 second after a fundamental reset of a device. The reset sequence above guarantees that normal operation will begin within this period as long as the serial EEPROM initialization process completes within 200 ms. Under normal circumstances, 200 ms is more than adequate to initialize every register in the device even with a Master SMBus operating frequency of 100 KHz.

Serial EEPROM initialization may cause writes to register fields that initiate side effects such as link retraining. These side effects are initiated at the point at which the write occurs. Therefore, serial EEPROM initialization should be structured in a manner so as to ensure proper configuration prior to initiation of these side effects.

The PES12NT3 provides a reset output signal for each downstream port implemented as a GPIO alternate function. The downstream port B reset output (PEBRSTN) signal is an alternate function of GPIO[0] and the downstream port C reset output (PECRSTN) signal is an alternate function of GPIO[1]. When a fundamental reset occurs, all of the GPIO pins default to GPIO inputs. Therefore, the downstream port resets are tri-stated. A system designer should use a pull-down on these signals if they are used as reset outputs.

Fundamental and hot resets in non-transparent mode are described in section Non-Transparent Mode Reset on page 2-9. The operation of a fundamental reset in Transparent mode with serial EEPROM initialization (i.e., SWMODE[3:0] = 0x1) is illustrated in Figure 2.5.

Notes

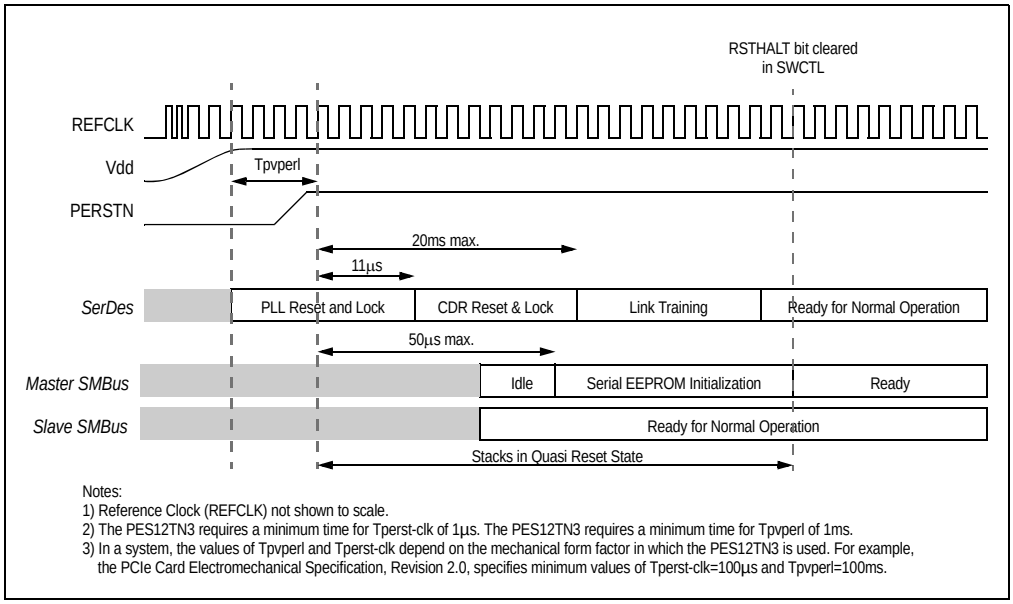

Figure 2.5 Fundamental Reset in Transparent Mode with Serial EEPROM initialization

Hot Reset

A hot reset may be initiated globally to the entire device, globally to downstream ports or locally to downstream port(s).

The PES12NT3 provides a reset output signal for each downstream port implemented as a GPIO alternate function. The downstream port B reset output (PEBRSTN) signal is an alternate function of GPIO[0] and the downstream port C reset output (PECRSTN) signal is an alternate function of GPIO[1]. When a hot reset occurs, the corresponding port reset output is asserted[1] for at least 250 ns. When a global hot reset occurs, all of the GPIO pins default to GPIO inputs. Therefore, the downstream port resets are tri-stated. A system designer should use a pull-down on these signals if they are used as reset outputs.

When the switch is configured for non-transparent operation, a hot reset may be initiated on the external side of the non-transparent bridge. Fundamental and hot resets in non-transparent mode are described in the Non-Transparent Mode Reset section.

Globally Initiated Hot Reset To Entire Device

A hot reset is initiated globally to the entire device when any of the following conditions occur.

- Reception of TS1 ordered-sets on the upstream port indicating a hot reset.
- Data link layer of the upstream port transitions to the DL_Down state.

Hot reset is only propagated downstream. TS1 ordered-sets indicating a hot reset received on a downstream port do not result in a hot reset of the downstream port or any function inside the switch.

When a globally initiated hot reset occurs, all of the logic associated with the transparent bridges, stacks and the switch core are reset except for the PLLs, SerDes, master SMBus interface, slave SMBus interface, and some registers. Regardless of the switch operating mode, a hot-reset does not result in reloading of the serial EEPROM. The value of register fields denoted as “sticky” or as Read and Write when Unlocked (i.e., RWL) are preserved in all ports across a hot-reset. All other register fields in all ports are reset to their initial values.

When a hot reset is initiated globally, each downstream port sends a hot-reset message to its link partner prior to being reset.

1. Since the PExRSTN signals are active low, the signal should be driven low for 250ns.

Notes

Globally Initiated Hot Reset To Downstream Ports

A hot reset is initiated globally to downstream ports when the following condition occurs:

– A one is written to the Secondary Bus Reset (SRESET) bit in the upstream port's (port A) Bridge Control Register (BCTRL).

When a globally initiated hot reset is initiated to downstream ports, all of the logic associated with the transparent bridges, stacks and FIFOs in the switch core associated with the downstream ports are reset except for the PLLs, SerDes, master SMBus interface, slave SMBus interface, and some registers. Regardless of the switch operating mode, it does not result in reloading of the serial EEPROM.

The value of register fields denoted as "sticky" or as Read and Write when Unlocked (i.e., RWL) in downstream ports are preserved. All other register fields are reset to their initial values.

When a hot reset is initiated globally to downstream ports, each downstream port sends a hot-reset message to its link partner prior to being reset. Unlike a globally initiated hot reset to the entire device, a globally initiated hot reset to downstream ports does not affect the state of the upstream port's configuration register except those required to update port status.

Locally Initiated Hot Reset to a Downstream Port

A hot reset is initiated locally to a downstream port by writing to the SRESET bit of a downstream port's BCTRL registers. When this occurs, a hot-reset message is sent on that port to its link partner. After the message is sent, the phy layer is effectively reset.

A locally initiated hot reset does not affect the state of any port (i.e., transparent bridge) configuration register except those required to update port status.

Non-Transparent Mode Reset

Fundamental and hot resets may be initiated on both the internal side and external sides of the non-transparent bridge. Associated with each side of the non-transparent bridge are control and status registers (NTBCTL and NTBSTS) that aid in the handling of hot and fundamental resets in non-transparent modes.

The Reset Action Enable (RAEN) bit in the PCIE_NTBCTL register together with the Reset Action (RA) field in that register allow a side (internal or external) of the non-transparent bridge to become "not ready" when a reset is detected on the opposite side of the non-transparent bridge. This allows a root on one side of the non-transparent bridge to configure the system before transactions are accepted on the opposite side of the non-transparent bridge.

Internal Side Fundamental Reset

In non-transparent mode, a fundamental reset from the internal side operates as described in Fundamental Reset on page 2-7. An internal side fundamental reset resets all logic in the device including both sides of the non-transparent bridge.

In addition to performing the actions outlined in that section, an internal side fundamental reset causes the Opposite Side Mode (OSMODE) field in the PCIE_NTBCTL register to be set to opposite side not ready. This disables accesses from the external side until the internal side root complex has configured the non-transparent bridge.

If a system designer wishes to have the external side root complex initialize the non-transparent bridge, then this can be achieved by initializing the state of the PCIE_NTBCTL and PCEE_NTBCTL registers via the serial EEPROM.

External Side Fundamental Reset

An external side fundamental reset is initiated when the switch is configured to operate in non-transparent mode and the PCI Express Non-Transparent Bridge Reset (PENTBRSTN) signal is asserted.

Assertion of the non-transparent bridge fundamental reset (PENTBRSTN) signal when the device is configured to operate in non-transparent mode and the Propagate External Fundamental Reset (PEFR) bit is set in the NTBCTL register of the internal or external side of the non-transparent bridge results in a funda-

Notes

mental reset of the entire device and behaves in the same manner as an internal side fundamental reset (see the Fundamental Reset on page 2-7). Otherwise, an external side fundament reset results in the following.

- The resetting of the transaction, data link and phy layers associated with the external side of the non-transparent bridge.
- The initialization of all registers associated with the external side of the non-transparent bridge are set to their initial values except those with a read and write when unlocked (RWL) attribute and those associated with the non-transparent bridge configuration capability structure.
- If the Reset Action Enable (RAEN) bit is set in the PCIE_NTBCTL register, then the action specified by the Reset Action (RA) field in that register is performed. This can result in the internal or external side of the non-transparent bridge becoming not ready and may be used by the system designer to block accesses until configuration of the non-transparent bridge has been performed by the internal or external root.
- The Opposite Side Reset Detected (OSRD) bit is set in the PCIE_INTSTS register and an interrupt or MSI is generated if enabled and selected by the PCIE_INTCTL0 register.
- The Opposite Side Fundamental Reset Detected (OSFRD) bit is set in the PCIE_NTBSTS register.
- The PES12NT3 provides a reset output signal for each downstream port implemented as a GPIO alternate function. The downstream port C reset output (PECRSTN) signal is an alternate function of GPIO[1]. When an external side fundamental reset occurs, the corresponding port reset output is asserted for at least 250 ns if the Non-Transparent Bridge Reset Output Select (NTBROS) field in the PA_SWCTL register is set to external reset. When an internal global hot reset occurs, all of the GPIO pins default to GPIO inputs. Therefore, the downstream port resets are tri-stated. A system designer should use a pull-down on these signals if they are used as reset outputs.

Internal Side Hot Reset

An internal side hot reset is initiated when any of the following conditions occur:

- Reception of TS1 ordered-sets on the upstream port indicating a hot reset.
- Data link layer of the upstream port transitions to the DL_Down state.
- A one is written to the Reset (RST) bit in the Port C Bridge Control Register (NTBCTL).
- A one is written to the Secondary Bus Reset (SRESET) bit in the upstream port's (port A) Bridge Control Register (BCTRL).

An internal side hot-reset results in the following:

- All of the logic associated with the internal and external sides of the non-transparent bridge is reset.
- The initialization of all registers associated with the internal and external sides of the non-transparent bridge to their initial values except those denoted as sticky, those with a read and write when unlocked (RWL) attribute, and those associated with the non-transparent bridge configuration capability structure.
- The Reset Action Enable (RAEN) bit and the Reset Action field in the PCEE_NTBCTL register are hardwired to zero since the external side of the NTB is also reset.
- The Opposite Side Reset Detected (OSRD) bit is set in the PCEE_INTSTS register. The OSRD bit is preserved across a hot reset since registers in the non-transparent bridge configuration capability structure are not reset.
- The Opposite Side Hot Reset Detected (OSHRD) bit is set in the PCEE_NTBSTS register. The OSHRD bit is sticky and thus preserved across a hot reset.
- The PES12NT3 provides a reset output signal for each downstream port implemented as a GPIO alternate function. The downstream port C reset output (PECRSTN) signal is an alternate function of GPIO[1]. When an internal side hot reset occurs, the corresponding port reset output is asserted[1] for 250ns.

External Side Hot Reset

An external side hot reset is initiated when the following condition occurs:

1. Since the PExRSTN signals are active low, the signal should be driven low for 250ns.

Notes

Reception of TS1 ordered-sets on the external side on the non-transparent bridge port indicating a hot reset.

The handling of an external side hot reset mirrors that of an external side fundament reset.

An external side hot-reset results in the following:

- All of the logic associated with the external side of the non-transparent bridge is reset except for the PLL and SerDes
- The initialization of all registers associated with the external side of the non-transparent bridge to their initial values except those denoted as sticky, those with a read and write when unlocked (RWL) attribute, sticky attribute, and those associated with the non-transparent bridge configuration capability structure.
- If the Reset Action Enable (RAEN) bit is set in the PCIE_NTBCTL register, then the action specified by the Reset Action (RA) field in that register is performed. This can result in the internal or external side of the non-transparent bridge becoming not ready and may be used by the system designer to block accesses until configuration of the non-transparent bridge has been performed by the internal or external root.
- The Opposite Side Reset Detected (OSRD) bit is set in the PCIE_INTSTS register and an interrupt or MSI is generated if enabled and selected by the PCIE_INTCTL0 register.
- The Opposite Side Hot Reset Detected (OSHRD) bit is set in the PCIE_NTBSTS register.
- The PES12NT3 provides a reset output signal for each downstream port implemented as a GPIO alternate function. The downstream port C reset output (PECRSTN) signal is an alternate function of GPIO[1]. When an external side hot reset occurs, the corresponding port reset output is asserted[1] for 250ns if the Non-Transparent Bridge Reset Output Select (NTBROS) field in the PA_SWCTL register is set to external reset.

1. Since the PECRSTN signals are active low, the signal should be driven low for 250ns.

Notes

Link Operation

Notes

Introduction

The PES12NT3 contains three ports. The default link width of each port is x4 and the SerDes lanes are statically assigned to a port.

Polarity Inversion

Each port of the PES12NT3 supports automatic polarity inversion as required by the PCIe® specification. Polarity inversion is a function of the receiver and not the transmitter. The transmitter never inverts its data. During link training, the receiver examines symbols six through 16 of the TS1 and TS2 ordered sets for inversion of the PExAP[n] and PExAN[n] signals. If an inversion is detected, then logic for the receiving lane automatically inverts received data.

Polarity inversion is a lane and not a link function. Therefore, it is possible for some lanes of link to be inverted and for others to not be inverted.

Link Width Negotiation

The PES12NT3 supports the option link variable width negotiation feature outlined in the PCIe specification. During link training, each of the x4 ports is capable of negotiating to a x4, x2 or x1 link width. The negotiated width of each link may be determined from the Link Width (LW) field in the corresponding port's PCI Express® Link Status (PCIELSTS) register.

The Maximum Link Width (MAXLNKWDTH) field in a port's PCI Express Link Capabilities (PCIELCAP) register contains the maximum link width of the port. This field is of RWL type and may be modified when the REGUNLOCK bit is set in the PA_SWCTL register. Modification of this field allows the maximum link width of the port to be configured. The new link width takes effect the next time link training occurs.

To force a link width to x2 despite a link partner's ability to negotiate to x4, the MAXLNKWDTH field could be configured through Serial EEPROM initialization and link retraining forced. Assuming the link partner has a link width greater than or equal to x2 and the capability to negotiate to a width of x2, the link width will negotiate to x2.

When a link negotiates to a width less than x4, the unused lanes are put in a low power state (i.e. L1 state).

Lane Reversal

The PCIe specification describes an optional lane reversal feature. The PES12NT3 does not support the automatic lane reversal feature outlined in the PCIe specification. However, it does support static lane reversal on a per port basis.

Associated with each PES12NT3 switch port is a lane reversal signal. The lane reversal signal for port A is PEALREV, for port B is PEBLREV, and port C is PECLREV. The status of the lane reversal signals sampled during a fundamental reset may be determined from the PALREV, PBLREV, and PCLREV fields in the PA_SWSTS register.

The port lane reversal signals are sampled during a fundamental reset and used as the initial value of the PALREV, PBLREV, and PCLREV fields in the PA_SWCTL register. When these bits are set, then the lanes of the corresponding port(s) are reversed during link training. Lane reversal mapping for the various non-trivial maximum link width configurations is illustrated in Figures 3.1 and 3.2.

Notes

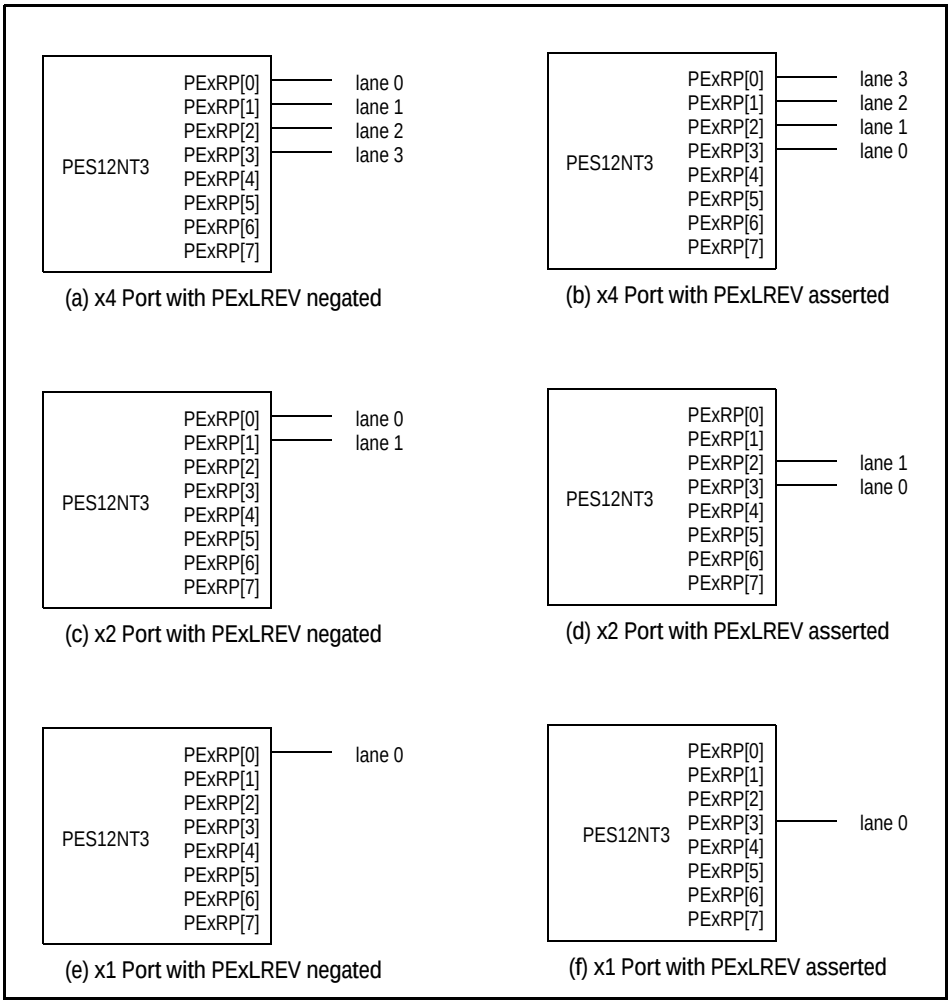

Figure 3.1 Lane Reversal for Maximum Link Width of x4

Notes

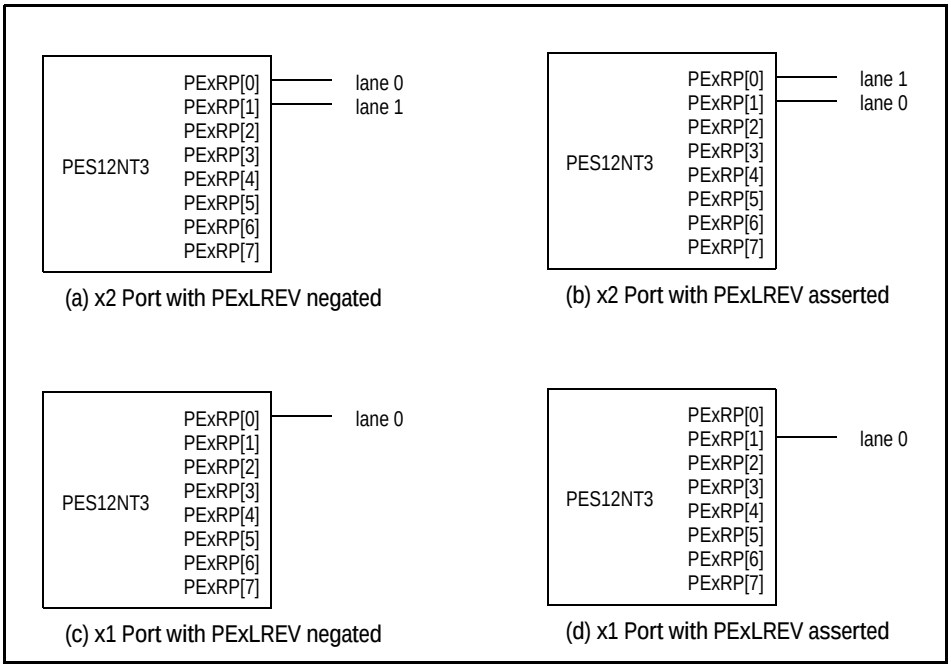

Figure 3.2 Lane Reversal for Maximum Link Width of x2

When link training occurs, the corresponding lane reversal bits in the PA_SWCTL register are examined. If a bit is set, then the lanes associated with that link are revered. This mechanism may be used to configure lane reversal via the serial EEPROM, slave SMBus, or root.

Link Retraining

Link retraining should not cause either a downstream component or an upstream component to reset or revert to default values.

Link Down

When a link goes down, all TLPs received by the port and queued in the switch are discarded and all TLPs received by other ports and destined to the port whose link is down are treated as Unsupported Requests (UR). While a link is down, it is possible to perform configuration read and write operations to the PCI-PCI bridge associated with the link. However, it is possible to lose configuration read or write completions when TLPs queued in the switch are discarded.[1] If this occurs, the root's completion timer associated with the transaction(s) will time-out and the transaction will be retired.

When a link comes up, flow control credits for the configured size of the IFB FIFOs are advertised.

Slot Power Limit Support

The Set_Slot_Power_Limit message is used to convey a slot power limit value from a downstream switch port (i.e., ports B or C) to the upstream port of a connected device or switch. A Set_Slot_Power_Limit message is set by downstream switch ports when either of the following events occurs:

- A configuration write is performed to the corresponding PCIESCAP register when the link associated with the downstream port is up.
- A link associated with the downstream port transitions from a non-operational state to an operational (i.e., up) state.

1. In the case of a configuration write that causes link retraining or a secondary bus reset, a completion corresponding to the configuration write is always returned and never lost.

Notes

Crosslink

Port A is an upstream port and only supports link training with a downstream port. Port B is a downstream port and only supports link training with an upstream port. Port C is an upstream port that supports crosslink operation. This allows port C to link train and operate with any standard PCIe upstream or downstream port. This feature enables the NTB port (i.e., port C) of two interconnected the PES12NT3 switches to link train and operate.

Link Status

Associated with each port is a Port Link Up (PxLINKUPN) status output. These outputs are provided on GPIO alternate functions. The PxLINKUPN status outputs may be used to provide a visual indication of system state, for error recovery or for debug. The PxLINKUPN output is asserted when the PCI Express data link layer is up (i.e., when the LTSSM is in the L0, L0s, L1 or recovery states). When the data link layer is down, this output is negated.

An interrupt may be generated by the external or internal NTB endpoints when a change occurs in link status of any of the switch ports. Change in switch port link status may be selectively reported as an interrupt (INTx or MSI) in the internal NTB domain, external NTB domain, or both.

Associated with each switch port are two status bits in the internal and external NTB endpoint INTSTS registers. When the data link layer associated with a switch port transitions from a DL_Down state to a DL_Up state, the corresponding PxLINKUP bit is set. When the data link layer associated with a switch port transitions from a DL_Up state to a DL_Down state, the corresponding PxLINKDN bit is set. The interrupt action (i.e., no action, INTx or MSI) taken when one of these bits is set is determined by the corresponding field in the associated NTB endpoint's INTCTL1 register.

Switch Operation

Notes

Introduction

The PES12NT3 utilizes an input buffered cut-through switch to forward PCIe® TLPs between switch ports. At a high level the switch may be viewed as consisting of three PCIe stacks and a switch core. The PCIe stacks are each responsible for performing the per port Phy, data link and transaction layer functions defined in the PCIe specification. The switch core is responsible for maintaining routing information in route map tables, maintaining per port ingress and egress flow control information, buffering TLPs, and forwarding TLPs between stacks.

An architectural block diagram of the PES12NT3 and switch core is provided in Figure 1.2 of Chapter 1. The buffering and data flow of the switch is graphically depicted in Figure 4.1 below.

Note that an ingress stack can transfer a TLP to its own egress stack through the switch core. This path is necessary since all transactions in the PES12NT3 are routed through the switch core, even those that could be satisfied locally, due to the fact that the switch core is responsible for maintaining flow control information.

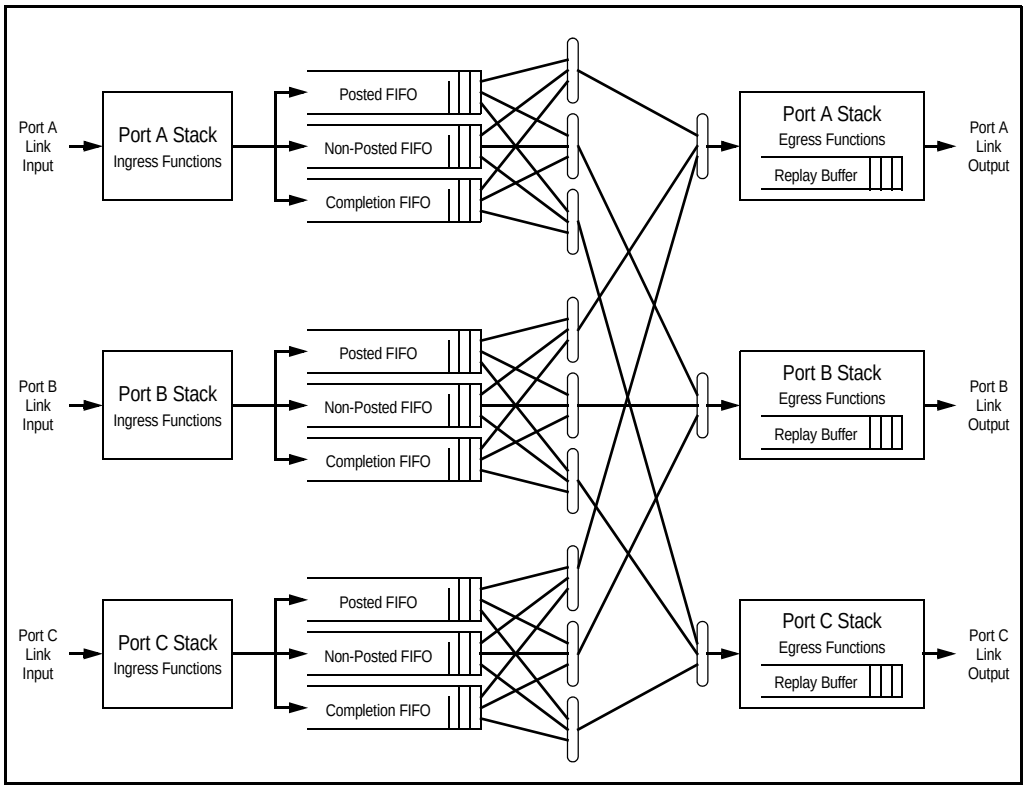

Figure 4.1 PES12NT3 Switch Data Flow and Buffering

TLPs are received by a port stack and passed to the switch core. Associated with each port in the switch core are three input buffers. One for posted transactions, one for non-posted transactions and one for completions. The size of each of these buffers is shown in Table 4.1. Associated with each TLP in a buffer is a descriptor. Thus, a buffer has a limitation on the total number of TLPs that can be stored as well as on the number of bytes.

Notes

Buffer	Size and Limitations
Posted FIFO	4 KB and up to 32 TLPs
Non-posted FIFO	1 KB and up to 32 TLPs
Completions FIFO	4 KB and up to 32 TLPs
Egress Stack Replay Buffer[1]	5120 bytes and up to 15 TLPs

Table 4.1 PES12NT3 Buffer Sizes

1. Stored with each TLP is a 32-bit LCRC as well as other information.

A flow control mechanism exists between the switch buffers and the transaction layer in the ingress stack to prevent overflows. This flow control mechanism forms the basis of the PCIe flow control credits advertised by the stack to the ingress port's link partner. When a TLP is sent to the switch core from an ingress stack, its header is looked-up in a routing map table and the TLP is queued in a buffer that corresponds to the TLP type (i.e., posted, non-posted or completion).

Scheduling of a TLP to be forwarded from an input buffer to an egress stack is performed by an egress scheduler and port arbiter associated with each egress stack. Thus, the PES12NT3 has three egress scheduler and three port arbiters. A flow control mechanism exists between the egress scheduler and the transaction layer in the egress stack. This flow control mechanism ensures that only TLPs which may be accepted by the egress stack's link partner are forwarded through the switch.

TLPs are routed in a cut-through manner through the PES12NT3 if the ingress link width is greater than or equal to the egress link width. If the ingress link width is less than the egress link width, then the entire TLP must be received before it is forwarded. The egress scheduler selects the TLP from each ingress port that may be forwarded to the associated egress port. If multiple ingress ports have TLPs which may be forwarded to the same egress port, the port scheduler selects the ingress port from which a TLP is forwarded.

Associated with each TLP in an input buffer is a timestamp. An egress scheduler always selects the TLP in the input buffer that contains the oldest timestamp. If that TLP is destined for a different egress port, then the egress scheduler makes no selection for that input port (i.e., TLPs are always forwarded from an ingress port in chronological order). TLP timestamps are also used to discard any TLP from the head of an input buffer that is more than 50 ms old. See section Switch Time-Outs on page 4-5 for additional details.

In making its selection, the egress scheduler considers the PCIe ordering rules. The PES12NT3 supports relaxed ordering for requests as well as completions. When the Disable Relaxed Ordering (DRO) bit is set in the port A Switch Control (SWCTL) register, the switch strongly orders all transactions regardless of the state of the relaxed ordering bit in TLPs.

The port scheduler associated with each egress port in the PES12NT3 supports hardwired round robin and weighted round robin with 32 phases. Both of these algorithms only arbitrate TLP requests and do not consider bandwidth consumption.

In addition to the input buffers in the switch core, each egress stack contains a replay FIFO. When the replay buffer fills, backpressure is provided to the switch core and no TLPs are forwarded to that egress port. Table 4.2 enumerates the default flow control credits advertised by each port of the switch core.

Notes

Flow Control Category	Default Advertised Credits	Notes
Posted Header	30 credits	Each credit represents 20 bytes (i.e., 5 doublewords) for a maximum of 600 bytes
Posted Data	204 credits	Each credit represents 16 bytes (i.e., 4 doublewords) for a maximum of 3264 bytes
Non-Posted Header	30 credits	Each credit represents 20 bytes (i.e., 5 doublewords) for a maximum of 600 bytes
Non-Posted Data	30 credits	Each credit represents 16 bytes (i.e., 4 doublewords) for a maximum of 480 bytes (note that non-posted data is assumed to consists of only one doubleword per header)
Completion Header	30 credits	Each credit represents 16 bytes (i.e., 4 doublewords) for a maximum of 480 bytes
Completion Data	204 credits	Each credit represents 16 bytes (i.e., 4 doublewords) for a maximum of 3264 bytes

Table 4.2 PES12NT3 Advertised Flow Control Credits

Each header credit is allocated 20 bytes (3 double doublewords) in a FIFO regardless of whether or not a credit represents 16 or 20 bytes. Each posted and completion data credit is allocated 16 bytes (2 double doublewords) in a FIFO. Non-posted data credits are allocated 8 bytes (one double doubleword). Two header and data credits are reserved in each FIFO for TLPs generated by the switch (e.g., configuration read completions).

The header and data flow control credits advertised may be configured on a per port basis via the Flow Control Credit Posted Configuration (FCPTCFG), Flow Control Credit Non-Posted Configuration (FCNPCFG) and Flow Control Credit Completion Configuration (FCCPCFG) registers. These registers may only be modified using the serial EEPROM or during initialization via the SMBus when the RSTHALT bit is set in the PA_SWCTL register. Modifying these registers in a running system produces undefined results.

Routing

The PES12NT3 supports routing of all transaction types defined in the PCIe specification. This includes routing using in specification defined transactions as well as those that may be used in vendor defined messages and in future revisions of the PCIe specifications.

Specifically, the PES12NT3 supports the following type of routing:

- Address routing with 32-bit or 64-bit format
- ID based routing using bus, device and function numbers.
- Implicit routing utilizing

  Route to root

  Broadcast from root

  Local - terminate at receiver

  Gathered and routed to root
- A summary of TLP types that use the above routing methods is provided in Table 4.3.

Notes

Routing Method	TLP Type Using Routing Method
Route by Address	MRd, MrdLk, MWr, IORd, IOWr, Msg, MsgD
ID Based Routing	CfgRd0, CfgWr0, CfgRd1, CfgWr1, Cpl, CpdD, CplLk, CplDLk, Msg, MsgD
Imlicit Routing - Route to Root	Msg, MsgD
Implicit Routing - Broadcast from Root[1]	Msg, MsgD
Implicit Routing - Local	Msg, MsgD
Implicit Routing - Gathered and Routed to Root	Only supported for PME_TO_Ack messages in response to a root initiated PME_Turn_Off message.

Table 4.3 Switch Routing Methods

1. Broadcast from root messages are only accepted from the root port (i.e., port A). An unsupported request is generated if a TLP with this routing method is received from any other port.

Data Integrity

PCI Express® provides reliable hop-by-hop communication between interconnected devices, such as roots, switches, and endpoints, by utilizing a 32-bit Link CRC (LCRC), sequence numbers, and a link level retransmission protocol. While this mechanism provides reliable communication between interconnected devices, it does not protect against corruption that may occur inside of a device. PCI Express defines an optional end-to-end data integrity mechanism that consists of appending a 32-bit end-to-end CRC (ECRC) computed at the source over the invariant fields of a Transaction Layer Packet (TLP) that is checked at the ultimate destination of the TLP. While this mechanism provides end-to-end error detection, unfortunately it is an optional PCI Express feature and has not been implemented in some North bridges and endpoints. In addition, the ECRC mechanism does not cover variant fields within a TLP.

Since deep sub-micron devices are known to be susceptible to single-event-upsets, a mechanism is desired that detects errors that occur within a PCI express switch. The PES12NT3 parity protects all TLPs in the switch, thus enabling corruption that may occur inside of the device to be detected and reported even in systems that do not implement ECRC.[1]

Associated with each port of the PES12NT3 is a PCI-PCI bridge. Located in the switch integrity region in extended configuration space of each PCI-PCI bridge are the Switch System Integrity Control (SWSICTL) and Switch System Integrity Parity Error Count (SWSIPECNT) registers. These registers provide control and status over switch errors associated with that switch port and may be read by a root or via the slave SMBus interface.

Data flowing into the PES12NT3 is protected by the LCRC. Within the Data Link (DL) layer of the switch ingress port, the LCRC is checked and 32-bit Doubleword (DWord) even parity is computed on the received TLP data. If an LCRC error is detected at this point, the link level retransmission protocol is used to recover from the error by forcing a retransmission by the link partner. As the TLP flows through the switch, its alignment or contents may be modified. In all such cases, parity is updated and not recomputed. Hence, any error that occurs is propagated and not masked by a parity regeneration. When the TLP reaches the DL layer of the switch egress port, parity is checked and in parallel a LCRC is computed. If the TLP is parity error free, then the LCRC and TLP contents are known to be correct and the LCRC is used to protect the packet through the lower portion of the DL layer, PHY layer, and link transmission.

If a parity error is detected by the DL layer of an egress port, then the TLP is nullified by inverting the computed LCRC and ending the packet with an EDB symbol. Nullified TLPs received by the link-partner are discarded. In addition to nullifying the TLP, the PES12NT3 performs the following when a parity error is detected: sends an error non-fatal (ERR_NONFATAL) message (if this message reporting is enabled) to the

1. Nullified TLPs are not parity protected and no parity errors are reported for nullified TLPs since these TLPs are discarded.

Notes

root; increments the End-to-End Parity Error Count (EEPERRC) field in the SWSIPECNT register associated with the port on which the error was detected; and sets the Detected Parity Error (DPE) bit in the PCISTS register if the error was detected by a downstream port or sets DPE bit in the PCI Secondary Status (SECSTS) register if the error was detected by an upstream port.

To prevent error flooding, error messages are not sent to the root once the EEPERRC field saturates. Since PCI Express switches do not normally generate ERR_NONFATAL messages, the Silent End-to-End Parity Checking bit (SEEPC) bit in the SWSICTL register is provided to disable generation of error messages and setting of the Detected Parity Error bit when internal corruption is detected.

The default state of the switch following a fundamental reset is to enable this error reporting. (Note that the Device Control register in the PCI Express capability structure also has a bit that enables generation of ERR_NONFATAL messages and that the default value of this bit is to disable these messages.)

In addition to TLPs that flow through the switch, cases exist in which TLPs are produced and consumed by the switch (e.g., a configuration requests and responses). Whenever a TLP is produced by the switch, parity is computed as the TLP is generated. Thus, error protection is provided on produced TLPs as they flow through the switch. In addition, parity is checked on all consumed TLPs. If an error is detected, the TLP is discarded and an error is reported using the mechanism described above.

This means that a parity error reported at a switch port cannot be definitively used to identify the location at which the error occurred as the error may have occurred when parity as generated at another port, in the switch core, or may have been generated locally (i.e., for ingress TLPs to the switch core which are consumed by the port such as Type 0 configuration read requests on the root port).

Switch Time-Outs

The switch discards any TLP that reaches the head of an input buffer and is more than 50ms old.

For non-posted and completion TLPs, the requester's completion time-out mechanism will detect discarded TLPs. No similar mechanism exists in PCIe for posted TLPs. Therefore, whenever a posted TLP is discarded by the switch due to a time-out, an error non-fatal (ERR_NONFATAL) message (if this message reporting is enabled) is sent to the root.

Whenever a TLP is discarded from a posted input buffer, the Posted TLP Time-out Count (PTLPTOC) field is incremented in the Switch System Integrity Time-Out Drop Count (SWSITDCNT) register in the port on which the TLP was received. This is a saturating counter that is automatically cleared when read. Whenever a TLP is discarded from a non-posted input buffer, the Non-Posted TLP Time-out Count (NPTLPTOC) field is incremented in this register and whenever a TLP is discarded from a completion input buffer, the Completion TLP Time-out Count (NPTLPTOC) field is incremented.

To prevent error flooding, error messages are not sent to the root once the PTLPTOC counter saturates. Since PCI Express switches do not normally generate ERR_NONFATAL messages, the Silent Posted TLP Time-out (SPTLPTO) bit in the SWSICTL register is provided to disable generation of error non-fatal messages. When this bit is set, ERR_NONFATAL messages are not generated when posted transactions received on the corresponding port are discarded. The PTLPTOC field however is always updated.

Interrupts

The PES12NT3 supports legacy PCI INTx emulation where x is A, B, C or D. Rather than use sideband INTx signals, PCIe defines two messages that indicate the assertion and negation of an interrupt signal. An Assert_INTx message is used to signal the assertion of an interrupt signal and an Deassert_INTx message is used to signal its negation.

The PES12NT3 maintains an aggregated INTx state for each of the four interrupt signals (i.e., A through D). The value of the INTA, INTB, INTC and INTD aggregated state may be determined by examining the corresponding fields in the PA_SWSTS register. The aggregated INTx state of each port for each of the four interrupt signals (i.e., A through D) on the primary side of its PCI to PCI bridge may be determined by examining the state of the INTA, INTB, INTC and INTD fields in the corresponding port's Interrupt Status (PA_INTSTS, PB_INTSTS, and PC_INTSTS) register.

Notes

An Assert_INTx message is sent to the root by the upstream port (i.e., port A), when the aggregated state of the corresponding interrupt in the switch transitions from a negated to an asserted state. A Deassert_INTx message is sent to the root by the upstream port when the aggregated state of the corresponding interrupt transitions from an asserted to a negated state.

Table 4.4 exhibits the interrupt sources that are aggregated by the switch.

PCI Compatible INTx	Interrupt Sources
INTA	- External downstream port B - External downstream port C - Non-transparent bridge internal endpoint
INTB	- External downstream port B - External downstream port C - Non-transparent bridge internal endpoint
INTC	- External downstream port B - External downstream port C - Non-transparent bridge internal endpoint
INTD	- External downstream port B - External downstream port C - Non-transparent bridge internal endpoint

Table 4.4 PCI Compatible INTx Aggregation

PCI to PCI bridges must map interrupts on the secondary side of the bridge according to the device number of the device on the secondary side of the bridge. No mapping is performed for the PCI to PCI bridges corresponding to downstream ports as these ports only connect to device zero. A mapping is performed for the upstream port (i.e., port A).This mapping is summarized in Table 4.6 for the PES12NT3.

Port A Interrupt	Interrupt Sources[1]
INTA	Port B INTA Port C INTD
INTB	Port B INTB Port C INTA
INTC	Port B INTC Port C INTB
INTD	Port B INTD Port C INTC

Table 4.5 PES12NT3 Upstream Port Bridge Interrupt Mapping

1. Port X INTy corresponds to external downstream generated INTy interrupts or INTy interrupts generated by the internal side of the non-transparent bridge (only for port C).

If a Downstream Port goes to DL_Down status, the INTx virtual wires associated with that port are deasserted, and the port A aggregates are updated accordingly. This may result in the upstream port generating a Deassert_Intx message.

Notes

Switch Core Errors

This section lists error conditions that are checked by the switch core. Due to limited buffering of Unsupported Request (UR) completions, it is possible for the PES12NT3 to discard UR completions if errors are generated faster than UR completions can be transmitted. Even when UR completions are discarded, error status bits are always correctly updated and an error message is generated.

Due to limited buffering, error messages may be collapsed if errors are generated faster than error messages can be transmitted. This means that multiple error conditions may result in only a single error message being generated. However, under no circumstances are error messages discarded.

Port arbitration should never be configured to starve a port. If a port arbitration table configuration results in port starvation, then TLPs generated by the port may be dropped (e.g., error messages, interrupts, configuration completions, etc.).

The following events received by the switch core from the upstream port are treated as Unsupported Requests (UR), and for non-posted transactions, result in a Unsupported Request (UR) completion being returned to the upstream port.

- Reception of a CfgRd0 or CfgWr0 TLP. All CfgRd0 and CfgWr0 TLPs should have been received and processed by the upstream stack. Therefore, the upstream stack should never pass a CfgRd0 or CfgWr0 to the switch core.
- Reception of a CfgRd1 or CfgWr1 TLP that is transformed into a CfgRd0 or CfgWr0 TLP destined to the link partner of a downstream port and in which the device number is non-zero (covers condition outlined in PCIe base 1.0a Section 7.3.1). The device number must be zero in CfgRd0 and CfgWr0 transactions to a downstream link partner.
- Reception of Msg or MsgD TLPs with route by address routing prior to initialization of the PCI-PCI bridge. Prior to initialization of the PCI-PCI bridge, no transactions should be routed to the switch core.
- Reception of route by address TLPs whose address matches an upstream port's memory or I/O base/limit pair and does not match a downstream ports' memory or I/O base/limit pair. TLPs that have no route (i.e., not destined for any upstream or downstream port) should be treated as unsupported requests.
- Reception of route by address TLPs destined to the upstream port. There are no route by address TLPs that should have been destined to the upstream port since the upstream port does not process these types of TLPs.
- Reception of TLPs that have no route (i.e., do not match an address or ID route through the switch). TLPs that have no route should be treated as unsupported requests.
- Reception of a TLP destined to a disabled downstream port (link down or MAE/IOAE bit cleared in PA_PCICMD register). TLPs destined to a disabled downstream port should be treated as unsupported requests.
- Reception of a TLP that matches a VGA region and the VGA Enable (VGAEN) bit is set in the upstream port but the TLP does not map to either downstream port (i.e., VGAEN is cleared in both downstream ports and the transaction does not map to any of the base/limit pairs associated with the downstream ports).

Notes

The following events received by the switch core from the downstream ports are treated as Unsupported Requests (UR) and for non-posted transactions, result in a Unsupported Request (UR) completion to be returned to the port on which the TLP was received.

- Reception of Msg or MsgD TLPs with route by address routing prior to initialization of the PCI-PCI bridge. Prior to initialization of the PCI-PCI bridge, no transactions should be routed to the switch core.
- Reception of Msg or MsgD TLPs with route by ID to the PCI-PCI bridge primary bus number after bus enumeration has completed. There are no entities that generate accept messages on the virtual PCI bus within the switch (i.e., the primary bus number).
- Reception of route by address TLPs whose address matches an upstream port's memory or I/O base/limit pair and does not match a downstream ports' memory or I/O base/limit pair. TLPs that have no route (i.e., not destined for any upstream or downstream port) should be treated as unsupported requests.
- Reception of TLPs that have no route (i.e., do not match an address or ID route through the switch). TLPs that have no route should be treated as unsupported requests.
- Reception of any configuration TLP. Configuration requests can only be generated by the root and received on the upstream port.
- Reception of a route by ID TLP to a port that has its primary bus number set to its secondary bus number. Such a port is uninitialized.
- Reception of a TLP that utilizes implicit routing - broadcast from root. Such a TLP can only be received by the upstream port.
- Reception of a TLP that matches a VGA region in a downstream port when the downstream port's VGA Enable (VGAEN) bit is set in its Bridge Control (BCTRL) register.
- Reception of a TLP destined to a disabled downstream port (link down or MAE/IOAE bit cleared in PCICMD register) or the upstream port when the Bus Master Enable (BME) bit is not set in the PCICMD register. TLPs destined to a disabled downstream port should be treated as unsupported requests.

Power Management

Notes

Introduction

A power management capability structure is located in the configuration space of each PCI-PCI bridge in the PES12NT3. The structure associated with a PCI-PCI bridge of a downstream port only affects that port. Entering the $D3_{hot}$ state allows the link associated with the bridge to enter the L1 state.

The power management capability structure associated with the root port (i.e., port A) affects the entire device. When the root port enters a low power state and the PME_TO_Ack messages are received, then the entire device is placed into a low power state. The PES12NT3 supports the following device power management states: D0 Uninitialized, D0 Active, $D3_{hot}$, and $D3_{cold}$. Transitioning a port's power management state from $D3_{hot}$ to $D0_{uninitialized}$ does not result in any logic being reset or re-initialization of register values.

A power management state transition diagram for the states supported by the PES12NT3 is provided in Figure 5.1 and described in Table 5.1.

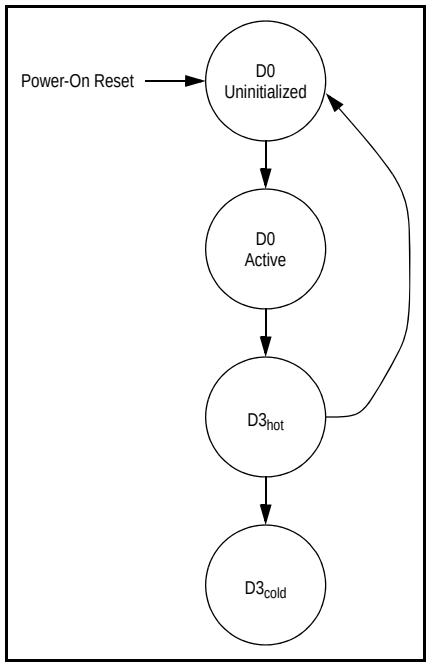

Figure 5.1 PES12NT3 Power Management State Transition Diagram

Notes

From State	To State	Description
Any	D0 Uninitialized	Power-on fundamental reset.
D0 Uninitialized	D0 Active	PCI-PCI bridge configured by software
D0 Active	$D3_{hot}$	The Power Management State (PMSTATE) field in the PCI Power Management Control and Status (PMCSR) register is written with the value that corresponds to the $D3_{hot}$ state.
$D3_{hot}$	D0 Uninitialized	The Power Management State (PMSTATE) field in the PCI Power Management Control and Status (PMCSR) register is written with the value that corresponds to D0 state.
$D3_{hot}$	$D3_{cold}$	Power is removed from the device.

Table 5.1 PES12NT3 Power Management State Transition Diagram

PME Messages

The PES12NT3 does not support generation of PME messages from the $D3_{cold}$ state. Downstream ports (i.e., PCI-PCI bridges associated with ports B and C) support the generation of hot-plug PME events (i.e., a PM_PME power management message) from the $D3_{hot}$ state. This includes both the case when the downstream port is in the $D3_{hot}$ state or the entire switch is in the $D3_{hot}$ state. The generation of a PME message by downstream ports necessitates the implementation of a PME service time-out mechanism to ensure that PME messages are not lost.

Link States

The PES12NT3 supports the following link states:

- L0 — Fully operational link state
- L0s — Automatically entered low power state with shortest exit latency
- L1 — (Port C does not support L1 ASPM).
  - Lower power state than L0s.
  - May be automatically entered or directed by software by placing the device in the $D3_{hot}$ state.
- L2/L3 Ready — The L2/L3 state is entered after the acknowledgement of a PM_Turn_Off Message. There is no TLP or DLLP communications over a link in this state.
- L3 — Link is completely unpowered and off.

Link states are shown in Figure 5.2.

Notes

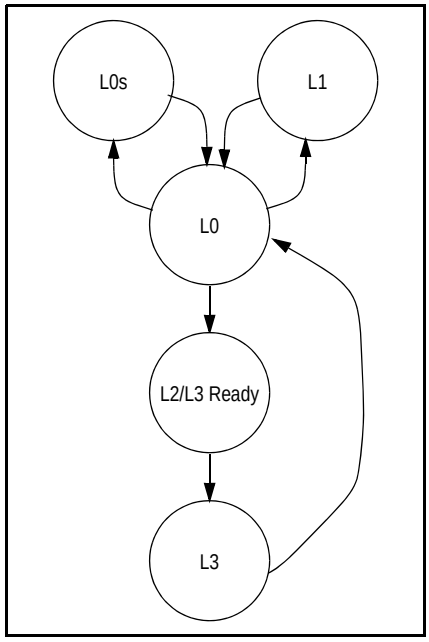

Figure 5.2 PES12NT3 ASPM Link Sate Transitions

Active State Power Management

The operation of Active State Power Management (ASPM) is orthogonal to power management. Once enabled by the ASPM field in the PCI Express® Link Control (PCIELCTL) register, ASPM link state transitions are initiated by hardware without software involvement. The PES12NT3 ASPM supports the required L0s state on all ports. The optional ASPM L1 is only supported on ports A and B.

Note: Port C, the non-transparent port, does not support L1 ASPM.

The L0s Entry Timer (L0SET) field in the PCI Power Management Proprietary Control (PMPC) register controls the amount of time L0s entry conditions must be met before the hardware transitions the link to the L0s state. The L1 Entry Timer (L1SET) field in the PCI Power Management Proprietary Control (PMPC) register controls the amount of time L1 entry conditions must be met before the hardware transitions the link to the L1 state. If these conditions are met and the link is in the L0 or L0s states, then the hardware will request a transition to the L1 state from its link partner. Note that L1 entry requests are only made by the PES12NT3 upstream port. If the link partner acknowledges the transition, then the L1 state is entered. Otherwise the L0s state is entered.

Notes

SMBus Interfaces

Notes

Introduction

The PES12NT3 contains two SMBus interfaces. The slave SMBus interface provides full access to all software visible registers in the PES12NT3, allowing every register in the device to be read or written by an external SMBus master. The slave SMBus may also be used to initialize the serial EEPROM used for initialization. The Master SMBus interface provides connection for an optional external serial EEPROM used for initialization and an optional I/O expander used for hot-plug signals.

Six pins make up each of the two SMBus interfaces. These pins consist of an SMBus clock pin, an SMBus data pin, and 4 SMBus address pins. As shown in Figure 6.1, the master and slave SMBuses may be used in a unified or split configuration.

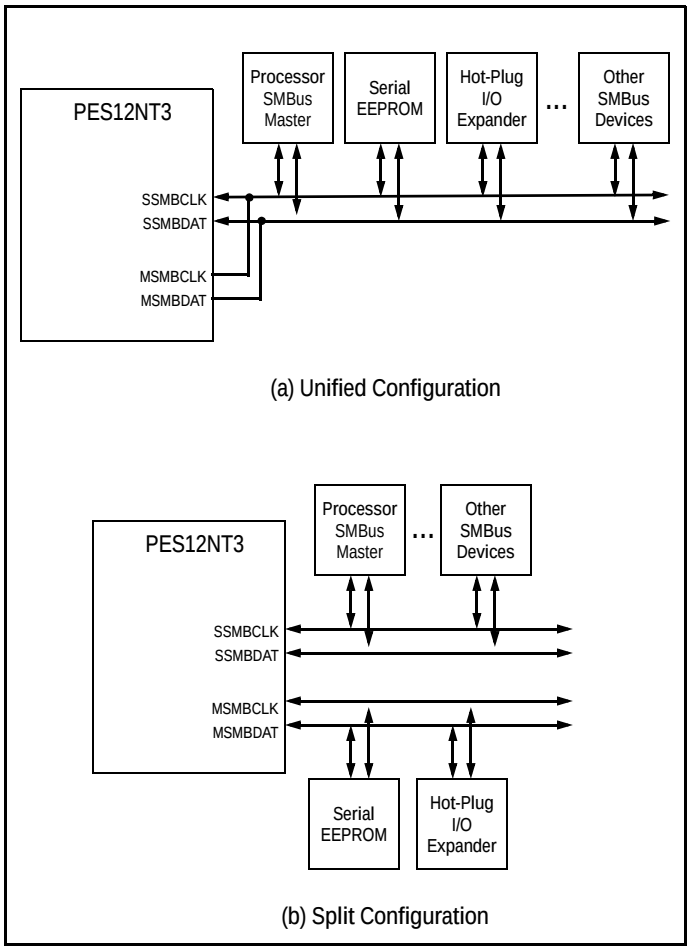

Figure 6.1 SMBus Interface Configuration Examples

In the unified configuration, shown in Figure 6.1(a), the master and slave SMBuses are tied together and the PES12NT3 acts both as an SMBus master as well as an SMBus slave on this bus. This requires that the external SMBus master or processor that has access to PES12NT3 registers support SMBus arbitra-

Notes

tion. In some systems, this external SMBus master interface may be implemented using general purpose I/O pins on a processor or microcontroller, and thus may not support SMBus arbitration. To support these systems, the PES12NT3 may be configured to operate in a split configuration as shown in Figure 6.1(b).

In the split configuration, the master and slave SMBuses operate as two independent buses and thus multi-master arbitration is not required.

SMBus Registers

Bit Field	Field Name	Type	Default Value	Description
0	Reserved	RO	0x0	Reserved field.
7:1	SSMBADDR	RO	HWINIT	Slave SMBus Address. This field contains the SMBus address assigned to the slave SMBus interface.
8	Reserved	RO	0x0	Reserved field.
15:9	MSMBADDR	RO	HWINIT	Master SMBus Address. This field contains the SMBus address assigned to the master SMBus interface.
23:16	Reserved	RO	0x0	Reserved field.
24	EEPROM-DONE	RO	0x0	Serial EEPROM Initialization Done. When the switch is configured to operate in a mode in which serial EEPROM initialization occurs during a fundamental reset, this bit is set when serial EEPROM initialization completes or when an error is detected.
25	NAERR	RW1C	0x0	No Acknowledge Error. This bit is set if an unexpected NACK is observed during a master SMBus transaction. The setting of this bit may indicate the following: that the addressed device does not exist on the SMBus (i.e., addressing error); data is unavailable or the device is busy; an invalid command was detected by the slave; or invalid data was detected by the slave.
26	LAERR	RW1C	0x0	Lost Arbitration Error. When the master SMBus interface loses arbitration for the SMBus, it automatically re-arbitrates for the SMBus. If the master SMBus interface loses 16 consecutive arbitration attempts, then the transaction is aborted and this bit is set.
27	OTHERERR	RW1C	0x0	Other Error. This bit is set if a misplaced START or STOP condition is detected by the master SMBus interface.
28	ICSERR	RW1C	0x0	Initialization Checksum Error. This bit is set if an invalid checksum is computed during Serial EEPROM initialization or when a configuration done command is not found in the serial EEPROM.
29	URIA	RW1C	0x0	Unmapped Register Initialization Attempt. This bit is set if an attempt is made to initialize via serial EEPROM a register that is not defined in the corresponding PCI configuration space.
31:30	Reserved	RO	0x0	Reserved field.

Table 6.1 SMBUSSTS - SMBus Status

Notes

Bit Field	Field Name	Type	Default Value	Description
15:0	MSMBCP	RW	HWINIT	Master SMBus Clock Prescalar. This field contains a clock prescalar value used during master SMBus transactions. The prescalar clock period is equal to 32 ns multiplied by the value in this field. When the field is cleared to zero or one, the clock is stopped. The initial value of this field is 0x0139 when the master SMBus is configured to operate in slow mode (i.e., 100 KHz) in the boot configuration and to 0x0053[1] when it is configured to operate in fast mode (i.e., 400 KHz).
16	MSMBIOM	RW	0x0	Master SMBus Ignore Other Masters. When this bit is set, the master SMBus proceeds with transactions regardless of whether it won or lost arbitration.
17	ICHECKSUM	RW	0x0	Ignore Checksum Errors. When this bit is set, serial EEPROM initialization checksum errors are ignored (i.e., the checksum always passes).
19:18	SSMBMODE	RW	0x0	Slave SMBus Mode. The slave SMBus contains internal glitch counters on the SSMBCLK and SSMBDAT signals that wait approximately 1 µS before sampling or driving these signals. This field allows the glitch counter time to be reduced or entirely removed. In some systems, this may permit high speed slave SMBus operation. 0x0 - (normal) Slave SMBus normal mode. Glitch counters operate with 1 µS delay. 0x1 - (fast) Slave SMBus interface fast mode. Glitch counters operate with 100 nS delay. 0x2 - (disabled) Slave SMBus interface with glitch counters disabled. Glitch counters operate with zero delay which effectively removes them. 0x3 - reserved.
21:20	MSMBMODE	RW	0x0	Master SMBus Mode. The master SMBus contains internal glitch counters on the MSMBCLK and MSMBDAT signals that wait approximately 1 µS before sampling or driving these signals. This field allows the glitch counter time to be reduced or entirely removed. In some systems, this may permit high speed master SMBus operation. 0x0 - (normal) Master SMBus normal mode. Glitch counters operate with 1 µS delay. 0x1 - (fast) Master SMBus interface fast mode. Glitch counters operate with 100 nS delay. 0x2 - (disabled) Master SMBus interface with glitch counters disabled. Glitch counters operate with zero delay which effectively removes them. 0x3 - reserved.
31:22	Reserved	RO	0x0	Reserved field.

Table 6.2 SMBUSCTL - SMBus Control

1. The MSMBCLK low minimum pulse width is equal to half the period programmed in this field. The value of 0x53, which corresponds to ~373 KHz, allows the min low pulse width to be satisfied. In systems where this timing parameter is not critical, the operating frequency may be increased.

Notes

Master SMBus Interface

The master SMBus interface is used during a fundamental reset to load configuration values from an optional serial EEPROM. It is also used to support an optional I/O expander for hot-plug signals.

Initialization

Master SMBus initialization occurs during a fundamental reset (see Fundamental Reset on page 2-6).

During a fundamental reset initialization sequence, the state of the Master SMBus Slow Mode (MSMBSMODE) signal is examined. If this signal is asserted, then the Master SMBus Clock Prescalar (MSMBCP) field in the port A SMBus Control (PA_SMBUSCTL) register is initialized to support 100 KHz SMBus operation. If the signal is negated, then the MSMBCP field is initialized for 400 KHz SMBus operation.

Serial EEPROM

During a fundamental reset, an optional serial EEPROM may be used to initialize any software visible register in the device.

Serial EEPROM loading occurs if the Switch Mode (SWMODE[3:0]) field selects an operating mode that performs serial EEPROM initialization (e.g., transparent mode with serial EEPROM initialization).

The address used by the SMBus interface to access the serial EEPROM is specified by the MSMBADDR[4:1] signals as shown in Table 6.3.

Address Bit	Address Bit Value
1	MSMBADDR[1]
2	MSMBADDR[2]
3	MSMBADDR[3]
4	MSMBADDR[4]
5	1
6	0
7	1

Table 6.3 Serial EEPROM SMBus Address

Device Initialization from a Serial EEPROM

During initialization from the optional serial EEPROM, the master SMBus interface reads configuration blocks from the serial EEPROM and updates corresponding registers in the PES12NT3.

Any PES12NT3 software visible register in the upstream port or downstream port(s) may be initialized with values stored in the serial EEPROM.

Each software visible register in the PES12NT3 has a CSR system address which is formed by adding the PCI configuration space offset value of the register to the base address of the configuration space in which the register is located. Configuration blocks stored in the serial EEPROM use this CSR system address shifted right two bits (i.e., configuration blocks in the serial EEPROM use doubleword CSR system addresses and not byte CSR system addresses). Base addresses for the PCI configuration spaces in the PES12NT3 are listed in Table 6.4.

Notes

PCI Configuration Space	Base Address Value used to form CSR System Address
Upstream Port A	0x0000
Downstream Port B	0x1000
Downstream Port C	0x2000
Internal Non-Transparent Bridge Endpoint	0x3000
External Non-Transparent Bridge Endpoint	0x3800

Table 6.4 Base Addresses for PCI Configuration Spaces in the PES12NT3

Since configuration blocks are used to store only the value of those registers that are initialized, a serial EEPROM much smaller than the total size of all of the configuration spaces may be used to initialize the device.

Any serial EEPROM compatible with those listed in Table 6.5 may be used to store PES12NT3 initialization values. Some of these devices are larger than the total size of all of the PCI configuration spaces in the PES12NT3 that may be initialized and thus may not be fully utilized.

Serial EEPROM	Size
24C32	4 KB
24C64	8 KB
24C128	16 KB
24C256	32 KB
24C512	64 KB

Table 6.5 PES12NT3 Compatible Serial EEPROMs

During serial EEPROM initialization, the master SMBus interface begins reading bytes starting at serial EEPROM address zero. These bytes are interpreted as configuration blocks and sequential reading of the serial EEPROM continues until the end of a configuration done block is reached or the serial EEPROM address rolls over from 0xFFFF to 0x0.

All register initialization performed by the serial EEPROM is performed in double word quantities. There are three configuration block types that may be stored in the serial EEPROM. The first type is a single double word initialization sequence. A double word initialization sequence occupies six byes in the serial EEPROM and is used to initialize a single double word quantity in the PES12NT3.

A single double word initialization sequence consists of three fields and its format is shown in Figure 6.2. The CSR_SYSADDR field contains the double word CSR system address of the double word to be initialized. The actual CSR system address, which is a byte address, equals this value with two lower zero bits appended. The next field is the TYPE field that indicates the type of the configuration block. For single double word initialization sequence, this value is always 0x0. The final DATA field contains the double word initialization value.

Notes

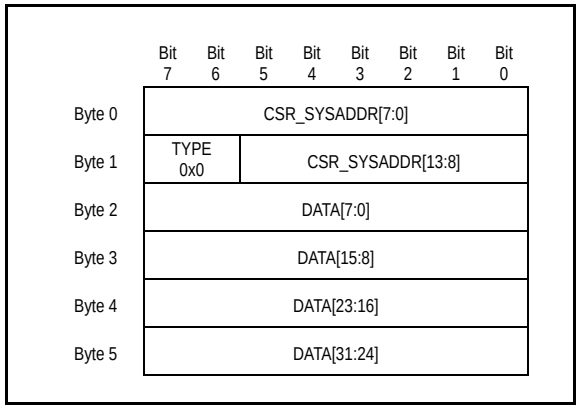

Figure 6.2 Single Double Word Initialization Sequence Format

The second type of configuration block is the sequential double word initialization sequence. It is similar to a single double word initialization sequence except that it contains a double word count that allows multiple sequential double words to be initialized in one configuration block.

A sequential double word initialization sequence consists of four required fields and one to 65535 double word initialization data fields. The format of a sequential double word initialization sequence is shown in Figure 6.3. The CSR_SYSADDR field contains the starting double word CSR system address to be initialized. The next field is the TYPE field that indicates the type of the configuration block. For sequential double word initialization sequences, this value is always 0x1. The NUMDW field specifies the number of double words initialized by the configuration block. This is followed by the number of DATA fields specified in the NUMDW field.

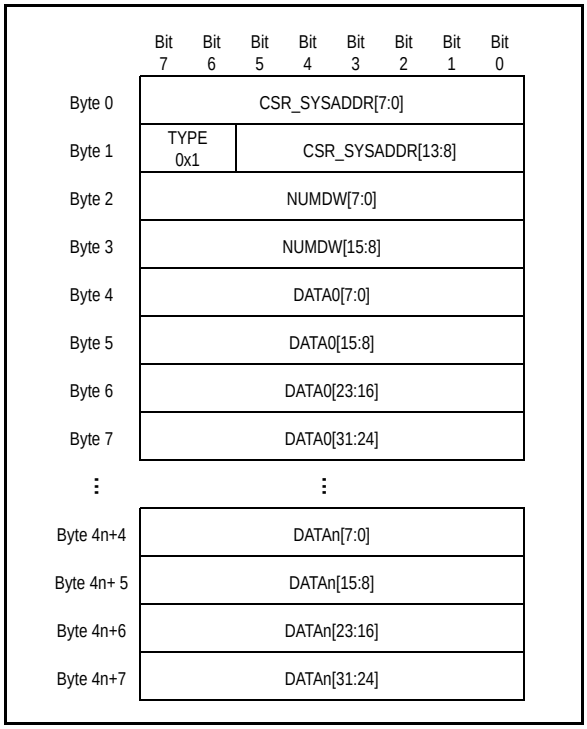

Figure 6.3 Sequential Double Word Initialization Sequence Format

The final type of configuration block is the configuration done sequence which is used to signify the end of a serial EEPROM initialization sequence.

Notes

If during serial EEPROM initialization, an attempt is made to initialize a register that is not defined in a configuration space (i.e., does not appear in Tables 9.6 through 9.10), then the Unmapped Register Initialization Attempt (URIA) bit is set in the SMBUSSTS register and the write is ignored.

The configuration done sequence consists of two fields and its format is shown in Figure 6.4. The CHECKSUM field contains the checksum of all of the bytes in all of the fields read from the serial EEPROM from the first configuration block to the end of this done sequence. The second field is the TYPE field which is always 0x3 for configuration done sequences.

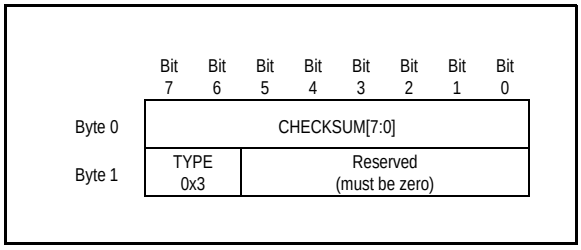

Figure 6.4 Configuration Done Sequence Format

The checksum in the configuration done sequence enables the integrity of the serial EEPROM initialization to be verified. Since uninitialized EEPROMs typically have a value of all ones, initialization from an uninitialized serial EEPROM will result in a checksum mismatch.

The checksum is computed in the following manner.An 8-bit counter is initialized to zero and the 8-bit sum is computed over the configuration bytes stored in the serial EEPROM, including the entire contents of the configuration done sequence, with the checksum field initialized to zero.[1] The 1's complement of this sum is placed in the checksum field.

The checksum is verified in the following manner. An 8-bit counter is cleared and the 8-bit sum is computed over the bytes read from the serial EEPROM, including the entire contents of the configuration done sequence.[2] The correct result should always be 0xFF (i.e., all ones). Checksum checking may be disabled by setting the Ignore Checksum Errors (ICHECKSUM) bit in the port A SMBus Control (PA_SMBUSCTL) register.

If an error is detected during loading of the serial EEPROM, then loading of the serial EEPROM is aborted and the RSTHALT bit is set in the PA_SWCTL register. This allows debugging of the error condition via the slave SMBus interface but prevents normal system operation with a potentially incorrectly initialized device. Error information is recorded in the PA_SMBUSSTS register. Once serial EEPROM initialization completes, or when an error is detected, the EEPROM Done (EEPROMDONE) bit is set in the port A SMBus Status (PA_SMBSTS) register.

A summary of possible errors during serial EEPROM initialization and specific action taken when detected is summarized in Table 6.6.

1. This includes the byte containing the TYPE field.

2. This includes the checksum byte as well as the byte that contains the type and reserved field.

Notes

Error	Action Taken
Configuration Done Sequence checksum mismatch with that computed by the PES12NT3	- Set RSTHALT bit in PA_SWCTL register - ICSERR bit is set in the PA_SMBUSSTS register - Abort initialization, set DONE bit in the PA_SMBUSSTS register
Serial EERPOM address roll-over from 0xFFFF to 0x0000	- Set RSTHALT bit in PA_SWCTL register - ICSERR bit is set in the PA_SMBUSSTS register - Abort initialization, set DONE bit in the PA_SMBUSSTS register
Invalid configuration block type (only invalid type is 0x2)	- Set RSTHALT bit in PA_SWCTL register - ICSERR bit is set in the PA_SMBUSSTS register - Abort initialization, set DONE bit in the PA_SMBUSSTS register
An unexpected NACK is observed during a master SMBus transaction	- Set RSTHALT bit in PA_SWCTL register - NAERR bit is set in the PA_SMBUSSTS register - Abort initialization, set DONE bit in the PA_SMBUSSTS register
Master SMBus interface loses 16 consecutive arbitration attempts	- Set RSTHALT bit in PA_SWCTL register - LAERR bit is set in the PA_SMBUSSTS register - Abort initialization, set DONE bit in the PA_SMBUSSTS register
A misplaced START or STOP condition is detected by the master SMBus interface	- Set RSTHALT bit in PA_SWCTL register - OTHERERR bit is set in the PA_SMBUSSTS register - Abort initialization, set DONE bit in the PA_SMBUSSTS register

Table 6.6 Serial EEPROM Initialization Errors

Programming the Serial EEPROM

The serial EEPROM may be programmed prior to board assembly or in-system via the slave SMBus interface or a PCIe® root. Programming the serial EEPROM via the slave SMBus is described in section Serial EEPROM Read or Write Operation on page 6-12. A PCIe root may read and write the serial EEPROM by performing configuration read and write transactions to the port A Serial EEPROM Interface (PA_EEPROMINTF) register.

To read a byte from the serial EEPROM, the root should configure the Address (ADDR) field in the PA_EEPROMINTF register with the byte address of the serial EEPROM location to be read and the Operation (OP) field to “read.” The Busy (BUSY) bit should then be checked. If the EEPROM is not busy, then the read operation may be initiated by performing a write to the Data (DATA) field. When the serial EEPROM read operation completes, the Done (DONE) bit in the PA_EEPROMINTF register is set and the busy bit is cleared. When this occurs, the DATA field contains the byte data of the value read from the serial EEPROM.

To write a byte to the serial EEPROM, the root should configure the ADDR field with the byte address of the serial EEPROM location to be written and set the OP field to “write.” If the serial EEPROM is not busy (i.e., the BUSY bit is cleared), then the write operation may be initiated by writing the value to be written to the DATA field. When the write operation completes, the DONE bit is set and the busy bit is cleared.

Initiating a serial EEPROM read or write operation when the BUSY bit is set produces undefined results. SMBus errors may occur when accessing the serial EEPROM. If an error occurs, then it is reported in the port A SMBus Status (PA_SMBUSSTS) register. Software should check for errors before and after each serial EEPROM access.

Hot-Plug I/O Expander

The PES12NT3 utilizes an external SMBus/I2C-bus I/O expander connected to the master SMBus interface for hot-plug related signals associated with downstream ports. See section Hot-Plug I/O Expander on page 6-3 for information on the operation of the hot-plug I/O expander.

Notes

Slave SMBus Interface

The slave SMBus interface provides the PES12NT3 with a configuration, management and debug interface. Using the slave SMBus interface, an external master can read or write any software visible register in the device.

Initialization

Slave SMBus initialization occurs during a fundamental reset (see Fundamental Reset on page 2-6). During the fundamental reset initialization sequence, the address is specified by the SSMBADDR[5,3:1] signals as shown in Table 6.7.

Address Bit	Address Bit Value
1	SSMBADDR[1]
2	SSMBADDR[2]
3	SSMBADDR[3]
4	0
5	SSMBADDR[5]
6	1
7	1

Table 6.7 Slave SMBus Address When a Static Address is Selected.

SMBus Transactions

The slave SMBus interface responds to the following SMBus transactions initiated by an SMBus master. See the SMBus 2.0 specification for a detailed description of these transactions.

- Byte and Word Write/Read
- Block Write/Read

Initiation of any SMBus transaction other than those listed above to the slave SMBus interface produces undefined results.

Associated with each of the above transactions is a command code. The command code format for operations supported by the slave SMBus interface is shown in Figure 6.5 and described in Table 6.8.

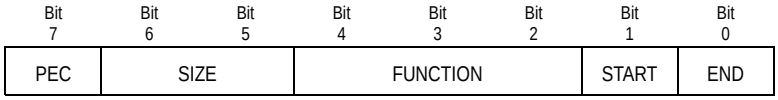

Figure 6.5 Slave SMBus Command Code Format

Notes

Bit Field	Name	Description
0	END	End of transaction indicator. Setting both START and END signifies a single transaction sequence 0 - Current transaction is not the last read or write sequence. 1 - Current transaction is the last read or write sequence.
1	START	Start of transaction indicator. Setting both START and END signifies a single transaction sequence 0 - Current transaction is not the first of a read or write sequence. 1 - Current transaction is the first of a read or write sequence.
4:2	FUNCTION	This field encodes the type of SMBus operation. 0 - CSR register read or write operation 1 - Serial EEPROM read or write operation 2 through 7 - Reserved
6:5	SIZE	This field encodes the data size of the SMBus transaction. 0 - Byte 1 - Word 2 - Block 3 - Reserved
7	PEC	This bit controls whether packet error checking is enabled for the current SMBus transaction. 0 - Packet error checking disabled for the current SMBus transaction. 1 - Packet error checking enabled for the current SMBus transaction.

Table 6.8 Slave SMBus Command Code Fields

The FUNCTION field in the command code indicates if the SMBus operation is a CSR register read/write or a serial EEPROM read/write operation. Since the format of these transactions is different. They will be described individually in the following sections.

If a command is issued while one is already in progress or if the slave is unable to supply data associated with a command, then the command is NACKed. This indicates to the master that the transaction should be retried.

CSR Register Read or Write Operation

Table 6.9 indicates the sequence of data as it is presented on the slave SMBus following the byte address of the Slave SMBus interface.

Notes

Byte Position	Field Name	Description
0	CCODE	**Command Code.** Slave Command Code field described in Table 6.8.
1	BYTCNT	**Byte Count.** The byte count field is only transmitted for block type SMBus transactions. SMBus word and byte accesses do not contain this field. The byte count field indicates the number of bytes following the byte count field when performing a write or setting up for a read. The byte count field is also used when returning data to indicate the number of following bytes (including status). *Note that the byte count field does not include the PEC byte if PEC is enabled.*
2	CMD	**Command.** This field encodes fields related to the CSR register read or write operation.
3	ADDRL	**Address Low.** Lower 8-bits of the doubleword CSR system address of register to access.
4	ADDRU	**Address Upper.** Upper 6-bits of the doubleword CSR system address of register to access. Bits 6 and 7 in the byte must be zero and are ignored by the hardware.
5	DATALL	**Data Low Low.** Bits [7:0] of data doubleword.
6	DATALM	**Data Low Middle.** Bits [15:8] of data doubleword.
7	DATAUM	**Data Upper Middle.** Bits [23:16] of data doubleword.
8	DATAUU	**Data Upper Upper.** Bits [31:24] of data doubleword.

Table 6.9 CSR Register Read or Write Operation Byte Sequence

The format of the CMD field is shown in Figure 6.6 and described in Table 6.10.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WERR	RERR	0	OP	BEUU	BEUM	BELM	BELL

Figure 6.6 CSR Register Read or Write CMD Field Format

Bit Field	Name	Type	Description
0	BELL	Read/Write	**Byte Enable Lower Lower.** When set, the byte enable for bits [7:0] of the data word is enabled.
1	BELM	Read/Write	**Byte Enable Lower Middle.** When set, the byte enable for bits [15:8] of the data word is enabled.
2	BEUM	Read/Write	**Byte Enable Upper Middle.** When set, the byte enable for bits [23:16] of the data word is enabled.
3	BEUU	Read/Write	**Byte Enable Upper Upper.** When set, the byte enable for bits [31:24] of the data word is enabled.

Table 6.10 CSR Register Read or Write CMD Field Description (Part 1 of 2)

Notes

Bit Field	Name	Type	Description
4	OP	Read/Write	CSR Operation. This field encodes the CSR operation to be performed. 0 - CSR write 1 - CSR read
5	0	0	Reserved. Must be zero
6	RERR	Read-Only and Clear	Read Error. This bit is set if the last CSR read SMBus transaction was not claimed by a device. Success indicates that the transaction was claimed and not that the operation completed without error.
7	WERR	Read-Only and Clear	Write Error. This bit is set if the last CSR write SMBus transaction was not claimed by a device. Success indicates that the transaction was claimed and not that the operation completed without error.

Table 6.10 CSR Register Read or Write CMD Field Description (Part 2 of 2)

Serial EEPROM Read or Write Operation

Table 6.11 indicates the sequence of data as it is presented on the slave SMBus following the byte address of the Slave SMBus interface.

Byte Position	Field Name	Description
0	CCODE	Command Code. Slave Command Code field described in Table 6.8.
1	BYTCNT	Byte Count. The byte count field is only transmitted for block type SMBus transactions. SMBus word and byte accesses do not contain this field. The byte count field indicates the number of bytes following the byte count field when performing a write or setting up for a read. The byte count field is also used when returning data to indicate the number of following bytes (including status).
2	CMD	Command. This field contains information related to the serial EEPROM transaction
3	EEADDR	Serial EEPROM Address. This field specifies the address of the Serial EEPROM on the Master SMBus when the USA bit is set in the CMD field. Bit zero must be zero and thus the 7-bit address must be left-justified.
4	ADDRL	Address Low. Lower 8-bits of the Serial EEPROM byte to access.
5	ADDRU	Address Upper. Upper 8-bits of the Serial EEPROM byte to access.
6	DATA	Data. Serial EEPROM value read or to be written.

Table 6.11 Serial EEPROM Read or Write Operation Byte Sequence

The format of the CMD field is shown in Figure 6.7 and described in Table 6.12

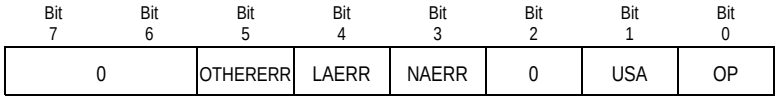

Figure 6.7 Serial EEPROM Read or Write CMD Field Format

Notes

Bit Field	Name	Type[1]	Description
0	OP	RW	Serial EEPROM Operation. This field encodes the serial EEPROM operation to be performed. 0 - Serial EEPROM write 1 - Serial EEPROM read
1	USA	RW	Use Specified Address. When this bit is set the serial EEPROM SMBus address specified in the EEADDR is used instead of that specified in the MSMBADDR field in the SMBUSSTS register.
2	Reserved		
3	NAERR	RC	No Acknowledge Error. This bit is set if an unexpected NACK is observed during a master SMBus transaction when accessing the serial EEPROM. This bit has the same function as the NAERR bit in the PA_SMBUSSTS register. The setting of this bit may indicate the following: that the addressed device does not exist on the SMBus (i.e., addressing error), data is unavailable or the device is busy, an invalid command was detected by the slave, invalid data was detected by the slave.
4	LAERR	RC	Lost Arbitration Error. This bit is set if the master SMBus interface loses 16 consecutive arbitration attempts when accessing the serial EEPROM. This bit has the same function as the LAERR bit in the PA_SMBUSSTS register.
5	OTHERERR	RC	Other Error. This bit is set if a misplaced START or STOP condition is detected by the master SMBus interface when accessing the serial EEPROM. This bit has the same function as the OTHERERR bit in the PA_SMBUSSTS register.
7:6	Reserved	0	Reserved. Must be zero

Table 6.12 Serial EEPROM Read or Write CMD Field Description

1. See Table 2 in About This Manual for a definition of these abbreviations.

Sample Slave SMBus Operation

This section illustrates sample Slave SMBus operations. Shaded items are driven by the PES12NT3's slave SMBus interface and non-shaded items are driven by an SMBus host.

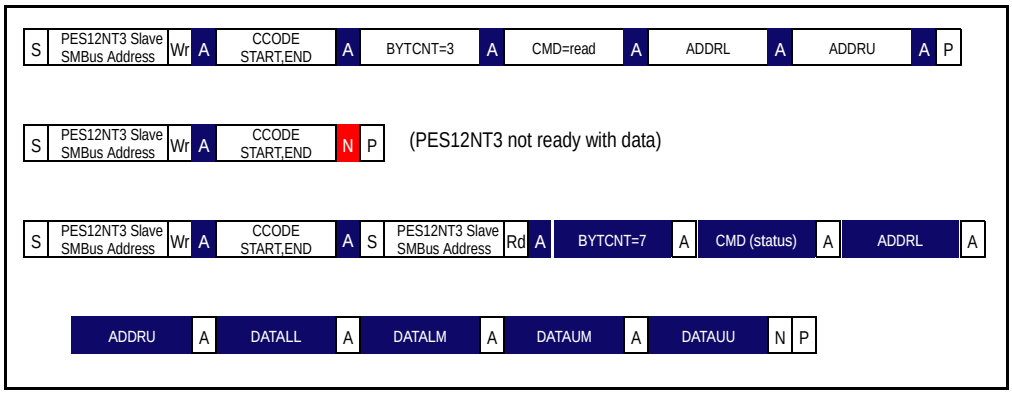

Figure 6.8 CSR Register Read Using SMBus Block Write/Read Transactions with PEC Disabled

Notes

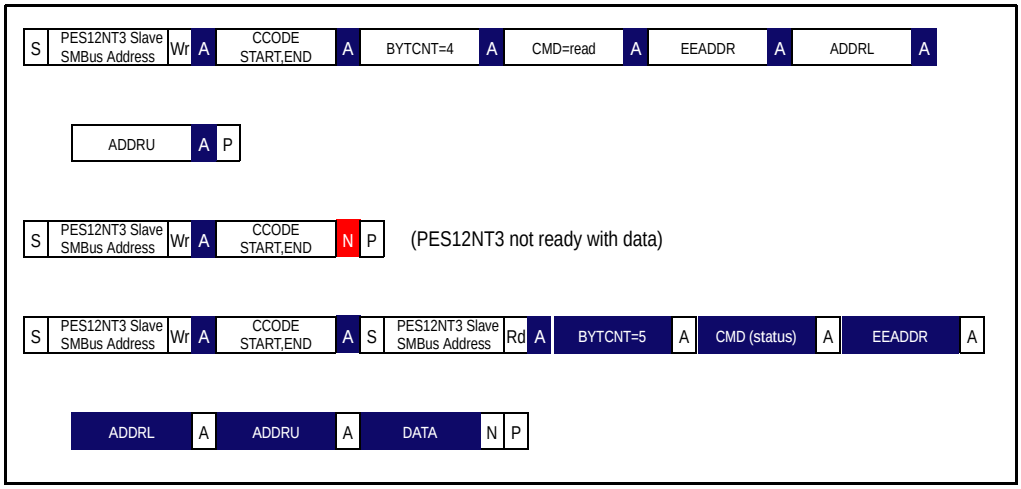

Figure 6.9 Serial EEPROM Read Using SMBus Block Write/Read Transactions with PEC Disabled

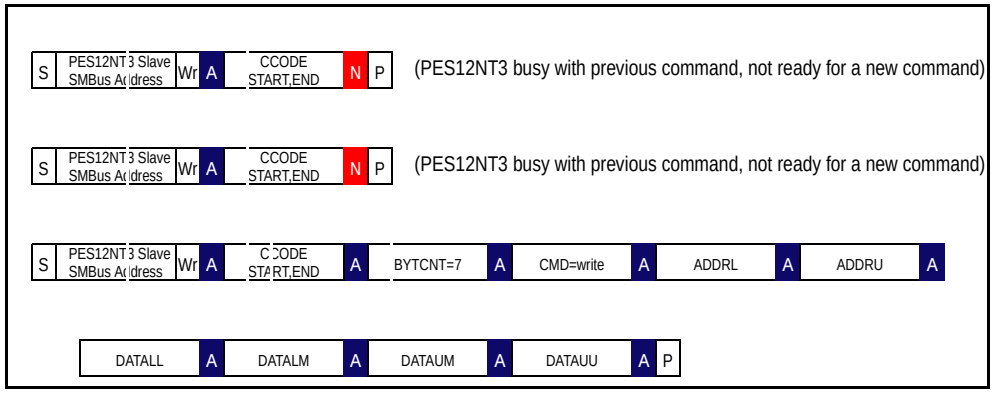

Figure 6.10 CSR Register Write Using SMBus Block Write Transactions with PEC Disabled

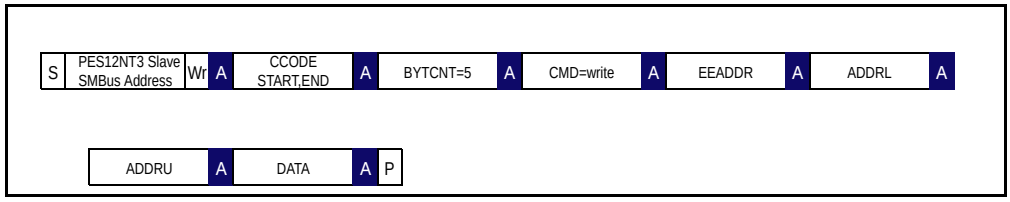

Figure 6.11 Serial EEPROM Write Using SMBus Block Write Transactions with PEC Disabled

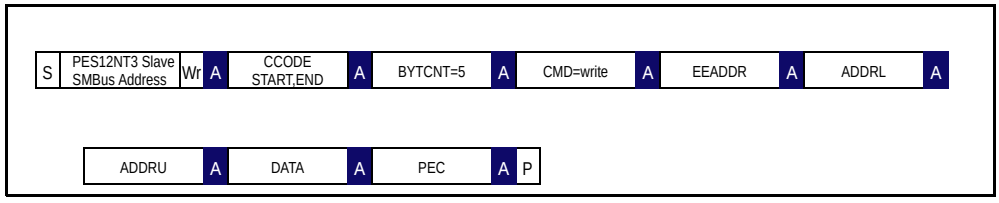

Figure 6.12 Serial EEPROM Write Using SMBus Block Write Transactions with PEC Enabled

Notes

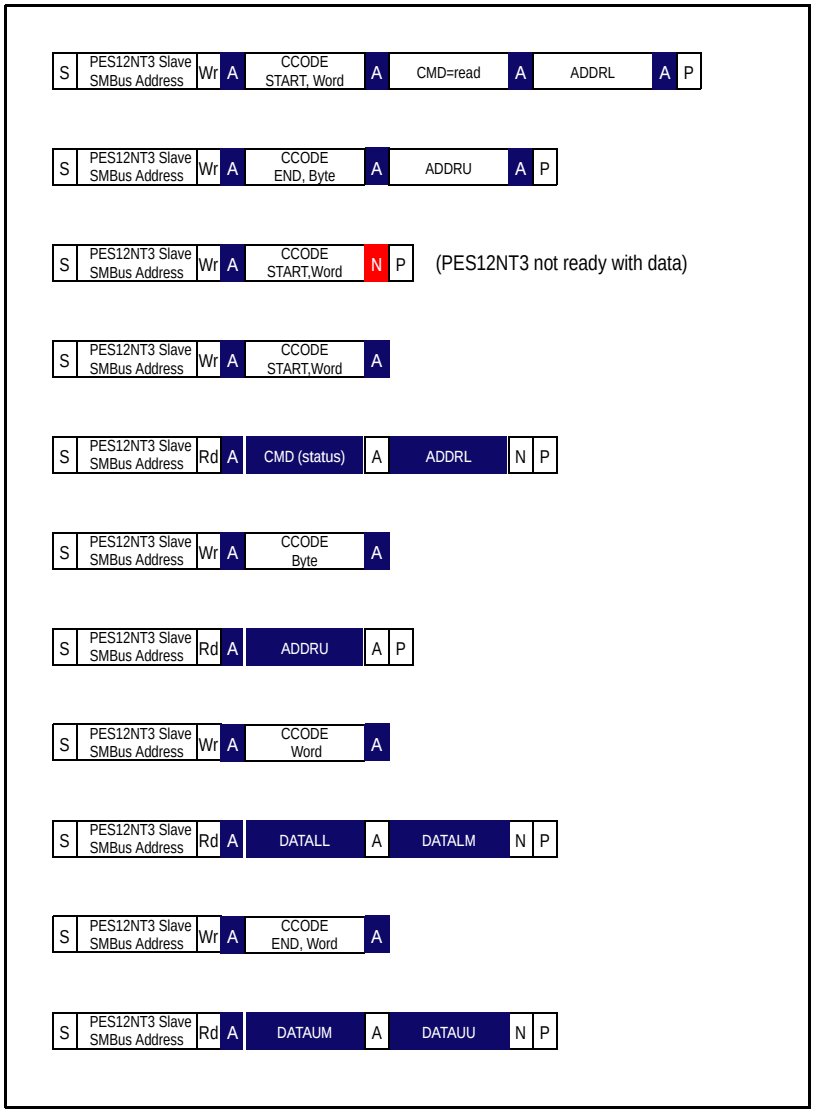

Figure 6.13 CSR Register Read Using SMBus Read and Write Transactions with PEC Disabled

Notes

NTB Upstream Port Failover

Notes

Introduction

The PES12NT3 supports an NTB upstream port failover mechanism that enables the construction of fault tolerant systems.

The NTB upstream port failover usage model is illustrated in Figure 7.1. In this usage there is a primary root and a secondary root. Both roots are active and may communicate using transactions flowing through the NTB, mechanisms provided by the NTB for interprocessor communications, or an out-of-band communications channel. In normal mode, the primary root is responsible for configuring and managing the internal PCIe hierarchy (i.e., the PCIe hierarchy consisting of upstream port A, downstream port B, P2P bridges, and the internal NTB endpoint).

NTB upstream port failover enables the swapping of the upstream port (i.e., port A) with the NTB port (i.e., port C). When a hardware or software failure is detected in the primary root, the PES12NT3 may be directed to operate in a failover mode. In failure mode, the secondary root (i.e., the root associated with port C) becomes the root responsible for configuring and managing the internal PCIe hierarchy and the primary root becomes the root of the external NTB hierarchy.

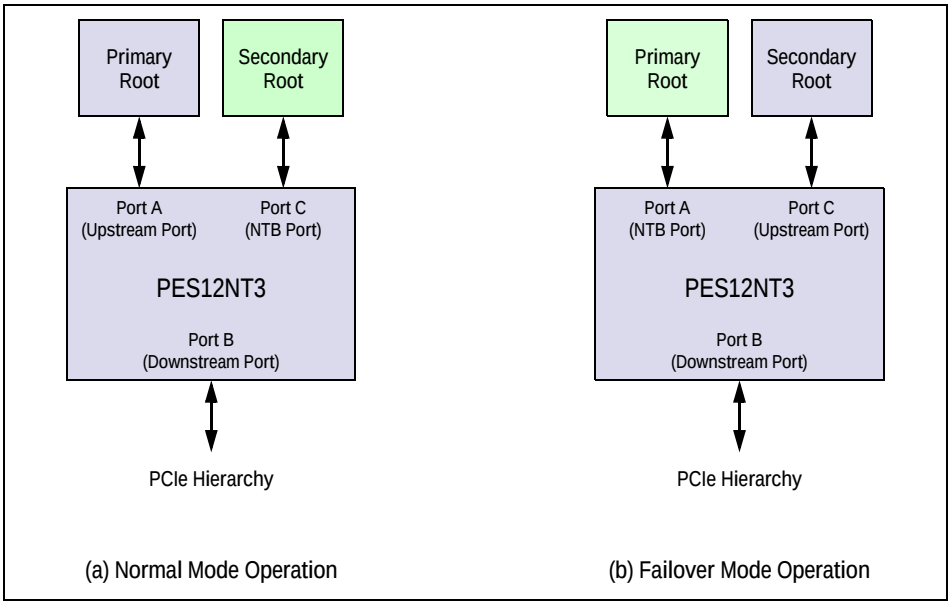

Figure 7.1 NTB Upstream Port Failover Usage Model

The PES12NT3 NTB upstream port failover architecture is shown in Figure 7.2. The two main components of this device are switch logic and a SerDes switch. The PES12NT3 switch logic implements a three port non-transparent switch that does not support NTB upstream port failover. It consists of PCIe stacks, a switch core and NTB logic. The SerDes switch enables SerDes lanes associated with port A and C to be passed through unmodified or swapped.

In normal mode, the SerDes switch operates in a pass-through configuration. This connects the external SerDes lanes associated with port A with the internal port A upstream port of the switch logic and the SerDes lanes associated with port C with the internal port C NTB port. In failover mode, the SerDes switch operates in a swapped configuration. This connects the SerDes lanes associated with port A to the internal port C NTB port and the external SerDes lanes associated with port C to the internal port A upstream port.

Notes

In failover mode the device associated with port C SerDes assumes all of the resources and responsibilities of the internal port A upstream port and visa versa. This means that the root associated with port C has direct access to all port A upstream port registers, receives internal PCIe hierarchy messages (e.g., error and INTx), and so on.

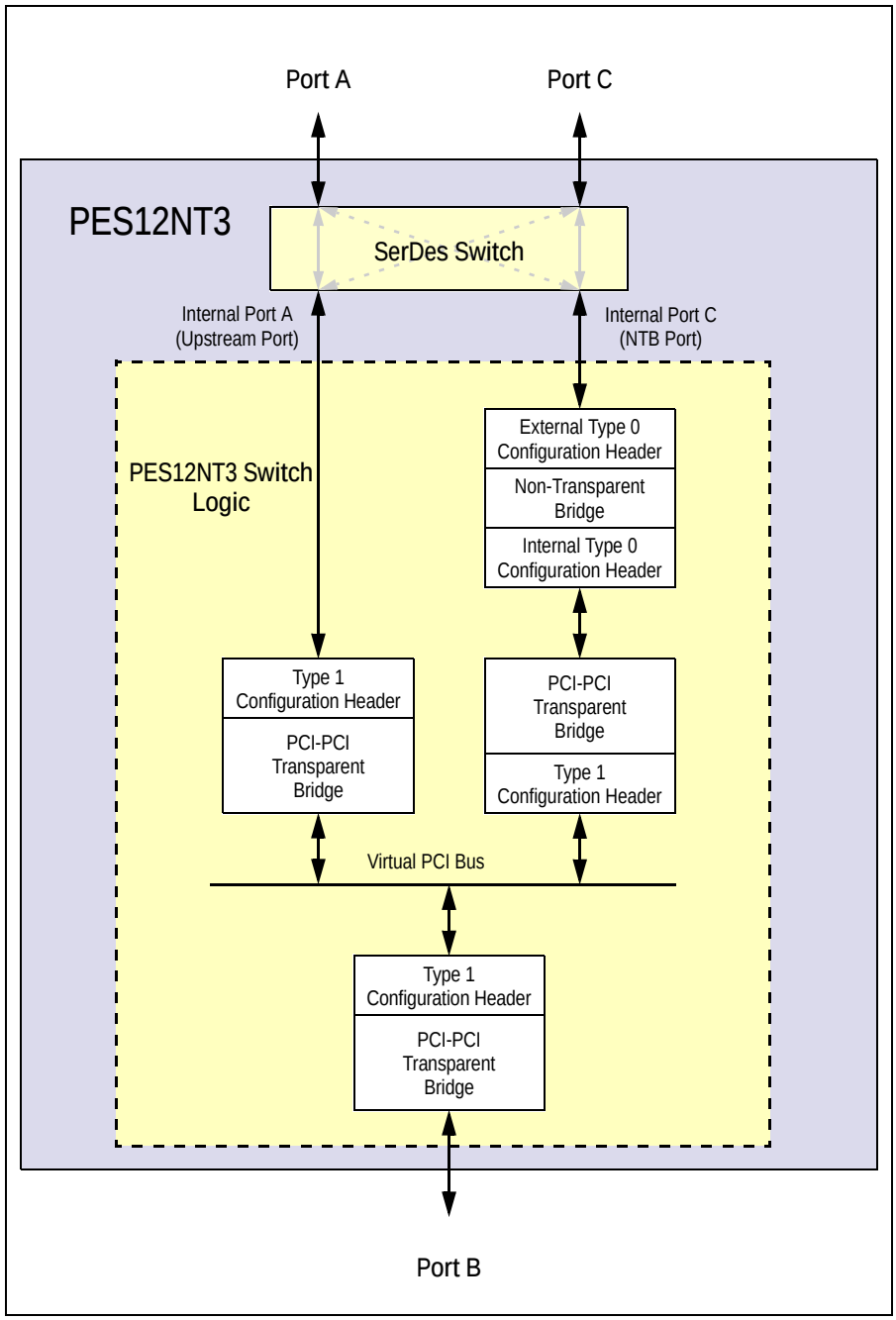

Figure 7.2 PES12NT3 NTB Upstream Port Failover Architecture

Failover

An upstream NTB port failover may be initiated statically through a fundamental reset or dynamically while the system is running.

Notes

A static NTB upstream port failover occurs when the state of the switch mode (SWMODE[3:0]) signals is modified and a fundamental reset is initiated. This results in the PES12NT3 operating in the mode selected by the switch mode signals in the boot configuration vector (i.e., a non-transparent mode or a non-transparent mode with failover). Since a fundamental reset is initiated in a static failover, it results in a complete loss of system state.

Dynamic NTB upstream port failover allows the operating mode of the PES12NT3 to be modified from normal to failover or failover to normal while the system is running and without a fundamental reset. Dynamic NTB upstream port failover may be configured to operate in a state-preserving manner. See section System State Preservation on page 7-5 for information on preserving system state during an a Dynamic upstream port failover.

When a dynamic failover occurs, upstream and NTB port data queued in the switch, data being transmitted, and data in the replay buffers may be lost. Thus, some interruption of PCIe traffic should be expected with a failover. While it may be possible to design a system in which no PCIe traffic is lost or corrupted during a failover, such an implementation is beyond the scope of this specification.

Registers used to manage failover are located in the address space of the external NTB endpoint. Thus, they may be accessed by the primary or secondary roots. They may also be accessed by any PCIe device in the internal or external PCIe hierarchies when NTB endpoint configuration space is memory mapped using BAR4.

The current failover state (i.e., normal mode or failover mode) may be determined by reading the Current Failover Mode (CFMODE) field in the Failover Status (FOVRSTS) register. Whenever, a dynamic upstream port failover is initiated (i.e., starts), the Failover Mode Change Initiated (FMODECI) bit is set in the FOVRSTS register. When a dynamic failover completes, the Failover Mode Change Completed (FMODECC) bit is set in the FOVRSTS register. These bits are sticky and thus their status is preserved across a hot-reset. The operation of the upstream port failover mechanism is unaffected by a hot-reset. Once a failover is initiated, the failover sequence runs to completion and can only be aborted by a fundamental reset.

Static Upstream Port Failover

A static upstream port failover requires a fundamental reset to be initiated whenever a failover mode change is required. Since the initial failover mode is selected by the switch mode in the boot configuration vector, the static upstream port failover feature may be viewed as nothing more than the ability to select the failover mode during a fundamental reset.

An static upstream port failover consists of the following steps:

- Assert the PCIe fundamental reset signal (PERSTN)
- Modify the switch mode (SWMODE) signals to the selected failover mode (i.e., normal mode or failover mode).
- Negate the PCIe fundamental reset signal (PERSTN)

Since initiation of an upstream port failover requires a fundamental reset of the internal PCIe hierarchy and external NTB endpoint, many systems may require the use of dynamic upstream port failover.

Dynamic Upstream Port Failover

Dynamic upstream port failover allows a failover to occur while the system is live and in a manner that preserves the system state.

When a dynamic upstream port failover is initiated, PES12NT3 takes the following actions.

- The LTSSM associated with the upstream port (i.e., port A) and the NTB port (i.e., port C) immediately transition to the Detect state and the data link layer transitions to the DL_Down state. This causes data in the replay buffer associated with ports A and C to be discarded and may cause data queued in the switch core for these ports to be discarded.
- The state of the SerDes switch is modified as selected by the failover mode (i.e., pass through or swapped).
- The LTSSM initiates link training on the upstream port (i.e., port A) and the NTB port (i.e., port C).

Notes

The PxLINKUP and PxLINKDN bits in the INTSTS registers associated with both the internal and external NTB endpoints are not set during a dynamic upstream port failover. The link down and later link up associated with a dynamic upstream port failover are masked from causing these bits from being set. See section Link Status on page 3-3 for a description of the PxLINKUP and PxLINKDN bits.

In most systems it is expected that only one failover mechanism will be enabled at a time. If a failover of the same type (i.e., software, signal, or watchdog timer) is initiated while one is already in progress, the second initiation will be lost. If a failover of a different type is initiated while one is in progress, the failover will be performed once the one in progress completes. Software may utilize the Failover Mode Change (FMODECC) and Failover Mode Change Initiated (FMODECI) bits in the FOVRSTS register to avoid failover race conditions.

The following sections describe the manner in which a dynamic upstream port failover may be initiated.

Software Initiated Failover

A failover may be initiated by modifying the state of the NTB Upstream Port Failover Mode Select (FOVRMSEL) field in the Failover Control (FOVRCTL) register. A software initiated failover may be instituted by software running on the primary or secondary root, software running on a device that writes to the USPSEL field via the SMBus, or via serial EEPROM initialization. The FOVRMSEL field should not be modified during an NTB upstream port failover (i.e., failover requests are not queued).

Signal Initiated Failover

An upstream port failover may be initiated by a change in the state of the NTB Upstream Port Failover (FAILOVERP) signal. Such a failover is initiated when the Signal Failover Enable (SIGFEN) bit is set in the Failover Control (FOVRCTL) register and the state of the FAILOVERP signal differs from the current failover mode reported in the CFMODE field of the FOVRSTS register.

The FAILOVERP signal is an alternate function of GPIO[5]. The state of the FAILOVERP signal always reflects the state of the GPIO[5] pin regardless of whether or not GPIO[5] is configured to operate as an alternate function. When FAILOVERP is negated (low), normal mode is selected. When FAILOVERP is asserted (high), failover mode is selected. The state of the FAILOVERP signal should not be modified more frequently than once per second. The behavior of the PES12NT3 is undefined when the FAILOVERP signal is modified more frequently than this rate.

Watchdog Timer Initiated Failover

An NTB upstream port failover may be initiated as the result of an expiration of a watchdog timer. Such a failover is initiated when the Timer Failover Enable (TIMFEN) bit is set in the Failover Control (FOVRCTL) register, and the Watchdog Timer Count (COUNT) field in the Failover Watchdog Timer (FOVRTIMER) transitions from a one to a zero.

When non-zero, the COUNT field in the USPFTIMER is decremented once per microsecond (1 µS). This provides a maximum watchdog timer interval of over one hour. Decrementing of the COUNT field ceases when zero is reached. The COUNT field may be written by software at any time. Modifying the count field is used to rearm the watchdog timer. If not expired, the watchdog timer continues to decrement across a hot-reset.

When a watchdog timer failover is initiated, the failover mode selected is the one not reported in the CFMODE field in the FOVERSTS register. For example, if the current mode is normal mode, then the mode following a watchdog timer initiated failover is failover mode.

Notes

System State Preservation

The PES12NT3 contains mechanisms that allow system state of the internal and/or external PCIe hierarchy domains to be preserved across a dynamic failover. They may also be used to inhibit the propagation of reset due to a link down or reception of TS1 ordered-sets indicating a hot reset.

- When the Internal Hierarchy Disable Link Down Hot Reset (IDLDHRST) bit is set in the FOVRCTL register, the resetting of the internal and external NTB domains is inhibited due to a Port A link down condition (i.e., a transition to DL_Down).
- When the External Hierarchy Disable Link Down Hot Reset (EDLDHRST) bit is set in the FOVRCTL register, the resetting of the external NTB domain is inhibited due to a Port C link down condition.
- When the Disable Failover Hot Reset (DFHRST) bit is set in the FOVRCTL register, the resetting of the internal and external NTB domains is inhibited due to Port A and C link down conditions resulting from a dynamic failover. Port A and C link down resulting from any other condition continues to generate a hot reset unless masked by the IDLDHRST or EDLDHRST bits.
- When the Internal Hierarchy Disable Hot Reset Propagation (IDHRSTPROP) bit is set in the FOVRCTL register, reception of TS1 ordered-sets on the upstream port indicating a hot reset is ignored.
- When the External Hierarchy Disable Hot Reset Propagation (EDHRSTPROP) bit is set in the FOVRCTL register, reception of TS1 ordered-sets on port C indicating a hot reset is ignored.

Notes

General Purpose I/O

Notes

Introduction

The PES12NT3 has eight General Purpose I/O (GPIO) pins that may be individually configured as: general purpose inputs, general purpose outputs, or alternate functions. GPIO pins are controlled by the General Purpose I/O Control and Status (GPIOCS) register located in upstream port A's PCI configuration space (see Table 8.1).

GPIO Registers

Bit Field	Field Name	Type	Default Value	Description
7:0	GPIOFUNC	RW	0x0	GPIO Function. Each bit in this field controls the corresponding GPIO pin. When set to a one, the corresponding GPIO pin operates as the alternate function as defined in Table 8.2. When a bit is cleared to a zero, the corresponding GPIO pin operates as a general purpose I/O pin.
15:8	GPIOCFG	RW	0x0	GPIO Configuration. Each bit in this field controls the corresponding GPIO pin. When a bit is configured as a general purpose I/O pin and the corresponding bit in this field is set, then the pin is configured as a GPIO output. When a bit is configured as a general purpose I/O pin and the corresponding bit in this field is zero, then the pin is configured as an input. When the pin is configured as an alternate function, the behavior of the pin is defined by the alternate function.
23:16	GPIOD	RW	HWINIT	GPIO Data. Each bit in this field controls the corresponding GPIO pin. Reading this field returns the current value of each GPIO pin regardless of GPIO pin mode (i.e., alternate function or GPIO pin). Writing a value to this field causes the corresponding pins which are configured as GPIO outputs to change state to the value written.
31:24	Reserved	RO	0x0	Reserved field.

Table 8.1 General Purpose IO Registers

As shown in Table 8.2, GPIO pins [5:0] are shared with other on-chip functions. The GPIO Function (GPIOFUNC) field in the GPIOCS register controls whether a GPIO bit operates as a general purpose I/O or as the specified alternate function.

Notes

GPIO Pin	Alternate Function Pin Name	Alternate Function Description	Alternate Function Pin Type
0	PEBRSTN	Reset output for downstream port B	Output
1	PECRSTN	Reset output for downstream port C	Output
2	PALINKUP	Port A link up status output	Output
3	PBLINKUP	Port B link up status output	Output
4	PCLINKUP	Port C link up status output	Output
5	FAILOVERP	NTB Upstream port failover input	Input

Table 8.2 General Purpose I/O Pin Alternate Function

After reset, all GPIO pins default to the GPIO input function. GPIO pins configured as GPIO inputs are sampled no more frequently than once every 128 ns and may be treated as asynchronous inputs.

When a GPIO pin is configured to use the GPIO function, the unneeded alternate function associated with the pin is held in an inactive state by internal logic. Care should be exercised when configuring the GPIO pins as outputs since an incorrect configuration could cause damage to external components as well as the PES12NT3.

GPIO Configuration

Each bit in the GPIOFUNC, GPIOCFG and GPIOD fields in the GPIOCS register is associated with the corresponding GPIO pin. Table 8.3 summarizes the configuration of GPIO pins.

GPIOFUNC	GPIOCFG	Pin Function
0	0	GPIO input
0	1	GPIO output
1	don't care	Alternate function

Table 8.3 GPIO Pin Configuration

GPIO Pin Configured as an Input

When configured as an input in the GPIOCFG field and as a GPIO function in the GPIOFUNC field, the GPIO pin is sampled and registered in the GPIOD field. The value of the input pin can be determined at any time by reading the GPIOD field. Note that the value in this field corresponds to the value of the pin irrespective of whether the pin is configured as a GPIO input, GPIO output or alternate function.

GPIO Pin Configured as an Output

When configured as an output in the GPIOCFG field and as a GPIO function in the GPIOFUNC field, the value in the corresponding bit position of the GPIOD field is driven on the pin. System designers should treat the GPIO outputs as asynchronous outputs. The actual value of the output pin can be determined by reading the GPIOD field.

GPIO Pin Configured as an Alternate Function

When configured as an alternate function in the GPIOFUNC field, the pin behaves as an described by the section associated with that function. The value of the alternate function pin can be determined at any time by reading the GPIOD field.

Non-Transparent Mode Operation

Notes

Introduction

The PCIe® architectural model is one in which a root, typically the main CPU, is responsible for configuring a tree of endpoints (i.e., a hierarchy of virtual PCI buses). Once configured, any endpoint or root may "initiate transactions. The root and endpoints share a common address space with routing configured in PCI-PCI bridges.

A limitation of the PCIe architectural model is that it allows only a single root and that the root and all of the endpoints must share a common address space. This limitation may be overcome through the use of a non-transparent bridge. A non-transparent bridge allows two roots or PCIe trees to be interconnected with one or more shared address windows between them.

Note: Port C of the PES12NT3 always operates in the non-transparent mode.

The device functionally operates as illustrated in Figure 9.1. In this mode, the PES12NT3 may be logically viewed as consisting of three PCI-PCI transparent bridges, one per port, and an internal virtual PCI bus. Port C is the non-transparent port. Beneath the transparent bridge associated with port C are two endpoints interconnected by non-transparent bridge functionality. When viewed externally, port C appears as an end-point device. When viewed internally, the non-transparent bridge beneath the PCI-PCI bridge associated with port C appears as an end-point device.

The endpoint and non-transparent bridge functionality closest to the PCI-PCI bridge is referred to as the *internal side* of the non-transparent bridge. The endpoint and non-transparent bridge associated with the port C link is referred to as the *external side* of the non-transparent bridge.

The non-transparent bridge requires configuration following a fundamental reset before it will bridge transactions between the internal and external sides. This configuration may be performed by the root associated with the internal side (port A), root associated with the external side (Port C), serial EEPROM, or master on the slave SMBus interface.

Associated with the upstream port and port B is a 4 KB configuration space and a Type 1 configuration header. The organization and function of these configuration spaces is exactly the same as in transparent mode and is described in Ports A and B Configuration Space Organization on page 9-18. Associated with the downstream non-transparent port is a 4 KB configuration space and Type 1 configuration header corresponding to the PCI-PCI bridge on the virtual PCI bus. The organization and function of this configuration space is exactly the same as in transparent mode except for the following.

Notes

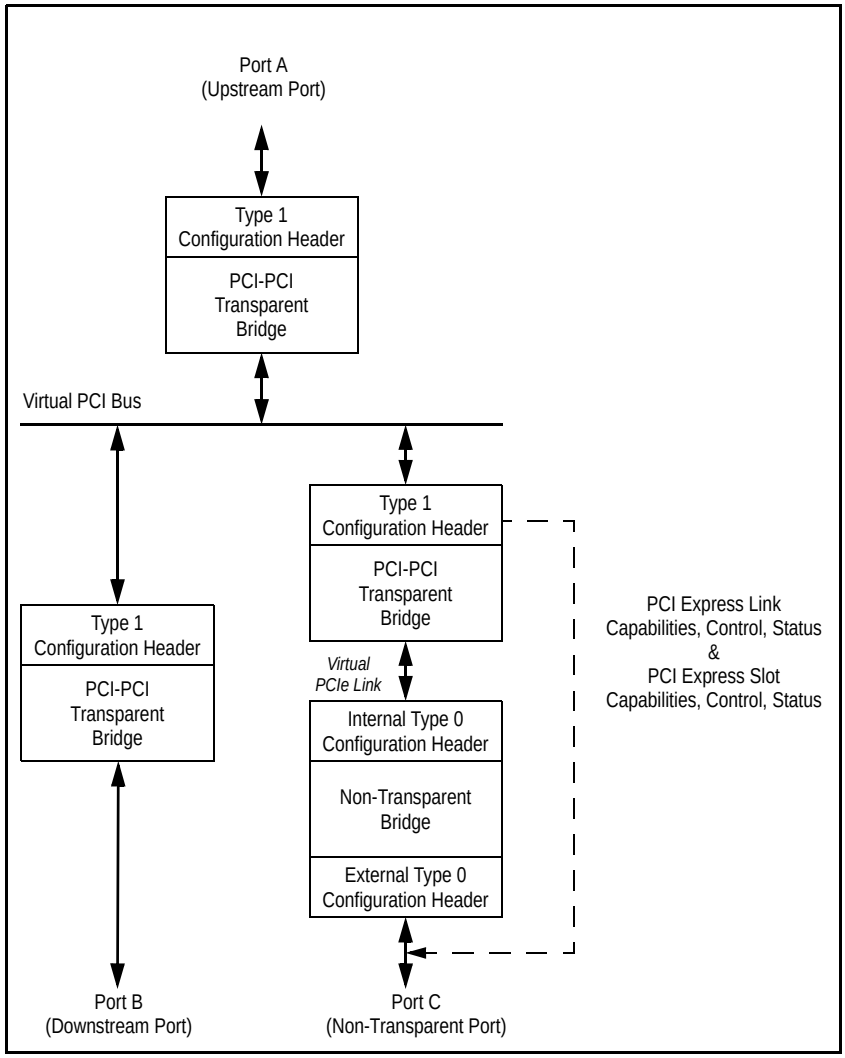

Figure 9.1 PES12NT3 Functional Block Diagram in Non-Transparent Mode

In a transparent switch, link registers in the downstream port of a switch correspond to the link associated with the downstream port. In the case of the non-transparent port, there is a virtual internal and external endpoint beneath the PCI-PCI bridge associated with the downstream port; however, the link capabilities still refer to the link associated with the downstream port of the switch (i.e., the external physical port C link).

The connection between the port C PCI-PCI bridge and the internal endpoint associated with the non-transparent bridge is an on-chip virtual PCIe link. The link capabilities, control and status registers of a device reflect the state of the link connection of the device to the upstream port of a switch or a root complex. Therefore, in the internal non-transparent bridge endpoint these registers reflect the “virtual” state of this on-chip connection. On the external non-transparent bridge endpoint, these registers reflect the actual state of physical link associated with port C and mirror the values of the corresponding fields in the port C PCI-PCI bridge.

Following configuration of the non-transparent bridge complex, the non-transparent bridge will appear as a PCI-PCI bridge followed by an endpoint on the internal side and an endpoint on the external side. Therefore, once configured the operation of the non-transparent bridge should be transparent to system software and drivers. However, PCIe software that uses the PCI Express Capability structure may need to be modified.

Notes

Transaction Routing

Transactions are routed by the port C PCI-PCI bridge in the same manner as in transparent mode. Thus, the issue of transaction routing relates to how transactions are routed between the internal and external endpoints associated with the non-transparent bridge.

PCIe defines the following transactions routing mechanisms.

- Address routing with 32-bit or 64-bit format
- ID based routing using bus, device and function numbers.
- Implicit routing utilizing

  Route to root

  Broadcast from root

  Local - terminate at receiver

  Gathered and routed to root

No messages are passed through the non-transparent bridge. If a message is received by an internal or external non-transparent endpoint that does not correspond to a message that should be processed by an endpoint, then the message is silently discarded.

Address Routing

Address routed transactions consist of those that require completions (i.e., non-posted transactions) and those that do not require completions (i.e., posted transactions). The behavior of posted transactions is discussed first since their behavior is a subset of non-posted transactions.

Mapping Table

Associated with the internal and external endpoints of the NTB are 16-entry mapping tables. The mapping table contains the bus, device and function numbers of initiators on that side of the NTB whose transactions may be forwarded to the opposite side of the NTB. The format of these tables is shown in Figure 9.2 and described in Table 9.1.

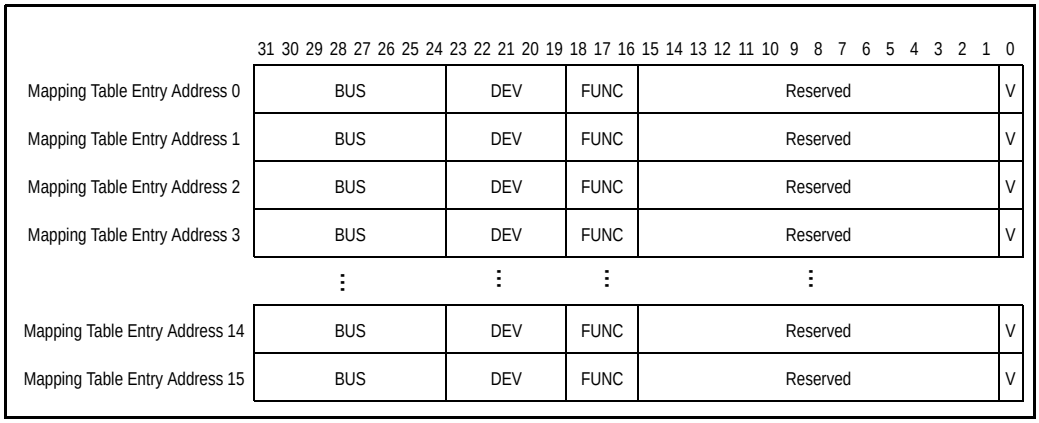

Figure 9.2 Internal and External Endpoint Non-Transparent Bridge Mapping Table Format

Bit Field	Name	Description
0	V	When set, this field indicates if the table entry is valid.

Table 9.1 Non-Transparent Bridge Mapping Table Fields

Notes

Bit Field	Name	Description
18:16	FUNC	This field contains the mapping table entry function number.
23:19	DEV	This field contains the mapping table entry device number.
31:24	BUS	This field contains the mapping table entry bus number.

Table 9.1 Non-Transparent Bridge Mapping Table Fields

The mapping tables are initialized using the Mapping Table Address (MTADDR) and Mapping Table Data (MTDATA) registers in the endpoint configuration spaces. To access a mapping table entry the Address (ADDR) field in the MTADDR register is initialized with the mapping table entry number. A read from the MTDATA register returns the current value of the entry while a write modifies the entry.

The MTDATA register must be accessed using Dword operations. Performing a byte or word operation to the MTDATA register results in no data being modified on a write and zero being returned on a read. In addition, the MTAERR bit is set in the NTB Status (NTBSTS) register.

Following a reset, all valid (V) bits are cleared. When a valid (V) bit is cleared, the FUNC, DEV, and BUS fields always return a value of zero when read even if they actually contain a non-zero value (i.e., invalid entries immediately return a value of zero and are not actually read from the mapping table).

Posted Address Routed Transactions

The internal and external Non-Transparent Bridge (NTB) endpoints contain five Base Address Registers (BARs) in their Type 0 configuration header. The internal endpoint BARs are PCIE_BAR[0..4] and the external endpoint BARs are PCEE_BAR[0..4]. BARs zero through three may each be used to map 32-bit prefetchable or non-prefetchable memory or I/O windows between the internal and external sides of the non-transparent bridge. Odd and even numbered BARs may be paired to form 64-bit prefetchable address windows. Thus, the internal and external endpoints may each be configured to support four 32-bit memory or I/O windows, two 64-bit windows or any combination of the two.

Each BAR has a corresponding setup register, translated base register, and translated limit register in the Non-Transparent Bridge Configuration Capability structure associated with that side of the non-transparent bridge. For example, PCIE_BAR0 has an associated setup register PCIE_BARSETUP0, translated base register PCIE_BARTBASE0, and translated limit register PCIE_BARTLIMIT0.

The setup register contains fields that configure the corresponding BAR. For example the type of BAR, memory or I/O, and the address window size are configured in this register. The base address of a BAR corresponds to those address bits which are examined to determine if an address falls into a region mapped by a BAR (i.e., those bits in the Base Address (BADDR) field that can be modified). The remaining BAR bits form an offset address (i.e., those bits in the Base Address (BADDR) field that cannot be modified and are read back as zero during configuration).

When an NTB endpoint receives a posted address routed transaction, its address and type are compared against BARs zero through three. If the type and address match a BAR, the bus, device and function of the requester ID in the transaction is associatively looked up in the mapping table for that side of the non-transparent bridge. If a valid entry is found that matches all three fields, the transaction is forwarded to the other side of the non-transparent bridge if it passes the limit check described below.

The behavior of the device is undefined if an address matches multiple BARs.

Notes

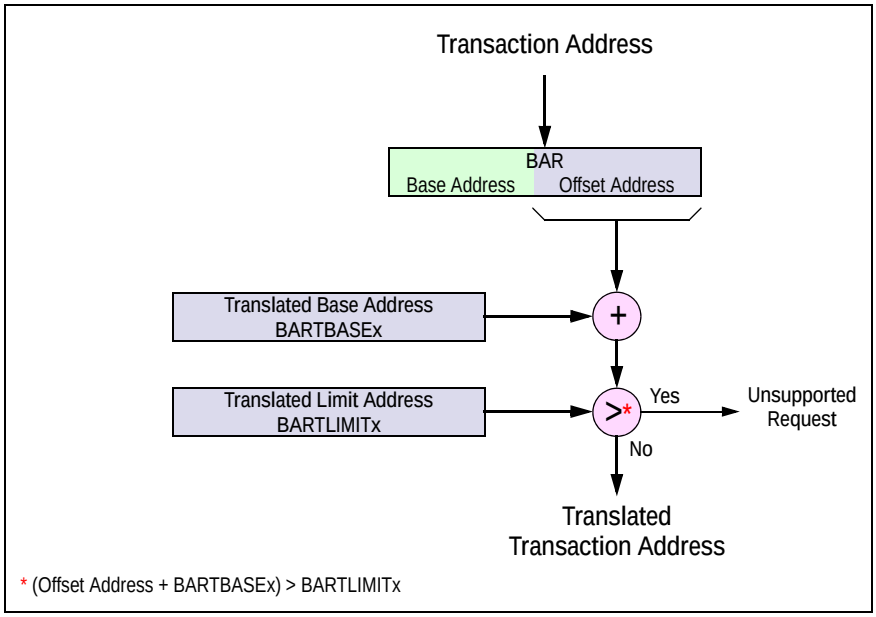

Figure 9.3 NTB Base and Limit Address Translation

A base and limit address translation mechanism is employed to translate the address of transactions that flow through the NTB. This is graphically illustrated in Figure 9.3. The translated address corresponds to the offset address bits of the matching BAR added to the value in the translated base address (BARTBASEx) register. If this value is less than or equal that stored in the corresponding translated limit address (BARTLIMITx) register, then the transaction, with the new translated address, is forwarded to the opposite side of the NTB. If the value is greater than the value in the BARTLIMITx register, then the transaction is treated in the same manner as a transaction that does not match any of the BARs.

The translated base address consists of the TBADDR field shifted left four bit positions (i.e., corresponding bit positions of this field and the offset address bits of the BAR are added). In the same manner, the translated limit address consists of the TLADDR field shifted left four bit positions. The bus number in the requester ID in the forwarded transaction is equal to the bus number of the NTB endpoint on the opposite side of the non-transparent bridge. The device and function number of the requester ID in the forwarded transaction is equal to the matching mapping entry table address. For example if the matching mapping table entry was 14, then the device number would be one and function number would be six.

If a posted address routed transaction is received that matches a BAR but whose requester ID is not in the mapping table, then the Forward Mapping Table Miss (FMTMISS) bit is set in the NTBSTS register of the NTB endpoint on which the transaction was received and the transaction is treated as an unsupported request. An address routed transaction received by the internal endpoint that maps to the external domain when the Port C link is down is treated as a mapping table miss. When this occurs, the Forward Mapping Table Miss (FMTMISS) bit is set in the internal NTB endpoint NTBSTS register and the transaction is treated as an unsupported request.

If an address routed transaction is received that does not match any of the BARs, the BAR Miss (BARMISS) bit is set in the NTBSTS register and the transaction is treated as an unsupported request. If I/O transactions are not enabled via the IOAE bit in the PCICMD register and an I/O request is received, the transaction is treated as an unsupported request. If memory transactions are not enabled via the MAE bit in the PCICMD register and a memory request is received, then the transaction is treated as an unsupported request. If the BME bit is cleared in the PC_PCICMD register or the PCIE_PCICMD register and a memory or I/O request is received on the external side of the NTB, then the transaction is treated as an unsupported request. If the corresponding case occurs on the external side of the NTB, then it is also treated as an unsupported request.

Notes

Treating a transaction as an unsupported request means setting the appropriate status bits and, if enabled, generating an error message. If the transaction was a non-posted, this also means generating a completion with status UR. See the PCIe base specification for details.

The NTB merely translates fields in TLPs, it does not restructure TLPs. Therefore, 32-bit address routed transactions must map to 32-bit address transactions on the other side of the NTB and 64-bit address routed transactions must map to 64-bit address transactions on the other side of the NTB. The behavior of the NTB when 32-bit address routed transactions are mapped to 64-bit addresses or 64-bit address routed transactions are mapped to 32-bit addresses is undefined.

Non-Posted Address Routed Transactions

Non-posted address routed transactions are handled by the NTB endpoints in exactly the same manner as posted address routed transactions except that there is a completion associated with the transaction that needs to traverse the non-transparent bridge from the opposite side to the side on which the original initiator is located.

Completion transactions are routed by ID (i.e., by bus, device, and function number). When a completion is generated, it is routed by ID back to the opposite side of the non-transparent bridge. This is because the bus number in the request transaction corresponds to that of the NTB and the NTB opposite side endpoint is the only device on that bus. When a completion is received by the opposite side NTB endpoint, a mapping table entry address is formed using the device and function numbers of the requesters ID field in the TLP. In the request transaction, these fields were initialized with a mapping table entry. Thus, in the completion transaction, these fields should point to the mapping table entry containing the bus, device and function numbers of the original requestor.

The mapping table entry address formed from the device and function numbers is used to index into the mapping table corresponding to the opposite side of the NTB from which the completion was received. If the mapping table entry is valid, then the completion is routed through the NTB. The bus, device and function numbers of the requester ID of the forwarded transaction are replaced with the corresponding values in the associated mapping table entry. The completer ID of the forwarded transaction is replaced with the bus, device and function numbers of the NTB endpoint on which the completion is emitted (i.e., the NTB endpoint side opposite to that on which the completion was received).

If the mapping table entry is invalid, or if the mapping table entry address does not point to a valid entry, then the transaction is treated as an unexpected completion and the Reverse Mapping Table Miss (RMTMISS) bit is set in the NTBSTS register of the NTB endpoint on which the transaction was received.

A completion received by the internal endpoint that maps to the external domain when the Port C link is down is treated as a mapping table miss. When this occurs, the transaction is treated as an unexpected completion and the Reverse Mapping Table Miss (RMTMISS) bit is set in the internal endpoint NTBSTS register.

ID Routing

Other than completion transactions described in section Address Routing on page 9-3, ID routing is not supported through the non-transparent bridge and are discarded.

Route to Root Implicit Routing

Route to root implicit routing is not supported through the non-transparent bridge and are discarded.

Broadcast from Root Implicit Routing

Broadcast from root implicit routing is not supported through the non-transparent bridge and is discarded.

Local Terminate at Receiver Implicit Routing

Local terminate at receiver implicit routed transactions terminate at the NTB endpoint at which they are received and therefore are not forwarded through the non-transparent bridge.

Notes

Gather and Route to Root Implicit Routing

Gather and route to root implicit routing is not supported through the non-transparent bridge and are discarded.

Non-Transparent Bridge Interprocessor Communications

The Non-Transparent Bridge Communications Capability Structure has a number of facilities to aid in interprocessor communications between processors on opposite sides of the NTB. These are graphically illustrated in Figure 9.4 and described in the following sections.

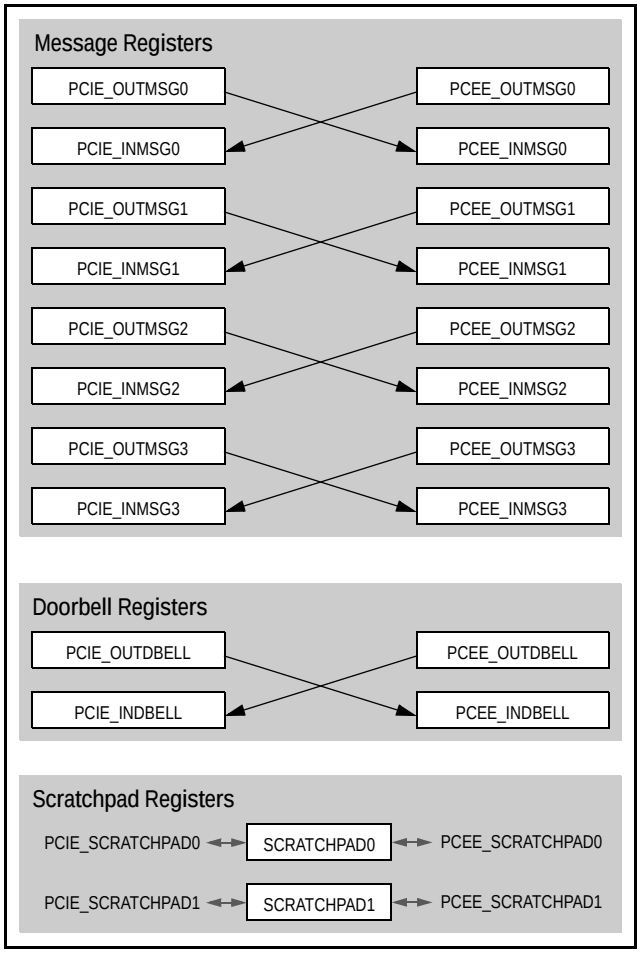

Figure 9.4 Non-Transparent Bridge Interprocessor Communications Facilities

Message Registers

The internal and external endpoints each have four Inbound Message (INMSG[0..3]) and Outbound Message (OUTMSG[0..3]) registers. OUTMSG registers may be read and written while INMSG registers are read only. When an OUTMSG register is written, the corresponding INMSG register on the opposite side of the NTB takes on the value written and the corresponding Inbound Message (INMSGx) bit is set in the Interrupt Status (INTSTS) register on the opposite side of the bridge.

This mechanism may be used to pass 32-bit quantities with interrupt notification. For example, when a processor on the internal side writes to PCIE_OUTMSG0, then PCEE_INMSG0 takes on the value written and the INMSG0 bit is set in the PCEE_INTSTS register. The setting of the INMSG0 bit may be used to generate an interrupt to the root on the external side.

Notes

Doorbell Registers

The internal and external endpoints each have an Inbound Doorbell (INDBELL) and Outbound Doorbell (OUTDBELL) register. The OUTDBELL register may be read and written while INDBELL register is read and cleared. The doorbell registers provide 32 doorbells in each direction through the non-transparent bridge. When a bit is set in the OUTDBELL register, the corresponding bit is set in the INDBELL register on the opposite side of the NTB. When any bit in the INDBELL register is set, then the INDBELL bit is set in the INTSTS register on that side of the non-transparent bridge and may be used to generate an interrupt.

Note that the INDBELL bits are of type RW1C and are set only when a bit in the corresponding OUTDBELL register transitions from a zero to a one.

Scratchpad Registers

There are two Scratchpad (SCRATCHPAD[0..1]) registers shared between the internal and external sides of the non-transparent bridge. Writing to a scratchpad register immediately modifies its value on both sides of the non-transparent bridge. There are no interrupts or other notification associated with scratchpad register modifications. Scratchpad registers may not be accessed using the Extended Configuration Space Data (ECFGDATA) register. The behavior of scratchpad register accesses using this mechanism is undefined.

Interrupts

There are 13 events that may cause an interrupt to be generated by a non-transparent bridge endpoint. Four of these correspond to the inbound message registers, one with the inbound doorbell register, one with detection of a fundamental or hot reset on the opposite side of the non-transparent bridge, one with modification of the power management state on the opposite side of the non-transparent bridge, and six associated with link status.

Internal NTB endpoint interrupts and MSIs are routed upstream to the internal root on port A while external NTB endpoint interrupts and MSIs are sent out on the link associated with the non-transparent bridge (i.e., port C link). Each interrupt source has an associated bit in the Interrupt Status (INTSTS) register. Associated with each bit in the INTSTS register is a configuration field in the Interrupt Control 0 (INTCTL0) or Interrupt Control 1 (INTCTL1) register. This field determines how the interrupt is handled. Each interrupt bit may be individually configured to generate an MSI, an ASSERT_INTx/DEASSERT_INTx message, or may be disabled (i.e., masked).

When an interrupt source is configured to generate an MSI, an MSI is generated if the corresponding source bit is set and the MSI is enabled (i.e., the EN bit is set in the MSICAP register). When an interrupt source is configured to generate INTx messages, ASSERT_INTx/DEASSERTx messages are generated if the corresponding source bit is set and endpoint interrupts are not disabled (i.e., the INTXD bit is cleared in the PCICMD register).

Note that a function is prohibited by the PCI 2.3 specification from requesting service via INTx messages if MSIs are enabled. The NTB endpoints are capable of generating INTx messages even when MSIs are enabled. It is the responsibility of system software to properly configure the NTB endpoints.

MSI and INTx Message Generation

Each of the status bits in the INTSTS register represents an interrupt source. When an interrupt source requests service, the corresponding bit in the INTSTS register is set. The action taken (i.e., disabled, INTx, or MSI) for a particular interrupt source is determined by a corresponding field in the INTCTL0 or INTCTL1 register.

An interrupt source may be mapped to one of the legacy interrupts (INTA, INTB, INTC, or INTD) or to a single MSI generated by the endpoint.

All of the interrupt sources which are mapped to an MSI are logically ORed to produce an *MSI request value*. Whenever the *MSI request value* transitions from false (i.e., no request) to true, an MSI message is generated to the address and with the data specified in the MSI capability structure. A new MSI is not generated until the *MSI request value* transitions to false and then again transitions to true. Thus, a non-

Notes

transparent bridge endpoint generates a single MSI message for all interrupt sources and this message is only generated when a falling edge would have occurred on a legacy PCI INTx# pin that corresponds to the *MSI request value*.[1]

All of the interrupt sources which map to a legacy interrupt INTx are logically ORed to produce an *INTx request value*. Whenever the I*NTx request value* transitions from false (i.e., no request) to true, an ASSERT_INTx message is generated (i.e., whenever a falling edge would have occurred on a legacy INTx# pin). Whenever the *INTx request value* transitions from true to false, a DEASSERT_INTx message is generated (i.e., on a rising edge of a legacy INTx# pin).

Each interrupt source in the INTSTS register may be masked at any time by setting the corresponding field in the INTCTL0 or INTCTL1 register to "disabled." This enables servicing of INTx and MSI interrupts using the standard per-vector masking approach outlined in "Servicing MSI and MSI_X Interrupt" on page 251 of the PCI Local Bus specification revision 3.0.

Non-Transparent Bridge TLP Processing

The PES12NT3 supports two forms of very basic processing on TLPs that flow through the non-transparent bridge. TLPs generated by the internal or external NTB endpoints are not affected by the TLP processing configuration fields described below. When the Force Relaxed Ordering (FRO) bit is set in the TLP Processing Control (TLPPCTL) register, the value of the relaxed ordering attribute of TLPs flowing through the NTB is set to the value dictated by the Relaxed Ordering Modification (ROM) field in the TLPPCTL register. This transformation is only performed on TLPs in which the relaxed ordering attribute is applicable:

- The relaxed ordering attribute is applicable to all TLPs except: configuration requests, I/O requests, memory requests that are Message Signaled Interrupts (MSIs), and Message requests (except where specifically permitted).
- Since MSIs cannot be distinguished from memory write transactions by the switch, the relaxed ordering attribute of MSIs will be modified.

When the Force No-Snoop (FNS) bit is set in the TLP Processing Control (TLPPCTL) register, the value of the no-snoop attribute of TLPs flowing through the NTB is set to the value dictated by the No-Snoop Modification (NSM) field in the TLPPCTL register. This transformation is only performed on TLPs in which the no-snoop attribute is applicable. The no-snoop attribute is applicable to all TLPs except: configuration requests, I/O requests, memory requests that are Message Signaled Interrupts (MSIs), and Message requests (except where specifically permitted). Since MSIs cannot be distinguished from memory write transactions by the switch, the no-snoop attribute of MSIs will be modified.

Configuration

For the non-transparent bridge to function properly, the port C PCI-PCI bridge must be properly configured. Its configuration is the same as in transparent mode and system software should ensure that transactions are properly routed to the internal NTB endpoint. Thus, the issue of NTB configuration relates to how the internal and external endpoints are configured. The organization of the port C PCI-PCI bridge configuration space is described in section section on page 9-59.

All normal PCIe endpoint configuration must be performed before the NTB will forward transactions. For example, the Memory Access Enable (MAE) and Bus Master Enable (BME) bits must be set in the internal and external PCI command registers (i.e., PCIE_PCICMD and PCEECMD) before memory transactions are routed through the non-transparent bridge.

Reading the Non-Transparent Bridge Endpoint Identification (NTBEPID) register returns the bus, device and function number of the last configuration write to the non-transparent bridge. This may be used by software to determine the ID of the non-transparent bridge.

[1] Note that INTx# is active low while *MSI request value* is active or true when high.

Notes

Configuration Space

Associated with the internal and external NTB endpoints is a 4 KB PCIe configuration space containing a Type 0 header. The organization of these configuration spaces is described in sections section NTB Endpoint Configuration Space Organization on page 9-65 through section Non-Transparent Bridge External Endpoint Registers on page 9-117. The NTB configuration spaces are symmetric, meaning that the same fields are located in the locations on both sides of the NTB.

Internal NTB endpoint configuration space registers may be configured by the internal root by performing configuration read and write operations. External NTB endpoint configuration space registers may be configured by the external root by performing configuration read and write operations.

Registers associated with the internal or external NTB endpoints occupy the bottom 2 KB of their configuration space. The upper 2KB of each endpoint's configuration space contains the configuration space of the endpoint associated with the opposite side of the NTB. Thus, an internal root may configure any external endpoint register simply by adding a 2 KB offset and referencing the internal NTB endpoint's configuration space. The external root has a similar capability.

The crosscoupling of NTB endpoint configuration spaces is graphically illustrated in Figure 9.5.

Software should ensure that there are four or less outstanding configuration transactions to an NTB configuration space. Exceeding this number of outstanding transactions may result in completions being dropped.

In some systems it may desirable to prevent modification of NTB configuration by endpoints on the opposite side of the NTB using configuration transactions. When the Opposite Side Configuration Protection (OSCFGPROT) bit is set in the Non-Transparent Bridge Control (NTBCTL) register, access to the non-transparent bridge configuration capability structure is disabled for this side as well as for the opposite side using a 2KB offset into the configuration window. This means that reading any register in this capability structure, except the NTBCFGC register, returns a value of zero and all writes are ignored. NTBCFGC returns it's default value regardless of the setting of the OSCFGPROT field, allowing normal traversal of the capability structure.

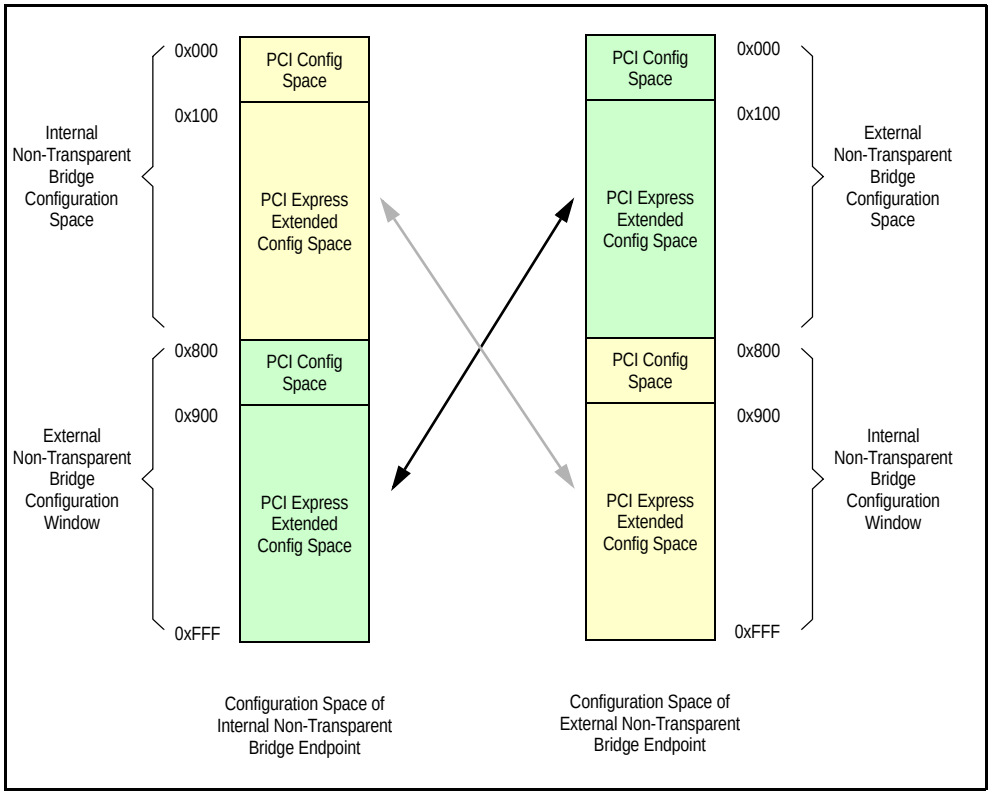

Figure 9.5 Non-Transparent Bridge Configuration Window

Notes

Memory Mapped Configuration Space

In PCIe only the root may perform configuration space read and write operations. Since the interprocessor communication facilities are mapped into configuration space, it is desirable to provide a means for any PCIe master to access configuration space. BAR4 of each NTB endpoint allows the entire 4 KB configuration space to be memory mapped into PCIe space allowing any master to access configuration registers. The organization of this 4 KB memory is the same as that for the corresponding configuration space.

BAR4 memory mapped configuration space may be accessed using byte, word, or doubleword transactions. The behavior of read or write transactions to this space of any other size, including zero, is undefined. Software should ensure that there are four or less outstanding read transactions to BAR4 mapped memory. Exceeding this number of outstanding transactions may result in completions being dropped.

In some systems it may desirable to prevent modification of NTB configuration by endpoints on the opposite side of the NTB using BAR4 mapped memory. When the Opposite Side Configuration Protection (OSCFGPROT) bit is set in the Non-Transparent Bridge Control (NTBCTL) register, access to the non-transparent bridge configuration capability structure is disabled for this side as well as for the opposite side using a 2KB offset into the configuration window. This means that reading any register in this capability structure, except the NTBCFGC register, returns a value of zero and all writes are ignored. NTBCFGC returns it's default value regardless of the setting of the OSCFGPROT field, allowing normal traversal of the capability structure.

Opposite Side Configuration Requests

The internal endpoint has the capability to generate configuration transactions on the external side of the NTB. This mechanism, referred to as punch through, is provided to facilitate systems in which there does not exist a root on the external side of the NTB. The external endpoint is unable to generate configuration transactions on the internal side of the NTB.

To generate a configuration transaction on the external side of the NTB, an internal endpoint or root should execute the following sequence:

1. Check if the punch through configuration interface is busy by examining the Busy (BUSY) bit in the Punch Through Configuration Status (PTCSTS) register and wait until the interface is not busy.
2. Configure the operation in the Punch Through Configuration Control (PTCCFG) register.
3. Write to the Punch Through Configuration Data (PTCDATA) register to initiate the configuration read or write operation as selected by the OP field in the PTCCFG register.
4. Wait for the operation to complete by examining the status of the Done (DONE) bit in the PTCSTS register.
5. Check the transaction completion status in the Status (STATUS) field of the PTCSTS register. If the initiated transaction was a read and it successfully completed, then the read result may be read from the PTCDATA register.

It is possible for a completion to not be generated in response to a punch-through configuration transaction. A punch-through operation may be aborted by writing a one to the DONE bit in the PTCSTS register. This will cause subsequent completions to be discarded until a new punch-through configuration transaction is generated. This mechanism should only be used when it is certain that a completion is lost and will never arrive.

Configuration Requests

The port C PCI-PCI bridge, internal NTB and external NTB endpoints all have configuration registers that may be accessed with Type 0 configuration read and write requests. PCIe allows multiple outstanding configuration read and write requests. The port C PCI-PCI bridge, internal NTB endpoint and external NTB endpoints each support a maximum of four outstanding configuration requests. Issuing more than four outstanding configuration requests to any of these entities may result in configuration requests being dropped.

Notes

Configuration accesses to different entities within the PES12NT3 may complete out-of-order and may limit the utility of multiple outstanding PCIe configuration accesses. For example, a configuration access that modifies a secondary or subordinate bus number which is immediately followed by a Type 1 configuration access that relies on the modified value for routing may result in an error when issued concurrently, but execute properly when issued in sequence. Configuration accesses to any particular entity always complete in order.

End-to-End CRC

End-to-End CRC (ECRC) is supported for transactions that are forwarded through the NTB. A new ECRC must be computed since the NTB modifies packets. When a transaction is forwarded through the NTB with ECRC enabled, the NTB computes the ECRC for the packet and in parallel computes a new ECRC for the modified packet. At the end of the packet, the NTB compares the computed ECRC for the original packet with that in the original packet. If no error is detected, then the ECRC in the modified packet is replaced with that computed for the new packet.

If an error is detected, then the ECRC in the modified packet is replaced with the inverted value of the ECRC computed for the new packet, the ECRC Error (ECRCERR) bit is set in the Non-Transparent Bridge Status (NTBSTS) register associated with the endpoint on which the packet was received, and a ERR_NONFATAL is generated to the root on which the packet was received if non-fatal error reporting is enabled in the corresponding device control register (i.e., Non-Fatal Error Reporting Enable (NTEREN) bit set in the PCIE_PCIEDCTL or PCEE_PCIEDCTL register).

The NTB does not support ECRC for TLPs that it generates (e.g., configuration responses, INTx messages, etc.). It also does not support ECRC for TLPs it consumes (e.g., configuration requests). However, if a TLP is received with an ECRC, the CRC is discarded and not checked and the transaction is performed.

Error Detection and Handling

This section describes error detection performed by an ingress or egress stack when the switch is configured to operate in non-transparent mode. In non-transparent mode the physical and data link layers are associated with the external NTB endpoint. This section describes error checks performed by these layers. Any error messages that are sent due to a detected errors are sent to the external root (i.e., the root on the external side of port C) and not to the internal root on port A.

Table 9.2 lists error checks performed by the physical layer and action taken when an error is detected.

Error Condition	PCIe Base 1.0a Specification Section	Action Taken
Invalid symbol or running disparity error detected.	4.2.1.3	Correctable error processing
Any TLP or DLLP framing rule violation.	4.2.2.1	Correctable error processing
8b/10b decode error	4.2.4.4	Correctable error processing
Any violation of the link initialization or training protocol	4.2.4	Uncorrectable error processing

Table 9.2 Physical Layer Errors

Table 9.3 lists error checks performed by the data link layer and action taken when an error is detected.

Notes

Error Condition	PCIe Base 1.0a Specification Section	Action Taken
TLP ending in ENDB with LCRC that does not match inverted calculated LCRC	3.5.3.1	TLP discarded
TLP received with incorrect LCRC	3.5.3.1	Correctable error processing
TLP received with sequence number not equal to NEXT_RCV_SEQ and this is not a duplicate TLP	3.5.3.1	Correctable error processing
Bad DLLP[1]	3.5.2.1	Correctable error processing
Replay time-out	3.5.2.1	Correctable error processing
REPLAY NUM rollover	3.5.2.1	Correctable error processing
Violation of flow control initialization protocol	3.3.1	Uncorrectable error processing
Sequence number specified by AckNak_Seq does not correspond to an unacknowledged TLP or to the value in ACKD_SEQ	3.5.2.1	Uncorrectable error processing

Table 9.3 Data Link Layer Errors

1. A bad DLLP is a DLP with a bad LCRC.

In non-transparent mode, any transaction layer related errors associated with the port C PCI-PCI bridge or internal NTB endpoint should have been handled at the ingress stack on which the TLP arrived. This section only lists error checks performed by the transaction layer associated with the external NTB endpoint. Any error messages that are sent due to detected errors are sent to the external root (i.e., the root on the external side of port C) and not to the internal root on port A.

Table 9.4 lists error checks performed by the transaction layer and action taken when an error is detected.

Error Condition	PCIe Base 1.0a Specification Section	Action Taken
ECRC check failure	2.7.1	None. The PES12NT3 does not check ECRC for transactions that terminate in the switch.
Malformed TLP	-	Fatal error processing.
Flow control protocol error	2.6.1	Not applicable. The PES12NT3 does not check for any flow control errors.
Receiver overflow	2.6.1.2	None.
Completer abort Completion time-out	2.3.1 2.8	Not applicable. The PES12NT3 never generates non-posted transactions.
Unsupported request	2.3.1	See section Switch Core Errors on page 4-7 and section Interrupts on page 4-5.
Unexpected completion	2.3.2	Non-fatal error processing.

Table 9.4 Transaction Layer Errors

Notes

Table 9.5 lists the error checks performed by the transaction layer for malformed TLPs.

TLP error checks are only performed when a TLP is received by the switch (i.e., by the stack associated with the port on which the switch receives the TLP). No checks are made for malformed TLPs inside the switch.

The Max_Payload_Size (MPS field in PCIEDCTL) must be the same for all devices which generate or receive transactions that flow through the non-transparent bridge. As a result, the MPS field should be set to the same value on both the internal and external sides of the non-transparent bridge and on any ingress port that receives transactions destined to the non-transparent bridge (since error checks are only performed when a TLP is received by the switch).

TLP Type	Error Check
All	LENGTH < Max_Payload_Size (i.e., MPS field in PCIEDCTL register)
I/O read request	LENGTH = 1 (doubleword) TC = 0, ATTR = 0 The actual packet length is correct (4 doublewords when CRC is present, 3doublewords otherwise)
I/O write request	LENGTH = 1 (doubleword) TC = 0 ATTR = 0 The actual packet length is correct (5 doublewords when CRC is present, 4 doublewords otherwise)
Configuration read request	LENGTH = 1 (doubleword) TC = 0, ATTR = 0 The actual packet length is correct (4 doublewords when CRC is present, 3 doublewords otherwise)
Configuration write request	LENGTH = 1 (doubleword) TC = 0 ATTR = 0 The actual packet length is correct (5 doublewords when CRC is present, 4 doublewords otherwise)
Memory read request (32- and 64-bit address mode)	The packet length is correct. 32-bit address mode: 3 doublewords when ECRC is present, 4 doublewords otherwise 64-bit address mode: 4 doublewords when ECRC is present, 5 doublewords otherwise

Table 9.5 Malformed TLP Error Checks (Part 1 of 2)

Notes

TLP Type	Error Check
Memory write request (32- and 64-bit address mode)	The packet length is correct. 32-bit address mode: - Number of doublewords received equals LENGTH + 4 when ECRC is present - Number of doublewords received equals LENGTH + 3 when a packet does not contain ECRC 64-bit address mode -Number of doublewords received equals LENGTH + 5 when ECRC is present - Number of doublewords received equals LENGTH + 4 when a packet does not contain ECRC
Completion with data	The packet length is correct. - Number of doublewords received equals LENGTH + 3 when a packet does not contain ECRC - Number of doublewords received equals LENGTH + 4 when ECRC is present - Number of doublewords received is not greater then MaxPayloadSize + 3/4
Message or message with data	The actual packet length is correct: - Number of received double words equals LENGTH + 4 when a packet does not contain ECRC - Number of received double words equals LENGTH + 5 when ECRC is present - Number of received doublewords is not greater then MaxPayloadSize + 4/5
Interrupt messages Power management messages Error signalling messages Unlock message Set slot power limit message	TC = 0 (a message of this type is considered a malformed TLP if it uses a traffic class designator other than TC0)

Table 9.5 Malformed TLP Error Checks (Part 2 of 2)

In addition to the switch core errors outlined in section Switch Core Errors on page 4-7, reception of the following TLPs by the internal or external NTB endpoints are treated as an Unsupported Request (UR) by the endpoint on which the TLP was received.

- Reception of route by address TLPs that have no route (i.e., do not match any of the BAR register windows of the endpoint)
- Reception of CfgRd1 or CfgWr1 TLPs

Power Management

The power management state of internal and external side of the non-transparent bridge may be determined by reading the PSTATE field in the PMCSR register associated with that non-transparent bridge endpoint. Whenever the PSTATE field is modified, the Opposite Side Power State Modified (OSPSTATEM) bit is set in the INTSTS register on the opposite side of the NTB. This may be used to signal an interrupt.

Notes

When an NTB endpoint's PSTATE field is set to $D3_{hot}$, the endpoint does not initiate bus transactions (i.e., transactions destined to that side of the NTB are dropped) and does not respond to transactions other than PCIe configuration transactions. All transactions other than PME_Turn_Off and configuration transactions received by an endpoint in the $D3_{hot}$ state are dropped and treated as unsupported requests. Unsupported request processing may result in the NTB endpoint initiating a completion and/or error message.

When the external NTB endpoint's power management state is set to $D3_{hot,}$ the port C external link attempts to enter the L1 state. In a PES12NT3 NTB to NTB link configuration, the two external NTB endpoints behave as downstream components. Therefore, neither NTB endpoint should be placed in a $D3_{hot}$ state since the L1 entry protocol for low power states is only defined between an upstream and a downstream component

Transitioning an NTB endpoint's power management state from $D3_{hot}$ to $D0_{uninitialized}$ does not result in any logic being reset or re-initialization of register values.

Both sides of the non-transparent bridge participate in the power fence protocol and respond to PME_Turn_Off messages with a PME_TO_ACK message. The message is sent in the direction from which the PME_Turn_Off message was received. Between the port C transparent bridge and the internal NTB endpoint is a virtual link. Capability, control and status registers associated with this link indicate that ASPM is implement and supported; however, since this is a virtual link internal to the device, no actual ASPM takes place.

Initializing the Non-Transparent Bridge

For memory transactions to be routed from the internal virtual PCI bus of the switch and out the port C link the following configuration should be performed.

- The Memory Access Enable (MAE) bit should be set in the PC_PCICMD register to enable the port C PCI-PCI bridge to forward memory transactions.
- The Memory Access Enable (MAE) bit should be set in the PCIE_PCICMD register to enable the internal endpoint of the non-transparent bridge to forward memory transactions.
- The Bus Master Enable (BME) bit should be set in the PCEE_PCICMD register to enable the external endpoint of the non-transparent bridge to generate transactions on the external link.
- In addition, the appropriate base, limit and BAR fields must be configured.

For I/O transactions to be routed from the internal virtual PCI bus of the switch and out the port C link the following configuration should be performed.

- The I/O Access Enable (IOAE) bit should be set in the PC_PCICMD register to enable the port C PCI-PCI bridge to forward I/O transactions.
- The I/O Access Enable (IOAE) bit should be set in the PCIE_PCICMD register to enable the internal endpoint of the non-transparent bridge to forward I/O transactions.
- The Bus Master Enable (BME) bit should be set in the PCEE_PCICMD register to enable the external endpoint of the non-transparent bridge to generate transactions on the external link.
- In addition, the appropriate base, limit and BAR fields must be configured.

For memory transactions to be routed from the external port C link to the internal virtual PCI bus of the switch the following configuration should be performed.

- The Memory Access Enable (MAE) bit should be set in the PCEE_PCICMD register to enable the external endpoint of the non-transparent bridge to forward memory transactions into the switch.
- The Bus Master Enable (BME) bit should be set in the PCIE_PCICMD register to enable the internal endpoint of the non-transparent bridge to generate transactions on the virtual PCIe link connecting the non-transparent bridge and the PCI-PCI bridge.
- The Bus Master Enable (BME) bit should be set in the PCI_PCICMD register to enable the port C PCI-PCI bridge to generate transactions on the virtual PCI bus within the switch.
- In addition, the appropriate base, limit and BAR fields must be configured.

Notes

For I/O transactions to be routed from the external port C link to the internal virtual PCI bus of the switch the following configuration should be performed.

- The I/O Access Enable (IOAE) bit should be set in the PCEE_PCICMD register to enable the external endpoint of the non-transparent bridge to forward I/O transactions into the switch.
- The Bus Master Enable (BME) bit should be set in the PCIE_PCICMD register to enable the internal endpoint of the non-transparent bridge to generate transactions on the virtual PCIe link connecting the non-transparent bridge and the PCI-PCI bridge.
- The Bus Master Enable (BME) bit should be set in the PCI_PCICMD register to enable the port C PCI-PCI bridge to generate transactions on the virtual PCI bus within the switch.
- In addition, the appropriate base, limit and BAR fields must be configured.

Notes

Ports A and B Configuration Space Organization

The organization of ports A and B configuration space is shown in Figure 9.6. Both ports share the same basic layout.

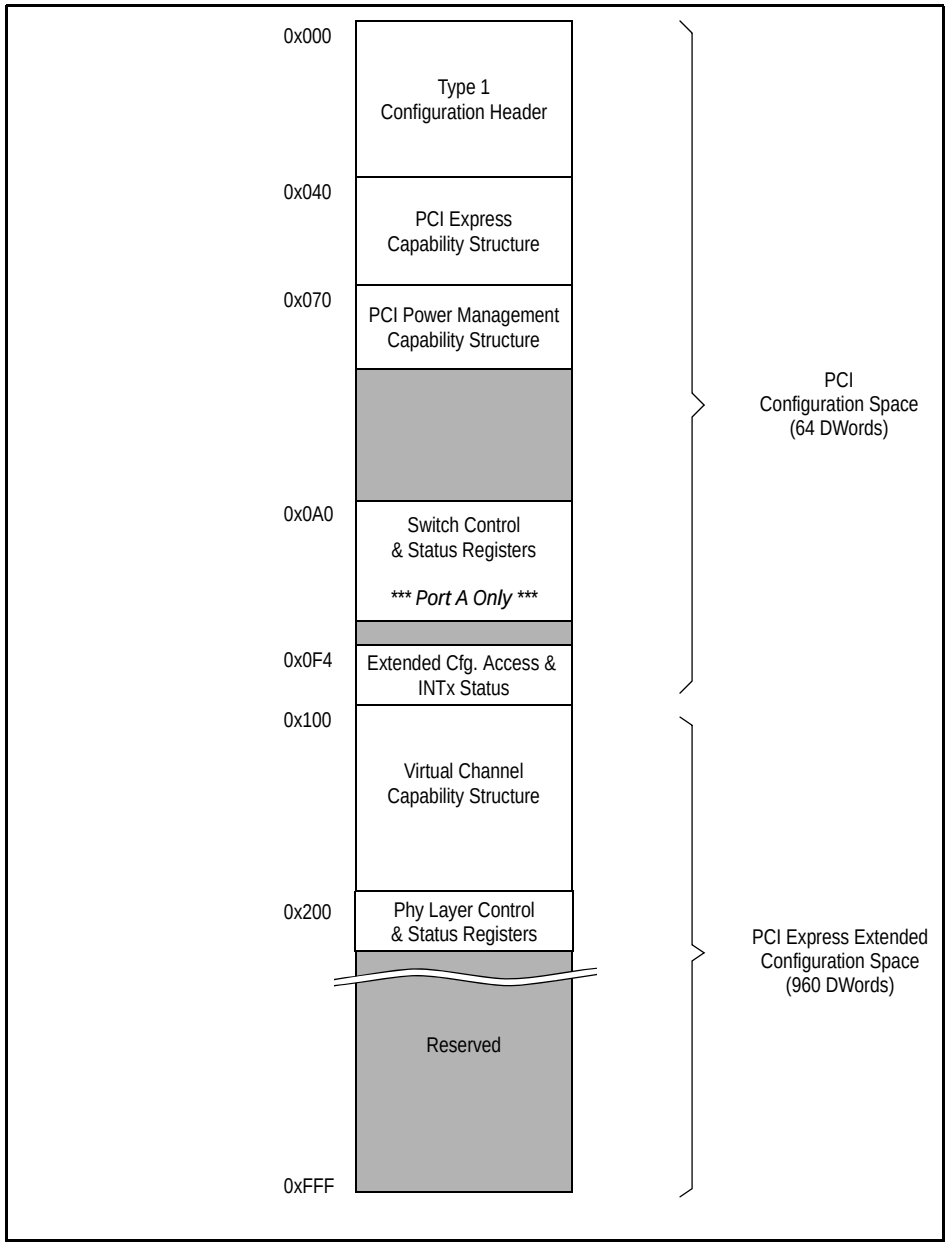

Figure 9.6 Configuration Space Organization for Ports A and B

Note: In pdf format, clicking on a register name in the Register Definition column creates a jump to the appropriate register. To return to the starting place in this table, click on the same register name (in blue) in the register section.

Notes

Upstream Port A Configuration Space Registers

All configuration space locations not listed in Table 9.6 return a value of zero when read. Writes to these locations are ignored and have no side-effects. Port A configuration space registers may be read and written via the slave SMBus interface and initialized from the serial EEPROM using the CSR system address formed by adding the base address 0x0000 to the PCI configuration space offset address.

Note: In pdf format, clicking on a register name in the Register Definition column creates a jump to the appropriate register. To return to the starting place in this table, click on the same register name (in blue) in the register section.

Cfg. Offset	Size	Register Mnemonic	Register Definition
0x000	Word	PA_VID	VID - Vendor Identification (0x000) on page 9-23
0x002	Word	PA_DID	DID - Device Identification (0x002) on page 9-23
0x004	Word	PA_PCICMD	PCICMD - PCI Command (0x004) on page 9-24
0x006	Word	PA_PCISTS	PCISTS - PCI Status (0x006) on page 9-25
0x008	Byte	PA_RID	RID - Revision Identification (0x008) on page 9-26
0x009	3 Bytes	PA_CCODE	CCODE - Class Code (0x009) on page 9-26
0x00C	Byte	PA_CLS	CLS - Cache Line Size (0x00C) on page 9-26
0x00D	Byte	PA_PLTIMER	PLTIMER - Primary Latency Timer (0x00D) on page 9-26
0x00E	Byte	PA_HDR	HDR - Header Type (0x00E) on page 9-26
0x00F	Byte	PA_BIST	BIST - Built-in Self Test (0x00F) on page 9-27
0x010	DWord	PA_BAR0	BAR0 - Base Address Register 0 (0x010) on page 9-27
0x014	DWord	PA_BAR1	BAR1 - Base Address Register 1 (0x014) on page 9-27
0x018	Byte	PA_PBUSN	PBUSN - Primary Bus Number Register (0x018) on page 9-27
0x019	Byte	PA_SBUSN	SBUSN - Secondary Bus Number Register (0x019) on page 9-27
0x01A	Byte	PA_SUBUSN	SUBUSN - Subordinate Bus Number Register (0x01A) on page 9-27
0x01B	Byte	PA_SLTIMER	SLTIMER - Secondary Latency Timer Register (0x01B) on page 9-28
0x01C	Byte	PA_IOBASE	IOBASE - I/O Base Register (0x01C) on page 9-28
0x01D	Byte	PA_IOLIMIT	IOLIMIT - I/O Limit Register (0x01D) on page 9-28
0x01E	Word	PA_SECSTS	SECSTS - Secondary Status (0x01E) on page 9-28
0x020	Word	PA_MBASE	MBASE - Memory Base (0x020) on page 9-29
0x022	Word	PA_MLIMIT	MLIMIT - Memory Limit (0x022) on page 9-29
0x024	Word	PA_PMBASE	PMBASE - Prefetchable Memory Base (0x024) on page 9-30
0x026	Word	PA_PMLIMIT	PMLIMIT - Prefetchable Memory Limit (0x026) on page 9-30
0x028	DWord	PA_PMBASEU	PMBASEU - Prefetchable Memory Base Upper (0x028) on page 9-31
0x02C	DWord	PA_PMLIMITU	PMLIMITU - Prefetchable Memory Limit Upper (0x02C) on page 9-31

Table 9.6 Upstream Port A Configuration Space Registers (Part 1 of 3)

Notes

Cfg. Offset	Size	Register Mnemonic	Register Definition
0x030	Word	PA_IOBASEU	IOBASEU - I/O Base Upper (0x030) on page 9-31
0x032	Word	PA_IOLIMITU	IOLIMITU - I/O Limit Upper (0x032) on page 9-31
0x034	Byte	PA_CAPPTR	CAPPTR - Capabilities Pointer (0x034) on page 9-31
0x038	DWord	PA_EROMBASE	EROMBASE - Expansion ROM Base Address Register (0x038) on page 9-32
0x03C	Byte	PA_INTRLINE	INTRLINE - Interrupt Line (0x03C) on page 9-32
0x03D	Byte	PA_INTRPIN	INTRPIN - Interrupt PIN (0x03D) on page 9-32
0x03E	Word	PA_BCTRL	BCTRL - Bridge Control Register (0x03E) on page 9-32
0x040	DWord	PA_PCIECAP	PCIECAP - PCI Express Capability (0x040) on page 9-33
0x044	DWord	PA_PCIEDCAP	PCIEDCAP - PCI Express Device Capabilities (0x044) on page 9-34
0x048	Word	PA_PCIEDCTL	PCIEDCTL - PCI Express Device Control (0x048) on page 9-34
0x04A	Word	PA_PCIEDSTS	PCIEDSTS - PCI Express Device Status (0x04A) on page 9-36
0x04C	DWord	PA_PCIELCAP	PCIELCAP - PCI Express Link Capabilities (0x04C) on page 9-36
0x050	Word	PA_PCIELCTL	PCIELCTL - PCI Express Link Control (0x050) on page 9-37
0x052	Word	PA_PCIELSTS	PCIELSTS - PCI Express Link Status (0x052) on page 9-38
0x070	DWord	PA_PMCAP	PMCAP - PCI Power Management Capabilities (0x070) on page 9-40
0x074	DWord	PA_PMCSR	PMCSR - PCI Power Management Control and Status (0x074) on page 9-41
0x078	DWord	PA_PMPC	PMPC - PCI Power Management Proprietary Control (0x078) on page 9-42
0x0A0	DWord	PA_SWSTS	SWSTS - Switch Status (0x0A0) on page 9-44
0x0A4	DWord	PA_SWCTL	SWCTL - Switch Control (0x0A4) on page 9-45
0x0A8	DWord	PA_GPIOCS	GPIOCS - General Purpose I/O Control and Status (0x0A8) on page 9-46
0x0AC	DWord	PA_SMBUSSTS	SMBUSSTS - SMBus Status (0x0AC) on page 9-47
0x0B0	DWord	PA_SMBUSCTL	SMBUSCTL - SMBus Control (0x0B0) on page 9-48
0x0B4	DWord	PA_EEPROMINTF	EEPROMINTF - Serial EEPROM Interface (0x0B4) on page 9-49
0x0F4	Word	PA_INTSTS	PA_INTSTS - Interrupt Status (0x0F4) on page 9-50
0x0F8	DWord	PA_ECFGADDR	ECFGADDR - Extended Configuration Space Access Address (0x0F8) on page 9-50
0x0FC	DWord	PA_ECFGDATA	ECFGDATA - Extended Configuration Space Access Data (0x0FC) on page 9-51
0x100	DWord	PA_PCIEVCECAP	PCIEVCECAP - PCI Express Virtual Channel Enhanced Capability Header (0x100) on page 9-51
0x104	DWord	PA_PVCCAP1	PVCCAP1- Port VC Capability 1 (0x104) on page 9-51
0x110	DWord	PA_VCR0CAP	VCR0CAP- VC Resource 0 Capability (0x110) on page 9-52

Table 9.6 Upstream Port A Configuration Space Registers (Part 2 of 3)

Notes

Cfg. Offset	Size	Register Mnemonic	Register Definition
0x114	DWord	PA_VCR0CTL	VCR0CTL- VC Resource 0 Control (0x114) on page 9-52
0x118	DWord	PA_VCR0STS	VCR0STS - VC Resource 0 Status (0x118) on page 9-53
0x120	DWord	PA_VCR0TBL0	VCR0TBL0 - VC Resource 0 Arbitration Table Entry 0 (0x120) on page 9-54
0x124	DWord	PA_VCR0TBL1	VCR0TBL1 - VC Resource 0 Arbitration Table Entry 1 (0x124) on page 9-55
0x200	DWord	PA_SERDESCTL	SERDESCTL - SerDes Control (0x200) on page 9-56
0x204—0x61C			Reserved

Table 9.6 Upstream Port A Configuration Space Registers (Part 3 of 3)

Downstream Port B Configuration Space Registers

All configuration space locations not listed in Table 9.7 return a value of zero when read. Writes to these locations are ignored and have no side-effects.Port B configuration space registers may be read and written via the slave SMBus interface and initialized from the serial EEPROM using the CSR system address formed by adding the base address 0x1000 to the PCI configuration space offset address.

Note: In pdf format, clicking on a register name in the Register Definition column creates a jump to the appropriate register. To return to the starting place in this table, click on the same register name (in blue) in the register section.

Cfg. Offset	Size	Register Mnemonic	Register Definition
0x000	Word	PB_VID	VID - Vendor Identification (0x000) on page 9-23
0x002	Word	PB_DID	DID - Device Identification (0x002) on page 9-23
0x004	Word	PB_PCICMD	PCICMD - PCI Command (0x004) on page 9-24
0x006	Word	PB_PCISTS	PCISTS - PCI Status (0x006) on page 9-25
0x008	Byte	PB_RID	RID - Revision Identification (0x008) on page 9-26
0x009	3 Bytes	PB_CCODE	CCODE - Class Code (0x009) on page 9-26
0x00C	Byte	PB_CLS	CLS - Cache Line Size (0x00C) on page 9-26
0x00D	Byte	PB_PLTIMER	PLTIMER - Primary Latency Timer (0x00D) on page 9-26
0x00E	Byte	PB_HDR	HDR - Header Type (0x00E) on page 9-26
0x00F	Byte	PB_BIST	BIST - Built-in Self Test (0x00F) on page 9-27
0x010	DWord	PB_BAR0	BAR0 - Base Address Register 0 (0x010) on page 9-27
0x014	DWord	PB_BAR1	BAR1 - Base Address Register 1 (0x014) on page 9-27
0x018	Byte	PB_PBUSN	PBUSN - Primary Bus Number Register (0x018) on page 9-27
0x019	Byte	PB_SBUSN	SBUSN - Secondary Bus Number Register (0x019) on page 9-27

Table 9.7 Downstream Port B Configuration Space Registers (Part 1 of 3)

Notes

Cfg. Offset	Size	Register Mnemonic	Register Definition
0x01A	Byte	PB_SUBUSN	SUBUSN - Subordinate Bus Number Register (0x01A) on page 9-27
0x01B	Byte	PB_SLTIMER	SLTIMER - Secondary Latency Timer Register (0x01B) on page 9-28
0x01C	Byte	PB_IOBASE	IOBASE - I/O Base Register (0x01C) on page 9-28
0x01D	Byte	PB_IOLIMIT	IOLIMIT - I/O Limit Register (0x01D) on page 9-28
0x01E	Word	PB_SECSTS	SECSTS - Secondary Status (0x01E) on page 9-28
0x020	Word	PB_MBASE	MBASE - Memory Base (0x020) on page 9-29
0x022	Word	PB_MLIMIT	MLIMIT - Memory Limit (0x022) on page 9-29
0x024	Word	PB_PMBASE	PMBASE - Prefetchable Memory Base (0x024) on page 9-30
0x026	Word	PB_PMLIMIT	PMLIMIT - Prefetchable Memory Limit (0x026) on page 9-30
0x028	DWord	PB_PMBASEU	PMBASEU - Prefetchable Memory Base Upper (0x028) on page 9-31
0x02C	DWord	PB_PMLIMITU	PMLIMITU - Prefetchable Memory Limit Upper (0x02C) on page 9-31
0x030	Word	PB_IOBASEU	IOBASEU - I/O Base Upper (0x030) on page 9-31
0x032	Word	PB_IOLIMITU	IOLIMITU - I/O Limit Upper (0x032) on page 9-31
0x034	Byte	PB_CAPPTR	CAPPTR - Capabilities Pointer (0x034) on page 9-31
0x038	DWord	PB_EROMBASE	EROMBASE - Expansion ROM Base Address Register (0x038) on page 9-32
0x03C	Byte	PB_INTRLINE	INTRLINE - Interrupt Line (0x03C) on page 9-32
0x03D	Byte	PB_INTRPIN	INTRPIN - Interrupt PIN (0x03D) on page 9-32
0x03E	Word	PB_BCTRL	BCTRL - Bridge Control Register (0x03E) on page 9-32
0x040	DWord	PB_PCIECAP	PCIECAP - PCI Express Capability (0x040) on page 9-33
0x044	DWord	PB_PCIEDCAP	PCIEDCAP - PCI Express Device Capabilities (0x044) on page 9-34
0x048	Word	PB_PCIEDCTL	PCIEDCTL - PCI Express Device Control (0x048) on page 9-34
0x04A	Word	PB_PCIEDSTS	PCIEDSTS - PCI Express Device Status (0x04A) on page 9-36
0x04C	DWord	PB_PCIELCAP	PCIELCAP - PCI Express Link Capabilities (0x04C) on page 9-36
0x050	Word	PB_PCIELCTL	PCIELCTL - PCI Express Link Control (0x050) on page 9-37
0x052	Word	PB_PCIELSTS	PCIELSTS - PCI Express Link Status (0x052) on page 9-38
0x054	DWord	PB_PCIESCAP	PCIESCAP - PCI Express Slot Capabilities (0x054) on page 9-38
0x058	Word	PB_PCIESCTL	PCIESCTL - PCI Express Slot Control (0x058) on page 9-39
0x05A	Word	PB_PCIESSTS	PCIESSTS - PCI Express Slot Status (0x5A) on page 9-40
0x070	DWord	PB_PMCAP	PMCAP - PCI Power Management Capabilities (0x070) on page 9-40

Table 9.7 Downstream Port B Configuration Space Registers (Part 2 of 3)

Notes

Cfg. Offset	Size	Register Mnemonic	Register Definition
0x074	DWord	PB_PMCSR	PMCSR - PCI Power Management Control and Status (0x074) on page 9-41
0x078	DWord	PB_PMPC	PMPC - PCI Power Management Proprietary Control (0x078) on page 9-42
0x0F4	Word	PA_INTSTS	PA_INTSTS - Interrupt Status (0x0F4) on page 9-50
0x0F8	DWord	PB_ECFGADDR	ECFGADDR - Extended Configuration Space Access Address (0x0F8) on page 9-50
0x0FC	DWord	PB_ECFGDATA	ECFGDATA - Extended Configuration Space Access Data (0x0FC) on page 9-51
0x100	DWord	PB_PCIEVCECAP	PCIEVCECAP - PCI Express Virtual Channel Enhanced Capability Header (0x100) on page 9-51
0x104	DWord	PB_PVCCAP1	PVCCAP1- Port VC Capability 1 (0x104) on page 9-51
0x110	DWord	PB_VCR0CAP	VCR0CAP- VC Resource 0 Capability (0x110) on page 9-52
0x114	DWord	PB_VCR0CTL	VCR0CTL- VC Resource 0 Control (0x114) on page 9-52
0x118	DWord	PB_VCR0STS	VCR0STS - VC Resource 0 Status (0x118) on page 9-53
0x120	DWord	PB_VCR0TBL0	VCR0TBL0 - VC Resource 0 Arbitration Table Entry 0 (0x120) on page 9-54
0x124	DWord	PB_VCR0TBL1	VCR0TBL1 - VC Resource 0 Arbitration Table Entry 1 (0x124) on page 9-55
0x200	DWord	PB_SERDESCTL	SERDESCTL - SerDes Control (0x200) on page 9-56
0x204 — 0x61C			Reserved

Table 9.7 Downstream Port B Configuration Space Registers (Part 3 of 3)

Generic PCI to PCI Bridge Registers

VID - Vendor Identification (0x000)

Bit Field	Field Name	Type	Default Value	Description
15:0	VID	RO	0x111D	Vendor Identification. This field contains the 16-bit vendor ID value assigned to IDT. See section Vendor ID on page 1-4.

DID - Device Identification (0x002)

Bit Field	Field Name	Type	Default Value	Description
15:0	DID	RO	-	Device Identification. This field contains the 16-bit device ID assigned by IDT to this non-transparent bridge. See section Device ID on page 1-4.

Notes

PCICMD - PCI Command (0x004)

Bit Field	Field Name	Type	Default Value	Description
0	IOAE	RW	0x0	I/O Access Enable. When this bit is cleared, the bridge does not respond to I/O accesses from the primary bus specified by IOBASE and IOLIMIT. 0x0 - (disable) Disable I/O space. 0x1 - (enable) Enable I/O space.
1	MAE	RW	0x0	Memory Access Enable. When this bit is cleared, the bridge does not respond to memory and prefetchable memory space access from the primary bus specified by MBASE, MLIMIT, PMBASE and PMLIMIT. 0x0 - (disable) Disable memory space. 0x1 - (enable) Enable memory space.
2	BME	RW	0x0	Bus Master Enable. When this bit is cleared, the bridge does not issue requests (e.g., memory, I/O and MSIs since they are in-band writes) on behalf of subordinate devices and responds to non-posted transactions with a Unsupported Request (UR) completion. This bit does not affect completions in either direction or the forwarding of non memory or I/O requests. 0x0 - (disable) Disable request forwarding. 0x1 - (enable) Enable request forwarding.
3	SSE	RO	0x0	Special Cycle Enable. Not applicable.
4	MWI	RO	0x0	Memory Write Invalidate. Not applicable.
5	VGAS	RO	0x0	VGA Palette Snoop. Not applicable.
6	PERRE	RW	0x0	Parity Error Enable. The Master Data Parity Error bit is set in the PCI Status register (PCISTS) if this bit is set and the bridge receives a poisoned completion or a poisoned write. If this bit is cleared, then the Master Data Parity Error bit in the PCI Status register is never set. 0x0 - (disable) Disable Master Parity Error bit reporting. 0x1 - (enable) Enable Master Parity Error bit reporting.
7	ADSTEP	RO	0x0	Address Data Stepping. Not applicable.
8	SERRE	RW	0x0	SERR Enable. Non-fatal and fatal errors detected by the bridge are reported to the Root Complex when this bit is set or the bits in the PCI Express Device Control register are set (see PCEE_PCIEDCTL - PCI Express Device Control (0x048)). 0x0 - (disable) Disable non-fatal and fatal error reporting if also disabled in Device Control register. 0x1 - (enable) Enable non-fatal and fatal error reporting.
9	FB2B	RO	0x0	Fast Back-to-Back Enable. Not applicable.
10	INTXD	RW	0x0	INTx Disable. Controls the ability of the PCI-PCI bridge to generate an INTx interrupt message.
15:11	Reserved	RO	0x0	Reserved field.

Notes

PCISTS - PCI Status (0x006)

Bit Field	Field Name	Type	Default Value	Description
2:0	Reserved	RO	0x0	Reserved field.
3	INTS	RO	0x0	INTx Status. This bit is set when an INTx interrupt is pending from the device. INTx emulation interrupts forwarded by switch ports from devices downstream of the bridge are not reflected in this bit. For all ports, this field is always zero.
4	CAPL	RO	0x1	Capabilities List. This bit is hardwired to one to indicate that the bridge implements an extended capability list item.
5	C66MHZ	RO	0x0	66 MHz Capable. Not applicable.
6	Reserved	RO	0x0	Reserved field.
7	FB2B	RO	0x0	Fast Back-to-Back (FB2B). Not applicable.
8	MDPED	RW1C	0x0	Master Data Parity Error Detected. This bit is set when the PERRE bit is set in the PCI Command register and the bridge receives a poisoned completion or poisoned write request on the primary side of the bridge. 0x0 -(noerror) no error. 0x1 - (error) Poisoned write request or completion received on primary side.
10:9	DEVT	RO	0x0	DEVSEL# Timing. Not applicable.
11	STAS	RO	0x0	Signalled Target Abort. Not applicable since a target abort is never signalled.
12	RTAS	RO	0x0	Received Target Abort. Not applicable.
13	RMAS	RO	0x0	Received Master Abort. Not applicable.
14	SSE	RW1C	0x0	Signalled System Error. This bit is set when the bridge sends a ERR_FATAL or ERR_NONFATAL message and the SERR Enable (SERRE) bit is set in the PCICMD register. 0x0 - (noerror) no error. 0x1 - (error) This bit is set when a fatal or non-fatal error is signalled.
15	DPE	RW1C	0x0	Detected Parity Error. This bit is set by the bridge whenever it receives a poisoned TLP on the primary side regardless of the state of the PERRE bit in the PCI Command register. For downstream ports, this bit is also set when a internal switch parity error is detected. See section Data Integrity on page 4-4.

Notes

RID - Revision Identification (0x008)

Bit Field	Field Name	Type	Default Value	Description
7:0	RID	RWL	-	**Revision ID.** This field contains the revision identification number for the device. See section Revision ID on page 1-5.

CCODE - Class Code (0x009)

Bit Field	Field Name	Type	Default Value	Description
7:0	INTF	RO	0x00	**Interface.** This value indicates that the device is a PCI-PCI bridge that does not support subtractive decode.
15:8	SUB	RO	0x04	**Sub Class Code.** This value indicates that the device is a PCI-PCI bridge.
23:16	BASE	RO	0x06	**Base Class Code.** This value indicates that the device is a bridge.

CLS - Cache Line Size (0x00C)

Bit Field	Field Name	Type	Default Value	Description
7:0	CLS	RW	0x00	**Cache Line Size.** This field has no effect on the bridge's functionality but may be read and written by software. This field is implemented for compatibility with legacy software.

PLTIMER - Primary Latency Timer (0x00D)

Bit Field	Field Name	Type	Default Value	Description
7:0	PLTIMER	RO	0x00	**Primary Latency Timer.** Not applicable.

HDR - Header Type (0x00E)

Bit Field	Field Name	Type	Default Value	Description
7:0	HDR	RO	0x01	**Header Type.** This value indicates a type 1 header with a single function bridge layout.

Notes

BIST - Built-in Self Test (0x00F)

Bit Field	Field Name	Type	Default Value	Description
7:0	BIST	RO	0x0	**BIST.** This value indicates that the bridge does not implement BIST.

BAR0 - Base Address Register 0 (0x010)

Bit Field	Field Name	Type	Default Value	Description
31:0	BAR	RO	0x0	**Base Address Register.** Not applicable.

BAR1 - Base Address Register 1 (0x014)

Bit Field	Field Name	Type	Default Value	Description
31:0	BAR	RO	0x0	**Base Address Register.** Not applicable.

PBUSN - Primary Bus Number Register (0x018)

Bit Field	Field Name	Type	Default Value	Description
7:0	PBUSN	RW	0x0	**Primary Bus Number.** This field is used to record the bus number of the PCI bus segment to which the primary interface of the bridge is connected.

SBUSN - Secondary Bus Number Register (0x019)

Bit Field	Field Name	Type	Default Value	Description
7:0	SBUSN	RW	0x0	**Secondary Bus Number.** This field is used to record the bus number of the PCI bus segment to which the secondary interface of the bridge is connected.

SUBUSN - Subordinate Bus Number Register (0x01A)

Bit Field	Field Name	Type	Default Value	Description
7:0	SUBUSN	RW	0x0	**Subordinate Bus Number.** The Subordinate Bus Number register is used to record the bus number of the highest numbered PCI bus segment which is behind (or subordinate to) the bridge.

Notes

SLTIMER - Secondary Latency Timer Register (0x01B)

Bit Field	Field Name	Type	Default Value	Description
7:0	SLTIMER	RO	0x0	Secondary Latency Timer. Not applicable.

IOBASE - I/O Base Register (0x01C)

Bit Field	Field Name	Type	Default Value	Description
0	IOCAP	RWL	0x1	I/O Capability. Indicates if the bridge supports 16-bit or 32-bit I/O addressing. 0x0 - (io16) 16-bit I/O addressing. 0x1 - (io32) 32-bit I/O addressing.
3:1	Reserved	RO	0x0	Reserved field.
7:4	IOBASE	RW	0xF	I/O Base. The IOBASE and IOLIMIT registers are used to control the forwarding of I/O transactions between the primary and secondary interfaces of the bridge. This field contains A[15:12] of the lowest I/O address aligned on a 4KB boundary that is below the primary interface of the bridge.

IOLIMIT - I/O Limit Register (0x01D)

Bit Field	Field Name	Type	Default Value	Description
0	IOCAP	RO	0x1	I/O Capability. Indicates if the bridge supports 16-bit or 32-bit I/O addressing. This bit always reflects the value of the IOCAP field in the IOBASE register.
3:1	Reserved	RO	0x0	Reserved field.
7:4	IOLIMIT	RW	0x0	I/O Limit. The IOBASE and IOLIMIT registers are used to control the forwarding of I/O transactions between the primary and secondary interfaces of the bridge. This field contains A[15:12] of the highest I/O address, with A[11:0] assumed to be 0xFFF, that is below the primary interface of the bridge.

SECSTS - Secondary Status (0x01E)

Bit Field	Field Name	Type	Default Value	Description
7:0	Reserved	RO	0x0	Reserved field.

Notes

Bit Field	Field Name	Type	Default Value	Description
8	MDPED	RW1C	0x0	Master Data Parity Error. This bit is set when the PERRE bit is set in the PCI Command register and the bridge receives a poisoned completion or generates a poisoned write request on the secondary side of the bridge. 0x0 - (noerror) no error. 0x1 - (error) poisoned write request or completion received on primary side.
10:9	DVSEL	RO	0x0	Not applicable.
11	STAS	RO	0x0	Signalled Target Abort Status. Not applicable.
12	RTAS	RO	0x0	Received Target Abort Status. Not applicable.
13	RMAS	RO	0x0	Received Master Abort Status. Not applicable.
14	SSE	RW1C	0x0	Signalled System Error. This bit is controlled by the SERR enable bit in the Bridge Control (BCTRL) register. If the SERRE bit is cleared in BCTRL, then this bit is never set. Otherwise, this bit is set if the secondary side of the bridge receives an ERR_FATAL or ERR_NONFATAL message.
15	DPE	RW1C	0x0	Detected Parity Error. This bit is set by the bridge whenever it receives a poisoned TLP on the secondary side regardless of the state of the PERRE bit in the PCI Command register For the upstream port, this bit is also set when a internal switch parity error is detected. See section Data Integrity on page 4-4.

MBASE - Memory Base (0x020)

Bit Field	Field Name	Type	Default Value	Description
3:0	Reserved	RO	0x0	Reserved field.
15:4	MBASE	RW	0xFFF	Memory Address Base. The MBASE and MLIMIT registers are used to control the forwarding of non-prefetchable transactions between the primary and secondary interfaces of the bridge. This field contains A[31:20] of the lowest address aligned on a 1MB boundary that is below the primary interface of the bridge.

MLIMIT - Memory Limit (0x022)

Bit Field	Field Name	Type	Default Value	Description
3:0	Reserved	RO	0x0	Reserved field.

Notes

Bit Field	Field Name	Type	Default Value	Description
15:4	MLIMIT	RW	0x0	Memory Address Limit. The MBASE and MLIMIT registers are used to control the forwarding of non-prefetchable transactions between the primary and secondary interfaces of the bridge. This field contains A[31:20] of the highest address, with A[19:0] assumed to be 0xF_FFFF, that is below the primary interface of the bridge.

PMBASE - Prefetchable Memory Base (0x024)

Bit Field	Field Name	Type	Default Value	Description
0	PMCAP	RWL	0x1	Prefetchable Memory Capability. Indicates if the bridge supports 32-bit or 64-bit prefetchable memory addressing. 0x0 - (prefmem32) 32-bit prefetchable memory addressing. 0x1 - (prefmem64) 64-bit prefetchable memory addressing.
3:1	Reserved	RO	0x0	Reserved field.
15:4	PMBASE	RW	0xFFF	Prefetchable Memory Address Base. The PMBASE, PMBASEU, PMLIMIT and PMLIMITU registers are used to control the forwarding of prefetchable transactions between the primary and secondary interfaces of the bridge. This field contains A[31:20] of the lowest memory address aligned on a 1MB boundary that is below the primary interface of the bridge. PMBASEU specifies the remaining bits.

PMLIMIT - Prefetchable Memory Limit (0x026)

Bit Field	Field Name	Type	Default Value	Description
0	PMCAP	RO	0x1	Prefetchable Memory Capability. Indicates if the bridge supports 32-bit or 64-bit prefetchable memory addressing. This bit always reflects the value in the PMCAP field in the PMBASE register.
3:1	Reserved	RO	0x0	Reserved field.
15:4	PMLIMIT	RW	0x0	Prefetchable Memory Address Limit. The PMBASE, PMBASEU, PMLIMIT and PMLIMITU registers are used to control the forwarding of prefetchable transactions between the primary and secondary interfaces of the bridge. This field contains A[31:20] of the highest memory address, with A[19:0] assumed to be 0xF_FFFF, that is below the primary interface of the bridge. PMLIMITU specifies the remaining bits.

Notes

PMBASEU - Prefetchable Memory Base Upper (0x028)

Bit Field	Field Name	Type	Default Value	Description
31:0	PMBASEU	RW	0xFFFF_FFFF	**Prefetchable Memory Address Base Upper.** This field specifies the upper 32-bits of PMBASE when 64-bit addressing is used. When the PMCAP field in the PMBASE register is cleared, this field becomes read-only with a value of zero.

PMLIMITU - Prefetchable Memory Limit Upper (0x02C)

Bit Field	Field Name	Type	Default Value	Description
31:0	PMLIMITU	RW	0x0	**Prefetchable Memory Address Limit Upper.** This field specifies the upper 32-bits of PMLIMIT. When the PMCAP field in the PMBASE register is cleared, this field becomes read-only with a value of zero.

IOBASEU - I/O Base Upper (0x030)

Bit Field	Field Name	Type	Default Value	Description
15:0	IOBASEU	RW	0xFFFF	**I/O Address Base Upper.** This field specifies the upper 16-bits of IOBASE. When the IOCAP field in the IOBASE register is cleared, this field becomes read-only with a value of zero.

IOLIMITU - I/O Limit Upper (0x032)

Bit Field	Field Name	Type	Default Value	Description
15:0	IOLIMITU	RW	0x0	**Prefetchable IO Limit Upper.** This field specifies the upper 16-bits of IOLIMIT. When the IOCAP field in the IOBASE register is cleared, this field becomes read-only with a value of zero.

CAPPTR - Capabilities Pointer (0x034)

Bit Field	Field Name	Type	Default Value	Description
7:0	CAPPTR	RO	0x40	**Capabilities Pointer.** This field specifies a pointer to the head of the capabilities structure.

Notes

EROMBASE - Expansion ROM Base Address Register (0x038)

Bit Field	Field Name	Type	Default Value	Description
31:0	EROMBASE	RO	0x0	Expansion ROM Base Address. The bridge does not implement an expansion ROM. Thus, this field is hardwired to zero.

INTRLINE - Interrupt Line (0x03C)

Bit Field	Field Name	Type	Default Value	Description
7:0	INTRLINE	RW	0x0	Interrupt Line. This register communicates interrupt line routing information. Values in this register are programmed by system software and are system architecture specific. The bridge does not use the value in this register. Legacy interrupts may be implemented by downstream ports.

INTRPIN - Interrupt PIN (0x03D)

Bit Field	Field Name	Type	Default Value	Description
7:0	INTRPIN	RWL	0x0	Interrupt Pin. Interrupt pin or legacy interrupt messages are not used by the bridge. This field should only be configured with values of 0x0 through 0x4.

BCTRL - Bridge Control Register (0x03E)

Bit Field	Field Name	Type	Default Value	Description
0	PERRE	RW	0x0	Parity Error Response Enable. This bit controls the bridges response to poisoned TLPs on the secondary interface. 0x0 - (ignore) Ignore poisoned TLPs (i.e., parity errors) on the secondary interface. 0x1 - (report) Enable poisoned TLP (i.e., parity error) detection and reporting on the secondary interface of the bridge.

Notes

Bit Field	Field Name	Type	Default Value	Description
1	SERRE	RW	0x0	System Error Enable. This bit controls forwarding of ERR_COR, ERR_NONFATAL, ERR_FATAL from the secondary interface of the bridge to the primary interface. Note that error reporting must be enabled in the Command register or PCI Express Capability structure, Device Control register for errors to be reported on the primary interface. 0x0 - (ignore) Do not forward errors from the secondary to the primary interface. 0x1 - (report) Enable forwarding of errors from secondary to the primary interface.
2	ISAEN	RO	0x0	ISA Enable. The PES12NT3 does not support this feature.
3	VGAEN	RW	0x0	VGA Enable. Controls the routing of processor-initiated transactions targeting VGA. 0 - (lock) Do not forward VGA compatible addresses from the primary interface to the secondary interface 1 - (forward) Forward VGA compatible addresses from the primary to the secondary interface.
5:4	Reserved	RO	0x0	Reserved field.
6	SRESET	RW	0x0	Secondary Bus Reset. Setting this bit triggers a hot reset down the secondary interface of the bridge.
15:7	Reserved	RO	0x0	Reserved field.

PCI Express Capability Structure

PCIECAP - PCI Express Capability (0x040)

Bit Field	Field Name	Type	Default Value	Description
7:0	CAPID	RO	0x10	Capability ID. The value of 0x10 identifies this capability as a PCI Express capability structure.
15:8	NXTPTR	RO	0x70	Next Pointer. This field contains a pointer to the next capability structure.
19:16	VER	RO	0x1	PCI Express Capability Version. This field indicates the PCI-SIG defined PCI Express capability structure version number.
23:20	TYPE	RO	-	Port Type.
24	SLOT	RWL	0x0	Slot Implemented. This bit is set when the PCI Express link associated with this Port is connected to a slot.
29:25	IMN	RO	0x0	Interrupt Message Number. The function is allocated only one (downstream ports) MSI or none (upstream ports). Therefore, this field is set to zero.
31:30	Reserved	RO	0x0	Reserved field.

Notes

PCIEDCAP - PCI Express Device Capabilities (0x044)

Bit Field	Field Name	Type	Default Value	Description
2:0	MPAYLOAD	RWL	0x4	Maximum Payload Size Supported. This field indicates the maximum payload size that the device can support for TLPs. The default value corresponds to 2048 bytes.
4:3	PFS	RO	0x0	Phantom Functions Supported. This field indicates the support for unclaimed function number to extend the number of outstanding transactions allowed by logically combining unclaimed function numbers. The value is hardwired to 0x0 to indicate that no function number bits are used for phantom functions.
5	ETAG	RO	0x1	Extended Tag Field Support. This field indicates the maximum supported size of the Tag field as a requester.
8:6	E0AL	RO	0x0	Endpoint L0s Acceptable Latency. This field indicates the acceptable total latency that an endpoint can withstand due to transition from the L0s state to the L0 state. The value is hardwired to 0x0 as this field does not apply to a switch.
11:9	E1AL	RO	0x0	Endpoint L1 Acceptable Latency. This field indicates the acceptable total latency that an endpoint can withstand due to transition from the L1 state to the L0 state. The value is hardwired to 0x0 as this field does not apply to a switch.
12	ABP	RWL	0x0	Attention Button Present. When set, this bit indicates that an Attention Button is implemented on the card/module. This bit should not be set on downstream ports.
13	AIP	RWL	0x0	Attention Indicator Present. When set, this bit indicates that an Attention Indicator is implemented on the card/module. This bit should not be set on downstream ports.
14	PIP	RWL	0x0	Power Indicator Present. When set, this bit indicates that a Power Indicator is implemented on the card/module. This bit should not be set on downstream ports.
25:18	CSPLV	RO	0x0	Captured Slot Power Limit Value. *(Upstream Port A only, hardwired to zero in downstream ports)* Captured Slot Power Limit Value (upstream Ports only, hardwired to zero in downstream ports) – In combination with the Slot Power Limit Scale value, specifies the upper limit on power supplied by slot.Power limit (in Watts) calculated by multiplying the value in this field by the value in the Slot Power Limit Scale field. This value is set by the Set_Slot_Power_Limit Message.

PCIEDCTL - PCI Express Device Control (0x048)

Bit Field	Field Name	Type	Default Value	Description
0	CEREN	RW	0x0	Correctable Error Reporting Enable. This bit controls reporting of correctable errors.

Notes

Bit Field	Field Name	Type	Default Value	Description
1	NFEREN	RW	0x0	Non-Fatal Error Reporting Enable. This bit controls reporting of non-fatal errors.
2	FEREN	RW	0x0	Fatal Error Reporting Enable. This bit controls reporting of fatal errors.
3	URREN	RW	0x0	Unsupported Request Reporting Enable. This bit controls reporting of unsupported requests.
4	ERO	RO	0x0	Enable Relaxed Ordering. When set, this bit enables relaxed ordering. The switch never sets the relaxed ordering bit in transactions it initiates as a requester.
7:5	MPS	RW	0x0	Max Payload Size. This field sets maximum TLP payload size for the device. 0x0 - (s128) 128 bytes max payload size 0x1 - (s256) 256 bytes max payload size 0x2 - (s512) 512 bytes max payload size 0x3 - (s1024) 1024 bytes max payload size 0x4 - (s2048) 2048 bytes max payload size 0x5 - reserved (treated as 128 bytes) 0x6 - reserved (treated as 128 bytes) 0x7 - reserved (treated as 128 bytes)
8	ETFEN	RW	0x0	Extended Tag Field Enable. Since the transparent bridge never generates a transaction that requires a completion, this bit has no functional effect on the device during normal operation.
9	PFEN	RO	0x0	Phantom Function Enable. The bridge does not support phantom function numbers. Therefore, this field is hard-wired to zero.
10	AUXPMEN	RO	0x0	Auxiliary Power PM Enable. The device does not implement this capability.
11	ENS	RO	0x0	Enable No Snoop. The transparent bridge does not generate transactions with the No Snoop bit set and passes transactions through the bridge with the No Snoop bit unmodified. Therefore, this field has no functional effect on the behavior of the transparent bridge.
14:12	MRRS	RO	0x0	Maximum Read Request Size. The transparent bridge does not generate transactions larger than 128 bytes and passes transactions through the bridge with the size unmodified. Therefore, this field has no functional effect on the behavior of the transparent bridge.
15	Reserved	RO	0x0	Reserved field.

Notes

PCIEDSTS - PCI Express Device Status (0x04A)

Bit Field	Field Name	Type	Default Value	Description
0	CED	RW1C	0x0	Correctable Error Detected. This bit indicates the status of correctable errors. Errors are logged in this register regardless of whether error reporting is enabled or not.
1	NFED	RW1C	0x0	Non-Fatal Error Detected. This bit indicates the status of correctable errors. Errors are logged in this register regardless of whether error reporting is enabled or not.
2	FED	RW1C	0x0	Fatal Error Detected. This bit indicates the status of Fatal errors. Errors are logged in this registers regardless of whether error reporting is enabled or not.
3	URD	RW1C	0x0	Unsupported Request Detected. This bit indicates the device received an Unsupported Request. Errors are logged in this register regardless of whether error reporting is enabled or not.
4	AUXPD	RO	0x0	Aux Power Detected. Devices that require AUX power, set this bit when AUX power is detected.This device does not require AUX power, hence the value is hardwired to zero.
5	TP	RO	0x0	Transactions Pending. The transparent bridge does not issue Non-Posted Requests on its own behalf. Therefore, this field is hardwired to zero.
15:6	Reserved	RO	0x0	Reserved field.

PCIELCAP - PCI Express Link Capabilities (0x04C)

Bit Field	Field Name	Type	Default Value	Description
3:0	MAXLNKSPD	RO	0x1	Maximum Link Speed. This field is hardwired to 0x1 to indicate 2.5 Gbps.
9:4	MAXLNKWDTH	RWL	0x4	Maximum Link Width. This field indicates the maximum link width of the given PCI Express link. This field may be overridden to allow the link width to be forced to a smaller value. Setting this field to a invalid or reserved value results in x1 being used. 1 - (x1) x1 link width 2 - (x2) x2 link width 4 - (x4) x4 link width others - reserved
11:10	ASPMS	RO	0x3	Active State Power Management (ASPM) Support. This field is hardwired to 0x3 to indicate L0s and L1 Support.

Notes

Bit Field	Field Name	Type	Default Value	Description
14:12	L0SEL	RWL	see text	L0s Exit Latency. This field indicates the L0s exit latency for the given PCI Express link. This field depends on whether a common or separate reference clock is used. When separate clocks are used, 1 µs to 2 µs is reported with a read-only value of 0x5. When a common clock is used, 256 ns to 512 ns is reported with a read-only value of 0x3
17:15	L1EL	RWL	0x2	L1 Exit Latency. This field indicates the L1 exit latency for the given PCI Express link. Transitioning from L1 to L0 always requires 2.3 µs. Therefore, a value 2 µs to less than 4 µs is reported with a default value of 0x2.
23:18	Reserved	RO	0x0	Reserved field.
31:24	PORTNUM	RO	Port A - 0x0 Port B - 0x1 Port C - 0x2	Port Number. This field indicates the PCI express port number.

PCIELCTL - PCI Express Link Control (0x050)

Bit Field	Field Name	Type	Default Value	Description
1:0	ASPM	RW	0x0	Active State Power Management (ASPM) Control. This field controls the level of ASPM supported by the link. The initial value corresponds to disabled. The value contained in Serial EEPROM may override this default value 0x0 - (disabled) disabled 0x1 - (l0s) L0s enable entry 0x2 - (l1) L1 enable entry 0x3 - (l0sl1) L0s and L1 enable entry
2	Reserved	RO	0x0	Reserved field.
3	RCB	RO	0x0	Read Completion Boundary. This field is not applicable and is hardwired to zero.
4	LDIS	RW	0x0	Link Disable. When set, this bit disables the link. This field is hardwired to 0x0 for the upstream port.
5	LRET	RW	0x0	Link Retrain. Writing a one to this field initiates Link retraining by directing the Physical Layer LTSSM to the Recovery state. This field always returns zero when read. For compliance with the PCIe specification, this bit has no effect on the upstream port when the REGUNLOCK bit is cleared in the PA_SWCTL register. When the REGUN-LOCK bit is set, writing a one to the LRET bit initiates link retraining on the upstream port.
6	CCLK	RW	0x0	Common Clock Configuration. When set, this bit indi-cates that this component and the component at the oppo-site end of the link are operating with a distributed common reference clock.

Notes

Bit Field	Field Name	Type	Default Value	Description
7	ESYNC	RW	0x0	Extended Sync. When set this bit forces transmission of 4096 FTS ordered sets in the L0s state followed by a single SKP ordered set.
15:8	Reserved	RO	0x0	Reserved field.

PCIELSTS - PCI Express Link Status (0x052)

Bit Field	Field Name	Type	Default Value	Description
3:0	LS	RO	0x1	Link Speed. This field is hardwired to 2.5 Gbps.
9:4	LW	ROS	HWINIT	Link Width. This field indicates the negotiated width of the link.
10	TERR	ROS	0x0	Training Error. When set, this bit indicates that a link training error has occurred.
11	LTRAIN	ROS	0x0	Link Training. When set, this bit indicates that link training is in progress.
12	SCLK	RWL	HWINIT	Slot Clock Configuration. When set, this bit indicates that the component uses the same physical reference clock that the platform provides. The initial value of this field is the state of the CCLKUS signal for port A and the CCLKDS signal for downstream ports B and C. The value contained in Serial EEPROM may override these default values.
15:13	Reserved	RO	0x0	Reserved field.

PCIESCAP - PCI Express Slot Capabilities (0x054)

Bit Field	Field Name	Type	Default Value	Description
0	ABP	RO	0x0	Attention Button Present. Hot-plug is not supported.
1	PCP	RO	0x0	Power Control Present. Hot-plug is not supported.
2	MRLP	RO	0x0	MRL Sensor Present. Hot-plug is not supported.
3	ATTIP	RO	0x0	Attention Indicator Present. Hot-plug is not supported.
4	PWRIP	RO	0x0	Power Indicator Present. Hot-plug is not supported.
5	HPS	RO	0x0	Hot Plug Surprise. Hot-plug is not supported.
6	HPC	RO	0x0	Hot Plug Capable. Hot-plug is not supported.

Notes

Bit Field	Field Name	Type	Default Value	Description
14:7	SPLV	RWL	0x0	**Slot Power Limit Value**. In combination with the Slot Power Limit Scale, this field specifies the upper limit on power supplied by the slot. A Set_Slot_Power_Limit message is generated using this field whenever this register is written or when the link transitions from a non DL_Up status to a DL_Up status. This bit is read-only and has a value of zero when the SLOT bit in the PCIECAP register is cleared.
16:15	SPLS	RWL	0x0	**Slot Power Limit Scale**. This field specifies the scale used for the Slot Power Limit Value (SPLV). 0x0 - (x1) 1.0x 0x1 - (xp1) 0.1x 0x2 - (xp01) 0.01x 0x3 - (xp001) 0.001x A Set_Slot_Power_Limit message is generated using this field whenever this register is written or when the link transitions from a non DL_Up status to a DL_Up status. This bit is read-only and has a value of zero when the SLOT bit in the PCIECAP register is cleared.
17	EIP	RWL	0x0	**Electromechanical Interlock Present**. Hot-plug is not supported.
18	NCCS	RO	0x0	**No Command Completed Support**. Hot-plug is not supported.
31:19	PSLOTNUM	RWL	0x0	**Physical Slot Number**. This field indicates the physical slot number attached to this port. For devices interconnected on the system board, this field should be initialized to zero. This bit is read-only and has a value of zero when the SLOT bit in the PCIECAP register is cleared.

PCIESCTL - PCI Express Slot Control (0x058)

Bit Field	Field Name	Type	Default Value	Description
0	ABPE	RO	0x0	**Attention Button Pressed Enable**. Hot-plug is not supported.
1	PFDE	RO	0x0	**Power Fault Detected Enable**. Hot-plug is not supported.
2	MRLSCE	RO	0x0	**MRL Sensor Change Enable**. Hot-plug is not supported.
3	PDCE	RO	0x0	**Presence Detected Changed Enable**. Hot-plug is not supported.
4	CCIE	RO	0x0	**Command Complete Interrupt Enable**. Hot-plug is not supported.
5	HPIE	RO	0x0	**Hot Plug Interrupt Enable**. Hot-plug is not supported.
7:6	AIC	RO	0x3	**Attention Indicator Control**. Hot-plug is not supported.
9:8	PIC	RO	0x1	**Power Indicator Control**. Hot-plug is not supported.

Notes

Bit Field	Field Name	Type	Default Value	Description
10	PCC	RO	0x0	**Power Controller Control**. Hot-plug is not supported.
11	EIC	RO	0x0	**Electromechanical Interlock Control**. Hot-plug is not supported.
15:12	Reserved	RO	0x0	Reserved field.

PCIESSTS - PCI Express Slot Status (0x5A)

Bit Field	Field Name	Type	Default Value	Description
0	ABP	RO	0x0	**Attention Button Pressed**. Hot-plug is not supported.
1	PFD	RO	0x0	**Power Fault Detected**. Hot-plug is not supported.
2	MRLSC	RO	0x0	**MRL Sensor Changed**. Hot-plug is not supported.
3	PSD	RO	0x0	**Presence Detected Changed**. Hot-plug is not supported.
4	CC	RO	0x0	**Command Completed**. Hot-plug is not supported.
5	MRLSS	RO	0x0	**MRL Sensor State**. Hot-plug is not supported.
6	PDS	RO	0x1	**Presence Detect State**. Hot-plug is not supported.
7	EIS	RO	0x0	**Electromechanical Interlock Status**. Hot-plug is not supported.
15:8	Reserved	RO	0x0	Reserved field.

Power Management Capability Structure

PMCAP - PCI Power Management Capabilities (0x070)

Bit Field	Field Name	Type	Default Value	Description
7:0	CAPID	RO	0x1	**Capability ID**. The value of 0x1 identifies this capability as a PCI power management capability structure.
15:8	NXTPTR	RO	0x0	**Next Pointer**. This field contains a pointer to the next capability structure.
18:16	VER	RO	0x2	**Power Management Capability Version**. This field indicates compliance with version two of the specification.
19	PMECLK	RO	0x0	**PME Clock**. Does not apply to PCI Express.
20	Reserved	RO	0x0	Reserved field.
21	DEVSP	RWL	0x0	**Device Specific Initialization**. The value of zero indicates that no device specific initialization is required.
24:22	AUXI	RO	0x0	**AUX Current**. not used

Notes

Bit Field	Field Name	Type	Default Value	Description
25	D1	RO	0x0	D1 Support. This field indicates that the PES12NT3 does not support D1.
26	D2	RO	0x0	D2 Support. This field indicates that the PES12NT3 does not support D2.
31:27	PME	RO	0b11001	PME Support. This field indicates the power states in which the port may generate a PME. Bits 27, 30 and 31 are set to indicate that the bridge will forward PME messages. The switch does not forward PME messages in $D3_{cold}$. This functionality may be supported in the system by routing WAKE# around the switch.

PMCSR - PCI Power Management Control and Status (0x074)

Bit Field	Field Name	Type	Default Value	Description
1:0	PSTATE	RW	0x0	Power State. This field is used to determine the current power state and to set a new power state. 0x0 - (d0) D0 state 0x1 - (d1) D1 state (not supported by PES12NT3 and reserved) 0x2- (d2) D2 state (not supported by PES12NT3 and reserved) 0x3 - (d3) $D3_{hot}$ state
7:2	Reserved	RO	0x0	Reserved field.
8	PMEE	RW	0x0 Sticky	PME Enable. When this bit is set, PME message generation is enabled for the port. If a hot plug wake-up event is desired when exiting the $D3_{cold}$ state, then this bit should be set during serial EEPROM initialization. A hot reset does not result in modification of this field.
12:9	DSEL	RO	0x0	Data Select. The optional data register is not implemented.
14:13	DSCALE	RO	0x0	Data Scale. The optional data register is not implemented.
15	PMES	RW1C	0x0 Sticky for ports B & C RO 0x0 for port A	PME Status. This bit is set if a PME is generated by the port even if the PMEE bit is cleared. This bit is not set when the bridge is propagating a PME message but the port is not itself generating a PME.
21:16	Reserved	RO	0x0	Reserved field.
22	B2B3	RO	0x0	B2/B3 Support. Does not apply to PCI Express.
23	BPCCE	RO	0x0	Bus Power/Clock Control Enable. Does not apply to PCI Express.
31:24	DATA	RO	0x0	Data. This optional field is not implemented.

Notes

PMPC - PCI Power Management Proprietary Control (0x078)

Mode 1

Bit Field	Field Name	Type	Default Value	Description
15:0	L1ET	RW	0x3E8	L1 Entry Timer. This field specifies the L1 entry timer value for the related port transmitter. If all L1 entry conditions are met for the specified amount of time, then the transmitter port enters L1. This field is used by the upstream ports and ignored by downstream ports. The timer value is specified in the number 1 µS clock cycles. The default value corresponds to 1 mS
27:16	L0ET	RW	0x6D6	L0s Entry Timer. This field specifies the L0s entry time value for the related port transmitter. If all L0s entry conditions are met for the specified amount of time, then the transmitter port enters L0s. The timer value is specified in the number 4ns clock cycles. The default value corresponds to the PCI Express value of 7 µS.
30:28	Reserved	RO	0x0	Reserved field.
31	MCS	RW	0x0	Mode Configuration Switch. When this bit is set to zero, the PMPC register is configured as Mode1, shown in this table. When this bit is set to one, the register is configured as Mode2, shown in the Mode2 table.

Notes

Mode 2

Bit Field	Field Name	Type	Default Value	Description
5:0	PMCS	RO	0x3F	Values for PM current state. This field denotes the current value of the internal PM State Machine. Note that the SMBus is generally used to read this field rather than Configuration Reads. L0 = 6'd0 L0s_entry = 6'd1 L0s = 6'd2 L1pcipm_0 = 6'd3 L1pcipm_1 = 6'd4 L1pcipm_2 = 6'd5 L1pcipm_3 = 6'd6 L1pcipm_4 = 6'd7 L1pcipm_5 = 6'd8 L1pcipm_6 = 6'd9 L1pcipm_7 = 6'd10 L1comply_0 = 6'd11 L1comply_1 = 6'd12 L1comply_2 = 6'd13 L1accept_0 = 6'd14 L1accept_1 = 6'd15 L1accept_2 = 6'd16 L1reject_0 = 6'd17 L1timed_0 = 6'd18 L1timed_1 = 6'd19 L1timed_2 = 6'd20 L1timed_3 = 6'd21 L1timed_nak = 6'd22 L1_entry_1 = 6'd23 L1_entry_2 = 6'd24 L1_entry_3 = 6'd25 L1 = 6'd26 L23ready__entry_1 = 6'd29 L23ready__entry_2 = 6'd30 L23ready__entry_3 = 6'd31 L23ready__entry_4 = 6'd32 L23ready__entry_5 = 6'd33 L23ready__entry_6 = 6'd34 L23ready = 6'd35 LDown = 6'd63
30:6	Reserved	RO	0x0	Reserved field.
31	MCS	RW	0x0	Mode Configuration Switch. When this bit is set to zero, the PMPC register is configured as Mode1, shown in the Mode1 table. When this bit is set to one, the register is configured as Mode2, shown in this table.

Notes

Switch Control and Status Registers

SWSTS - Switch Status (0x0A0)

Bit Field	Field Name	Type	Default Value	Description
3:0	SWMODE	RO	HWINIT	Switch Mode. The value of this field encodes the switch mode sampled on the Switch Mode (SWMODE[3:0]) signals when exiting reset. 0x0 - Reserved 0x1 - Reserved 0x2 - (ntb) Non-transparent mode 0x3 - (ntbinit) Non-transparent mode with serial EEPROM initialization 0x4 - (ntbfailover) Non-transparent failover mode 0x5 - ntbfailoverinit) Non-transparent failover mode with serial EEPROM initialization 0x6 through 0xF - Reserved
4	CCLKDS	RO	HWINIT	Common Clock Downstream. This bit reflects the value of the CCLKDS signal sampled during the fundamental reset.
5	CCLKUS	RO	HWINIT	Common Clock Upstream. This bit reflects the value of the CCLKUS signal sampled during the fundamental reset.
6	MSMBSMODE	RO	HWINIT	Master SMBus Slow Mode. This bit reflects the value of the MSMBSMODE signal sampled during the fundamental reset.
7	PALREV	RO	HWINIT	PCI Express Port A Lane Reverse. This bit reflects the value of the PALREV signal sampled during the fundamental reset.
8	PBLREV	RO	HWINIT	PCI Express Port B Lane Reverse. This bit reflects the value of the PBLREV signal sampled during the fundamental reset.
9	PCLREV	RO	HWINIT	PCI Express Port C Lane Reverse. This bit reflects the value of the PCLREV signal sampled during the fundamental reset.
10	REFCLKM	RO	HWINIT	PCI Express Reference Clock Mode Select. This bit reflects the value of the REFCLKM signal sampled during the fundamental reset.
11	RSTHALT	RO	HWINIT	Reset Halt. This bit reflects the value of the RSTHALT signal sampled during the fundamental reset.
12	Reserved	RO	0x0	Reserved field.
16:13	MARKER	RW	0x0 Sticky	Marker. This field is preserved across a hot reset and is available for general software use. A hot reset does not result in modification of this field.
19:17	Reserved	RO	0x0	Reserved field.
20	INTA	RO	0x0	INTA Aggregated State. Aggregated switch state for INTA. 0x0 - (negated) INTA negated 0x1 - (asserted) INTA asserted

Notes

Bit Field	Field Name	Type	Default Value	Description
21	INTB	RO	0x0	INTB Aggregated State. Aggregated switch state for INTB. 0x0 - (negated) INTB negated 0x1 - (asserted) INTB asserted
22	INTC	RO	0x0	INTC Aggregated State. Aggregated switch state for INTC. 0x0 - (negated) INTC negated 0x1 - (asserted) INTC asserted
23	INTD	RO	0x0	INTD Aggregated State. Aggregated switch state for INTD. 0x0 - (negated) INTD negated 0x1 - (asserted) INTD asserted
31:24	Reserved	RO	0x0	Reserved field.

SWCTL - Switch Control (0x0A4)

Bit Field	Field Name	Type	Default Value	Description
0	RST	RW	0x0	Reset. Writing a one to this bit initiates a fundamental reset. Writing a zero has no effect. This field always returns a value of zero when read.
1	RSTHALT	RW	HWINIT	Reset Halt. When this bit is set, all of the switch logic except the SMBus interface remains in a reset state. In this state, registers in the device may be initialized by the slave SMBus interface. When this bit is cleared, normal operation ensues. Setting or clearing this bit has no effect following a reset operation. This bit may be set by asserting the RSTHALT signal during a reset operation or through initialization by the serial EEPROM.
2	REGUNLOCK	RW	0x0	Register Unlock. When this bit is set, the contents of registers and fields of type Read and Write when Unlocked (RWL) are modified when written to. When this bit is cleared, all registers and fields denoted as RWL become read-only. While the initial value of this field is cleared, it is set during a reset operation, thus allowing serial EEPROM initialization to modify the contents of RWL fields.
3	DRO	RW	0x0	Disable Relaxed Ordering. The switch implements relaxed ordering for TLPs with the relaxed ordering bit set. When the DRO bit is set, the switch strongly orders all transactions regardless of the state of the relaxed ordering bit in TLPs.

Notes

Bit Field	Field Name	Type	Default Value	Description
4	PALREV	RW	HWINIT	Port A Lane Reversal. When this bit is set, the lanes associated with port A are reversed. The initial value of this register corresponds to the state of the PALREV pin. However, this value may be overridden by the serial EEPROM, SMBus, or PCIe configuration write. Modifications to this bit take effect the next time link training occurs.
5	PBLREV	RW	HWINIT	Port B Lane Reversal. When this bit is set, the lanes associated with port B are reversed. The initial value of this register corresponds to the state of the PBLREV pin. However, this value may be overridden by the serial EEPROM, SMBus, or PCIe configuration write. Modifications to this bit take effect the next time link training occurs.
6	PCLREV	RW	HWINIT	Port C Lane Reversal. When this bit is set, the lanes associated with port C are reversed. The initial value of this register corresponds to the state of the PCLREV pin. However, this value may be overridden by the serial EEPROM, SMBus, or PCIe configuration write. Modifications to this bit take effect the next time link training occurs.
7	Reserved	RO	0x0	Reserved field.
8	NTBROS	RW	0x0	Non-Transparent Bridge Reset Output Select. This field selects whether internal or external reset indication are signalled on the PECRSTN pin (GPIO[1] alternate function) when the switch is configured to operate in non-transparent mode. 0x0 - (extreset) external reset. In this mode, the PECRSTN pin is asserted when an external hot or fundamental reset is detected. 0x1 - (intreset) internal reset. In this mode, the PECRSTN pin is asserted when an internal hot reset is detected. Fundamental reset result in the GPIO pin being configured as a GPIO input (i.e., tri-stated).
31:9	Reserved	RW	0x0	Reserved field.

GPIOCS - General Purpose I/O Control and Status (0x0A8)

Bit Field	Field Name	Type	Default Value	Description
7:0	GPIOFUNC	RW	0x0 Sticky	GPIO Function. Each bit in this field controls the corresponding GPIO pin. When set to a one, the corresponding GPIO pin operates as the alternate function as defined in Chapter 8, General Purpose I/O. When a bit is cleared to a zero, the corresponding GPIO pin operates as a general purpose I/O pin.

Notes

Bit Field	Field Name	Type	Default Value	Description
15:8	GPIOCFG	RW	0x0 Sticky	GPIO Configuration. Each bit in this field controls the corresponding GPIO pin. When a bit is configured as a general purpose I/O pin and the corresponding bit in this field is set, then the pin is configured as a GPIO output. When a bit is configured as a general purpose I/O pin and the corresponding bit in this field is zero, then the pin is configured as an input. When the pin is configured as an alternate function, the behavior of the pin is defined by the alternate function.
23:16	GPIOD	RW	HWINIT Sticky	GPIO Data. Each bit in this field controls the corresponding GPIO pin. Reading this field returns the current value of each GPIO pin regardless of GPIO pin mode (i.e., alternate function or GPIO pin). Writing a value to this field causes the corresponding pins which are configured as GPIO outputs to change state to the value written.
31:24	Reserved	RO	0x0	Reserved field.

SMBUSSTS - SMBus Status (0x0AC)

Bit Field	Field Name	Type	Default Value	Description
0	Reserved	RO	0x0	Reserved field.
7:1	SSMBADDR	RO	HWINIT	Slave SMBus Address. This field contains the SMBus address assigned to the slave SMBus interface.
8	Reserved	RO	0x0	Reserved field.
15:9	MSMBADDR	RO	HWINIT	Master SMBus Address. This field contains the SMBus address assigned to the master SMBus interface.
23:16	Reserved	RO	0x0	Reserved field.
24	EEPROMDONE	RO	0x0	Serial EEPROM Initialization Done. When the switch is configured to operate in a mode in which serial EEPROM initialization occurs during a fundamental reset, this bit is set when serial EEPROM initialization completes or when an error is detected.
25	NAERR	RW1C	0x0	No Acknowledge Error. This bit is set if an unexpected NACK is observed during a master SMBus transaction. The setting of this bit may indicate the following: that the addressed device does not exist on the SMBus (i.e., addressing error); data is unavailable or the device is busy; an invalid command was detected by the slave; or invalid data was detected by the slave.
26	LAERR	RW1C	0x0	Lost Arbitration Error. When the master SMBus interface loses arbitration for the SMBus, it automatically re-arbitrates for the SMBus. If the master SMBus interface loses 16 consecutive arbitration attempts, then the transaction is aborted and this bit is set.

Notes

Bit Field	Field Name	Type	Default Value	Description
27	OTHERERR	RW1C	0x0	Other Error. This bit is set if a misplaced START or STOP condition is detected by the master SMBus interface.
28	ICSERR	RW1C	0x0	Initialization Checksum Error. This bit is set if an invalid checksum is computed during Serial EEPROM initialization or when a configuration done command is not found in the serial EEPROM.
29	URIA	RW1C	0x0	Unmapped Register Initialization Attempt. This bit is set if an attempt is made to initialize via serial EEPROM a register that is not defined in the corresponding PCI configuration space.
31:30	Reserved	RO	0x0	Reserved field.

SMBUSCTL - SMBus Control (0x0B0)

Bit Field	Field Name	Type	Default Value	Description
15:0	MSMBCP	RW	HWINIT	Master SMBus Clock Prescalar. This field contains a clock prescalar value used during master SMBus transactions. The prescalar clock period is equal to 32 ns multiplied by the value in this field. When the field is cleared to zero or one, the clock is stopped. The initial value of this field is 0x0139 when the master SMBus is configured to operate in slow mode (i.e., 100 KHz) in the boot configuration and to 0x0053[1] when it is configured to operate in fast mode (i.e., 400 KHz).
16	MSMBIOM	RW	0x0	Master SMBus Ignore Other Masters. When this bit is set, the master SMBus proceeds with transactions regardless of whether it won or lost arbitration.
17	ICHECKSUM	RW	0x0	Ignore Checksum Errors. When this bit is set, serial EEPROM initialization checksum errors are ignored (i.e., the checksum always passes).
19:18	SSMBMODE	RW	0x0	Slave SMBus Mode. The slave SMBus contains internal glitch counters on the SSMBCLK and SSMBDAT signals that wait approximately 1 µS before sampling or driving these signals. This field allows the glitch counter time to be reduced or entirely removed. In some systems, this may permit high speed slave SMBus operation. 0x0 - (normal) Slave SMBus normal mode. Glitch counters operate with 1 µS delay. 0x1 - (fast) Slave SMBus interface fast mode. Glitch counters operate with 100 nS delay. 0x2 - (disabled) Slave SMBus interface with glitch counters disabled. Glitch counters operate with zero delay which effectively removes them. 0x3 - reserved.

Notes

Bit Field	Field Name	Type	Default Value	Description
21:20	MSMBMODE	RW	0x0	Master SMBus Mode. The master SMBus contains internal glitch counters on the MSMBCLK and MSMBDAT signals that wait approximately 1 µS before sampling or driving these signals. This field allows the glitch counter time to be reduced or entirely removed. In some systems, this may permit high speed master SMBus operation. 0x0 - (normal) Master SMBus normal mode. Glitch counters operate with 1 µS delay. 0x1 - (fast) Master SMBus interface fast mode. Glitch counters operate with 100 nS delay. 0x2 - (disabled) Master SMBus interface with glitch counters disabled. Glitch counters operate with zero delay which effectively removes them. 0x3 - reserved.
31:22	Reserved	RO	0x0	Reserved field.

[1] The MSMBCLK low minimum pulse width is equal to half the period programmed in this field. The value of 0x53, which corresponds to~373 KHz, allows the min low pulse width to be satisfied. In systems where this timing parameter is not critical, the operating frequency may be increased.

EEPROMINTF - Serial EEPROM Interface (0x0B4)

Bit Field	Field Name	Type	Default Value	Description
15:0	ADDR	RW	0x0	EEPROM Address. This field contains the byte address in the Serial EEPROM to be read or written.
23:16	DATA	RW	0x0	EEPROM Data. A write to this field will initiates a serial EEPROM read or write operation, as selected by the OP field, to the address specified in the ADDR field. When a write operation is selected, the value written to this field is the value written to the serial EEPROM. When a read operation is selected, the value written to this field is ignored and the value read from the serial EEPROM may be read from this field when the DONE bit is set.
24	BUSY	RO	0x0	EEPROM Busy. This bit is set when a serial EEPROM read or write operation is in progress. 0x0 - (idle) serial EEPROM interface idle 0x1 - (busy) serial EEPROM interface operation in progress
25	DONE	RW1C	0x0	EEPROM Operation Completed. This bit is set when a serial EEPROM operation has completed. 0x0 - (notdone) interface is idle or operation in progress 0x1 - (done) operation completed
26	OP	RW	0x0	EEPROM Operation Select. This field selects the type of EEPROM operation to be performed when the DATA field is written 0x0 - (write) serial EEPROM write 0x1 - (read) serial EEPROM read
31:27	Reserved	RO	0x0	Reserved field.

Notes

Extended Configuration Space Access and INTx Status Registers

PA_INTSTS - Interrupt Status (0x0F4)

Bit Field	Field Name	Type	Default Value	Description
0	INTA	RO	0x0	INTA Aggregated State. Aggregated port state for INTA. 0x0 - (negated) INTA negated 0x1 - (asserted) INTA asserted
1	INTB	RO	0x0	INTB Aggregated State. Aggregated port state for INTB. 0x0 - (negated) INTB negated 0x1 - (asserted) INTB asserted
2	INTC	RO	0x0	INTC Aggregated State. Aggregated port state for INTC. 0x0 - (negated) INTC negated 0x1 - (asserted) INTC asserted
3	INTD	RO	0x0	INTD Aggregated State. Aggregated port state for INTD. 0x0 - (negated) INTD negated 0x1 - (asserted) INTD asserted
31:4	Reserved	RO	0x0	Reserved field.

ECFGADDR - Extended Configuration Space Access Address (0x0F8)

Bit Field	Field Name	Type	Default Value	Description
1:0	Reserved	RO	0x0	Reserved field.
7:2	REG	RW	0x0	Register Number. This field selects the configuration register number as defined by Section 7.2.2 of the PCI Express Base Specification, Rev. 1.0a
11:8	EREG	RW	0x0	Extended Register Number. This field selects the extended configuration register number as defined by Section 7.2.2 of the PCI Express Base Specification, Rev. 1.0a
31:12	Reserved	RO	0x0	Reserved field.

Notes

ECFGDATA - Extended Configuration Space Access Data (0x0FC)

Bit Field	Field Name	Type	Default Value	Description
31:0	DATA	RW	0x0	Configuration Data. A read from this field will return the configuration space register value pointed to by the ECFGADDR register. A write to this field will update the contents of the configuration space register pointed to by the ECFGADDR register with the value written. For both reads and writes, the byte enables correspond to those used to access this field. When the ECFGADDR register points to the ECFGDATA register, then reads from ECFGDATA return zero and writes are ignored. When the ECFGADDR register points to itself, writes to the ECFGDATA register modify the contents of the ECFGADDR register. SMBus reads of this field return a value of zero and SMBus writes have no effect.

PCI Express Virtual Channel Capability

PCIEVCECAP - PCI Express Virtual Channel Enhanced Capability Header (0x100)

Bit Field	Field Name	Type	Default Value	Description
15:0	CAPID	RO	0x2	Capability ID. The value of 0x2. indicates a virtual channel capability structure.
19:16	CAPVER	RO	0x1	Capability Version. The value of 0x1. indicates compatibility with version 1 of the specification.
31:20	NXTPTR	RO	0x0	Next Pointer. The value of 0x0 indicates that there are no extended capabilities.

PVCCAP1- Port VC Capability 1 (0x104)

Bit Field	Field Name	Type	Default Value	Description
2:0	EVCCNT	RO	0x0	Extended VC Count. The value 0x0 indicates only implementation of the default VC.
6:4	LPEVCCNT	RO	0x0	Low Priority Extended VC Count. The value of 0x0 indicates only implementation of the default VC.
9:8	REFCLK	RO	0x0	Reference Clock. Time-based WRR is not implemented.
11:10	PATBLSIZ	RO	0x1	Port Arbitration Table Entry Size. This field indicates the size of the port arbitration table in the device. The value in the PES12NT3 is set to 0x1 to indicate a 2-bit table. 0x0 - (bit1) Port arbitration table is 1-bit 0x1 - (bit2) Port arbitration table is 2-bits 0x2 - (bit4) Port arbitration table is 4-bits 0x3 - (bit8) Port arbitration table is 8-bits

Notes

Bit Field	Field Name	Type	Default Value	Description
31:12	Reserved	RO	0x0	Reserved field.

VCR0CAP- VC Resource 0 Capability (0x110)

Bit Field	Field Name	Type	Default Value	Description
7:0	PARBC	RWL	0x1	Port Arbitration Capability. This field indicates the type of port arbitration supported by the VC. Each bit corresponds to a Port Arbitration capability. When more than one arbitration scheme is supported, multiple bits may be set. The PES12NT3 supports hardware fixed round robin only. bit 0 - hardware fixed round robin bit 1 - N/As bit 2 - N/A bit 3 - N/A bit 4 - N/A bit 5 - N/A
13:8	Reserved	RO	0x0	Reserved field.
14	APS	RO	0x0	Advanced Packet Switching. Not supported.
15	RJST	RO	0x0	Reject Snoop Transactions. Not supported for switch ports.
22:16	MAXTS	RO	0x0	Maximum Time Slots. Since this VC does not support time-based WRR, this field is not valid.
23	Reserved	RO	0x0	Reserved field.
31:24	PATBLOFFSET	RWL	0x0	Port Arbitration Table Offset. This field contains the offset of the port arbitration table from the base address of the Virtual Channel Capability structure in double quad words (16 bytes).

VCR0CTL- VC Resource 0 Control (0x114)

Bit Field	Field Name	Type	Default Value	Description
7:0	TCVCMAP	bit 0 RO bits 1 through 7 RW	0xFF	TC/VC Map. This field indicates the TCs that are mapped to the VC resource. Each bit corresponds to a TC. When a bit is set, the corresponding TC is mapped to the VC.
15:8	Reserved	RO	0x0	Reserved field.

Notes

Bit Field	Field Name	Type	Default Value	Description
16	LPAT	RW	0x0	Load Port Arbitration Table. This bit, when set, updates the Port Arbitration logic from the Port Arbitration Table for the VC resource. In addition, this field is only valid when the Port Arbitration Table is used by the selected Port Arbitration scheme (that is indicated by a set bit in the Port Arbitration Capability field selected by Port Arbitration Select). Software sets this bit to signal hardware to update Port Arbitration logic with new values stored in Port Arbitration Table; clearing this bit has no effect. Software uses the Port Arbitration Table Status bit to confirm whether the new values of Port Arbitration Table are completely latched by the arbitration logic. This bit always returns 0 when read.
19:17	PARBSEL	RW	0x0	Port Arbitration Select. This field configures the VC resource to provide a particular Port Arbitration service. The permissible values of this field is a number that corresponds to one of the asserted bits in the Port Arbitration Capability field of the VC resource.
23:20	Reserved	RO	0x0	Reserved field.
26:24	VCID	RO	0x0	VC ID. This field assigns a VC ID to the VC resource. Since the PES12NT3 implements only a single VC, this field is hardwired to zero.
30:27	Reserved	RO	0x0	Reserved field.
31	VCEN	RO	0x1	VC Enable. This field, when set, enables a virtual channel. Since the PES12NT3 implements only a single VC, this field is hardwired to one (enabled).

VCR0STS - VC Resource 0 Status (0x118)

Bit Field	Field Name	Type	Default Value	Description
0	PATS	RO	0x0	Port Arbitration Table Status. This bit indicates the coherency status of the port arbitration table associated with the VC resource and is valid only when the port arbitration table is used by the selected arbitration algorithm. This bit is set when any entry of the port arbitration table is written by software and remains set until hardware finishes loading the value after software sets the LPAT field in the VCR0CTL register.
1	VCNEG	RO	0x0	VC Negotiation Pending. Since the PES12NT3 implements only a single VC (i.e., the default VC) this field indicates the status of the process of flow control initialization.
30:2	Reserved	RO	0x0	Reserved field.

Notes

VCR0TBL0 - VC Resource 0 Arbitration Table Entry 0 (0x120)

Bit Field	Field Name	Type	Default Value	Description
1:0	PHASE0	RW	0x0	Phase 0. This field contains the port ID for the corresponding port arbitration period. Selecting an invalid port ID results in the entry being skipped without delay. The port arbitration behavior when this field contains an illegal value (i.e., reserved or the egress port ID) is undefined. 0x0 - (port_a) Port A (upstream port) 0x1 - (port_b) Port B 0x2 - (port_c) Port C 0x3 - reserved
3:2	PHASE1	RW	0x0	Phase 1. This field contains the port ID for the corresponding port arbitration period.
5:4	PHASE2	RW	0x0	Phase 2. This field contains the port ID for the corresponding port arbitration period.
7:6	PHASE3	RW	0x0	Phase 3. This field contains the port ID for the corresponding port arbitration period.
9:8	PHASE4	RW	0x0	Phase 4. This field contains the port ID for the corresponding port arbitration period.
11:10	PHASE5	RW	0x0	Phase 5. This field contains the port ID for the corresponding port arbitration period.
13:12	PHASE6	RW	0x0	Phase 6. This field contains the port ID for the corresponding port arbitration period.
15:14	PHASE7	RW	0x0	Phase 7. This field contains the port ID for the corresponding port arbitration period.
17:16	PHASE8	RW	0x0	Phase 8. This field contains the port ID for the corresponding port arbitration period.
19:18	PHASE9	RW	0x0	Phase 9. This field contains the port ID for the corresponding port arbitration period.
21:20	PHASE10	RW	0x0	Phase 10. This field contains the port ID for the corresponding port arbitration period.
23:22	PHASE11	RW	0x0	Phase 11. This field contains the port ID for the corresponding port arbitration period.
25:24	PHASE12	RW	0x0	Phase 12. This field contains the port ID for the corresponding port arbitration period.
27:26	PHASE13	RW	0x0	Phase 13. This field contains the port ID for the corresponding port arbitration period.
29:28	PHASE14	RW	0x0	Phase 14. This field contains the port ID for the corresponding port arbitration period.
31:30	PHASE15	RW	0x0	Phase 15. This field contains the port ID for the corresponding port arbitration period.

Notes

VCR0TBL1 - VC Resource 0 Arbitration Table Entry 1 (0x124)

Bit Field	Field Name	Type	Default Value	Description
1:0	PHASE16	RW	0x0	Phase 16. This field contains the port ID for the corresponding port arbitration period. Selecting an invalid port ID results in the entry being skipped without delay. 0x0 - (port_a) Port A (upstream port) 0x1 - (port_b) Port B 0x2 - (port_c) Port C 0x3 - reserved
3:2	PHASE17	RW	0x0	Phase 17. This field contains the port ID for the corresponding port arbitration period.
5:4	PHASE18	RW	0x0	Phase 18. This field contains the port ID for the corresponding port arbitration period.
7:6	PHASE19	RW	0x0	Phase 19. This field contains the port ID for the corresponding port arbitration period.
9:8	PHASE20	RW	0x0	Phase 20. This field contains the port ID for the corresponding port arbitration period.
11:10	PHASE21	RW	0x0	Phase 21. This field contains the port ID for the corresponding port arbitration period.
13:12	PHASE22	RW	0x0	Phase 22. This field contains the port ID for the corresponding port arbitration period.
15:14	PHASE23	RW	0x0	Phase 23. This field contains the port ID for the corresponding port arbitration period.
17:16	PHASE24	RW	0x0	Phase 24. This field contains the port ID for the corresponding port arbitration period.
19:18	PHASE25	RW	0x0	Phase 25. This field contains the port ID for the corresponding port arbitration period.
21:20	PHASE26	RW	0x0	Phase 26. This field contains the port ID for the corresponding port arbitration period.
23:22	PHASE27	RW	0x0	Phase 27. This field contains the port ID for the corresponding port arbitration period.
25:24	PHASE28	RW	0x0	Phase 28. This field contains the port ID for the corresponding port arbitration period.
27:26	PHASE29	RW	0x0	Phase 29. This field contains the port ID for the corresponding port arbitration period.
29:28	PHASE30	RW	0x0	Phase 30. This field contains the port ID for the corresponding port arbitration period.
31:30	PHASE31	RW	0x0	Phase 31. This field contains the port ID for the corresponding port arbitration period.

Notes

Physical Layer Control and Status Registers

SERDESCTL - SerDes Control (0x200)

Bit Field	Field Name	Type	Default Value	Description
3:0	TXEQL	RW	0x8	Transmit Driver Equalization Level. This field controls the SerDes transmit driver equalization. 0x0 - (de000) de-emphasis of 0.00 dB 0x1 - (de035) de-emphasis of -0.35 dB 0x2 - (de072) de-emphasis of -0.72 dB 0x3 - (de111) de-emphasis of -1.11 dB 0x4 - (de151) de-emphasis of -1.51 dB 0x5 - (de194) de-emphasis of -1.94 dB 0x6 - (de238) de-emphasis of -2.38 dB 0x7 - (de285) de-emphasis of -2.85dB 0x8 - (de335) de-emphasis of -3.84 dB 0x9 - (de388) de-emphasis of -3.88 dB 0xA - (de444) de-emphasis of -4.44 dB 0xB- (de504) de-emphasis of -5.04 dB 0xC - (de568) de-emphasis of -5.68dB 0xD - (de638) de-emphasis of -6.38 dB 0xE - (de713) de-emphasis of -7.13 dB 0xF - (de796) de-emphasis of -7.96 dB
7:4	TXDCSF	RW	0x0	Transmit Driver Current Scale Factor. The actual drive current is equal to the nominal drive current selected by the TXNDC field multiplied by the scale factor selected in this field. 0x0 - (sf100) scale factor of 1.00 0x1 - (sf105) scale factor of 1.05 0x2 - (sf110) scale factor of 1.10 0x3 - (sf115) scale factor of 1.15 0x4 - (sf120) scale factor of 1.20 0x5 - (sf125) scale factor of 1.25 0x6 - (sf130) scale factor of 1.30 0x7 - (sf135) scale factor of 1.35 0x8 - (sf060) scale factor of 0.60 0x9 - (sf065) scale factor of 0.65 0xA - (sf070) scale factor of 0.70 0xB - (sf075) scale factor of 0.75 0xC - (sf080) scale factor of 0.80 0xD - (sf085) scale factor of 0.85 0xE - (sf090) scale factor of 0.90 0xF - (sf095) scale factor of 0.95
9:8	TXNDC	RW	0x0	Transmit Driver Nominal Drive Current. This field selects the SerDes transmitter nominal drive current. 0x0 - (med) 20 mA nominal drive current 0x1 -(low) 10 mA nominal drive current 0x2 -(high) 28 mA nominal drive current 0x3 -reserved
11:10	TXTERM	RW	0x0	Transmitter Termination Adjustment. This field controls the SerDes transmitter termination value. 0x0 - (nom) nominal transmit termination value of 50 ohms 0x1 -(m17) termination value of nominal - 17% 0x2 -(p10) termination value of nominal + 10% 0x3 -(m15) termination value of nominal - 15%

Notes

Bit Field	Field Name	Type	Default Value	Description
13:12	RXTERM	RW	0x0	Receiver Termination Adjustment. This field controls the SerDes receiver termination value. 0x0 - (nom) nominal transmit termination value of 50 ohms 0x1 -(m17) termination value of nominal - 17% 0x2 -(p10) termination value of nominal + 10% 0x3 -(m15) termination value of nominal - 15%
14	HIVMODE	RW	0x0	High Voltage Mode. This field selects the SerDes Vdd/ VddA supply voltage. 0x0 - (low) 1.0V supply 0x1 - (high) 1.2V supply
16:15	RXEQ	RW	0x0	Receive Equalization. This field selects the SerDes receiver equalization. 0x0 - (max) maximum receive equalization 0x1 - (min) minimum receive equalization 0x2 - (off) turn off receive equalization 0x3 - reserved
31:17	Reserved	RO	0x0	Reserved field.

Notes

Non Transparent Port C Configuration Space Organization

The organization of port C configuration space is shown in Figure 9.7.

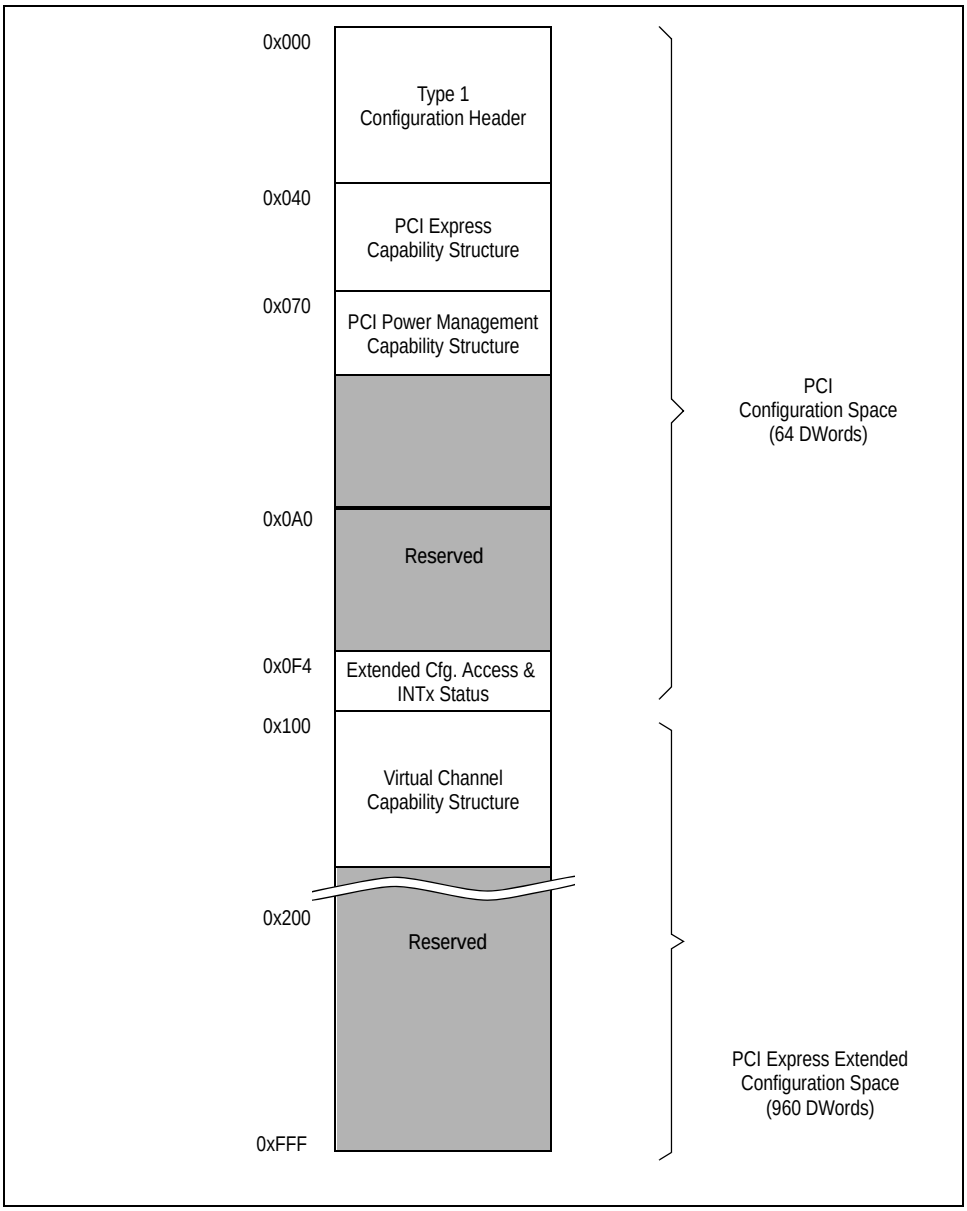

Figure 9.7 Port C Configuration Space Organization in Non-Transparent Mode

Notes

Non-Transparent Mode Downstream Port C Configuration Space Organizations Registers

All configuration space locations not listed in Table 9.8 return a value of zero when read. Writes to these locations are ignored and have no side-effects.Port C configuration space registers may be read and written via the slave SMBus interface and initialized from the serial EEPROM using the CSR system address formed by adding the base address 0x1000 to the PCI configuration space offset address.

Note: The registers for port C are defined in section Generic Registers on page 9-23 except for the six registers with offset address range from 0x04C through 0x05A in section Port C Specialized Registers on page 9-61.

Note: In pdf format, clicking on a register name in the Register Definition column creates a jump to the appropriate register. To return to the starting place in this table, click on the same register name (in blue) in the register section.

Cfg. Offset	Size	Register Mnemonic	Register Definition
0x000	Word	PC_VID	VID - Vendor Identification (0x000) on page 9-23
0x002	Word	PC_DID	DID - Device Identification (0x002) on page 9-23
0x004	Word	PC_PCICMD	PCICMD - PCI Command (0x004) on page 9-24
0x006	Word	PC_PCISTS	PCISTS - PCI Status (0x006) on page 9-25
0x008	Byte	PC_RID	RID - Revision Identification (0x008) on page 9-26
0x009	3 Bytes	PC_CCODE	CCODE - Class Code (0x009) on page 9-26
0x00C	Byte	PC_CLS	CLS - Cache Line Size (0x00C) on page 9-26
0x00D	Byte	PC_PLTIMER	PLTIMER - Primary Latency Timer (0x00D) on page 9-26
0x00E	Byte	PC_HDR	HDR - Header Type (0x00E) on page 9-26
0x00F	Byte	PC_BIST	BIST - Built-in Self Test (0x00F) on page 9-27
0x010	DWord	PC_BAR0	BAR0 - Base Address Register 0 (0x010) on page 9-27
0x014	DWord	PC_BAR1	BAR1 - Base Address Register 1 (0x014) on page 9-27
0x018	Byte	PC_PBUSN	PBUSN - Primary Bus Number Register (0x018) on page 9-27
0x019	Byte	PC_SBUSN	SBUSN - Secondary Bus Number Register (0x019) on page 9-27
0x01A	Byte	PC_SUBUSN	SUBUSN - Subordinate Bus Number Register (0x01A) on page 9-27
0x01B	Byte	PC_SLTIMER	SLTIMER - Secondary Latency Timer Register (0x01B) on page 9-28
0x01C	Byte	PC_IOBASE	IOBASE - I/O Base Register (0x01C) on page 9-28
0x01D	Byte	PC_IOLIMIT	IOLIMIT - I/O Limit Register (0x01D) on page 9-28
0x01E	Word	PC_SECSTS	SECSTS - Secondary Status (0x01E) on page 9-28
0x020	Word	PC_MBASE	MBASE - Memory Base (0x020) on page 9-29
0x022	Word	PC_MLIMIT	MLIMIT - Memory Limit (0x022) on page 9-29
0x024	Word	PC_PMBASE	PMBASE - Prefetchable Memory Base (0x024) on page 9-30
0x026	Word	PC_PMLIMIT	PMLIMIT - Prefetchable Memory Limit (0x026) on page 9-30
0x028	DWord	PC_PMBASEU	PMBASEU - Prefetchable Memory Base Upper (0x028) on page 9-31

Table 9.8 Downstream Port C Configuration Space Registers in Non-Transparent Mode (Part 1 of 3)

Notes

Cfg. Offset	Size	Register Mnemonic	Register Definition
0x02C	DWord	PC_PMLIMITU	PMLIMITU - Prefetchable Memory Limit Upper (0x02C) on page 9-31
0x030	Word	PC_IOBASEU	IOBASEU - I/O Base Upper (0x030) on page 9-31
0x032	Word	PC_IOLIMITU	IOLIMITU - I/O Limit Upper (0x032) on page 9-31
0x034	Byte	PC_CAPPTR	CAPPTR - Capabilities Pointer (0x034) on page 9-31
0x038	DWord	PC_EROMBASE	EROMBASE - Expansion ROM Base Address Register (0x038) on page 9-32
0x03C	Byte	PC_INTRLINE	INTRLINE - Interrupt Line (0x03C) on page 9-32
0x03D	Byte	PC_INTRPIN	INTRPIN - Interrupt PIN (0x03D) on page 9-32
0x03E	Word	PC_BCTRL	BCTRL - Bridge Control Register (0x03E) on page 9-32
0x040	DWord	PC_PCIECAP	PCIECAP - PCI Express Capability (0x040) on page 9-33
0x044	DWord	PC_PCIEDCAP	PCIEDCAP - PCI Express Device Capabilities (0x044) on page 9-34
0x048	Word	PC_PCIEDCTL	PCIEDCTL - PCI Express Device Control (0x048) on page 9-34
0x04A	Word	PC_PCIEDSTS	PCIEDSTS - PCI Express Device Status (0x04A) on page 9-36
0x04C	DWord	PC_PCIELCAP	PC_PCIELCAP - Port C NTB Mode PCI Express Link Capabilities (0x04C) on page 9-61
0x050	Word	PC_PCIELCTL	PC_PCIELCTL - Port C NTB Mode PCI Express Link Control (0x050) on page 9-62
0x052	Word	PC_PCIELSTS	PC_PCIELSTS - Port C NTB Mode PCI Express Link Status (0x052) on page 9-63
0x054	DWord	PC_PCIESCAP	PC_PCIESCAP - Port C NTB Mode PCI Express Slot Capabilities (0x054) on page 9-63
0x058	Word	PC_PCIESCTL	PC_PCIESCTL - Port C NTB Mode PCI Express Slot Control (0x058) on page 9-64
0x05A	Word	PC_PCIESSTS	PC_PCIESSTS - Port C NTB Mode PCI Express Slot Status (0x5A) on page 9-64
0x070	DWord	PC_PMCAP	PMCAP - PCI Power Management Capabilities (0x070) on page 9-40
0x074	DWord	PC_PMCSR	PMCSR - PCI Power Management Control and Status (0x074) on page 9-41
0x078	DWord	PC_PMPC	PMPC - PCI Power Management Proprietary Control (0x078) on page 9-42
0x0F8	Word	PC_ECFGADDR	ECFGADDR - Extended Configuration Space Access Address (0x0F8) on page 9-50
0x0FC	Word	PC_ECFGDATA	ECFGDATA - Extended Configuration Space Access Data (0x0FC) on page 9-51
0x100	DWord	PC_PCIEVCECAP	PCIEVCECAP - PCI Express Virtual Channel Enhanced Capability Header (0x100) on page 9-51
0x104	DWord	PC_PVCCAP1	PVCCAP1- Port VC Capability 1 (0x104) on page 9-51
0x110	DWord	PC_VCR0CAP	VCR0CAP- VC Resource 0 Capability (0x110) on page 9-52
0x114	DWord	PC_VCR0CTL	VCR0CTL- VC Resource 0 Control (0x114) on page 9-52

Table 9.8 Downstream Port C Configuration Space Registers in Non-Transparent Mode (Part 2 of 3)

Notes

Cfg. Offset	Size	Register Mnemonic	Register Definition
0x118	DWord	PC_VCR0STS	VCR0STS - VC Resource 0 Status (0x118) on page 9-53
0x120	DWord	PC_VCR0TBL0	VCR0TBL0 - VC Resource 0 Arbitration Table Entry 0 (0x120) on page 9-54
0x124	DWord	PC_VCR0TBL1	VCR0TBL1 - VC Resource 0 Arbitration Table Entry 1 (0x124) on page 9-55
0x200	DWord	PC_SERDESCTL	SERDESCTL - SerDes Control (0x200) on page 9-56
0x204 — 0x61C			Reserved

Table 9.8 Downstream Port C Configuration Space Registers in Non-Transparent Mode (Part 3 of 3)

Port C Specialized Registers

PC_PCIELCAP - Port C NTB Mode PCI Express Link Capabilities (0x04C)

Bit Field	Field Name	Type	Default Value	Description
3:0	MAXLNKSPD	RO	0x1	Maximum Link Speed. This field is hardwired to 0x1 to indicate 2.5 Gbps.
9:4	MAXLNK-WDTH	RWL	0x4	Maximum Link Width. This field indicates the maximum link width of the given PCI Express link. This field may be overridden to allow the link width to be forced to a smaller value. Setting this field to a invalid or reserved value results in x1 being used. 0 - reserved 1 - (x1) x1 link width 2 - (x2) x2 link width 4 - (x4) x4 link width others - reserved
11:10	ASPMS	RO	0x1	Active State Power Management (ASPM) Support. This field is hardwired to 0x1 to indicate L0s Support. Unlike the other ports, Port C does not support L1 ASPM.
14:12	L0SEL	RO	see text	L0s Exit Latency. This field indicates the L0s exit latency for the given PCI Express link. This field depends of whether a common or separate reference clock is used When separate clocks are used 1 us to 2 us is reported with a read only value of 0x5. When a common clock is used 256 ns to 512 ns is reported with a read-only value of 0x3

Notes

Bit Field	Field Name	Type	Default Value	Description
17:15	L1EL	RO	see text	L1 Exit Latency. This field indicates the L1 exit latency for the given PCI Express link. This field is affected by the deep L1 and D3 disable bits (i.e., DEEPD3DIS and DEEPL1DIS). In DEEPD3DIS or DEEPL1DIS modes, a value of less than 1us is reported with a read only value of 0x0. In default mode, a value of between 8us to less than 16us is reported with a read only value of 0x4.
23:18	Reserved	RO	0x0	Reserved field.
31:24	PORTNUM	RWL	Port C - 0x2	Port Number. This field indicates the PCI express port number.

PC_PCIELCTL - Port C NTB Mode PCI Express Link Control (0x050)

Bit Field	Field Name	Type	Default Value	Description
1:0	ASPM	RW	0x0	Active State Power Management (ASPM) Control. This field controls the level of ASPM supported by the link. The initial value corresponds to disabled. The value contained in Serial EEPROM may override this default value 0x0 -(disabled) disabled 0x1 -(l0s) L0s enable entry 0x2 -(l1) L1 enable entry 0x3 -(l0sl1) L0s and L1 enable entry
2	Reserved	RO	0x0	Reserved field.
3	RCB	RO	0x0	Read Completion Boundary. This field is not applicable and is hardwired to zero.
4	LDIS	RW	0x0	Link Disable. Between the port C transparent bridge and the internal NTB endpoint is a “virtual link.” This virtual link does not have an associated LTSSM and therefore cannot be disabled. This bit is read-write but has no functional affect on the operation of the device.
5	LRET	RW	0x0	Link Retrain. Writing a one to this field initiates Link retraining by directing the Physical Layer LTSSM to the Recovery state. This field always returns zero when read.
6	CCLK	RW	0x0	Common Clock Configuration. When set, this bit indicates that this component and the component at the opposite end of the link are operating with a distributed common reference clock.
7	ESYNC	RW	0x0	Extended Sync. When set this bit forces transmission of 4096 FTS ordered sets in the L0s state followed by a single SKP ordered set.
15:8	Reserved	RO	0x0	Reserved field.

Notes

PC_PCIELSTS - Port C NTB Mode PCI Express Link Status (0x052)

Bit Field	Field Name	Type	Default Value	Description
3:0	LS	RO	0x1	**Link Speed**. This field is hardwired to 2.5 Gbps.
9:4	LW	RO	HWINIT	**Link Width**. This field indicates the negotiated width of the link.
10	TERR	RO	0x0	**Training Error**. When set, this bit indicates that a link training error has occurred.
11	LTRAIN	RO	0x0	**Link Training**. When set, this bit indicates that link training is in progress.
12	SCLK	RWL	HWINIT	**Slot Clock Configuration**. When set, this bit indicates that the component uses the same physical reference clock that the platform provides. The initial value of this field is the state of the CCLKUS signal for port A and the CCLKDS signal for downstream ports B and C. The value contained in Serial EEPROM may override these default values.
15:13	Reserved	RO	0x0	Reserved field.

PC_PCIESCAP - Port C NTB Mode PCI Express Slot Capabilities (0x054)

Bit Field	Field Name	Type	Default Value	Description
0	ABP	RO	0x0	**Attention Button Present**. Hot-plug is not supported.
1	PCP	RO	0x0	**Power Control Present**. Hot-plug is not supported.
2	MRLP	RO	0x0	**MRL Sensor Present**. Hot-plug is not supported.
3	ATTIP	RO	0x0	**Attention Indicator Present**. Hot-plug is not supported.
4	PWRIP	RO	0x0	**Power Indicator Present**. Hot-plug is not supported.
5	HPS	RO	0x0	**Hot Plug Surprise**. Hot-plug is not supported.
6	HPC	RO	0x0	**Hot Plug Capable**. Hot-plug is not supported.
14:7	SPLV	RO	0x0	**Slot Power Limit Value**. Feature not supported between the Port C PCI-to-PCI bridge and the internal endpoint.
16:15	SPLS	RO	0x0	**Slot Power Limit Scale**. Feature not supported between the Port C PCI-to-PCI bridge and the internal endpoint.
17	EIP	RO	0x0	**Electromechanical Interlock Present**. Hot-plug is not supported.
18	NCCS	RO	0x0	**No Command Completed Support**. Hot-plug is not supported.
31:19	PSLOTNUM	RWL	0x0	**Physical Slot Number**. This field indicates the physical slot number attached to this port. For devices interconnected on the system board, this field should be initialized to zero. This bit is read-only and has a value of zero when the SLOT bit in the PCIECAP register is cleared.

Notes

PC_PCIESCTL - Port C NTB Mode PCI Express Slot Control (0x058)

Bit Field	Field Name	Type	Default Value	Description
0	ABPE	RO	0x0	Attention Button Pressed Enable. Hot-plug is not supported.
1	PFDE	RO	0x0	Power Fault Detected Enable. Hot-plug is not supported.
2	MRLSCE	RO	0x0	MRL Sensor Change Enable. Hot-plug is not supported.
3	PDCE	RO	0x0	Presence Detected Changed Enable. Hot-plug is not supported.
4	CCIE	RO	0x0	Command Complete Interrupt Enable. Hot-plug is not supported.
5	HPIE	RO	0x0	Hot Plug Interrupt Enable. Hot-plug is not supported.
7:6	AIC	RO	0x0	Attention Indicator Control. Hot-plug is not supported.
9:8	PIC	RO	0x0	Power Indicator Control. Hot-plug is not supported.
10	PCC	RO	0x0	Power Controller Control. Hot-plug is not supported.
11	EIC	RO	0x0	Electromechanical Interlock Control. Hot-plug is not supported.
15:12	Reserved	RO	0x0	Reserved field.

PC_PCIESSTS - Port C NTB Mode PCI Express Slot Status (0x5A)

Bit Field	Field Name	Type	Default Value	Description
0	ABP	RO	0x0	Attention Button Pressed. Hot-plug is not supported.
1	PFD	RO	0x0	Power Fault Detected. Hot-plug is not supported.
2	MRLSC	RO	0x0	MRL Sensor Changed. Hot-plug is not supported.
3	PSD	RO	0x0	Presence Detected Changed. Hot-plug is not supported.
4	CC	RO	0x0	Command Completed. Hot-plug is not supported.
5	MRLSS	RO	0x0	MRL Sensor State. Hot-plug is not supported.
6	PDS	RO	0x1	Presence Detect State. Hot-plug is not supported.
7	EIS	RO	0x0	Electromechanical Interlock Status. Hot-plug is not supported.
15:8	Reserved	RO	0x0	Reserved field.

Notes

NTB Endpoint Configuration Space Organization

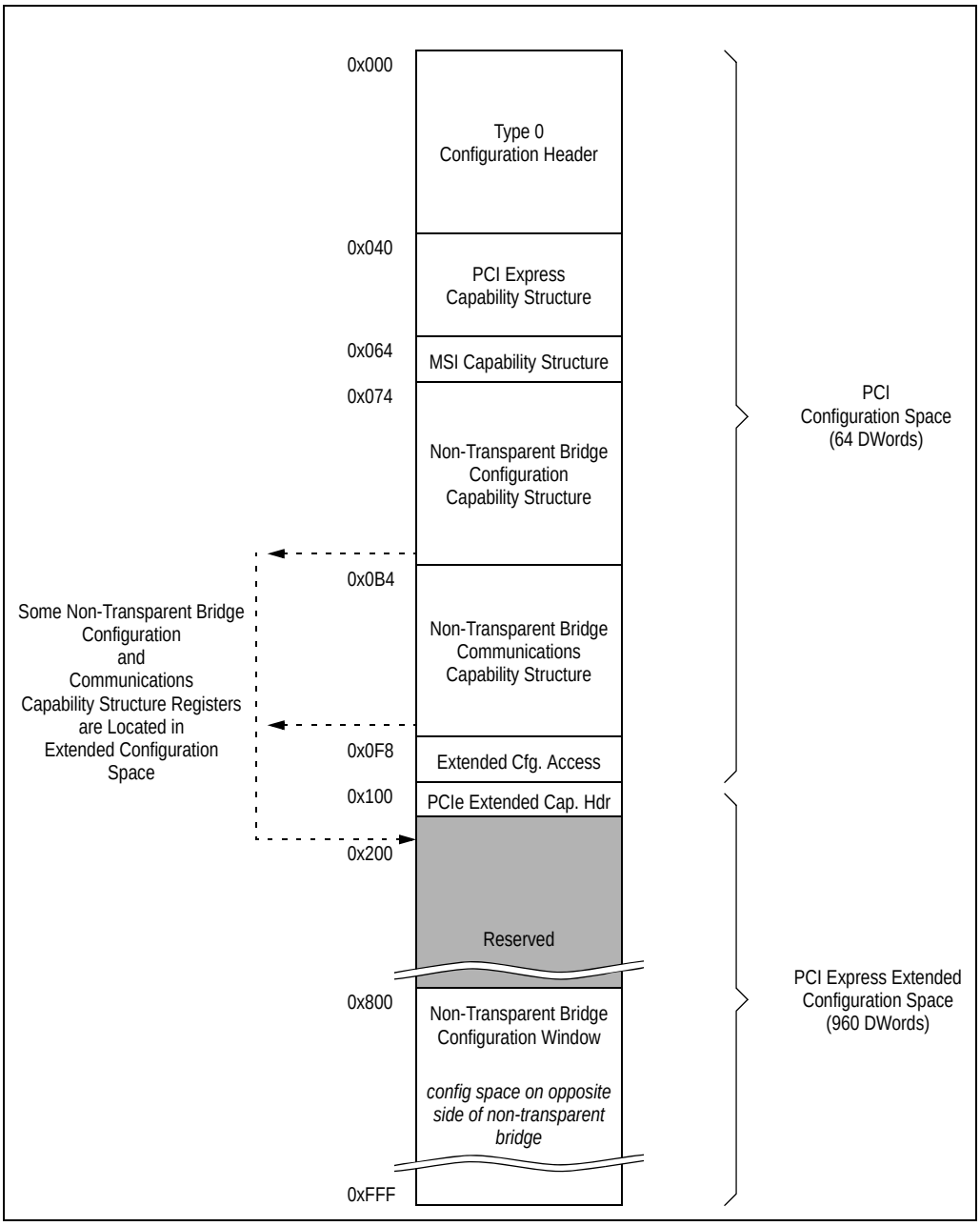

Figure 9.8 Non-Transparent Bridge Endpoint Configuration Space Layout

NTB Internal Endpoint Configuration Space Registers

All configuration space locations not listed in Table 9.9 return a value of zero when read. Writes to these locations are ignored and have no side-effects. Non-transparent bridge internal endpoint configuration space registers may be read and written via the slave SMBus interface using the base address 0x3000 added to the PCI configuration space offset address of the register to be accessed.

Note: In pdf format, clicking on a register name in the Register Definition column creates a jump to the appropriate register. To return to the starting place in this table, click on the same register name (in blue) in the register section.

Notes

Cfg. Offset	Size	Register Mnemonic	Register Definition
0x000	Word	PCIE_VID	PCIE_VID - Vendor Identification (0x000) on page 9-69
0x002	Word	PCIE_DID	PCIE_DID - Device Identification (0x002) on page 9-69
0x004	Word	PCIE_PCICMD	PCIE_PCICMD - PCI Command (0x004) on page 9-69
0x006	Word	PCIE_PCISTS	PCIE_PCISTS - PCI Status (0x006) on page 9-70
0x008	Byte	PCIE_RID	PCIE_RID - Revision Identification (0x008) on page 9-72
0x009	3 Bytes	PCIE_CCODE	PCIE_CCODE - Class Code (0x009) on page 9-72
0x00C	Byte	PCIE_CLS	PCIE_CLS - Cache Line Size (0x00C) on page 9-72
0x00D	Byte	PCIE_MLTIMER	PCIE_MLTIMER - Master Latency Timer (0x00D) on page 9-72
0x00E	Byte	PCIE_HDR	PCIE_HDR - Header Type (0x00E) on page 9-72
0x00F	Byte	PCIE_BIST	PCIE_BIST - Built-on Self Test (0x00F) on page 9-73
0x010	DWord	PCIE_BAR0	PCIE_BAR0 - Base Address Register 0 (0x010) on page 9-73
0x014	DWord	PCIE_BAR1	PCIE_BAR1 - Base Address Register 1 (0x014) on page 9-74
0x018	DWord	PCIE_BAR2	PCIE_BAR2 - Base Address Register 2 (0x018) on page 9-74
0x01C	DWord	PCIE_BAR3	PCIE_BAR3 - Base Address Register 3 (0x01C) on page 9-75
0x020	DWord	PCIE_BAR4	PCIE_BAR4 - Base Address Register 4 (0x020) on page 9-76
0x02C	Word	PCIE_SUBVID	PCIE_SUBVID - Subsystem Vendor ID Pointer (0x02C) on page 9-77
0x02E	Word	PCIE_SUBID	PCIE_SUBID - Subsystem ID Pointer (0x02E) on page 9-77
0x034	Byte	PCIE_CAPPTR	PCIE_CAPPTR - Capabilities Pointer (0x034) on page 9-77
0x03C	Byte	PCIE_INTRLINE	PCIE_INTRLINE - Interrupt Line (0x03C) on page 9-77
0x03D	Byte	PCIE_INTRPIN	PCIE_INTRPIN - Interrupt PIN (0x03D) on page 9-77
0x03E	Byte	PCIE_MINGNT	PCIE_MINGNT - Minimum Grant (0x03E) on page 9-77
0x03F	Byte	PCIE_MAXLAT	PCIE_MAXLAT - Maximum Latency (0x03F) on page 9-78
0x040	DWord	PCIE_PCIECAP	PCIE_PCIECAP - PCI Express Capability (0x040) on page 9-78
0x044	DWord	PCIE_PCIEDCAP	PCIE_PCIEDCAP - PCI Express Device Capabilities (0x044) on page 9-78
0x048	Word	PCIE_PCIEDCTL	PCIE_PCIEDCTL - PCI Express Device Control (0x048) on page 9-79
0x04A	Word	PCIE_PCIEDSTS	PCIE_PCIEDSTS PCI Express Device Status (0x04A) on page 9-80
0x04C	DWord	PCIE_PCIELCAP	PCIE_PCIELCAP - PCI Express Link Capabilities (0x04C) on page 9-81
0x050	Word	PCIE_PCIELCTL	PCIE_PCIELCTL - PCI Express Link Control (0x050) on page 9-81
0x052	Word	PCIE_PCIELSTS	PCIE_PCIELSTS - PCI Express Link Status (0x052) on page 9-82
0x064	DWord	PCIE_MSICAP	PCIE_MSICAP - Message Signaled Interrupt Capability and Control (0x064) on page 9-82

Table 9.9 Non-Transparent Bridge Internal Endpoint Configuration Space Registers (Part 1 of 4)

Notes

Cfg. Offset	Size	Register Mnemonic	Register Definition
0x068	DWord	PCIE_MSIADDR	PCIE_MSIADDR - Message Signaled Interrupt Address (0x068) on page 9-83
0x06C	DWord	PCIE_MSIUADDR	PCIE_MSIUADDR - Message Signaled Interrupt Upper Address (0x06C) on page 9-83
0x070	DWord	PCIE_MSIMDATA	PCIE_MSIMDATA - Message Signaled Interrupt Message Data (0x070) on page 9-83
0x074	DWord	PCIE_NTBCFGC	PCIE_NTBCFGC - Non-Transparent Bridge Configuration Capability (0x074) on page 9-83
0x078	Byte	PCIE_NTBCTL	PCIE_NTBCTL - Non-Transparent Bridge Control (0x078) on page 9-84
0x079	Byte	PCIE_NTBSTS	PCIE_NTBSTS - Non-Transparent Bridge Status (0x079) on page 9-85
0x07A	Word	PCIE_NTBEPID	PCIE_NTBEPID - Non-Transparent Bridge Endpoint Identification (0x07A) on page 9-86
0x07C	DWord	PCIE_BARSETUP0	PCIE_BARSETUP0 - BAR 0 Setup (0x07C) on page 9-87
0x080	DWord	PCIE_BARTBASE0	PCIE_BARTBASE0 - BAR 0 Translated Base Address (0x080) on page 9-88
0x084	DWord	PCIE_BARSETUP1	PCIE_BARSETUP1 - BAR 1 Setup (0x084) on page 9-89
0x088	DWord	PCIE_BARTBASE1	PCIE_BARTBASE1 - BAR 1 Translated Base Address (0x088) on page 9-90
0x08C	DWord	PCIE_BARSETUP2	PCIE_BARSETUP2 - BAR 2 Setup (0x08C) on page 9-91
0x090	DWord	PCIE_BARTBASE2	PCIE_BARTBASE2 - BAR 2 Translated Base Address (0x090) on page 9-92
0x094	DWord	PCIE_BARSETUP3	PCIE_BARSETUP3 - BAR 3 Setup (0x094) on page 9-93
0x098	DWord	PCIE_BARTBASE3	PCIE_BARTBASE3 - BAR 3 Translated Base Address (0x098) on page 9-94
0x09C	DWord	PCIE_BARSETUP4	PCIE_BARSETUP4 - BAR 4 Setup (0x09C) on page 9-95
0x0A0	DWord	PCIE_PTCCFG	PCIE_PTCCFG - Punch Through Configuration Control (0x0A0) on page 9-95
0x0A4	DWord	PCIE_PTCDATA	PCIE_PTCDATA - Punch Through Configuration Data (0x0A4) on page 9-96
0x0A8	DWord	PCIE_PTCSTS	PCIE_PTCSTS - Punch Through Configuration Status (0x0A8) on page 9-97
0x0AC	DWord	PCIE_MTADDR	PCIE_MTADDR - Mapping Table Address (0x0AC) on page 9-97
0x0B0	DWord	PCIE_MTDATA	PCIE_MTDATA - Mapping Table DATA (0x0B0) on page 9-98
0x0B4	DWord	PCIE_NTBCOMC	PCIE_NTBCOMC - Non-Transparent Bridge Communications Capability (0x0B4) on page 9-99
0x0B8	DWord	PCIE_INMSG0	PCIE_INMSG[0|1|2|3] - Inbound Message [0|1|2|3] (0x0B8-0C4) on page 9-99
0x0BC	DWord	PCIE_INMSG1	PCIE_INMSG[0|1|2|3] - Inbound Message [0|1|2|3] (0x0B8-0C4) on page 9-99

Table 9.9 Non-Transparent Bridge Internal Endpoint Configuration Space Registers (Part 2 of 4)

Notes

Cfg. Offset	Size	Register Mnemonic	Register Definition
0x0C0	DWord	PCIE_INMSG2	PCIE_INMSG[0|1|2|3] - Inbound Message [0|1|2|3] (0x0B8-0C4) on page 9-99
0x0C4	DWord	PCIE_INMSG3	PCIE_INMSG[0|1|2|3] - Inbound Message [0|1|2|3] (0x0B8-0C4) on page 9-99
0x0C8	DWord	PCIE_OUTMSG0	PCIE_OUTMSG[0|1|2|3] - Outbound Message [0|1|2|3] (0x0C8-0D4) on page 9-99
0x0CC	DWord	PCIE_OUTMSG1	PCIE_OUTMSG[0|1|2|3] - Outbound Message [0|1|2|3] (0x0C8-0D4) on page 9-99
0x0D0	DWord	PCIE_OUTMSG2	PCIE_OUTMSG[0|1|2|3] - Outbound Message [0|1|2|3] (0x0C8-0D4) on page 9-99
0x0D4	DWord	PCIE_OUTMSG3	PCIE_OUTMSG[0|1|2|3] - Outbound Message [0|1|2|3] (0x0C8-0D4) on page 9-99
0x0D8	DWord	PCIE_SCRATCHPAD0	PCIE_SCRATCHPAD[0..1] - Scratchpad [0..1] (0x0D8-ODC) on page 9-100
0x0DC	DWord	PCIE_SCRATCHPAD1	PCIE_SCRATCHPAD[0..1] - Scratchpad [0..1] (0x0D8-ODC) on page 9-100
0x0E0	DWord	PCIE_INDBELL	PCIE_INDBELL - Inbound Doorbell (0x0E0) on page 9-100
0x0E4	DWord	PCIE_OUTDBELL	PCIE_OUTDBELL - Outbound Doorbell (0x0E4) on page 9-100
0x0E8	DWord	PCIE_INTSTS	PCIE_INTSTS - Interrupt Status (0x0E8) on page 9-100
0x0EC	DWord	PCIE_INTCTL0	PCIE_INTCTL0 - Interrupt Control 0 (0x0EC) on page 9-102
0x0F0	DWord	PCIE_PMCAP	PCIE_PMCAP - PCI Power Management Capabilities (0x0F0) on page 9-105
0x0F4	DWord	PCIE_PMCSR	PCIE_PMCSR - PCI Power Management Control and Status (0x0F4) on page 9-106
0x0F8	DWord	PCIE_ECFGADDR	PCIE_ECFGADDR - Extended Configuration Space Access Address (0x0F8) on page 9-107
0x0FC	DWord	PCIE_ECFGDATA	PCIE_ECFGDATA - Extended Configuration Space Access Data (0x0FC) on page 9-107
0x100	DWord	PCIE_PCIEECAP	PCIE_PCIEECAP - PCI Express Extended Capability on page 9-107
0x200	DWord	PCIE_NTBCFG	PCIE_NTBCFG - Non-Transparent Bridge Configuration (0x200) on page 9-108
0x210	DWord	PCIE_INTCTL1	PCIE_INTCTL1 - Interrupt Control 1 (0x210) on page 9-108
0x214	DWord	PCIE_TLPPCTL	PCIE_TLPPCTL - TLP Processing Control (0x214) on page 9-112
0x218	DWord	PCIE_BARTLIMIT0	PCIE_BARTLIMIT0 - BAR 0 Translated Limit Address (0x218) on page 9-112
0x21C	DWord	PCIE_BARTLIMIT1	PCIE_BARTLIMIT1 - BAR 1 Translated Limit Address (0x21C) on page 9-113

Table 9.9 Non-Transparent Bridge Internal Endpoint Configuration Space Registers (Part 3 of 4)

Notes

Cfg. Offset	Size	Register Mnemonic	Register Definition
0x220	DWord	PCIE_BARTLIMIT2	PCIE_BARTLIMIT2 - BAR 2 Translated Limit Address (0x220) on page 9-113
0x224	DWord	PCIE_BARTLIMIT3	PCIE_BARTLIMIT3 - BAR 3 Translated Limit Address (0x224) on page 9-113
0x400 through 0xFFF			Reserved field.

Table 9.9 Non-Transparent Bridge Internal Endpoint Configuration Space Registers (Part 4 of 4)

Non-Transparent Bridge Internal Endpoint Registers

PCIE_VID - Vendor Identification (0x000)

Bit Field	Field Name	Type	Default Value	Description
15:0	VID	RO	0x111D	Vendor Identification. This field contains the 16-bit vendor ID value assigned to IDT. See section Vendor ID on page 1-4.

PCIE_DID - Device Identification (0x002)

Bit Field	Field Name	Type	Default Value	Description
15:0	DID	RO	—	Device Identification. This field contains the 16-bit device ID assigned by IDT to this non-transparent bridge. See section Device ID on page 1-4.

PCIE_PCICMD - PCI Command (0x004)

Bit Field	Field Name	Type	Default Value	Description
0	IOAE	RW	0x0	I/O Access Enable. When this bit is cleared, the non-transparent bridge does not respond to I/O access. 0x0 -(disable) Disable I/O space. 0x1 - (enable) Enable I/O space.
1	MAE	RW	0x0	Memory Access Enable. When this bit is cleared, the non-transparent bridge does not respond to memory space access. 0x0 -(disable) Disable memory space. 0x1 - (enable) Enable memory space.

Notes

Bit Field	Field Name	Type	Default Value	Description
2	BME	RW	0x0	**Bus Master Enable.** When this bit is cleared the non-transparent bridge does not issue requests (e.g., memory, I/O and MSIs since they are in-band writes) on behalf of devices on the other side of the bridge and responds to non-posted transactions with a Unsupported Request (UR) completion. This bit does not affect completions in either direction or the forwarding of non-memory or I/O requests. 0x0 - (disable) Disable request forwarding. 0x1 - (enable) Enable request forwarding.
3	SSE	RO	0x0	**Special Cycle Enable.** Not applicable.
4	MWI	RO	0x0	**Memory Write Invalidate.** Not applicable.
5	VGAS	RO	0x0	**VGA Palette Snoop.** Not applicable.
6	PERRE	RW	0x0	**Parity Error Enable.** The Master Data Parity Error bit is set in the PCI Status register if this bit is set and the non-transparent bridge receives a poisoned completion or generates a poisoned write. If this bit is set, then the Master Data Parity Error bit in the PCI Status register is never set. 0x0 - (disable) Disable Master Parity Error bit reporting. 0x1 - (enable) Enable Master Parity Error bit reporting.
7	ADSTEP	RO	0x0	**Address Data Stepping.** Not applicable.
8	SERRE	RW	0x0	**SERR Enable.** Non-fatal and fatal errors detected by the bridge are reported to the Root Complex. 0x0 - (disable) Disable non-fatal and fatal error reporting. 0x1 - (enable) Enable non-fatal and fatal error reporting.
9	FB2B	RO	0x0	**Fast Back-to-Back Enable.** Not applicable.
10	INTXD	RW	0x0	**INTx Disable.** This bit disables the bridges ability to generate INTx interrupts. This bit only affects legacy INTx interrupts generated by the bridge and does not affect MSIs 0x0 - (enable) Enable ability to generate INTx interrupt messages. 0x1 - (disable) Disable ability to generate INTx interrupt messages. This bit has no effect on the external side of the non-transparent bridge, as the external side of the non-transparent bridge never generates INTx interrupts.
15:11	Reserved	RO	0x0	Reserved field.

PCIE_PCISTS - PCI Status (0x006)

Bit Field	Field Name	Type	Default Value	Description
2:0	Reserved	RO	0x0	Reserved field.

Notes

Bit Field	Field Name	Type	Default Value	Description
3	INTS	RO	0x0	INTx Status. This bit is set when an INTx interrupt is pending from the device. INTx emulation interrupts forwarded by switch ports from devices downstream of the bridge are not reflected in this bit.
4	CAPL	RO	0x1	Capabilities List. This bit is hardwired to one to indicate that the bridge implements an extended capability list item.
5	C66MHZ	RO	0x0	66 MHz Capable. Not applicable.
6	Reserved	RO	0x0	Reserved field.
7	RB2B	RO	0x0	Fast Back-to-Back (FB2B). Not applicable.
8	MDPED	RW1C	0x0	Master Data Parity Error Detected. This bit is set when the PERRE bit is set in the PCI Command register and the bridge receives a poisoned completion or poisoned write request. 0x0 -(noerror) no error. 0x1 - (error) Poisoned write request or completion received.
10:9	DEVT	RO	0x0	DEVSEL# TIming. Not applicable.
11	STAS	RO	0x0	Signalled Target Abort. Not applicable.
12	RTAS	RW1C	0x0	Received Target Abort. This bit is set when the non-transparent bridge receives a Completer Abort (CA) completion status for a transaction it issued. 0x0 -(noerror) no error. 0x1 - (error) This bit is set when a Completer Abort (CA) completion is received.
13	RMAS	RW1C	0x0	Received Master Abort. This bit is set when the non-transparent bridge receives a Unsupported Request (UR) completion status for a transaction it issued. 0x0 - (noerror) no error. 0x1 - (error) This bit is set when a Unsupported Request (UR) completion is received.
14	SSE	RW1C	0x0	Signalled System Error. This bit is set when the non-transparent bridge sends a ERR_FATAL or ERR_NONFATAL message and the SERR Enable (SERRE) bit is set in the PCICMD register. 0x0 - (noerror) no error. 0x1 - (error) This bit is set when a fatal or non-fatal error is signalled.
15	DPE	RW1C	0x0	Detected Parity Error. This bit is set by the non-transparent bridge whenever it receives a poisoned TLP regardless of the state of the PERRE bit in the PCI Command register

Notes

PCIE_RID - Revision Identification (0x008)

Bit Field	Field Name	Type	Default Value	Description
7:0	RID	RWL	—	Revision ID. This field contains the revision identification number for the device. See <blue>17.4 “Revision ID” on page 17-2.

PCIE_CCODE - Class Code (0x009)

Bit Field	Field Name	Type	Default Value	Description
7:0	INTF	RO	0x00	Interface. No standard interface defined.
15:8	SUB	RO	0x80	Sub Class Code. This value indicates that the device is classified as “other.”
23:16	BASE	RO	0x06	Base Class Code. This value indicates that the device is a bridge.

PCIE_CLS - Cache Line Size (0x00C)

Bit Field	Field Name	Type	Default Value	Description
7:0	CLS	RW	0x0	Cache Line Size. This field has no effect on the bridges functionality but may be read and written by software.

PCIE_MLTIMER - Master Latency Timer (0x00D)

Bit Field	Field Name	Type	Default Value	Description
7:0	MLTIMER	RO	0x0	Master Latency Timer. Not applicable.

PCIE_HDR - Header Type (0x00E)

Bit Field	Field Name	Type	Default Value	Description
7:0	HDR	RO	0x00	Header Type. This value indicates a type 0 header with a single function.

Notes

PCIE_BIST - Built-on Self Test (0x00F)

Bit Field	Field Name	Type	Default Value	Description
7:0	BIST	RO	0x0	BIST. This value indicates that the non-transparent bridge does not implement BIST.

PCIE_BAR0 - Base Address Register 0 (0x010)

Bit Field	Field Name	Type	Default Value	Description
0	MEMSI	RO	—	Memory Space Indicator. This bit determines if the base address register maps into memory space or I/O space. The value of this field is determined by the MEMSI field in the BARSETUP0 register. 0x0 -(memory) memory space. 0x1 -(io) I/O space.
2:1	TYPE	RO	—	Address Type. When the MEMSI field indicates memory space, this field specifies if a 32-bit or 64-bit address format is used. The value of this field is determined by the TYPE field in the BARSETUP0 register. When the MEMSI field indicates I/O space, this field is always zero. 0x0 -(addr32) 32-bit addressing. Located in lower 4 GB address space. 0x1 -(reserved) reserved. 0x2 -(addr64) 64-bit addressing. 0x3 -(reserved) reserved.
3	PREF	RO	—	Prefetchable. If the MEMSI field selects memory, this field indicates if the memory is prefetchable. When the MEMSI field indicates I/O space, this field is always zero. The value of this field is determined by the PREF field in the BARSETUP0 register. 0x0 -(nonprefetch) non-prefetchable. 0x1 -(prefetch) prefetchable.
31:4	BADDR	RW	0x0	Base Address. This field specifies the address bits to be used by the non-transparent bridge in decoding and accepting transactions. See the PCI and PCI Express specifications for more information. The value of the SIZE field in the BARSETUP0 register controls which bits in this field may be modified. Bits that cannot be modified are always zero. When the MEMSI indicates memory and the TYPE field indicates 64-bit addressing, the upper bits of the address of the BADDR field are contained in the next consecutive odd numbered BAR which in this case is BAR1. See the PCI and PCI Express specifications for more information.

Notes

PCIE_BAR1 - Base Address Register 1 (0x014)

When the MEMSI field in BARSETUP0 is set to memory space (i.e., zero) and the TYPE field is set to 64-bit addressing, BAR1 takes on the function of the upper 32-bits of the BADDR field in BAR0. Otherwise, the BAR format below is used.

Bit Field	Field Name	Type	Default Value	Description
0	MEMSI	RO	—	Memory Space Indicator. This bit determines if the base address register maps into memory space or I/O space. The value of this field is determined by the MEMSI field in the BARSETUP1 register. 0x0 - (memory) memory space. 0x1 - (io) I/O space.
2:1	TYPE	RO	—	Address Type. When the MEMSI field indicates memory space, this field specifies if a 32-bit or 64-bit address format is used. Since this is an odd-numbered BAR, it can only be configured for a 32-bit address format. 0x0 -(addr32) 32-bit addressing. Located in lower 4 GB address space. 0x1 - (reserved) reserved. 0x1 - (reserved) reserved. 0x3 - (reserved) reserved.
3	PREF	RO	—	Prefetchable. If the MEMSI field selects memory, this field indicates if the memory is prefetchable. When the MEMSI field indicates I/O space, this field is always zero. The value of this field is determined by the MEMSI field in the BARSETUP1 register. 0x0 - (nonprefetch) non-prefetchable. 0x1 - (prefetch) prefetchable.
31:4	BADDR	RW	0x0	Base Address. This field specifies the address bits to be used by the non-transparent bridge in decoding and accepting transactions. See the PCI and PCI Express specifications for more information. The value of the SIZE field in the BARSETUP1 register controls which bits in this field may be modified. Bits that cannot be modified are always zero.

PCIE_BAR2 - Base Address Register 2 (0x018)

Bit Field	Field Name	Type	Default Value	Description
0	MEMSI	RO	—	Memory Space Indicator. This bit determines if the base address register maps into memory space or I/O space. The value of this field is determined by the MEMSI field in the BARSETUP2 register. 0x0 - (memory) memory space. 0x1 - (io) I/O space.

Notes

Bit Field	Field Name	Type	Default Value	Description
2:1	TYPE	RO	—	Address Type. When the MEMSI field indicates memory space, this field specifies if a 32-bit or 64-bit address format is used. The value of this field is determined by the TYPE field in the BARSETUP2 register. When the MEMSI field indicates I/O space, this field is always zero. 0x0 - (addr32) 32-bit addressing. Located in lower 4 GB address space. 0x1 - (reserved) reserved. 0x2 - (addr64) 64-bit addressing. 0x3 - (reserved) reserved.
3	PREF	RO	—	Prefetchable. If the MEMSI field selects memory, this field indicates if the memory is prefetchable. When the MEMSI field indicates I/O space, this field is always zero. The value of this field is determined by the PREF field in the BARSETUP2 register. 0x0 - (nonprefetch) non-prefetchable. 0x1 - (prefetch) prefetchable.
31:4	BADDR	RW	0x0	Base Address. This field specifies the address bits to be used by the non-transparent bridge in decoding and accepting transactions. See the PCI and PCI Express specifications for more information. The value of the SIZE field in the BARSETUP2 register controls which bits in this field may be modified. Bits that cannot be modified are always zero. When the MEMSI indicates memory and the TYPE field indicates 64-bit addressing, the upper bits of the address of the BADDR field are contained in the next consecutive odd numbered BAR which in this case is BAR3. See the PCI and PCI Express specifications for more information.

PCIE_BAR3 - Base Address Register 3 (0x01C)

When the MEMSI field in BARSETUP2 is set to memory space (i.e., zero) and the TYPE field is set to 64-bit addressing, BAR3 takes on the function of the upper 32-bits of the BADDR field in BAR2. Otherwise, the BAR format below is used.

Bit Field	Field Name	Type	Default Value	Description
0	MEMSI	RO	—	Memory Space Indicator. This bit determines if the base address register maps into memory space or I/O space. The value of this field is determined by the MEMSI field in the BARSETUP3 register. 0x0 - (memory) memory space. 0x1 - (io) I/O space.

Notes

Bit Field	Field Name	Type	Default Value	Description
2:1	TYPE	RO	—	Address Type. When the MEMSI field indicates memory space, this field specifies if a 32-bit or 64-bit address format is used. Since this is an odd-numbered BAR, it can only be configured for a 32-bit address format. 0x0 - (addr32) 32-bit addressing. Located in lower 4 GB address space. 0x1 - (reserved) reserved. 0x1 - (reserved) reserved. 0x3 - (reserved) reserved.
3	PREF	RO	—	Prefetchable. If the MEMSI field selects memory, this field indicates if the memory is prefetchable. When the MEMSI field indicates I/O space, this field is always zero. The value of this field is determined by the MEMSI field in the BARSETUP3 register. 0x0 - (nonprefetch) non-prefetchable. 0x1 - (prefetch) prefetchable.
31:4	BADDR	RW	0x0	Base Address. This field specifies the address bits to be used by the non-transparent bridge in decoding and accepting transactions. See the PCI and PCI Express specifications for more information. The value of the SIZE field in the BARSETUP3 register controls which bits in this field may be modified. Bits that cannot be modified are always zero.

PCIE_BAR4 - Base Address Register 4 (0x020)

The entire configuration space of the non-transparent bridge may be mapped in to PCI Express memory space using this BAR. Software should ensure that there are four or less outstanding read transactions to BAR4 mapped memory. Exceeding this number of outstanding transactions may result in completions being dropped.

Bit Field	Field Name	Type	Default Value	Description
0	MEMSI	RO	0x0	Memory Space Indicator. This bit determines if the base address register maps into memory space or I/O space. Memory space is always selected. 0x0 - (memory) memory space. 0x1 - (io) I/O space.
2:1	TYPE	RO	0x0	Address Type. 32-bit address is always selected.
3	PREF	RO	0x0	Prefetchable. Configuration registers are always non-prefetchable.
6:4	Reserved	RO	0x0	Reserved field.
31:7	BADDR	RW	0x0	Base Address. This field specifies the address bits to be used by the non-transparent bridge in decoding and accepting transactions. See the PCI and PCI Express specifications for more information. This space always requests a memory size of 4KB.

Notes

PCIE_SUBVID - Subsystem Vendor ID Pointer (0x02C)

Bit Field	Field Name	Type	Default Value	Description
15:0	SUBVID	RWL	0x0	Subsystem Vendor ID. This field identifies the vendor of the subsystem.

PCIE_SUBID - Subsystem ID Pointer (0x02E)

Bit Field	Field Name	Type	Default Value	Description
15:0	SUBID	RWL	0x0	Subsystem ID. This field identifies the subsystem.

PCIE_CAPPTR - Capabilities Pointer (0x034)

Bit Field	Field Name	Type	Default Value	Description
7:0	CAPPTR	RO	0x40	Capabilities Pointer. This field specifies a pointer to the head of the capabilities structure.

PCIE_INTRLINE - Interrupt Line (0x03C)

Bit Field	Field Name	Type	Default Value	Description
7:0	INTRLINE	RW	0x0	Interrupt Line. This register communicates interrupt line routing information. Values in this register are programmed by system software and are system architecture specific. The bridge does not use the value in this register.

PCIE_INTRPIN - Interrupt PIN (0x03D)

Bit Field	Field Name	Type	Default Value	Description
7:0	INTRPIN	RWL	0x0	Interrupt Pin. Interrupt pin or legacy interrupt messages are not used by the bridge.

PCIE_MINGNT - Minimum Grant (0x03E)

Bit Field	Field Name	Type	Default Value	Description
7:0	MINGNT	RO	0x0	Minimum Grant. Not applicable.

Notes

PCIE_MAXLAT - Maximum Latency (0x03F)

Bit Field	Field Name	Type	Default Value	Description
7:0	MAXLAT	RO	0x0	Maximum Latency. Not applicable.

PCI Express Capability Structure

PCIE_PCIECAP - PCI Express Capability (0x040)

Bit Field	Field Name	Type	Default Value	Description
7:0	CAPID	RO	0x10	Capability ID. The value of 0x10 identifies this capability as a PCI Express capability structure.
15:8	NXTPTR	RO	0x64	Next Pointer. This field contains a pointer to the next capability structure.
19:16	VER	RO	0x1	PCI Express Capability Version. This field indicates the PCI-SIG defined PCI Express capability structure version number.
23:20	TYPE	RWL	0x0	Port Type. The non-transparent bridge is advertised as a PCI Express endpoint device.The value contained in Serial EEPROM may override this default value.
24	SLOT	RWL	0x0	Slot Implemented. This bit is set when the PCI Express link associated with this Port is connected to a slot.
29:25	IMN	RO	0x0	Interrupt Message Number. The function is allocated only one MSI.
31:30	Reserved	RO	0x0	Reserved field.

PCIE_PCIEDCAP - PCI Express Device Capabilities (0x044)

Bit Field	Field Name	Type	Default Value	Description
2:0	MPAYLOAD	RWL	0x4	Maximum Payload Size Supported. This field indicates the maximum payload size that the device can support for TLPs. The default value corresponds to 2048 bytes.
4:3	PFS	RO	0x0	Phantom Functions Supported. This field indicates the support for unclaimed function number to extend the number of outstanding transactions allowed by logically combining unclaimed function numbers. The value is hardwired to 0x0 to indicate that no function number bits are used for phantom functions.
5	ETAG	RO	0x1	Extended Tag Field Support. This field indicates the maximum supported size of the Tag field as a requester. The value is hardwired to 0x1 to indicate that an 8-bit tag field is supported.

Notes

Bit Field	Field Name	Type	Default Value	Description
8:6	E0AL	RO	0x7	Endpoint L0s Acceptable Latency. This field indicates the acceptable total latency that an endpoint can withstand due to transition from the L0s state to the L0 state. The value is hardwired to 0x3 to indicate more than 4 us.
11:9	E1AL	RO	0x7	Endpoint L1 Acceptable Latency. This field indicates the acceptable total latency that an endpoint can withstand due to transition from the L1 state to the L0 state. The value is hardwired to 0x3 to indicate more than 64 us.
12	ABP	RO	0x0	Attention Button Present. When set, this bit indicates that an Attention Button is implemented on the card/module. The value contained in Serial EEPROM may override this default value.
13	AIP	RO	0x0	Attention Indicator Present. When set, this bit indicates that an Attention Indicator is implemented on the card/module. The value contained in Serial EEPROM may override this default value.
14	PIP	RO	0x0	Power Indicator Present. When set, this bit indicates that a Power Indicator is implemented on the card/module. The value contained in Serial EEPROM may override this default value.
31:15	Reserved	RO	0x0	Reserved field.

PCIE_PCIEDCTL - PCI Express Device Control (0x048)

Bit Field	Field Name	Type	Default Value	Description
0	CEREN	RW	0x0	Correctable Error Reporting Enable. This bit controls reporting of correctable errors.
1	NFEREN	RW	0x0	Non-Fatal Error Reporting Enable. This bit controls reporting of non-fatal errors.
2	FEREN	RW	0x0	Fatal Error Reporting Enable. This bit controls reporting of fatal errors.
3	URREN	RW	0x0	Unsupported Request Reporting Enable. This bit controls reporting of unsupported requests.
4	ERO	RW	0x1	Enable Relaxed Ordering. When set, this bit enables relaxed ordering. When this bit is cleared, the relaxed ordering attributed is set to strongly ordered for all transactions flowing from the opposite side of the non-transparent bridge to the current side. When this bit is set, transactions flow from the opposite side to the current side of the non-transparent bridge without modification to the relaxed ordering attribute.

Notes

Bit Field	Field Name	Type	Default Value	Description
7:5	MPS	RW	0x0	Max Payload Size. This field sets maximum TLP payload size for the device. 0x0 - (s128) 128 bytes max payload size 0x1 - (s256) 256 bytes max payload size 0x2 - (s512) 512 bytes max payload size 0x3 - (s1024) 1024 bytes max payload size 0x4 - (s2048) 2048 bytes max payload size 0x5 - reserved (treated as 128 bytes) 0x6 - reserved (treated as 128 bytes) 0x7 - reserved (treated as 128 bytes)
8	ETFEN	RW	0x0	Extended Tag Field Enable. The tag field is not modified in transactions that pass through the non-transparent bridge. In addition, the tag field is always zero for all transactions generated by the internal or external endpoints of the non-transparent bridge. Therefore, this field has no functional effect on the behavior of the non-transparent bridge.
9	PFEN	RO	0x0	Phantom Function Enable. The bridge does not support phantom function numbers. Therefore, this field is hard-wired to zero.
10	AUXPMEN	RO	0x0	Auxiliary Power PM Enable.The device does not implement this capability.
11	ENS	RW	0x0	Enable No Snoop. The non-transparent bridge does not generate transactions with the No Snoop bit set and passes transactions through the bridge with the No Snoop bit unmodified. Therefore, this field has no functional effect on the behavior of the non-transparent bridge.
14:12	MRRS	RW	0x2	Maximum Read Request Size. The non-transparent bridge does not generate transactions larger than 128 bytes and passes transactions through the bridge with the size unmodified. Therefore, this field has no functional effect on the behavior of the non-transparent bridge.
15	Reserved	RO	0x0	Reserved field.

PCIE_PCIEDSTS PCI Express Device Status (0x04A)

Bit Field	Field Name	Type	Default Value	Description
0	CED	RW1C	0x0	Correctable Error Detected. This bit indicates the status of correctable errors. Errors are logged in this register regardless of whether error reporting is enabled or not.
1	NFED	RW1C	0x0	Non-Fatal Error Detected. This bit indicates the status of correctable errors. Errors are logged in this register regardless of whether error reporting is enabled or not.
2	FED	RW1C	0x0	Fatal Error Detected. This bit indicates the status of Fatal errors. Errors are logged in this registers regardless of whether error reporting is enabled or not.

Notes

Bit Field	Field Name	Type	Default Value	Description
3	URD	RW1C	0x0	Unsupported Request Detected. This bit indicates the device received an Unsupported Request. Errors are logged in this register regardless of whether error reporting is enabled or not.
4	AUXPD	RO	0x0	Aux Power Detected. Devices that require AUX power, set this bit when AUX power is detected.This device does not require AUX power, hence the value is hardwired to zero.
5	TP	RO	0x0	Transactions Pending. The non-transparent bridge does not issue Non-Posted Requests on its own behalf. Therefore, this field is hardwired to zero.
15:6	Reserved	RO	0x0	Reserved field.

PCIE_PCIELCAP - PCI Express Link Capabilities (0x04C)

Bit Field	Field Name	Type	Default Value	Description
3:0	MAXLNKSPD	RO	0x1	Maximum Link Speed. This field is hardwired to 2.5 Gbps.
9:4	MAXLNKWDTH	RO	0x8	Maximum Link Width. This field is hardwired to 0x8.
11:10	ASPMS	RO	0x01	Active State Power Management. This field is hardwired to indicate L0s entry supported. However, since this is a “virtual” link, ASPM is not supported.
14:12	L0SEL	RO	0x0	L0s Exit Latency. Hardwired to indicate less than 64ns.
17:15	L1EL	RO	0x0	L1 Exit Latency.Hardwired to indicate less than 1us.
23:18	Reserved	RO	0x0	Reserved field.
31:24	PORTNUM	RO	0x0	Port Number. Hardwired to indicate port 0.

PCIE_PCIELCTL - PCI Express Link Control (0x050)

Bit Field	Field Name	Type	Default Value	Description
1:0	ASPM	RW	0x0	Active State Power Management (ASPM) Control. This field controls the level of ASPM supported by the link. This field is zero to indicate that ASPM is disabled on the “virtual” link.
2	Reserved	RO	0x0	Reserved field.
3	RCB	RO	0x0	Read Completion Boundary. This field is not applicable to the non-transparent bridge and is hardwired to zero.
4	LDIS	RO	0x0	Link Disable. Not applicable for endpoints.
5	LRET	RO	0x0	Link Retrain. Not applicable for endpoints.

Notes

Bit Field	Field Name	Type	Default Value	Description
6	CCLK	RW	0x0	**Common Clock Configuration**. Not applicable for "virtual" links.
7	ESYNC	RW	0x0	**Extended Sync**. Not applicable for "virtual" links.
15:8	Reserved	RO	0x0	Reserved field.

PCIE_PCIELSTS - PCI Express Link Status (0x052)

Bit Field	Field Name	Type	Default Value	Description
3:0	LS	RO	0x1	**Link Speed**. This field is hardwired to 2.5 Gbps.
9:4	LW	RO	0x8	**Link Width**. This field is hardwired to indicate a x8 link.
10	TERR	RO	0x0	**Training Error**. Not applicable for endpoints.
11	LTRAIN	RO	0x0	**Link Training**. Not applicable for endpoints.
12	SCLK	RO	0x0	**Slot Clock Configuration**. Not applicable for "virtual" links.
15:13	Reserved	RO	0x0	Reserved field.

Message Signaled Interrupt Capability Structure

PCIE_MSICAP - Message Signaled Interrupt Capability and Control (0x064)

Bit Field	Field Name	Type	Default Value	Description
7:0	CAPID	RO	0x5	**Capability ID**. The value of 0x5 identifies this capability as a MSI capability structure.
15:8	NXTPTR	RO	0x74	**Next Pointer**. This field contains a pointer to the next capability structure.
16	EN	RW	0x0	**Enable**. This bit enables MSI. 0x0 - (disable) disabled 0x1 - (enable) enabled
19:17	MMC	RO	0x0	**Multiple Message Capable**. This field contains the number of requested messages. The non-transparent bridge requests one message.
22:20	MME	RO	0x0	**Multiple Message Enable**. Hardwired to one message.
23	A64	RO	0x1	**64-bit Address Capable**. The non-transparent bridge is capable of generating messages using a 64-bit address.
31:24	Reserved	RO	0x0	Reserved field.

Notes

PCIE_MSIADDR - Message Signaled Interrupt Address (0x068)

Bit Field	Field Name	Type	Default Value	Description
1:0	Reserved	RO	0x0	Reserved field.
31:2	ADDR	RW	0x0	Message Address. This field specifies the lower portion of the DWORD address of the MSI memory write transaction.

PCIE_MSIUADDR - Message Signaled Interrupt Upper Address (0x06C)

Bit Field	Field Name	Type	Default Value	Description
31:0	UADDR	RW	0x0	Upper Message Address. This field specifies the upper portion of the DWORD address of the MSI memory write transaction. If the contents of this field are non-zero, then 64-bit address is used in the MSI memory write transaction. If the contents of this field are zero, then the 32-bit address specified in the MSIADDR field is used.

PCIE_MSIMDATA - Message Signaled Interrupt Message Data (0x070)

Bit Field	Field Name	Type	Default Value	Description
15:0	MDATA	RW	0x0	Message Data. This field contains the lower 16-bits of data that are written when a MSI is signalled.
31:16	Reserved	RO	0x0	Reserved field.

Non-Transparent Bridge Configuration Capability Structure

PCIE_NTBCFGC - Non-Transparent Bridge Configuration Capability (0x074)

Bit Field	Field Name	Type	Default Value	Description
7:0	VSID	RW	0x9	Vendor Specific Capability ID. The value of 0x9 identifies this capability as a vendor specific ID. Writes are allowed to this field for testing purposes only. Writes should never be performed to this field during normal operation.
15:8	NXTPTR	RW	0xB4	Next Pointer. This field contains a pointer to the next capability structure. Writes are allowed to this field for testing purposes only. Writes should never be performed to this field during normal operation.

Notes

Bit Field	Field Name	Type	Default Value	Description
23:16	CLENGTH	RW	0x40	Capability Length. This field defines the length in bytes of the capability. It includes the VSID and NXTPTR fields. Writes are allowed to this field for testing purposes only. Writes should never be performed to this field during normal operation.
31:24	IDTCAP	RW	0x1	IDT Capability. This field defines an IDT proprietary PCI, PCI-X or PCI Express capability. The value of 0x1 identifies this as a non-transparent bridge configuration capability structure. Writes are allowed to this field for testing purposes only. Writes should never be performed to this field during normal operation.

PCIE_NTBCTL - Non-Transparent Bridge Control (0x078)

Bit Field	Field Name	Type	Default Value	Description
1:0	OSMODE	RW	0x0 (external) 0x1 (internal) Not reset by external fundamental reset or external hot reset Reset by internal fundamental or hot reset	Opposite Side Mode. This field controls the operating mode of the opposite side of the non-transparent bridge. When the opposite side is set to not ready, all configuration transactions received on the opposite side of the non-transparent bridge are responded to with a configuration request retry status completion and all other transactions are ignored. When the opposite side is set to disabled, transactions received on the opposite side of the non-transparent bridge are discarded. Transactions still flow in the opposite direction (i.e., from the current side to opposite side). Note that phy and data link layer operations still continue. Whenever received transactions are discarded, they are accounted for by the flow control protocol at the data link layer. This means that flow control credits are returned even for discarded transactions. If the OSMODE field for one side, side A, is not ready or disabled and the OSMODE field for the other side, side B, becomes not ready or disabled, then this is a configuration/programming error. To prevent deadlock, when this occurs the side that was not ready or disabled first (i.e, in this example side A) automatically transitions to enabled. 0x0 - (enabled) opposite side enabled 0x1 - (notready) opposite side not ready 0x2 - (disabled) opposite side disabled 0x3 - (reserved) reserved

Notes

Bit Field	Field Name	Type	Default Value	Description
2	OSCFGPROT	RW	0x0[1]	Opposite Side Configuration Protection.When this bit is set, all configuration and BAR4 writes from the opposite side of the non-transparent bridge to the internal or external non-transparent bridge configuration capability structure are ignored (i.e., they are completed normally but do not modify any values). Reads to this space via configuration or BAR4 accesses when this bit is set return a value of zero for all registers in the non-transparent bridge configuration capability structure except for the NTBCFGC register, which returns its actual value.
3	RAEN	RW	0x0[1]	Reset Action Enable. When set, this bit enables the side effect specified by the Reset Action (RA) field in this register when a fundamental or hot reset is detected on the opposite side of the non-transparent bridge. This field is only relevant for the internal side of the non-transparent bridge and is read-only 0x0 in the external side of the non-transparent bridge.
4	RA	RW	0x0[1]	Reset Action. This field specifies the action to be taken when the RAEN bit is set in this register and a fundament or hot reset is detected on the opposite side of the non-transparent bridge. This field is only relevant for the internal side of the non-transparent bridge and is read-only 0x0 in the external side of the non-transparent bridge. 0x0 -(thissidenotready) this side not ready. This causes the OSMODE field in the NTBCTL register on the opposite side of the non-transparent bridge to be set to not ready. 0x1 -(oppositesidenotready) opposite side not ready. This causes the OSMODE field in this register to be set to not ready.
5	PEFR	RW	0x0[1]	Propagate External Fundamental Reset. When this bit is set and the device is configured to operate in non-transparent mode, then assertion of the PENTBRSTN signal results in a fundamental reset of the entire device.
6	Reserved	RO	0x0	Reserved field.
7	RST	RW	0x0	Fundamental Reset. Writing a one to this bit initiates a fundamental reset to the entire device. Writing a zero has no effect. This field always returns a value of zero when read.

[1] Not reset by external fundamental reset or internal/external hot reset

PCIE_NTBSTS - Non-Transparent Bridge Status (0x079)

Bit Field	Field Name	Type	Default Value	Description
0	OSFRD	RW1C	depends on reset condition[1]	Opposite Side Fundamental Reset Detected. This bit is set when a fundamental reset is detected on the opposite side of the non-transparent bridge.

Notes

Bit Field	Field Name	Type	Default Value	Description
1	OSHRD	RW1C	0x0[1]	Opposite Side Hot Reset Detected. This bit is set when a hot reset is detected on the opposite side of the non-transparent bridge.
2	OSRIP	RO	0x0[1]	Opposite Side Reset in Progress. This bit is set when a hot or fundamental reset is in progress on the opposite side of the non-transparent bridge. When this bit is set, configuration registers associated with the opposite side of the non-transparent bridge should not be accessed and transactions should not be forwarded through the bridge. The behavior of these operations during an opposite side reset is undefined.
3	FMTMISS	RW1C	0x0[1]	Forward Mapping Table Miss. This bit is set when an address routed transaction (e.g., a read request) is received by the this side of the non-transparent bridge, maps through the bridge, but whose requester does match the bus/device/function of an entry in the mapping table.
4	RMTMISS	RW1C	0x0[1]	Reverse Mapping Table Miss. This bit is set when a route by ID transaction (e.g., a completion) is received by the opposite side of the non-transparent bridge that does match the bus/device/function of an entry in the mapping table.
5	MTAERR	RW1C	0x0[1]	Mapping Table Access Error. This bit is set when the MDATA register is read or written and the ADDR field in the MTADDR register points to an invalid address.
6	ECRCERR	RW1C	0x0[1]	ECRC Error. This bit is set when a TLP with ECRC enabled is received by the non-transparent bridge and an ECRC error is detected in the TLP. Since ECRC is not checked for TLPs consumed by the NTB (e.g., configuration requests), this bit is never set due to ECRC errors in TLPs consumed by the NTB.
7	BARMISS	RW1C	0x0[1]	BARMISS. This bit is set when a TLP received by this side of the non-transparent bridge does not map to any of the BAR regions and is discarded.

1. Not reset by external fundamental reset or internal/external hot reset

PCIE_NTBEPID - Non-Transparent Bridge Endpoint Identification (0x07A)

Bit Field	Field Name	Type	Default Value	Description
2:0	FUNC	RO	0x0	Function Number. This field contains the function number value of the last configuration write transaction to this configuration space of the non-transparent bridge.
7:3	DEV	RO	0x0	Device Number. This field contains the device number value of the last configuration write transaction to this configuration space of the non-transparent bridge.

Notes

Bit Field	Field Name	Type	Default Value	Description
15:8	BUS	RO	0x0	Bus Number. This field contains the bus number value of the last configuration write transaction to this configuration space of the non-transparent bridge.

PCIE_BARSETUP0 - BAR 0 Setup (0x07C)

Bit Field	Field Name	Type	Default Value	Description
0	MEMSI	RW	0x0[1]	MEMSI Select. This field determines the MEMSI type returned in the MEMSI field of the corresponding BAR. 0x0 - (memory) memory space. 0x1 - (io) I/O space.
2:1	TYPE	RW	0x0[1]	Address Select. This field determines the value reported in the TYPE field of the corresponding BAR and selects the address space decoding used when memory space is selected in the MEMSI field in this register. When the MEMSI field indicates I/O space, this field is always zero. 0x0 -(addr32) 32-bit addressing. Located in lower 4 GB address space. 0x1 -(reserved) reserved. 0x2 -(addr64) 64-bit addressing. 0x3 -(reserved) reserved.
3	PREF	RW	0x0[1]	Prefetchable Select. This field determines the value reported in the PREF field of the corresponding BAR. 0x0 - (nonprefetch) non-prefetchable. 0x1 - (prefetch) prefetchable.

Notes

Bit Field	Field Name	Type	Default Value	Description
9:4	SIZE	RW	0x0[1]	Address Space Size. This field selects the size, in address bits, of the address space for the corresponding BAR or BAR pair when 64-bit addressing is selected. Assuming the size field is set to a valid value, the size of the address space requested by the BADDR field in the corresponding BAR is equal to 2^{SIZE} or 2^{64} when this field is zero. Bits in the BAR BADDR field correspond to PCI Express address bits. For example, bit 0 or the BAR BADDR field corresponds to PCI Express Address bit 4. Setting this field to zero allows all bits in the corresponding BAR BADDR field to be modified (i.e., selects entire 64-bit address space). Otherwise, setting this SIZE field to a non-zero value allows bits in the BAR BADDR field that correspond to PCI Express address bits greater than or equal to the SIZE field to be modified. Corresponding bits less than the SIZE field and greater than or equal to four always return a value of zero when read and cannot be modified. Setting the SIZE field to a value less than four results in all bits in the corresponding BAR BADDR field to take on a read-only zero value that effectively disables the BAR. The smallest memory size that may be requested by PCI Express is 128 (i.e., SIZE equal to 7) and the largest is 2^{32} bytes for 32-bit address space and 2^{64} bytes for 64-bit address space. The smallest I/O size that may be requested by the PES12NT3 is 16 bytes (i.e., SIZE equal to 4) while the largest allowed by PCI express is 256 bytes. The PES12NT3 does not enforce the minimum memory size or the maximum I/O size in hardware. Therefore, it 128 is the responsibility of the user to ensure that these requirements are met. Setting the SIZE field to a value greater than 32 when then MEMSI and TYPE fields in this register select I/O space or 32-bit memory space, results in bits greater than 32 being ignored (i.e., only the TYPE field can enable 64-bit addressing).
30:10	Reserved	RO	0x0	Reserved field.
31	EN	RW	0x0[1]	BAR Enable. When cleared, the corresponding BAR is disabled and returns a zero when read. 0x0 - (disabled) disabled. 0x1 - (enabled) enabled.

1. Not reset by external fundamental reset or internal/external hot reset

PCIE_BARTBASE0 - BAR 0 Translated Base Address (0x080)

Bit Field	Field Name	Type	Default Value	Description
3:0	Reserved	RO	0x0	Reserved field.

Notes

Bit Field	Field Name	Type	Default Value	Description
31:4	TBADDR	RW	0x0[1]	Translated Base Address. This field specifies the translated base address for transactions that map through BAR0 of the non-transparent bridge. When 64-bit addressing is selected, the translated base address consists of the value in this field together with the upper 32 bits of the address contained in the BARTBASE1 register.

1. Not reset by external fundamental reset or internal/external hot reset

PCIE_BARSETUP1 - BAR 1 Setup (0x084)

When the MEMSI field in BARSETUP0 is set to memory space (i.e., zero) and the TYPE field is set to 64-bit addressing, BAR1 takes on the function of the upper 32-bits of the BADDR field in BAR0. In this mode, the BARSETUP1 register takes on a read-only value of zero.

Bit Field	Field Name	Type	Default Value	Description
0	MEMSI	RW	0x0[1]	MEMSI Select. This field determines the MEMSI type returned in the MEMSI field of the corresponding BAR. 0x0 - (memory) memory space. 0x1 - (io) I/O space.
2:1	TYPE	RW	0x0[1]	Address Select. This field determines the value reported in the TYPE field of the corresponding BAR and selects the address space decoding used when memory space is selected in the MEMSI field in this register. When the MEMSI field indicates I/O space, this field is always zero. 0x0 -(addr32) 32-bit addressing. Located in lower 4 GB address space. 0x1 -(reserved) reserved. 0x2 -(reserved) reserved. 0x3 -(reserved) reserved.
3	PREF	RW	0x0[1]	Prefetchable Select. This field determines the value reported in the PREF field of the corresponding BAR. 0x0 - (nonprefetch) non-prefetchable. 0x1 - (prefetch) prefetchable.

Notes

Bit Field	Field Name	Type	Default Value	Description
9:4	SIZE	RW	0x0[1]	Address Space Size. This field selects the size, in address bits, of the address space for the corresponding BAR or BAR pair when 64-bit addressing is selected. Assuming the size field is set to a valid value, the size of the address space requested by the BADDR field in the corresponding BAR is equal to 2^{SIZE} or 2^{64} when this field is zero. Bits in the BAR BADDR field correspond to PCI Express address bits. For example, bit 0 or the BAR BADDR field corresponds to PCI Express Address bit 4. Setting this field to zero allows all bits in the corresponding BAR BADDR field to be modified (i.e., selects entire 64-bit address space). Otherwise, setting this SIZE field to a non-zero value allows bits in the BAR BADDR field that correspond to PCI Express address bits greater than or equal to the SIZE field to be modified. Corresponding bits less than the SIZE field and greater than or equal to four always return a value of zero when read and cannot be modified. Setting the SIZE field to a value less than four results in all bits in the corresponding BAR BADDR field to take on a read-only zero value that effectively disables the BAR. The smallest memory size that may be requested by PCI Express is 128 (i.e., SIZE equal to 7) and the largest is 2^{32} bytes for 32-bit address space. The smallest I/O size that may be requested by the PES12NT3 is 16 bytes (i.e., SIZE equal to 4) while the largest allowed by PCI express is 256 bytes. The PES12NT3 does not enforce the minimum memory size or the maximum I/O size in hardware. Therefore, it 128 is the responsibility of the user to ensure that these requirements are met. Setting the SIZE field to a value greater than 32 when then MEMSI and TYPE fields in this register select I/O space or 32-bit memory space, results in bits greater than 32 being ignored (i.e., only the TYPE field can enable 64-bit addressing).
30:10	Reserved	RO	0x0	Reserved field.
31	EN	RW	0x0[1]	BAR Enable. When cleared, the corresponding BAR is disabled and returns a zero when read. 0x0 - (disabled) disabled. 0x1 - (enabled) enabled.

1. Not reset by external fundamental reset or internal/external hot reset

PCIE_BARTBASE1 - BAR 1 Translated Base Address (0x088)

When the MEMSI field in BARSETUP0 is set to memory space (i.e., zero) and the TYPE field is set to 64-bit addressing, BARTBASE1 takes on the function of the upper 32-bits of the TBADDR field in BARTBASE0. In this mode, all 32-bits of BARTBASE1 may be read and written.

Bit Field	Field Name	Type	Default Value	Description
3:0	Reserved	RO	0x0	Reserved field.

Notes

Bit Field	Field Name	Type	Default Value	Description
31:4	TBADDR	RW	0x0[1]	Translated Base Address. This field specifies the translated base address for transactions that map through BAR1 of the non-transparent bridge.

1. Not reset by external fundamental reset or internal/external hot reset

PCIE_BARSETUP2 - BAR 2 Setup (0x08C)

Bit Field	Field Name	Type	Default Value	Description
0	MEMSI	RW	0x0[1]	MEMSI Select. This field determines the MEMSI type returned in the MEMSI field of the corresponding BAR. 0x0 - (memory) memory space. 0x1 - (io) I/O space.
2:1	TYPE	RW	0x0[1]	Address Select. This field determines the value reported in the TYPE field of the corresponding BAR and selects the address space decoding used when memory space is selected in the MEMSI field in this register. When the MEMSI field indicates I/O space, this field is always zero. 0x0 -(addr32) 32-bit addressing. Located in lower 4 GB address space. 0x1 -(reserved) reserved. 0x2 -(addr64) 64-bit addressing. 0x3 -(reserved) reserved.
3	PREF	RW	0x0[1]	Prefetchable Select. This field determines the value reported in the PREF field of the corresponding BAR. 0x0 - (nonprefetch) non-prefetchable. 0x1 - (prefetch) prefetchable.

Notes

Bit Field	Field Name	Type	Default Value	Description
9:4	SIZE	RW	0x0[1]	Address Space Size. This field selects the size, in address bits, of the address space for the corresponding BAR or BAR pair when 64-bit addressing is selected. Assuming the size field is set to a valid value, the size of the address space requested by the BADDR field in the corresponding BAR is equal to 2^{SIZE} or 2^{64} when this field is zero. Bits in the BAR BADDR field correspond to PCI Express address bits. For example, bit 0 or the BAR BADDR field corresponds to PCI Express Address bit 4. Setting this field to zero allows all bits in the corresponding BAR BADDR field to be modified (i.e., selects entire 64-bit address space). Otherwise, setting this SIZE field to a non-zero value allows bits in the BAR BADDR field that correspond to PCI Express address bits greater than or equal to the SIZE field to be modified. Corresponding bits less than the SIZE field and greater than or equal to four always return a value of zero when read and cannot be modified. Setting the SIZE field to a value less than four results in all bits in the corresponding BAR BADDR field to take on a read-only zero value that effectively disables the BAR. The smallest memory size that may be requested by PCI Express is 128 (i.e., SIZE equal to 7) and the largest is 2^{32} bytes for 32-bit address space and 2^{64} bytes for 64-bit address space. The smallest I/O size that may be requested by the PES12NT3 is 16 bytes (i.e., SIZE equal to 4) while the largest allowed by PCI express is 256 bytes. The PES12NT3 does not enforce the minimum memory size or the maximum I/O size in hardware. Therefore, it 128 is the responsibility of the user to ensure that these requirements are met. Setting the SIZE field to a value greater than 32 when then MEMSI and TYPE fields in this register select I/O space or 32-bit memory space, results in bits greater than 32 being ignored (i.e., only the TYPE field can enable 64-bit addressing).
30:10	Reserved	RO	0x0	Reserved field.
31	EN	RW	0x0[1]	BAR Enable. When cleared, the corresponding BAR is disabled and returns a zero when read. 0x0 - (disabled) disabled. 0x1 - (enabled) enabled.

1. Not reset by external fundamental reset or internal/external hot reset

PCIE_BARTBASE2 - BAR 2 Translated Base Address (0x090)

Bit Field	Field Name	Type	Default Value	Description
3:0	Reserved	RO	0x0	Reserved field.

Notes

Bit Field	Field Name	Type	Default Value	Description
31:4	TBADDR	RW	0x0[1]	Translated Base Address. This field specifies the translated base address for transactions that map through BAR2 of the non-transparent bridge. When 64-bit addressing is selected, the translated base address consists of the value in this field together with the upper 32 bits of the address contained in the BARTBASE1 register.

1. Not reset by external fundamental reset or internal/external hot reset

PCIE_BARSETUP3 - BAR 3 Setup (0x094)

When the MEMSI field in BARSETUP2 is set to memory space (i.e., zero) and the TYPE field is set to 64-bit addressing, BAR3 takes on the function of the upper 32-bits of the BADDR field in BAR2. In this mode, the BARSETUP3 register takes on a read-only value of zero.

Bit Field	Field Name	Type	Default Value	Description
0	MEMSI	RW	0x0[1]	MEMSI Select. This field determines the MEMSI type returned in the MEMSI field of the corresponding BAR. 0x0 - (memory) memory space. 0x1 - (io) I/O space.
2:1	TYPE	RW	0x0[1]	Address Select. This field determines the value reported in the TYPE field of the corresponding BAR and selects the address space decoding used when memory space is selected in the MEMSI field in this register. When the MEMSI field indicates I/O space, this field is always zero. 0x0 -(addr32) 32-bit addressing. Located in lower 4 GB address space. 0x1 - (reserved) reserved. 0x2 - (reserved) reserved. 0x3 - (reserved) reserved.
3	PREF	RW	0x0[1]	Prefetchable Select. This field determines the value reported in the PREF field of the corresponding BAR. 0x0 - (nonprefetch) non-prefetchable. 0x1 - (prefetch) prefetchable.

Notes

Bit Field	Field Name	Type	Default Value	Description
9:4	SIZE	RW	0x0[1]	Address Space Size. This field selects the size, in address bits, of the address space for the corresponding BAR or BAR pair when 64-bit addressing is selected. Assuming the size field is set to a valid value, the size of the address space requested by the BADDR field in the corresponding BAR is equal to 2^{SIZE} or 2^{64} when this field is zero. Bits in the BAR BADDR field correspond to PCI Express address bits. For example, bit 0 or the BAR BADDR field corresponds to PCI Express Address bit 4. Setting this field to zero allows all bits in the corresponding BAR BADDR field to be modified (i.e., selects entire 64-bit address space). Otherwise, setting this SIZE field to a non-zero value allows bits in the BAR BADDR field that correspond to PCI Express address bits greater than or equal to the SIZE field to be modified. Corresponding bits less than the SIZE field and greater than or equal to four always return a value of zero when read and cannot be modified. Setting the SIZE field to a value less than four results in all bits in the corresponding BAR BADDR field to take on a read-only zero value that effectively disables the BAR. The smallest memory size that may be requested by PCI Express is 128 (i.e., SIZE equal to 7) and the largest is 2^{32} bytes for 32-bit address space. The smallest I/O size that may be requested by the PES12NT3 is 16 bytes (i.e., SIZE equal to 4) while the largest allowed by PCI express is 256 bytes. The PES12NT3 does not enforce the minimum memory size or the maximum I/O size in hardware. Therefore, it 128 is the responsibility of the user to ensure that these requirements are met.
30:10	Reserved	RO	0x0	Reserved field.
31	EN	RW	0x0[1]	BAR Enable. When cleared, the corresponding BAR is disabled and returns a zero when read. 0x0 - (disabled) disabled. 0x1 - (enabled) enabled.

1. Not reset by external fundamental reset or internal/external hot reset

PCIE_BARTBASE3 - BAR 3 Translated Base Address (0x098)

When the MEMSI field in BARSETUP2 is set to memory space (i.e., zero) and the TYPE field is set to 64-bit addressing, BARTBASE3 takes on the function of the upper 32-bits of the TBADDR field in BARTBASE2. In this mode, all 32-bits of BARTBASE3 may be read and written.

Bit Field	Field Name	Type	Default Value	Description
3:0	Reserved	RO	0x0	Reserved field.

Notes

Bit Field	Field Name	Type	Default Value	Description
31:4	TBADDR	RW	0x0[1]	Translated Base Address. This field specifies the translated base address for transactions that map through BAR3 of the non-transparent bridge. When a transaction address is translated, the PCI address bits from bit 31 through the bit specified by the SIZE field are replaced by the corresponding bits in this field.

1. Not reset by external fundamental reset or internal/external hot reset

PCIE_BARSETUP4 - BAR 4 Setup (0x09C)

Bit Field	Field Name	Type	Default Value	Description
0	MEMSI	RO	0x0	MEMSI Select. This field determines the MEMSI type returned in the MEMSI field of the corresponding BAR. Memory space is always selected. 0x0 - (memory) memory space. 0x1 - (io) I/O space.
2:1	TYPE	RO	0x0	Address Select. This field determines the value reported in the TYPE field of the corresponding BAR. 32-bit addressing is always selected.
3	PREF	RO	0x0	Prefetchable Select. This field determines the value reported in the PREF field of the corresponding BAR. Non-prefetchable space is always selected.
9:4	SIZE	RO	0xC	Address Space Size. This field selects the size, in address bits, of the address space for the corresponding BAR. A 4KB address space is always requested.
30:10	Reserved	RO	0x0	Reserved field.
31	EN	RW	0x0[1]	BAR Enable. When cleared, the corresponding BAR is disabled and returns a zero when read. 0x0 - (disabled) disabled. 0x1 - (enabled) enabled.

1. Not reset by external fundamental reset or internal/external hot reset

PCIE_PTCCFG - Punch Through Configuration Control (0x0A0)

Bit Field	Field Name	Type	Default Value	Description
1:0	Reserved	RO	0x0	Reserved field.
7:2	REG	RW	0x0[1]	Register Number. This field selects the configuration register number as defined by Section 7.2.2 of the PCI Express Base Specification, Rev. 1.0a
11:8	EREG	RW	0x0[1]	Extended Register Number. This field selects the extended configuration register number as defined by Section 7.2.2 of the PCI Express Base Specification, Rev. 1.0a

Notes

Bit Field	Field Name	Type	Default Value	Description
14:12	FUNC	RW	0x0[1]	Function Number. This field selects the function number as defined by Section 7.2.2 of the PCI Express Base Specification, Rev. 1.0a
19:15	DEV	RW	0x0[1]	Device Number. This field selects the device number as defined by Section 7.2.2 of the PCI Express Base Specification, Rev. 1.0a
27:20	BUS	RW	0x0[1]	Bus Number. This field selects the bus number as defined by Section 7.2.2 of the PCI Express Base Specification, Rev. 1.0a
29:28	Reserved	RO	0x0	Reserved field.
30	CFGTYPE	RW	0x0	Configuration Access Type. This field selects the type of configuration access generated using the punch through mechanism. 0x0 - (type0) type 0 configuration access 0x1 - (type1) type 1 configuration access
31	OP	RW	0x0[1]	Operation Select. This field selects the type of configuration operation to be performed when the PTCDATA register is written 0x0 - (read) configuration read 0x1 - (write) configuration write

1. Not reset by external fundamental reset or internal/external hot reset

PCIE_PTCDATA - Punch Through Configuration Data (0x0A4)

Bit Field	Field Name	Type	Default Value	Description
31:0	DATA	RW	0x0[1]	Configuration Data. A write to this field will generate a configuration read or write transaction, as selected by the OP field in the PTCCFG register, on the opposite side of the non-transparent bridge. The byte enables in the generated transaction on the opposite side of the non-transparent bridge match those of the write to this register. When a configuration write operation is selected, the value written to this field is the value used in the configuration write transaction. When a configuration read operation is selected, the value written to this field is ignored and the value returned by the read may be read from this field when the DONE bit is set in the PTCSTS register. Status for the generated transaction is reported in the PTCSTS register.

1. Not reset by external fundamental reset or internal/external hot reset

Notes

PCIE_PTCSTS - Punch Through Configuration Status (0x0A8)

Bit Field	Field Name	Type	Default Value	Description
0	BUSY	ROS	0x0	Punch Through Configuration Interface Busy. This bit is set when a punch through configuration transaction is in progress. 0x0 - (idle) configuration transaction interface is idle 0x1 - (busy) configuration transaction in progress
1	DONE	RW1C	0x0[1]	Punch Through Configuration Transaction Completed. This bit is set when a punch through configuration transaction has completed and the STATUS field is valid. Writing a one to this bit clears the status bit or aborts a punch through operation in progress. 0x0 -(notdone) configuration transaction interface is idle or transaction in flight. 0x1 -(done) configuration transaction completed
4:2	STATUS	RO	0x0	Punch Through Configuration Transaction Status. This field contains the completion status of the last punch through configuration transaction and is valid only when the DONE bit in this register is set. 0x0 - sc) successful completion 0x1 - (ur) unsupported request 0x2 - (crs) configuration request retry 0x3 - (ca) completer abort 0x4 - (ra) requester abort 0x5 through 0x7 - reserved
5	PTABORT	RO	0x0	Punch Through Abort Status. This bit is set if the last punch through configuration transaction was aborted (i.e., the STATUS field in this register is set to requester abort). This bit will remain set until the next punch through configuration transaction is initiated.
6:30	Reserved	RO	0x0	Reserved field.
31	PTC	RO	0x1	Punch Through Capable. This field indicates whether or not punch through transactions are supported by the non-transparent bridge endpoint. 0x0 -(unsupported) punch through configuration transactions are not supported. In this configuration all other fields in the PTCCFG, PTCDATA and PTCSTS register are hardwired to zero. 0x1 -(supported) punch through configuration transactions are supported as defined in the PTCCFG, PTCDATA, and PTCSTS registers.

1. Not reset by external fundamental reset or internal/external hot reset

PCIE_MTADDR - Mapping Table Address (0x0AC)

Bit Field	Field Name	Type	Default Value	Description
1:0	Reserved	RO	0x0	Reserved field.

Notes

Bit Field	Field Name	Type	Default Value	Description
5:2	ADDR	RW	0x0[1]	Mapping Table Address. This field contains the DWord address of a mapping table entry.
31:6	Reserved	RO	0x0	Reserved field.

1. Not reset by external fundamental reset or internal/external hot reset

PCIE_MTDATA - Mapping Table DATA (0x0B0)

Bit Field	Field Name	Type	Default Value	Description
0	V	RW	0x0[1]	Mapping Table Entry Valid. Reading this field returns the mapping table entry pointed to by the ADDR field in the MTADDR register. Writing this field updates the mapping table entry pointed to by the ADDR field. Only DWord accesses are supported to this register. Non DWord accesses result in an unsupported request completion. When set, this field indicates if the table entry is valid.
15:1	Reserved	RO	0x0	Reserved field.
18:16	FUNC	RW	0x0[1]	Mapping Table Function Number. Reading this field returns the mapping table entry pointed to by the ADDR field in the MTADDR register. Writing this field updates the mapping table entry pointed to by the ADDR field. Only DWord accesses are supported to this register. Non DWord accesses result in an unsupported request completion. This field contains the mapping table entry function number.
23:19	DEV	RW	0x0[1]	Mapping Table Device Number. Reading this field returns the mapping table entry pointed to by the ADDR field in the MTADDR register. Writing this field updates the mapping table entry pointed to by the ADDR field. Only DWord accesses are supported to this register. Non DWord accesses result in an unsupported request completion. This field contains the mapping table entry device number.
31:24	BUS	RW	0x0[1]	Mapping Table Bus Number. Reading this field returns the mapping table entry pointed to by the ADDR field in the MTADDR register. Writing this field updates the mapping table entry pointed to by the ADDR field. Only DWord accesses are supported to this register. Non DWord accesses result in an unsupported request completion. This field contains the mapping table entry bus number.

1. Not reset by external fundamental reset or internal/external hot reset

Notes

Non-Transparent Bridge Communications Capability Structure

PCIE_NTBCOMC - Non-Transparent Bridge Communications Capability (0x0B4)

Bit Field	Field Name	Type	Default Value	Description
7:0	VSID	RO	0x9	Vendor Specific Capability ID. The value of 0x9 identifies this capability as a vendor specific ID.
15:8	NXTPTR	RO	0xF0	Next Pointer. This field contains a pointer to the next capability structure.
23:16	CLENGTH	RO	0x3C	Capability Length. This field defines the length in bytes of the capability. It includes the VSID and NXTPTR fields.
31:24	IDTCAP	RO	0x2	IDT Capability. This field defines an IDT proprietary PCI, PCI-X or PCI Express capability. The value of 0x2 identifies this as a non-transparent bridge communications capability structure

PCIE_INMSG[0|1|2|3] - Inbound Message [0|1|2|3] (0x0B8-0C4)

Bit Field	Field Name	Type	Default Value	Description
31:0	INMSG	RO	0x0	Inbound Message. This read only field contains the value written by an agent to the corresponding Outbound Message [0|1|2|3] (OUTMSG[0|1|2|3]) register located in PCI configuration space on the opposite side of the non-transparent bridge.

PCIE_OUTMSG[0|1|2|3] - Outbound Message [0|1|2|3] (0x0C8-0D4)

Bit Field	Field Name	Type	Default Value	Description
31:0	OUTMSG	RW	0x0	Outbound Message. When written, the value in this field and that of the corresponding Inbound Message [0|1|2|3] (INMSG[0|1|2|3]) register located in PCI configuration space on the opposite side of the non-transparent bridge are modified with the value written. In addition, the corresponding Inbound Message (INMSG[0|1|2|3]) bit is set in the Interrupt Status (INTSTS) register located in PCI configuration space on the opposite side of the non-transparent bridge.

Notes

PCIE_SCRATCHPAD[0..1] - Scratchpad [0..1] (0x0D8-ODC)

Bit Field	Field Name	Type	Default Value	Description
31:0	SCRATCHPAD	RW	0x0	Scratchpad Value. This scratchpad register may be read and written from both sides of the non-transparent bridge. Scratchpad registers may not be accessed using the Extended Configuration Space Data (ECFGDATA) register. The behavior of scratchpad register accesses using this mechanism is undefined.

PCIE_INDBELL - Inbound Doorbell (0x0E0)

Bit Field	Field Name	Type	Default Value	Description
31:0	INDBELL	RW1C	0x0	Inbound Doorbell. Each bit in this field corresponds to status of one of the 32 inbound doorbells.The state of these bits is determined by the value written by an agent to the Outbound Doorbell (OUTDBELL) register located in PCI configuration space on the opposite side of the of the non-transparent bridge.

PCIE_OUTDBELL - Outbound Doorbell (0x0E4)

Bit Field	Field Name	Type	Default Value	Description
31:0	OUTDBELL	RW	0x0	Outbound Doorbell. Each bit in this field corresponds to status of one of the 32 outbound doorbells. Setting a bid in this register results in the corresponding bit being set in the Inbound Doorbell (INDBELL) register located in PCI configuration space on the opposite side of the non-transparent bridge.

PCIE_INTSTS - Interrupt Status (0x0E8)

Bit Field	Field Name	Type	Default Value	Description
0	INMSG0	RW1C	0x0	Inbound Message 0. This bit is set whenever a value is written to the OUTMSG0 register located in PCI configuration space on the opposite side of the non-transparent bridge. The action taken when this bit is set is determined by the Interrupt Control 0 (INTCTL0) register.
1	INMSG1	RW1C	0x0	Inbound Message 1. This bit is set whenever a value is written to the OUTMSG1 register located in PCI configuration space on the opposite side of the non-transparent bridge. The action taken when this bit is set is determined by the Interrupt Control 0 (INTCTL0) register.

Notes

Bit Field	Field Name	Type	Default Value	Description
2	INMSG2	RW1C	0x0	Inbound Message 2. This bit is set whenever a value is written to the OUTMSG2 register located in PCI configuration space on the opposite side of the non-transparent bridge. The action taken when this bit is set is determined by the Interrupt Control 0 (INTCTL0) register.
3	INMSG3	RW1C	0x0	Inbound Message 3. This bit is set whenever a value is written to the OUTMSG3 register located in PCI configuration space on the opposite side of the non-transparent bridge. The action taken when this bit is set is determined by the Interrupt Control 0 (INTCTL0) register.
4	INDBELL	RO	0x0	Inbound Doorbell. This bit is set whenever a bit is set in the Inbound Doorbell (INDBELL) register. The action taken when this bit is set is determined by the Interrupt Control 0 (INTCTL0) register.
5	OSRD	RW1C	depends on reset condition Sticky	Opposite Side Reset Detected. This bit is set whenever a fundamental or hot reset is detected on the opposite side of the non-transparent bridge. The action taken when this bit is set is determined by the Interrupt Control 0 (INTCTL0) register.
6	OSPSTATEM	RW1C	0x0	Opposite Side Power State Modification. This bit is set whenever a modification is made to the PSTATE field in the PMCSR register on the opposite side of the non-transparent bridge.
7	PALINKUP	RW1C	Undefined Sticky	Port A Link Up. This bit is set whenever the port A data link layer transitions from a DL_Down to a DL_Up state. The action taken when this bit is set is determined by the Interrupt Control 1 (INTCTL1) register.
8	PALINKDN	RW1C	Undefined Sticky	Port A Link Down. This bit is set whenever the port A data link layer transitions from a DL_up to a DL_Down state. The action taken when this bit is set is determined by the Interrupt Control 1 (INTCTL1) register.
9	PBLINKUP	RW1C	Undefined Sticky	Port B Link Up. This bit is set whenever the port B data link layer transitions from a DL_Down to a DL_Up state. The action taken when this bit is set is determined by the Interrupt Control 1 (INTCTL1) register.
10	PBLINKDN	RW1C	Undefined Sticky	Port B Link Down. This bit is set whenever the port B data link layer transitions from a DL_up to a DL_Down state. The action taken when this bit is set is determined by the Interrupt Control 1 (INTCTL1) register.
11	PCLINKUP	RW1C	Undefined Sticky	Port C Link Up. This bit is set whenever the port C data link layer transitions from a DL_Down to a DL_Up state. The action taken when this bit is set is determined by the Interrupt Control 1 (INTCTL1) register.
12	PCLINKDN	RW1C	Undefined Sticky	Port C Link Down. This bit is set whenever the port C data link layer transitions from a DL_up to a DL_Down state. The action taken when this bit is set is determined by the Interrupt Control 1 (INTCTL1) register.
31:13	Reserved	RO	0x0	Reserved field.

Notes

PCIE_INTCTL0 - Interrupt Control 0 (0x0EC)

Bit Field	Field Name	Type	Default Value	Description
2:0	INMSG0	RW	0x0	Inbound Message 0 Configuration. This field encodes the action taken when the INMSG0 bit in the INTSTS register is set, or cleared when INTx interrupt signalling is enabled. Regardless of the value of this field, an MSI is only sent when Enable (EN) bit is set in the MSICAP register. Similarly, and INTx message is only sent if not disabled by the INTXD bit in the PCICMD register. The action (i.e., this field) should not be modified while the corresponding bit is set. Modifying the action when the corresponding bit is set produces undefined results. 0x0 -(disabled) interrupt is masked/disabled. 0x1 -(msi) send a Message Signalled Interrupt (MSI) as specified by the MSI capability structure. 0x2 -(int_a) generate INTA assertion and negation messages. 0x3 -(int_b) generate INTB assertion and negation messages. 0x4 -(int_c) generate INTC assertion and negation messages. 0x5 -(int_d) generate INTD assertion and negation messages. 0x6 though 0x8 -(reserved) reserved.
5:3	INMSG1	RW	0x0	Inbound Message 1 Configuration. This field encodes the action taken when the INMSG1 bit in the INTSTS register is set, or cleared when INTx interrupt signalling is enabled. Regardless of the value of this field, an MSI is only sent when Enable (EN) bit is set in the MSICAP register. Similarly, and INTx message is only sent if not disabled by the INTXD bit in the PCICMD register. The action (i.e., this field) should not be modified while the corresponding bit is set. Modifying the action when the corresponding bit is set produces undefined results. 0x0 -(disabled) interrupt is masked/disabled. 0x1 -(msi) send a Message Signalled Interrupt (MSI) as specified by the MSI capability structure. 0x2 -(int_a) generate INTA assertion and negation messages. 0x3 -(int_b) generate INTB assertion and negation messages. 0x4 -(int_c) generate INTC assertion and negation messages. 0x5 -(int_d) generate INTD assertion and negation messages. 0x6 though 0x8 -(reserved) reserved.

Notes

Bit Field	Field Name	Type	Default Value	Description
8:6	INMSG2	RW	0x0	Inbound Message 2 Configuration. This field encodes the action taken when the INMSG2 bit in the INTSTS register is set, or cleared when INTx interrupt signalling is enabled. Regardless of the value of this field, an MSI is only sent when Enable (EN) bit is set in the MSICAP register. Similarly, and INTx message is only sent if not disabled by the INTXD bit in the PCICMD register. The action (i.e., this field) should not be modified while the corresponding bit is set. Modifying the action when the corresponding bit is set produces undefined results. 0x0 -(disabled) interrupt is masked/disabled. 0x1 -(msi) send a Message Signalled Interrupt (MSI) as specified by the MSI capability structure. 0x2 -(int_a) generate INTA assertion and negation messages. 0x3 -(int_b) generate INTB assertion and negation messages. 0x4 -(int_c) generate INTC assertion and negation messages. 0x5 -(int_d) generate INTD assertion and negation messages. 0x6 though 0x8 -(reserved) reserved.
11:9	INMSG3	RW	0x0	Inbound Message 3 Configuration. This field encodes the action taken when the INMSG3 bit in the INTSTS register is set, or cleared when INTx interrupt signalling is enabled. Regardless of the value of this field, an MSI is only sent when Enable (EN) bit is set in the MSICAP register. Similarly, and INTx message is only sent if not disabled by the INTXD bit in the PCICMD register. The action (i.e., this field) should not be modified while the corresponding bit is set. Modifying the action when the corresponding bit is set produces undefined results. 0x0 -(disabled) interrupt is masked/disabled. 0x1 -(msi) send a Message Signalled Interrupt (MSI) as specified by the MSI capability structure. 0x2 -(int_a) generate INTA assertion and negation messages. 0x3 -(int_b) generate INTB assertion and negation messages. 0x4 -(int_c) generate INTC assertion and negation messages. 0x5 -(int_d) generate INTD assertion and negation messages. 0x6 though 0x8 -(reserved) reserved.

Notes

Bit Field	Field Name	Type	Default Value	Description
14:12	INDBELL	RW	0x0	Inbound Doorbell Configuration. This field encodes the action taken when the INMSG1 bit in the INTSTS register is set, or cleared when INTx interrupt signalling is enabled. Regardless of the value of this field, an MSI is only sent when Enable (EN) bit is set in the MSICAP register. Similarly, and INTx message is only sent if not disabled by the INTXD bit in the PCICMD register. The action (i.e., this field) should not be modified while the corresponding bit is set. Modifying the action when the corresponding bit is set produces undefined results. 0x0 -(disabled) interrupt is masked/disabled. 0x1 -(msi) send a Message Signalled Interrupt (MSI) as specified by the MSI capability structure. 0x2 -(int_a) generate INTA assertion and negation messages. 0x3 -(int_b) generate INTB assertion and negation messages. 0x4 -(int_c) generate INTC assertion and negation messages. 0x5 -(int_d) generate INTD assertion and negation messages. 0x6 though 0x7 -(reserved) reserved.
17:15	OSRD	RW	0x0	Opposite Side Reset Detected Configuration. This field encodes the action taken when the OSRD bit in the INTSTS register is set, or cleared when INTx interrupt signalling is enabled. Regardless of the value of this field, an MSI is only sent when Enable (EN) bit is set in the MSICAP register. Similarly, and INTx message is only sent if not disabled by the INTXD bit in the PCICMD register. The action (i.e., this field) should not be modified while the corresponding bit is set. Modifying the action when the corresponding bit is set produces undefined results. 0x0 -(disabled) interrupt is masked/disabled. 0x1 -(msi) send a Message Signalled Interrupt (MSI) as specified by the MSI capability structure. 0x2 -(int_a) generate INTA assertion and negation messages. 0x3 -(int_b) generate INTB assertion and negation messages. 0x4 -(int_c) generate INTC assertion and negation messages. 0x5 -(int_d) generate INTD assertion and negation messages. 0x6 though 0x7 -(reserved) reserved.

Notes

Bit Field	Field Name	Type	Default Value	Description
20:18	OSPSTATEM	RW	0x0	Opposite Side Power State Modification Configuration. This field encodes the action taken when the OSPSTATEM bit in the INTSTS register is set, or cleared when INTx interrupt signalling is enabled. Regardless of the value of this field, an MSI is only sent when Enable (EN) bit is set in the MSICAP register. Similarly, and INTx message is only sent if not disabled by the INTXD bit in the PCICMD register. The action (i.e., this field) should not be modified while the corresponding bit is set. Modifying the action when the corresponding bit is set produces undefined results. 0x0 -(disabled) interrupt is masked/disabled. 0x1 -(msi) send a Message Signalled Interrupt (MSI) as specified by the MSI capability structure. 0x2 -(int_a) generate INTA assertion and negation messages. 0x3 -(int_b) generate INTB assertion and negation messages. 0x4 -(int_c) generate INTC assertion and negation messages. 0x5 -(int_d) generate INTD assertion and negation messages. 0x6 though 0x7 -(reserved) reserved.
28:21	Reserved	RO	0x0	Reserved field.
31:29	MSITC	RW	0x0	MSI Traffic Class. This field contains the traffic class to be used with MSI transaction. 0x0 -(tc0) traffic class 0 0x1 -(tc1) traffic class 1 0x2 -(tc2) traffic class 2 0x3 -(tc3) traffic class 3 0x4 -(tc4) traffic class 4 0x5 -(tc5) traffic class 5 0x6 -(tc6) traffic class 6 0x7 -(tc7) traffic class 7

Power Management Capability Structure

PCIE_PMCAP - PCI Power Management Capabilities (0x0F0)

Bit Field	Field Name	Type	Default Value	Description
7:0	CAPID	RO	0x1	Capability ID. The value of 0x1 identifies this capability as a PCI power management capability structure.
15:8	NXTPTR	RO	0x0	Next Pointer. This field contains 0x0 indicating that it is the last capability.
18:16	VER	RO	0x2	Power Management Capability Version. This field indicates compliance with version two of the specification.
19	PMECLK	RO	0x0	PME Clock. Does not apply to PCI Express.
20	Reserved	RO	0x0	Reserved field.

Notes

Bit Field	Field Name	Type	Default Value	Description
21	DEVSP	RWL	0x0	**Device Specific Initialization.** The value of zero indicates that no device specific initialization is required.
24:22	AUXI	RO	0x0	**AUX Current.** not used
25	D1	RO	0x0	**D1 Support.** This field indicates that the PES12NT3 does not support D1.
26	D2	RO	0x0	**D2 Support.** This field indicates that the PES12NT3 does not support D2.
31:27	PME	RO	0x0	**PME Support.** Non-transparent bridge endpoints never generate a PME message. This field indicates the power states in which the port may generate a PME.

PCIE_PMCSR - PCI Power Management Control and Status (0x0F4)

Bit Field	Field Name	Type	Default Value	Description
1:0	PSTATE	RW	0x0	**Power State.** This field is used to determine the current power state and to set a new power state. 0x0 - (d0) D0 state 0x1 -(d1) D1 state (not supported by the PES12NT3 and reserved) 0x2- (d2) D2 state (not supported by the PES12NT3 and reserved) 0x3 -(d3) $D3_{hot}$ state
7:2	Reserved	RO	0x0	Reserved field.
8	PMEE	RO	0x0	**PME Enable.** Non-transparent bridge endpoints never generate PM_PME messages. Therefore, this bit is hard-wired to zero.
12:9	DSEL	RO	0x0	**Data Select.** The optional data register is not implemented.
14:13	DSCALE	RO	0x0	**Data Scale.** The optional data register is not implemented.
15	PMES	RO	0x0	**PME Status.** Non-transparent bridge endpoints don't support PME notification. Therefore, this bit is hardwired to zero.
21:16	Reserved	RO	0x0	Reserved field.
22	B2B3	RO	0x0	**B2/B3 Support.** Does not apply to PCI Express.
23	BPCCE	RO	0x0	**Bus Power/Clock Control Enable.** Does not apply to PCI Express.
31:24	DATA	RO	0x0	**Data.** This optional field is not implemented.

Notes

Extended Configuration Space Access Registers

PCIE_ECFGADDR - Extended Configuration Space Access Address (0x0F8)

Bit Field	Field Name	Type	Default Value	Description
1:0	Reserved	RO	0x0	Reserved field.
7:2	REG	RW	0x0	Register Number. This field selects the configuration register number as defined by Section 7.2.2 of the PCI Express Base Specification, Rev. 1.0a
11:8	EREG	RW	0x0	Extended Register Number. This field selects the extended configuration register number as defined by Section 7.2.2 of the PCI Express Base Specification, Rev. 1.0a
31:12	Reserved	RO	0x0	Reserved field.

PCIE_ECFGDATA - Extended Configuration Space Access Data (0x0FC)

Bit Field	Field Name	Type	Default Value	Description
31:0	DATA	RW	0x0	Configuration Data. A read from this field will return the configuration space register value pointed to by the ECFGADDR register. A write to this field will update the contents of the configuration space register pointed to by the ECFGADDR register with the value written. For both reads and writes, the byte enables correspond to those used to access this field. When the ECFGADDR register points to the ECFGDATA register, then reads from ECFGDATA return zero and writes are ignored. When the ECFGADDR register points to itself, writes to the ECFGDATA register modify the contents of the ECFGADDR register. Note: Accessing the ECFGDATA or ECFGDATA data registers on the opposite side of the non-transparent bridge produces undefined results.

PCI Express Extended Capability Header

PCIE_PCIEECAP - PCI Express Extended Capability

Bit Field	Field Name	Type	Default Value	Description
15:0	CAPID	RO	0x0	Capability ID. The value of 0x0. indicates that the non-transparent bridge endpoint does not implement any extended capabilities.
19:16	CAPVER	RO	0x0	Capability Version. Not applicable.
31:20	NXTPTR	RO	0x0	Next Pointer. The value of 0x0 indicates that there are no extended capabilities.

Notes

Non-Transparent Bridge Control and Status Registers

PCIE_NTBCFG - Non-Transparent Bridge Configuration (0x200)

Bit Field	Field Name	Type	Default Value	Description
31:0	Reserved	RW	0x0	Reserved field.

PCIE_INTCTL1 - Interrupt Control 1 (0x210)

Bit Field	Field Name	Type	Default Value	Description
2:0	PALINKUP	RW	0x0	Port A Link Up Configuration. This field encodes the action taken when the PALINKUP bit in the INTSTS register is set, or cleared when INTx interrupt signalling is enabled. Regardless of the value of this field, an MSI is only sent when the Enable (EN) bit is set in the MSICAP register. Similarly, and INTx message is only sent if not disabled by the INTXD bit in the PCICMD register. The action (i.e., this field) should not be modified while the corresponding bit is set. Modifying the action when the corresponding bit is set produces undefined results. 0x0 -(disabled) interrupt is masked/disabled. 0x1 -(msi) send a Message Signalled Interrupt (MSI) as specified by the MSI capability structure. 0x2 -(int_a) generate INTA assertion and negation messages. 0x3 -(int_b) generate INTB assertion and negation messages. 0x4 -(int_c) generate INTC assertion and negation messages. 0x5 -(int_d) generate INTD assertion and negation messages. 0x6 though 0x8 -(reserved) reserved.

Notes

Bit Field	Field Name	Type	Default Value	Description
5:3	PALINKDN	RW	0x0	Port A Link Down Configuration. This field encodes the action taken when the PALINKDN bit in the INTSTS register is set, or cleared when INTx interrupt signalling is enabled. Regardless of the value of this field, an MSI is only sent when the Enable (EN) bit is set in the MSICAP register. Similarly, and INTx message is only sent if not disabled by the INTXD bit in the PCICMD register. The action (i.e., this field) should not be modified while the corresponding bit is set. Modifying the action when the corresponding bit is set produces undefined results. 0x0 -(disabled) interrupt is masked/disabled. 0x1 -(msi) send a Message Signalled Interrupt (MSI) as specified by the MSI capability structure. 0x2 -(int_a) generate INTA assertion and negation messages. 0x3 -(int_b) generate INTB assertion and negation messages. 0x4 -(int_c) generate INTC assertion and negation messages. 0x5 -(int_d) generate INTD assertion and negation messages. 0x6 though 0x8 -(reserved) reserved.
8:6	PBLINKUP	RW	0x0	Port B Link Up Configuration. This field encodes the action taken when the PBLINKUP bit in the INTSTS register is set, or cleared when INTx interrupt signalling is enabled. Regardless of the value of this field, an MSI is only sent when the Enable (EN) bit is set in the MSICAP register. Similarly, and INTx message is only sent if not disabled by the INTXD bit in the PCICMD register. The action (i.e., this field) should not be modified while the corresponding bit is set. Modifying the action when the corresponding bit is set produces undefined results. 0x0 -(disabled) interrupt is masked/disabled. 0x1 -(msi) send a Message Signalled Interrupt (MSI) as specified by the MSI capability structure. 0x2 -(int_a) generate INTA assertion and negation messages. 0x3 -(int_b) generate INTB assertion and negation messages. 0x4 -(int_c) generate INTC assertion and negation messages. 0x5 -(int_d) generate INTD assertion and negation messages. 0x6 though 0x8 -(reserved) reserved.

Notes

Bit Field	Field Name	Type	Default Value	Description
11:9	PBLINKDN	RW	0x0	Port B Link Down Configuration. This field encodes the action taken when the PBLINKDN bit in the INTSTS register is set, or cleared when INTx interrupt signalling is enabled. Regardless of the value of this field, an MSI is only sent when the Enable (EN) bit is set in the MSICAP register. Similarly, and INTx message is only sent if not disabled by the INTXD bit in the PCICMD register. The action (i.e., this field) should not be modified while the corresponding bit is set. Modifying the action when the corresponding bit is set produces undefined results. 0x0 -(disabled) interrupt is masked/disabled. 0x1 -(msi) send a Message Signalled Interrupt (MSI) as specified by the MSI capability structure. 0x2 -(int_a) generate INTA assertion and negation messages. 0x3 -(int_b) generate INTB assertion and negation messages. 0x4 -(int_c) generate INTC assertion and negation messages. 0x5 -(int_d) generate INTD assertion and negation messages. 0x6 though 0x8 -(reserved) reserved.
14:12	PCLINKUP	RW	0x0	Port C Link Up Configuration. This field encodes the action taken when the PCLINKUP bit in the INTSTS register is set, or cleared when INTx interrupt signalling is enabled. Regardless of the value of this field, an MSI is only sent when the Enable (EN) bit is set in the MSICAP register. Similarly, and INTx message is only sent if not disabled by the INTXD bit in the PCICMD register. The action (i.e., this field) should not be modified while the corresponding bit is set. Modifying the action when the corresponding bit is set produces undefined results. 0x0 -(disabled) interrupt is masked/disabled. 0x1 -(msi) send a Message Signalled Interrupt (MSI) as specified by the MSI capability structure. 0x2 -(int_a) generate INTA assertion and negation messages. 0x3 -(int_b) generate INTB assertion and negation messages. 0x4 -(int_c) generate INTC assertion and negation messages. 0x5 -(int_d) generate INTD assertion and negation messages. 0x6 though 0x8 -(reserved) reserved.

Notes

Bit Field	Field Name	Type	Default Value	Description
17:15	PCLINKDN	RW	0x0	Port C Link Down Configuration. This field encodes the action taken when the PCLINKDN bit in the INTSTS register is set, or cleared when INTx interrupt signalling is enabled. Regardless of the value of this field, an MSI is only sent when the Enable (EN) bit is set in the MSICAP register. Similarly, and INTx message is only sent if not disabled by the INTXD bit in the PCICMD register. The action (i.e., this field) should not be modified while the corresponding bit is set. Modifying the action when the corresponding bit is set produces undefined results. 0x0 -(disabled) interrupt is masked/disabled. 0x1 -(msi) send a Message Signalled Interrupt (MSI) as specified by the MSI capability structure. 0x2 -(int_a) generate INTA assertion and negation messages. 0x3 -(int_b) generate INTB assertion and negation messages. 0x4 -(int_c) generate INTC assertion and negation messages. 0x5 -(int_d) generate INTD assertion and negation messages. 0x6 though 0x8 -(reserved) reserved.
31:18	Reserved	RO	0x0	Reserved field.

Notes

PCIE_TLPPCTL - TLP Processing Control (0x214)

Bit Field	Field Name	Type	Default Value	Description
0	FRO	RW	0x0 Sticky	Force Relaxed Ordering. When this bit is set, all TLPs in which the relaxed attribute is applicable are modified as dictated by the Relaxed Ordering Modification (ROM) field in this register for TLPs flowing through the NTB from this side to the opposite side. When this bit is set, the state of the Enable Relaxed Ordering (ERO) bit in the PCI Express Device Control (PCIEDCTL) is ignored and has no functional affect on the operation of the device.
1	ROM	RW	0x0 Sticky	Relaxed Ordering Modification. When the FRO bit is set in this register, this field indicates the value that the relaxed ordering attribute should take on for all TLPs flowing through the NTB and in which the relaxed ordering attribute is applicable. 0x0 - (zero) Clear relaxed ordering attribute 0x1 - (one) Set relaxed ordering attribute
2	FNS	RW	0x0 Sticky	Force No-Snoop. When this bit is set, all TLPs in which the no-snoop attribute is applicable are modified as dictated by the No-Snoop Modification (NSM) field in this register for TLPs flowing through the NTB from this side to the opposite side.
3	NSM	RW	0x0 Sticky	No Snoop Modification. When the FNS bit is set in this register, this field indicates the value that the no-snoop attribute should take on for all TLPs flowing through the NTB and in which the no-snoop attribute is applicable. 0x0 - (zero) Clear no-snoop attribute 0x1 - (one) Set no-snoop attribute
31:4	Reserved	RO	0x0	Reserved field.

PCIE_BARTLIMIT0 - BAR 0 Translated Limit Address (0x218)

Bit Field	Field Name	Type	Default Value	Description
3:0	Reserved	RO	0x0	Reserved field.
31:4	TLADDR	RW	0xFFF_FFFF[1]	Translated Limit Address. This field specifies the translated limit address for transactions that map through BAR0 of the non-transparent bridge. When 64-bit addressing is selected, the translated limit address consists of the value in this field together with the upper 32 bits of the address contained in the BARTBASE1 register. A translation fails the limit test if the address is greater than the value specified in this field.

1. Not reset by external fundamental reset or internal/external hot reset

Notes

PCIE_BARTLIMIT1 - BAR 1 Translated Limit Address (0x21C)

When the MEMSI field in BARSETUP0 is set to memory space (i.e., zero) and the TYPE field is set to 64-bit addressing, BARTLIMIT1 takes on the function of the upper 32-bits of the TLADDR field in BARTLIMIT0. In this mode, all 32-bits of BARTLIMIT1 may be read and written.

Bit Field	Field Name	Type	Default Value	Description
3:0	Reserved	RO	0x0	Reserved field.
31:4	TLADDR	RW	0xFFF_FFFF[1]	Translated Limit Address. This field specifies the translated limit address for transactions that map through BAR1 of the non-transparent bridge. A translation fails the limit test if the address is greater than the value specified in this field.

1. Not reset by external fundamental reset or internal/external hot reset

PCIE_BARTLIMIT2 - BAR 2 Translated Limit Address (0x220)

Bit Field	Field Name	Type	Default Value	Description
3:0	Reserved	RO	0x0	Reserve field.
31:4	TLADDR	RW	0xFFF_FFFF[1]	Translated Limit Address. This field specifies the translated limit address for transactions that map through BAR2 of the non-transparent bridge. When 64-bit addressing is selected, the translated limit address consists of the value in this field together with the upper 32 bits of the address contained in the BARTBASE3 register. A translation fails the limit test if the address is greater than the value specified in this field.

1. Not reset by external fundamental reset or internal/external hot reset

PCIE_BARTLIMIT3 - BAR 3 Translated Limit Address (0x224)

When the MEMSI field in BARSETUP2 is set to memory space (i.e., zero) and the TYPE field is set to 64-bit addressing, BARTLIMIT3 takes on the function of the upper 32-bits of the TLADDR field in BARTLIMIT2. In this mode, all 32-bits of BARTLIMIT1 may be read and written.

Bit Field	Field Name	Type	Default Value	Description
3:0	Reserved	RO	0x0	Reserved field.
31:4	TLADDR	RW	0xFFF_FFFF[1]	Translated Limit Address. This field specifies the translated limit address for transactions that map through BAR3 of the non-transparent bridge. A translation fails the limit test if the address is greater than the value specified in this field.

1. Not reset by external fundamental reset or internal/external hot reset

Notes

NTB External Endpoint Configuration Space Registers

All configuration space locations not listed in Table 9.10 return a value of zero when read. Writes to these locations are ignored and have no side-effects.

Non-transparent bridge external endpoint configuration space registers may be read and written via the slave SMBus interface and initialized from the serial EEPROM using the CSR system address formed by adding the base address 0x3000 to the PCI configuration space offset address.

Note: In pdf format, clicking on a register name in the Register Definition column creates a jump to the appropriate register. To return to the starting place in this table, click on the same register name (in blue) in the register section.

Cfg. Offset	Size	Register Mnemonic	Register Definition
0x000	Word	PCEE_VID	PCEE_VID - Vendor Identification (0x000) on page 9-117
0x002	Word	PCEE_DID	PCEE_DID - Device Identification (0x002) on page 9-117
0x004	Word	PCEE_PCICMD	PCEE_PCICMD - PCI Command (0x004) on page 9-118
0x006	Word	PCEE_PCISTS	PCEE_PCISTS - PCI Status (0x006) on page 9-119
0x008	Byte	PCEE_RID	PCEE_RID - Revision Identification (0x008) on page 9-120
0x009	3 Bytes	PCEE_CCODE	PCEE_CCODE - Class Code (0x009) on page 9-120
0x00C	Byte	PCEE_CLS	PCEE_CLS - Cache Line Size (0x00C) on page 9-120
0x00D	Byte	PCEE_MLTIMER	PCEE_MLTIMER - Master Latency Timer (0x00D) on page 9-120
0x00E	Byte	PCEE_HDR	PCEE_HDR - Header Type (0x00E) on page 9-120
0x00F	Byte	PCEE_BIST	PCEE_BIST - Built-on Self Test (0x00F) on page 9-121
0x010	DWord	PCEE_BAR0	PCEE_BAR0 - Base Address Register 0 (0x010) on page 9-121
0x014	DWord	PCEE_BAR1	PCEE_BAR1 - Base Address Register 1 (0x014) on page 9-122
0x018	DWord	PCEE_BAR2	PCEE_BAR2 - Base Address Register 2 (0x018) on page 9-122
0x01C	DWord	PCEE_BAR3	PCEE_BAR3 - Base Address Register 3 (0x01C) on page 9-123
0x020	DWord	PCEE_BAR4	PCEE_BAR4 - Base Address Register 4 (0x020) on page 9-124
0x02C	Word	PCEE_SUBVID	PCEE_SUBVID - Subsystem Vendor ID Pointer (0x02C) on page 9-125
0x02E	Word	PCEE_SUBID	PCEE_SUBID - Subsystem ID Pointer (0x02E) on page 9-125
0x034	Byte	PCEE_CAPPTR	PCEE_CAPPTR - Capabilities Pointer (0x034) on page 9-125
0x03C	Byte	PCEE_INTRLINE	PCEE_INTRLINE - Interrupt Line (0x03C) on page 9-125
0x03D	Byte	PCEE_INTRPIN	PCEE_INTRPIN - Interrupt PIN (0x03D) on page 9-125
0x03E	Byte	PCEE_MINGNT	PCEE_MINGNT - Minimum Grant (0x03E) on page 9-125
0x03F	Byte	PCEE_MAXLAT	PCEE_MAXLAT - Maximum Latency (0x03F) on page 9-126
0x040	DWord	PCEE_PCIECAP	PCEE_PCIECAP - PCI Express Capability (0x040) on page 9-126
0x044	DWord	PCEE_PCIEDCAP	PCEE_PCIEDCAP - PCI Express Device Capabilities (0x044) on page 9-126

Table 9.10 Non-Transparent Bridge External Endpoint Configuration Space Registers (Part 1 of 4)

Notes

Cfg. Offset	Size	Register Mnemonic	Register Definition
0x048	Word	PCEE_PCIEDCTL	PCEE_PCIEDCTL - PCI Express Device Control (0x048) on page 9-127
0x04A	Word	PCEE_PCIEDSTS	PCEE_PCIEDSTS PCI Express Device Status (0x04A) on page 9-128
0x04C	DWord	PCEE_PCIELCAP	PCEE_PCIELCAP - PCI Express Link Capabilities (0x04C) on page 9-129
0x050	Word	PCEE_PCIELCTL	PCEE_PCIELCTL - PCI Express Link Control (0x050) on page 9-129
0x052	Word	PCEE_PCIELSTS	PCEE_PCIELSTS - PCI Express Link Status (0x052) on page 9-130
0x064	DWord	PCEE_MSICAP	PCEE_MSICAP - Message Signaled Interrupt Capability and Control (0x064) on page 9-130
0x068	DWord	PCEE_MSIADDR	PCEE_MSIADDR - Message Signaled Interrupt Address (0x068) on page 9-131
0x06C	DWord	PCEE_MSIUADDR	PCEE_MSIUADDR - Message Signaled Interrupt Upper Address (0x06C) on page 9-131
0x070	DWord	PCEE_MSIMDATA	PCEE_MSIMDATA - Message Signaled Interrupt Message Data (0x070) on page 9-131
0x074	DWord	PCEE_NTBCFGC	PCEE_NTBCFGC - Non-Transparent Bridge Configuration Capability (0x074) on page 9-131
0x078	Byte	PCEE_NTBCTL	PCEE_NTBCTL - Non-Transparent Bridge Control (0x078) on page 9-132
0x079	Byte	PCEE_NTBSTS	PCEE_NTBSTS - Non-Transparent Bridge Status (0x079) on page 9-133
0x07A	Word	PCEE_NTBEPID	PCEE_NTBEPID - Non-Transparent Bridge Endpoint Identification (0x07A) on page 9-134
0x07C	DWord	PCEE_BARSETUP0	PCEE_BARSETUP0 - BAR 0 Setup (0x07C) on page 9-135
0x080	DWord	PCEE_BARTBASE0	PCEE_BARTBASE0 - BAR 0 Translated Base Address (0x080) on page 9-136
0x084	DWord	PCEE_BARSETUP1	PCEE_BARSETUP1 - BAR 1 Setup (0x084) on page 9-137
0x088	DWord	PCEE_BARTBASE1	PCEE_BARTBASE1 - BAR 1 Translated Base Address (0x088) on page 9-138
0x08C	DWord	PCEE_BARSETUP2	PCEE_BARSETUP2 - BAR 2 Setup (0x08C) on page 9-139
0x090	DWord	PCEE_BARTBASE2	PCEE_BARTBASE2 - BAR 2 Translated Base Address (0x090) on page 9-140
0x094	DWord	PCEE_BARSETUP3	PCEE_BARSETUP3 - BAR 3 Setup (0x094) on page 9-141
0x098	DWord	PCEE_BARTBASE3	PCEE_BARTBASE3 - BAR 3 Translated Base Address (0x098) on page 9-142
0x09C	DWord	PCEE_BARSETUP4	PCEE_BARSETUP4 - BAR 4 Setup (0x09C) on page 9-143
0x0A0	DWord	PCEE_PTCCFG	PCEE_PTCCFG - Punch Through Configuration Control (0x0A0) on page 9-143
0x0A4	DWord	PCEE_PTCDATA	PCEE_PTCDATA - Punch Through Configuration Data (0x0A4) on page 9-144

Table 9.10 Non-Transparent Bridge External Endpoint Configuration Space Registers (Part 2 of 4)

Notes

Cfg. Offset	Size	Register Mnemonic	Register Definition
0x0A8	DWord	PCEE_PTCSTS	PCEE_PTCSTS - Punch Through Configuration Status (0x0A8) on page 9-145
0x0AC	DWord	PCEE_MTADDR	PCEE_MTADDR - Mapping Table Address (0x0AC) on page 9-145
0x0B0	DWord	PCEE_MTDATA	PCEE_MTDATA - Mapping Table DATA (0x0B0) on page 9-146
0x0B4	DWord	PCEE_NTBCOMC	PCEE_NTBCOMC - Non-Transparent Bridge Communications Capability (0x0B4) on page 9-147
0x0B8	DWord	PCEE_INMSG0	PCEE_INMSG[0|1|2|3] - Inbound Message [0|1|2|3] (0x0B8-0C4) on page 9-147
0x0BC	DWord	PCEE_INMSG1	PCEE_INMSG[0|1|2|3] - Inbound Message [0|1|2|3] (0x0B8-0C4) on page 9-147
0x0C0	DWord	PCEE_INMSG2	PCEE_INMSG[0|1|2|3] - Inbound Message [0|1|2|3] (0x0B8-0C4) on page 9-147
0x0C4	DWord	PCEE_INMSG3	PCEE_INMSG[0|1|2|3] - Inbound Message [0|1|2|3] (0x0B8-0C4) on page 9-147
0x0C8	DWord	PCEE_OUTMSG0	PCEE_OUTMSG[0|1|2|3] - Outbound Message [0|1|2|3] (0x0C8-0D4) on page 9-147
0x0CC	DWord	PCEE_OUTMSG1	PCEE_OUTMSG[0|1|2|3] - Outbound Message [0|1|2|3] (0x0C8-0D4) on page 9-147
0x0D0	DWord	PCEE_OUTMSG2	PCEE_OUTMSG[0|1|2|3] - Outbound Message [0|1|2|3] (0x0C8-0D4) on page 9-147
0x0D4	DWord	PCEE_OUTMSG3	PCEE_OUTMSG[0|1|2|3] - Outbound Message [0|1|2|3] (0x0C8-0D4) on page 9-147
0x0D8	DWord	PCEE_SCRATCHPAD0	PCEE_SCRATCHPAD[0..1] - Scratchpad [0..1] (0x0D8-ODC) on page 9-148
0x0DC	DWord	PCEE_SCRATCHPAD1	PCEE_SCRATCHPAD[0..1] - Scratchpad [0..1] (0x0D8-ODC) on page 9-148
0x0E0	DWord	PCEE_INDBELL	PCEE_INDBELL - Inbound Doorbell (0x0E0) on page 9-148
0x0E4	DWord	PCEE_OUTDBELL	PCEE_OUTDBELL - Outbound Doorbell (0x0E4) on page 9-148
0x0E8	DWord	PCEE_INTSTS	PCEE_INTSTS - Interrupt Status (0x0E8) on page 9-148
0x0EC	DWord	PCEE_INTCTL0	PCEE_INTCTL0 - Interrupt Control 0 (0x0EC) on page 9-150
0x0F0	DWord	PCEE_PMCAP	PCEE_PMCAP - PCI Power Management Capabilities (0x0F0) on page 9-153
0x0F4	DWord	PCEE_PMCSR	PCEE_PMCSR - PCI Power Management Control and Status (0x0F4) on page 9-154
0x0F8	DWord	PCEE_ECFGADDR	PCEE_ECFGADDR - Extended Configuration Space Access Address (0x0F8) on page 9-155
0x0FC	DWord	PCEE_ECFGDATA	PCEE_ECFGDATA - Extended Configuration Space Access Data (0x0FC) on page 9-155
0x100	DWord	PCEE_PCIEECAP	PCEE_PCIEECAP - PCI Express Extended Capability on page 9-155
0x200	DWord	PCEE_NTBCFG	PCEE_NTBCFG - Non-Transparent Bridge Configuration (0x200) on page 9-156

Table 9.10 Non-Transparent Bridge External Endpoint Configuration Space Registers (Part 3 of 4)

Notes

Cfg. Offset	Size	Register Mnemonic	Register Definition
0x210	DWord	PCEE_INTCTL1	PCEE_INTCTL1 - Interrupt Control 1 (0x210) on page 9-156
0x214	DWord	PCEE_TLPPCTL	PCEE_TLPPCTL - TLP Processing Control (0x214) on page 9-160
0x218	DWord	PCEE_BARTLIMIT0	PCEE_BARTLIMIT0 - BAR 0 Translated Limit Address (0x218) on page 9-160
0x21C	DWord	PCEE_BARTLIMIT1	PCEE_BARTLIMIT1 - BAR 1 Translated Limit Address (0x21C) on page 9-161
0x220	DWord	PCEE_BARTLIMIT2	PCEE_BARTLIMIT2 - BAR 2 Translated Limit Address (0x220) on page 9-161
0x224	DWord	PCEE_BARTLIMIT3	PCEE_BARTLIMIT3 - BAR 3 Translated Limit Address (0x224) on page 9-161
0x228	DWord	PCEE_FOVRSTS	PCEE_FOVRSTS - Failover Status (0x228) on page 9-162
0x22C	DWord	PCEE_FOVRCTL	PCEE_FOVRCTL - Failover Control (0x22C) on page 9-162
0x230	DWord	PCEE_FOVRTIMER	PCEE_FOVRTIMER - Failover Watchdog Timer (0x230) on page 9-163
0x400 through 0xFFF			Reserved field.

Table 9.10 Non-Transparent Bridge External Endpoint Configuration Space Registers (Part 4 of 4)

Non-Transparent Bridge External Endpoint Registers

PCEE_VID - Vendor Identification (0x000)

Bit Field	Field Name	Type	Default Value	Description
15:0	VID	RO	0x111D	Vendor Identification. This field contains the 16-bit vendor ID value assigned to IDT. See section Vendor ID on page 1-4.

PCEE_DID - Device Identification (0x002)

Bit Field	Field Name	Type	Default Value	Description
15:0	DID	RO	—	Device Identification. This field contains the 16-bit device ID assigned by IDT to this non-transparent bridge. See section Device ID on page 1-4.

Notes

PCEE_PCICMD - PCI Command (0x004)

Bit Field	Field Name	Type	Default Value	Description
0	IOAE	RW	0x0	I/O Access Enable. When this bit is cleared, the non-transparent bridge does not respond to I/O access. 0x0 -(disable) Disable I/O space. 0x1 - (enable) Enable I/O space.
1	MAE	RW	0x0	Memory Access Enable. When this bit is cleared, the non-transparent bridge does not respond to memory space access. 0x0 -(disable) Disable memory space. 0x1 - (enable) Enable memory space.
2	BME	RW	0x0	Bus Master Enable. When this bit is cleared the non-transparent bridge does not issue requests (e.g., memory, I/O and MSIs since they are in-band writes) on behalf of devices on the other side of the bridge and responds to non-posted transactions with a Unsupported Request (UR) completion. This bit does not affect completions in either direction or the forwarding of non-memory or I/O requests. 0x0 - (disable) Disable request forwarding. 0x1 - (enable) Enable request forwarding.
3	SSE	RO	0x0	Special Cycle Enable. Not applicable.
4	MWI	RO	0x0	Memory Write Invalidate. Not applicable.
5	VGAS	RO	0x0	VGA Palette Snoop. Not applicable.
6	PERRE	RW	0x0	Parity Error Enable. The Master Data Parity Error bit is set in the PCI Status register if this bit is set and the non-transparent bridge receives a poisoned completion or generates a poisoned write. If this bit is set, then the Master Data Parity Error bit in the PCI Status register is never set. 0x0 - (disable) Disable Master Parity Error bit reporting. 0x1 - (enable) Enable Master Parity Error bit reporting.
7	ADSTEP	RO	0x0	Address Data Stepping. Not applicable.
8	SERRE	RW	0x0	SERR Enable. Non-fatal and fatal errors detected by the bridge are reported to the Root Complex. 0x0 - (disable) Disable non-fatal and fatal error reporting. 0x1 - (enable) Enable non-fatal and fatal error reporting.
9	FB2B	RO	0x0	Fast Back-to-Back Enable. Not applicable.
10	INTXD	RW	0x0	INTx Disable. This bit disables the bridges ability to generate INTx interrupts. This bit only affects legacy INTx interrupts generated by the bridge and does not affect MSIs 0x0 - (enable) Enable ability to generate INTx interrupt messages. 0x1 - (disable) Disable ability to generate INTx interrupt messages. This bit has no effect on the external side of the non-transparent bridge, as the external side of the non-transparent bridge never generates INTx interrupts.
15:11	Reserved	RO	0x0	Reserved field.

Notes

PCEE_PCISTS - PCI Status (0x006)

Bit Field	Field Name	Type	Default Value	Description
2:0	Reserved	RO	0x0	Reserved field.
3	INTS	RO	0x0	INTx Status. This bit is set when an INTx interrupt is pending from the device. INTx emulation interrupts forwarded by switch ports from devices downstream of the bridge are not reflected in this bit.
4	CAPL	RO	0x1	Capabilities List. This bit is hardwired to one to indicate that the bridge implements an extended capability list item.
5	C66MHZ	RO	0x0	66 MHz Capable. Not applicable.
6	Reserved	RO	0x0	Reserved field.
7	RB2B	RO	0x0	Fast Back-to-Back (FB2B). Not applicable.
8	MDPED	RW1C	0x0	Master Data Parity Error Detected. This bit is set when the PERRE bit is set in the PCI Command register and the bridge receives a poisoned completion or poisoned write request. 0x0 -(noerror) no error. 0x1 - (error) Poisoned write request or completion received.
10:9	DEVT	RO	0x0	DEVSEL# TIming. Not applicable.
11	STAS	RO	0x0	Signalled Target Abort. Not applicable.
12	RTAS	RW1C	0x0	Received Target Abort. This bit is set when the non-transparent bridge receives a Completer Abort (CA) completion status for a transaction it issued. 0x0 -(noerror) no error. 0x1 - (error) This bit is set when a Completer Abort (CA) completion is received.
13	RMAS	RW1C	0x0	Received Master Abort. This bit is set when the non-transparent bridge receives a Unsupported Request (UR) completion status for a transaction it issued. 0x0 - (noerror) no error. 0x1 - (error) This bit is set when a Unsupported Request (UR) completion is received.
14	SSE	RW1C	0x0	Signalled System Error. This bit is set when the non-transparent bridge sends a ERR_FATAL or ERR_NONFATAL message and the SERR Enable (SERRE) bit is set in the PCICMD register. 0x0 - (noerror) no error. 0x1 - (error) This bit is set when a fatal or non-fatal error is signalled.
15	DPE	RW1C	0x0	Detected Parity Error. This bit is set by the non-transparent bridge whenever it receives a poisoned TLP regardless of the state of the PERRE bit in the PCI Command register

Notes

PCEE_RID - Revision Identification (0x008)

Bit Field	Field Name	Type	Default Value	Description
7:0	RID	RWL	—	Revision ID. This field contains the revision identification number for the device. See <blue>17.4 “Revision ID” on page 17-2.

PCEE_CCODE - Class Code (0x009)

Bit Field	Field Name	Type	Default Value	Description
7:0	INTF	RO	0x00	Interface. No standard interface defined.
15:8	SUB	RO	0x80	Sub Class Code. This value indicates that the device is classified as “other.”
23:16	BASE	RO	0x06	Base Class Code. This value indicates that the device is a bridge.

PCEE_CLS - Cache Line Size (0x00C)

Bit Field	Field Name	Type	Default Value	Description
7:0	CLS	RW	0x0	Cache Line Size. This field has no effect on the bridges functionality but may be read and written by software.

PCEE_MLTIMER - Master Latency Timer (0x00D)

Bit Field	Field Name	Type	Default Value	Description
7:0	MLTIMER	RO	0x0	Master Latency Timer. Not applicable.

PCEE_HDR - Header Type (0x00E)

Bit Field	Field Name	Type	Default Value	Description
7:0	HDR	RO	0x00	Header Type. This value indicates a type 0 header with a single function.

Notes

PCEE_BIST - Built-on Self Test (0x00F)

Bit Field	Field Name	Type	Default Value	Description
7:0	BIST	RO	0x0	BIST. This value indicates that the non-transparent bridge does not implement BIST.

PCEE_BAR0 - Base Address Register 0 (0x010)

Bit Field	Field Name	Type	Default Value	Description
0	MEMSI	RO	—	Memory Space Indicator. This bit determines if the base address register maps into memory space or I/O space. The value of this field is determined by the MEMSI field in the BARSETUP0 register. 0x0 -(memory) memory space. 0x1 -(io) I/O space.
2:1	TYPE	RO	—	Address Type. When the MEMSI field indicates memory space, this field specifies if a 32-bit or 64-bit address format is used. The value of this field is determined by the TYPE field in the BARSETUP0 register. When the MEMSI field indicates I/O space, this field is always zero. 0x0 -(addr32) 32-bit addressing. Located in lower 4 GB address space. 0x1 -(reserved) reserved. 0x2 -(addr64) 64-bit addressing. 0x3 -(reserved) reserved.
3	PREF	RO	—	Prefetchable. If the MEMSI field selects memory, this field indicates if the memory is prefetchable. When the MEMSI field indicates I/O space, this field is always zero. The value of this field is determined by the PREF field in the BARSETUP0 register. 0x0 -(nonprefetch) non-prefetchable. 0x1 -(prefetch) prefetchable.
31:4	BADDR	RW	0x0	Base Address. This field specifies the address bits to be used by the non-transparent bridge in decoding and accepting transactions. See the PCI and PCI Express specifications for more information. The value of the SIZE field in the BARSETUP0 register controls which bits in this field may be modified. Bits that cannot be modified are always zero. When the MEMSI indicates memory and the TYPE field indicates 64-bit addressing, the upper bits of the address of the BADDR field are contained in the next consecutive odd numbered BAR which in this case is BAR1. See the PCI and PCI Express specifications for more information.

Notes

PCEE_BAR1 - Base Address Register 1 (0x014)

When the MEMSI field in BARSETUP0 is set to memory space (i.e., zero) and the TYPE field is set to 64-bit addressing, BAR1 takes on the function of the upper 32-bits of the BADDR field in BAR0. Otherwise, the BAR format below is used.

Bit Field	Field Name	Type	Default Value	Description
0	MEMSI	RO	—	Memory Space Indicator. This bit determines if the base address register maps into memory space or I/O space. The value of this field is determined by the MEMSI field in the BARSETUP1 register. 0x0 - (memory) memory space. 0x1 - (io) I/O space.
2:1	TYPE	RO	—	Address Type. When the MEMSI field indicates memory space, this field specifies if a 32-bit or 64-bit address format is used. Since this is an odd-numbered BAR, it can only be configured for a 32-bit address format. 0x0 -(addr32) 32-bit addressing. Located in lower 4 GB address space. 0x1 - (reserved) reserved. 0x1 - (reserved) reserved. 0x3 - (reserved) reserved.
3	PREF	RO	—	Prefetchable. If the MEMSI field selects memory, this field indicates if the memory is prefetchable. When the MEMSI field indicates I/O space, this field is always zero. The value of this field is determined by the MEMSI field in the BARSETUP1 register. 0x0 - (nonprefetch) non-prefetchable. 0x1 - (prefetch) prefetchable.
31:4	BADDR	RW	0x0	Base Address. This field specifies the address bits to be used by the non-transparent bridge in decoding and accepting transactions. See the PCI and PCI Express specifications for more information. The value of the SIZE field in the BARSETUP1 register controls which bits in this field may be modified. Bits that cannot be modified are always zero.

PCEE_BAR2 - Base Address Register 2 (0x018)

Bit Field	Field Name	Type	Default Value	Description
0	MEMSI	RO	—	Memory Space Indicator. This bit determines if the base address register maps into memory space or I/O space. The value of this field is determined by the MEMSI field in the BARSETUP2 register. 0x0 - (memory) memory space. 0x1 - (io) I/O space.

Notes

Bit Field	Field Name	Type	Default Value	Description
2:1	TYPE	RO	—	Address Type. When the MEMSI field indicates memory space, this field specifies if a 32-bit or 64-bit address format is used. The value of this field is determined by the TYPE field in the BARSETUP2 register. When the MEMSI field indicates I/O space, this field is always zero. 0x0 - (addr32) 32-bit addressing. Located in lower 4 GB address space. 0x1 - (reserved) reserved. 0x2 - (addr64) 64-bit addressing. 0x3 - (reserved) reserved.
3	PREF	RO	—	Prefetchable. If the MEMSI field selects memory, this field indicates if the memory is prefetchable. When the MEMSI field indicates I/O space, this field is always zero. The value of this field is determined by the PREF field in the BARSETUP2 register. 0x0 - (nonprefetch) non-prefetchable. 0x1 - (prefetch) prefetchable.
31:4	BADDR	RW	0x0	Base Address. This field specifies the address bits to be used by the non-transparent bridge in decoding and accepting transactions. See the PCI and PCI Express specifications for more information. The value of the SIZE field in the BARSETUP2 register controls which bits in this field may be modified. Bits that cannot be modified are always zero. When the MEMSI indicates memory and the TYPE field indicates 64-bit addressing, the upper bits of the address of the BADDR field are contained in the next consecutive odd numbered BAR which in this case is BAR3. See the PCI and PCI Express specifications for more information.

PCEE_BAR3 - Base Address Register 3 (0x01C)

When the MEMSI field in BARSETUP2 is set to memory space (i.e., zero) and the TYPE field is set to 64-bit addressing, BAR3 takes on the function of the upper 32-bits of the BADDR field in BAR2. Otherwise, the BAR format below is used.

Bit Field	Field Name	Type	Default Value	Description
0	MEMSI	RO	—	Memory Space Indicator. This bit determines if the base address register maps into memory space or I/O space. The value of this field is determined by the MEMSI field in the BARSETUP3 register. 0x0 - (memory) memory space. 0x1 - (io) I/O space.

Notes

Bit Field	Field Name	Type	Default Value	Description
2:1	TYPE	RO	—	Address Type. When the MEMSI field indicates memory space, this field specifies if a 32-bit or 64-bit address format is used. Since this is an odd-numbered BAR, it can only be configured for a 32-bit address format. 0x0 - (addr32) 32-bit addressing. Located in lower 4 GB address space. 0x1 - (reserved) reserved. 0x1 - (reserved) reserved. 0x3 - (reserved) reserved.
3	PREF	RO	—	Prefetchable. If the MEMSI field selects memory, this field indicates if the memory is prefetchable. When the MEMSI field indicates I/O space, this field is always zero. The value of this field is determined by the MEMSI field in the BARSETUP3 register. 0x0 - (nonprefetch) non-prefetchable. 0x1 - (prefetch) prefetchable.
31:4	BADDR	RW	0x0	Base Address. This field specifies the address bits to be used by the non-transparent bridge in decoding and accepting transactions. See the PCI and PCI Express specifications for more information. The value of the SIZE field in the BARSETUP3 register controls which bits in this field may be modified. Bits that cannot be modified are always zero.

PCEE_BAR4 - Base Address Register 4 (0x020)

The entire configuration space of the non-transparent bridge may be mapped in to PCI Express memory space using this BAR. Software should ensure that there are four or less outstanding read transactions to BAR4 mapped memory. Exceeding this number of outstanding transactions may result in completions being dropped.

Bit Field	Field Name	Type	Default Value	Description
0	MEMSI	RO	0x0	Memory Space Indicator. This bit determines if the base address register maps into memory space or I/O space. Memory space is always selected. 0x0 - (memory) memory space. 0x1 - (io) I/O space.
2:1	TYPE	RO	0x0	Address Type. 32-bit address is always selected.
3	PREF	RO	0x0	Prefetchable. Configuration registers are always non-prefetchable.
6:4	Reserved	RO	0x0	Reserved field.
31:7	BADDR	RW	0x0	Base Address. This field specifies the address bits to be used by the non-transparent bridge in decoding and accepting transactions. See the PCI and PCI Express specifications for more information. This space always requests a memory size of 4KB.

Notes

PCEE_SUBVID - Subsystem Vendor ID Pointer (0x02C)

Bit Field	Field Name	Type	Default Value	Description
15:0	SUBVID	RWL	0x0	Subsystem Vendor ID. This field identifies the vendor of the subsystem.

PCEE_SUBID - Subsystem ID Pointer (0x02E)

Bit Field	Field Name	Type	Default Value	Description
15:0	SUBID	RWL	0x0	Subsystem ID. This field identifies the subsystem.

PCEE_CAPPTR - Capabilities Pointer (0x034)

Bit Field	Field Name	Type	Default Value	Description
7:0	CAPPTR	RO	0x40	Capabilities Pointer. This field specifies a pointer to the head of the capabilities structure.

PCEE_INTRLINE - Interrupt Line (0x03C)

Bit Field	Field Name	Type	Default Value	Description
7:0	INTRLINE	RW	0x0	Interrupt Line. This register communicates interrupt line routing information. Values in this register are programmed by system software and are system architecture specific. The bridge does not use the value in this register.

PCEE_INTRPIN - Interrupt PIN (0x03D)

Bit Field	Field Name	Type	Default Value	Description
7:0	INTRPIN	RWL	0x0	Interrupt Pin. Interrupt pin or legacy interrupt messages are not used by the bridge.

PCEE_MINGNT - Minimum Grant (0x03E)

Bit Field	Field Name	Type	Default Value	Description
7:0	MINGNT	RO	0x0	Minimum Grant. Not applicable.

Notes

PCEE_MAXLAT - Maximum Latency (0x03F)

Bit Field	Field Name	Type	Default Value	Description
7:0	MAXLAT	RO	0x0	Maximum Latency. Not applicable.

PCI Express Capability Structure

PCEE_PCIECAP - PCI Express Capability (0x040)

Bit Field	Field Name	Type	Default Value	Description
7:0	CAPID	RO	0x10	Capability ID. The value of 0x10 identifies this capability as a PCI Express capability structure.
15:8	NXTPTR	RO	0x64	Next Pointer. This field contains a pointer to the next capability structure.
19:16	VER	RO	0x1	PCI Express Capability Version. This field indicates the PCI-SIG defined PCI Express capability structure version number.
23:20	TYPE	RWL	0x0	Port Type. The non-transparent bridge is advertised as a PCI Express endpoint device.The value contained in Serial EEPROM may override this default value.
24	SLOT	RWL	0x0	Slot Implemented. This bit is set when the PCI Express link associated with this Port is connected to a slot.
29:25	IMN	RO	0x0	Interrupt Message Number. The function is allocated only one MSI.
31:30	Reserved	RO	0x0	Reserved field.

PCEE_PCIEDCAP - PCI Express Device Capabilities (0x044)

Bit Field	Field Name	Type	Default Value	Description
2:0	MPAYLOAD	RWL	0x4	Maximum Payload Size Supported. This field indicates the maximum payload size that the device can support for TLPs. The default value corresponds to 2048 bytes.
4:3	PFS	RO	0x0	Phantom Functions Supported. This field indicates the support for unclaimed function number to extend the number of outstanding transactions allowed by logically combining unclaimed function numbers. The value is hardwired to 0x0 to indicate that no function number bits are used for phantom functions.
5	ETAG	RO	0x1	Extended Tag Field Support. This field indicates the maximum supported size of the Tag field as a requester. The value is hardwired to 0x1 to indicate that an 8-bit tag field is supported.

Notes

Bit Field	Field Name	Type	Default Value	Description
8:6	E0AL	RO	0x7	Endpoint L0s Acceptable Latency. This field indicates the acceptable total latency that an endpoint can withstand due to transition from the L0s state to the L0 state. The value is hardwired to 0x3 to indicate more than 4 us.
11:9	E1AL	RO	0x7	Endpoint L1 Acceptable Latency. This field indicates the acceptable total latency that an endpoint can withstand due to transition from the L1 state to the L0 state. The value is hardwired to 0x3 to indicate more than 64 us.
12	ABP	RO	0x0	Attention Button Present. When set, this bit indicates that an Attention Button is implemented on the card/module. The value contained in Serial EEPROM may override this default value.
13	AIP	RO	0x0	Attention Indicator Present. When set, this bit indicates that an Attention Indicator is implemented on the card/module. The value contained in Serial EEPROM may override this default value.
14	PIP	RO	0x0	Power Indicator Present. When set, this bit indicates that a Power Indicator is implemented on the card/module. The value contained in Serial EEPROM may override this default value.
31:15	Reserved	RO	0x0	Reserved field.

PCEE_PCIEDCTL - PCI Express Device Control (0x048)

Bit Field	Field Name	Type	Default Value	Description
0	CEREN	RW	0x0	Correctable Error Reporting Enable. This bit controls reporting of correctable errors.
1	NFEREN	RW	0x0	Non-Fatal Error Reporting Enable. This bit controls reporting of non-fatal errors.
2	FEREN	RW	0x0	Fatal Error Reporting Enable. This bit controls reporting of fatal errors.
3	URREN	RW	0x0	Unsupported Request Reporting Enable. This bit controls reporting of unsupported requests.
4	ERO	RW	0x1	Enable Relaxed Ordering. When set, this bit enables relaxed ordering. When this bit is cleared, the relaxed ordering attributed is set to strongly ordered for all transactions flowing from the opposite side of the non-transparent bridge to the current side. When this bit is set, transactions flow from the opposite side to the current side of the non-transparent bridge without modification to the relaxed ordering attribute.

Notes

Bit Field	Field Name	Type	Default Value	Description
7:5	MPS	RW	0x0	Max Payload Size. This field sets maximum TLP payload size for the device. 0x0 - (s128) 128 bytes max payload size 0x1 - (s256) 256 bytes max payload size 0x2 - (s512) 512 bytes max payload size 0x3 - (s1024) 1024 bytes max payload size 0x4 - (s2048) 2048 bytes max payload size 0x5 - reserved (treated as 128 bytes) 0x6 - reserved (treated as 128 bytes) 0x7 - reserved (treated as 128 bytes)
8	ETFEN	RW	0x0	Extended Tag Field Enable. The tag field is not modified in transactions that pass through the non-transparent bridge. In addition, the tag field is always zero for all transactions generated by the internal or external endpoints of the non-transparent bridge. Therefore, this field has no functional effect on the behavior of the non-transparent bridge.
9	PFEN	RO	0x0	Phantom Function Enable. The bridge does not support phantom function numbers. Therefore, this field is hard-wired to zero.
10	AUXPMEN	RO	0x0	Auxiliary Power PM Enable.The device does not implement this capability.
11	ENS	RW	0x0	Enable No Snoop. The non-transparent bridge does not generate transactions with the No Snoop bit set and passes transactions through the bridge with the No Snoop bit unmodified. Therefore, this field has no functional effect on the behavior of the non-transparent bridge.
14:12	MRRS	RW	0x2	Maximum Read Request Size. The non-transparent bridge does not generate transactions larger than 128 bytes and passes transactions through the bridge with the size unmodified. Therefore, this field has no functional effect on the behavior of the non-transparent bridge.
15	Reserved	RO	0x0	Reserved field.

PCEE_PCIEDSTS PCI Express Device Status (0x04A)

Bit Field	Field Name	Type	Default Value	Description
0	CED	RW1C	0x0	Correctable Error Detected. This bit indicates the status of correctable errors. Errors are logged in this register regardless of whether error reporting is enabled or not.
1	NFED	RW1C	0x0	Non-Fatal Error Detected. This bit indicates the status of correctable errors. Errors are logged in this register regardless of whether error reporting is enabled or not.
2	FED	RW1C	0x0	Fatal Error Detected. This bit indicates the status of Fatal errors. Errors are logged in this registers regardless of whether error reporting is enabled or not.

Notes

Bit Field	Field Name	Type	Default Value	Description
3	URD	RW1C	0x0	Unsupported Request Detected. This bit indicates the device received an Unsupported Request. Errors are logged in this register regardless of whether error reporting is enabled or not.
4	AUXPD	RO	0x0	Aux Power Detected. Devices that require AUX power, set this bit when AUX power is detected.This device does not require AUX power, hence the value is hardwired to zero.
5	TP	RO	0x0	Transactions Pending. The non-transparent bridge does not issue Non-Posted Requests on its own behalf. Therefore, this field is hardwired to zero.
15:6	Reserved	RO	0x0	Reserved field.

PCEE_PCIELCAP - PCI Express Link Capabilities (0x04C)

Bit Field	Field Name	Type	Default Value	Description
3:0	MAXLNKSPD	RO	0x1	Maximum Link Speed. This field is hardwired to 2.5 Gbps.
9:4	MAXLNKWDTH	RO	0x8	Maximum Link Width. This field is hardwired to 0x8.
11:10	ASPMS	RO	0x01	Active State Power Management. This field is hardwired to indicate L0s entry supported. However, since this is a “virtual” link, ASPM is not supported.
14:12	L0SEL	RO	0x0	L0s Exit Latency. Hardwired to indicate less than 64ns.
17:15	L1EL	RO	0x0	L1 Exit Latency.Hardwired to indicate less than 1us.
23:18	Reserved	RO	0x0	Reserved field.
31:24	PORTNUM	RO	0x0	Port Number. Hardwired to indicate port 0.

PCEE_PCIELCTL - PCI Express Link Control (0x050)

Bit Field	Field Name	Type	Default Value	Description
1:0	ASPM	RW	0x0	Active State Power Management (ASPM) Control. This field controls the level of ASPM supported by the link. This field is zero to indicate that ASPM is disabled on the “virtual” link.
2	Reserved	RO	0x0	Reserved field.
3	RCB	RO	0x0	Read Completion Boundary. This field is not applicable to the non-transparent bridge and is hardwired to zero.
4	LDIS	RO	0x0	Link Disable. Not applicable for endpoints.
5	LRET	RO	0x0	Link Retrain. Not applicable for endpoints.

Notes

Bit Field	Field Name	Type	Default Value	Description
6	CCLK	RW	0x0	**Common Clock Configuration**. Not applicable for "virtual" links.
7	ESYNC	RW	0x0	**Extended Sync**. Not applicable for "virtual" links.
15:8	Reserved	RO	0x0	Reserved field.

PCEE_PCIELSTS - PCI Express Link Status (0x052)

Bit Field	Field Name	Type	Default Value	Description
3:0	LS	RO	0x1	**Link Speed**. This field is hardwired to 2.5 Gbps.
9:4	LW	RO	0x8	**Link Width**. This field is hardwired to indicate a x8 link.
10	TERR	RO	0x0	**Training Error**. Not applicable for endpoints.
11	LTRAIN	RO	0x0	**Link Training**. Not applicable for endpoints.
12	SCLK	RO	0x0	**Slot Clock Configuration**. Not applicable for "virtual" links.
15:13	Reserved	RO	0x0	Reserved field.

Message Signaled Interrupt Capability Structure

PCEE_MSICAP - Message Signaled Interrupt Capability and Control (0x064)

Bit Field	Field Name	Type	Default Value	Description
7:0	CAPID	RO	0x5	**Capability ID**. The value of 0x5 identifies this capability as a MSI capability structure.
15:8	NXTPTR	RO	0x74	**Next Pointer**. This field contains a pointer to the next capability structure.
16	EN	RW	0x0	**Enable**. This bit enables MSI. 0x0 - (disable) disabled 0x1 - (enable) enabled
19:17	MMC	RO	0x0	**Multiple Message Capable**. This field contains the number of requested messages. The non-transparent bridge requests one message.
22:20	MME	RO	0x0	**Multiple Message Enable**. Hardwired to one message.
23	A64	RO	0x1	**64-bit Address Capable**. The non-transparent bridge is capable of generating messages using a 64-bit address.
31:24	Reserved	RO	0x0	Reserved field.

Notes

PCEE_MSIADDR - Message Signaled Interrupt Address (0x068)

Bit Field	Field Name	Type	Default Value	Description
1:0	Reserved	RO	0x0	Reserved field.
31:2	ADDR	RW	0x0	Message Address. This field specifies the lower portion of the DWORD address of the MSI memory write transaction.

PCEE_MSIUADDR - Message Signaled Interrupt Upper Address (0x06C)

Bit Field	Field Name	Type	Default Value	Description
31:0	UADDR	RW	0x0	Upper Message Address. This field specifies the upper portion of the DWORD address of the MSI memory write transaction. If the contents of this field are non-zero, then 64-bit address is used in the MSI memory write transaction. If the contents of this field are zero, then the 32-bit address specified in the MSIADDR field is used.

PCEE_MSIMDATA - Message Signaled Interrupt Message Data (0x070)

Bit Field	Field Name	Type	Default Value	Description
15:0	MDATA	RW	0x0	Message Data. This field contains the lower 16-bits of data that are written when a MSI is signalled.
31:16	Reserved	RO	0x0	Reserved field.

Non-Transparent Bridge Configuration Capability Structure

PCEE_NTBCFGC - Non-Transparent Bridge Configuration Capability (0x074)

Bit Field	Field Name	Type	Default Value	Description
7:0	VSID	RW	0x9	Vendor Specific Capability ID. The value of 0x9 identifies this capability as a vendor specific ID. Writes are allowed to this field for testing purposes only. Writes should never be performed to this field during normal operation.
15:8	NXTPTR	RW	0xB4	Next Pointer. This field contains a pointer to the next capability structure. Writes are allowed to this field for testing purposes only. Writes should never be performed to this field during normal operation.

Notes

Bit Field	Field Name	Type	Default Value	Description
23:16	CLENGTH	RW	0x40	Capability Length. This field defines the length in bytes of the capability. It includes the VSID and NXTPTR fields. Writes are allowed to this field for testing purposes only. Writes should never be performed to this field during normal operation.
31:24	IDTCAP	RW	0x1	IDT Capability. This field defines an IDT proprietary PCI, PCI-X or PCI Express capability. The value of 0x1 identifies this as a non-transparent bridge configuration capability structure. Writes are allowed to this field for testing purposes only. Writes should never be performed to this field during normal operation.

PCEE_NTBCTL - Non-Transparent Bridge Control (0x078)

Bit Field	Field Name	Type	Default Value	Description
1:0	OSMODE	RW	0x0 (external) 0x1 (internal) Not reset by external fundamental reset or external hot reset Reset by internal fundamental or hot reset	Opposite Side Mode. This field controls the operating mode of the opposite side of the non-transparent bridge. When the opposite side is set to not ready, all configuration transactions received on the opposite side of the non-transparent bridge are responded to with a configuration request retry status completion and all other transactions are ignored. When the opposite side is set to disabled, transactions received on the opposite side of the non-transparent bridge are discarded. Transactions still flow in the opposite direction (i.e., from the current side to opposite side). Note that phy and data link layer operations still continue. Whenever received transactions are discarded, they are accounted for by the flow control protocol at the data link layer. This means that flow control credits are returned even for discarded transactions. If the OSMODE field for one side, side A, is not ready or disabled and the OSMODE field for the other side, side B, becomes not ready or disabled, then this is a configuration/programming error. To prevent deadlock, when this occurs the side that was not ready or disabled first (i.e, in this example side A) automatically transitions to enabled. 0x0 - (enabled) opposite side enabled 0x1 - (notready) opposite side not ready 0x2 - (disabled) opposite side disabled 0x3 - (reserved) reserved

Notes

Bit Field	Field Name	Type	Default Value	Description
2	OSCFGPROT	RW	0x0[1]	Opposite Side Configuration Protection.When this bit is set, all configuration and BAR4 writes from the opposite side of the non-transparent bridge to the internal or external non-transparent bridge configuration capability structure are ignored (i.e., they are completed normally but do not modify any values). Reads to this space via configuration or BAR4 accesses when this bit is set return a value of zero for all registers in the non-transparent bridge configuration capability structure except for the NTBCFGC register, which returns its actual value.
3	RAEN	RW	0x0[1]	Reset Action Enable. When set, this bit enables the side effect specified by the Reset Action (RA) field in this register when a fundamental or hot reset is detected on the opposite side of the non-transparent bridge. This field is only relevant for the internal side of the non-transparent bridge and is read-only 0x0 in the external side of the non-transparent bridge.
4	RA	RW	0x0[1]	Reset Action. This field specifies the action to be taken when the RAEN bit is set in this register and a fundament or hot reset is detected on the opposite side of the non-transparent bridge. This field is only relevant for the internal side of the non-transparent bridge and is read-only 0x0 in the external side of the non-transparent bridge. 0x0 -(thissidenotready) this side not ready. This causes the OSMODE field in the NTBCTL register on the opposite side of the non-transparent bridge to be set to not ready. 0x1 -(oppositesidenotready) opposite side not ready. This causes the OSMODE field in this register to be set to not ready.
5	PEFR	RW	0x0[1]	Propagate External Fundamental Reset. When this bit is set and the device is configured to operate in non-transparent mode, then assertion of the PENTBRSTN signal results in a fundamental reset of the entire device.
6	Reserved	RO	0x0	Reserved field.
7	RST	RW	0x0	Fundamental Reset. Writing a one to this bit initiates a fundamental reset to the entire device. Writing a zero has no effect. This field always returns a value of zero when read.

1. Not reset by external fundamental reset or internal/external hot reset

PCEE_NTBSTS - Non-Transparent Bridge Status (0x079)

Bit Field	Field Name	Type	Default Value	Description
0	OSFRD	RW1C	depends on reset condition[1]	Opposite Side Fundamental Reset Detected. This bit is set when a fundamental reset is detected on the opposite side of the non-transparent bridge.

Notes

Bit Field	Field Name	Type	Default Value	Description
1	OSHRD	RW1C	0x0[1]	Opposite Side Hot Reset Detected. This bit is set when a hot reset is detected on the opposite side of the non-transparent bridge.
2	OSRIP	RO	0x0[1]	Opposite Side Reset in Progress. This bit is set when a hot or fundamental reset is in progress on the opposite side of the non-transparent bridge. When this bit is set, configuration registers associated with the opposite side of the non-transparent bridge should not be accessed and transactions should not be forwarded through the bridge. The behavior of these operations during an opposite side reset is undefined.
3	FMTMISS	RW1C	0x0[1]	Forward Mapping Table Miss. This bit is set when an address routed transaction (e.g., a read request) is received by the this side of the non-transparent bridge, maps through the bridge, but whose requester does match the bus/device/function of an entry in the mapping table.
4	RMTMISS	RW1C	0x0[1]	Reverse Mapping Table Miss. This bit is set when a route by ID transaction (e.g., a completion) is received by the opposite side of the non-transparent bridge that does match the bus/device/function of an entry in the mapping table.
5	MTAERR	RW1C	0x0[1]	Mapping Table Access Error. This bit is set when the MDATA register is read or written and the ADDR field in the MTADDR register points to an invalid address.
6	ECRCERR	RW1C	0x0[1]	ECRC Error. This bit is set when a TLP with ECRC enabled is received by the non-transparent bridge and an ECRC error is detected in the TLP. Since ECRC is not checked for TLPs consumed by the NTB (e.g., configuration requests), this bit is never set due to ECRC errors in TLPs consumed by the NTB.
7	BARMISS	RW1C	0x0[1]	BARMISS. This bit is set when a TLP received by this side of the non-transparent bridge does not map to any of the BAR regions and is discarded.

1. Not reset by external fundamental reset or internal/external hot reset

PCEE_NTBEPID - Non-Transparent Bridge Endpoint Identification (0x07A)

Bit Field	Field Name	Type	Default Value	Description
2:0	FUNC	RO	0x0	Function Number. This field contains the function number value of the last configuration write transaction to this configuration space of the non-transparent bridge.
7:3	DEV	RO	0x0	Device Number. This field contains the device number value of the last configuration write transaction to this configuration space of the non-transparent bridge.

Notes

Bit Field	Field Name	Type	Default Value	Description
15:8	BUS	RO	0x0	Bus Number. This field contains the bus number value of the last configuration write transaction to this configuration space of the non-transparent bridge.

PCEE_BARSETUP0 - BAR 0 Setup (0x07C)

Bit Field	Field Name	Type	Default Value	Description
0	MEMSI	RW	0x0[1]	MEMSI Select. This field determines the MEMSI type returned in the MEMSI field of the corresponding BAR. 0x0 - (memory) memory space. 0x1 - (io) I/O space.
2:1	TYPE	RW	0x0[1]	Address Select. This field determines the value reported in the TYPE field of the corresponding BAR and selects the address space decoding used when memory space is selected in the MEMSI field in this register. When the MEMSI field indicates I/O space, this field is always zero. 0x0 -(addr32) 32-bit addressing. Located in lower 4 GB address space. 0x1 -(reserved) reserved. 0x2 -(addr64) 64-bit addressing. 0x3 -(reserved) reserved.
3	PREF	RW	0x0[1]	Prefetchable Select. This field determines the value reported in the PREF field of the corresponding BAR. 0x0 - (nonprefetch) non-prefetchable. 0x1 - (prefetch) prefetchable.

Notes

Bit Field	Field Name	Type	Default Value	Description
9:4	SIZE	RW	0x0[1]	Address Space Size. This field selects the size, in address bits, of the address space for the corresponding BAR or BAR pair when 64-bit addressing is selected. Assuming the size field is set to a valid value, the size of the address space requested by the BADDR field in the corresponding BAR is equal to 2^{SIZE} or 2^{64} when this field is zero. Bits in the BAR BADDR field correspond to PCI Express address bits. For example, bit 0 or the BAR BADDR field corresponds to PCI Express Address bit 4. Setting this field to zero allows all bits in the corresponding BAR BADDR field to be modified (i.e., selects entire 64-bit address space). Otherwise, setting this SIZE field to a non-zero value allows bits in the BAR BADDR field that correspond to PCI Express address bits greater than or equal to the SIZE field to be modified. Corresponding bits less than the SIZE field and greater than or equal to four always return a value of zero when read and cannot be modified. Setting the SIZE field to a value less than four results in all bits in the corresponding BAR BADDR field to take on a read-only zero value that effectively disables the BAR. The smallest memory size that may be requested by PCI Express is 128 (i.e., SIZE equal to 7) and the largest is 2^{32} bytes for 32-bit address space and 2^{64} bytes for 64-bit address space. The smallest I/O size that may be requested by the PES12NT3 is 16 bytes (i.e., SIZE equal to 4) while the largest allowed by PCI express is 256 bytes. The PES12NT3 does not enforce the minimum memory size or the maximum I/O size in hardware. Therefore, it 128 is the responsibility of the user to ensure that these requirements are met. Setting the SIZE field to a value greater than 32 when then MEMSI and TYPE fields in this register select I/O space or 32-bit memory space, results in bits greater than 32 being ignored (i.e., only the TYPE field can enable 64-bit addressing).
30:10	Reserved	RO	0x0	Reserved field.
31	EN	RW	0x0[1]	BAR Enable. When cleared, the corresponding BAR is disabled and returns a zero when read. 0x0 - (disabled) disabled. 0x1 - (enabled) enabled.

1. Not reset by external fundamental reset or internal/external hot reset

PCEE_BARTBASE0 - BAR 0 Translated Base Address (0x080)

Bit Field	Field Name	Type	Default Value	Description
3:0	Reserved	RO	0x0	Reserved field.

Notes

Bit Field	Field Name	Type	Default Value	Description
31:4	TBADDR	RW	0x0[1]	Translated Base Address. This field specifies the translated base address for transactions that map through BAR0 of the non-transparent bridge. When 64-bit addressing is selected, the translated base address consists of the value in this field together with the upper 32 bits of the address contained in the BARTBASE1 register.

1. Not reset by external fundamental reset or internal/external hot reset

PCEE_BARSETUP1 - BAR 1 Setup (0x084)

When the MEMSI field in BARSETUP0 is set to memory space (i.e., zero) and the TYPE field is set to 64-bit addressing, BAR1 takes on the function of the upper 32-bits of the BADDR field in BAR0. In this mode, the BARSETUP1 register takes on a read-only value of zero.

Bit Field	Field Name	Type	Default Value	Description
0	MEMSI	RW	0x0[1]	MEMSI Select. This field determines the MEMSI type returned in the MEMSI field of the corresponding BAR. 0x0 - (memory) memory space. 0x1 - (io) I/O space.
2:1	TYPE	RW	0x0[1]	Address Select. This field determines the value reported in the TYPE field of the corresponding BAR and selects the address space decoding used when memory space is selected in the MEMSI field in this register. When the MEMSI field indicates I/O space, this field is always zero. 0x0 -(addr32) 32-bit addressing. Located in lower 4 GB address space. 0x1 -(reserved) reserved. 0x2 -(reserved) reserved. 0x3 -(reserved) reserved.
3	PREF	RW	0x0[1]	Prefetchable Select. This field determines the value reported in the PREF field of the corresponding BAR. 0x0 - (nonprefetch) non-prefetchable. 0x1 - (prefetch) prefetchable.

Notes

Bit Field	Field Name	Type	Default Value	Description
9:4	SIZE	RW	0x0[1]	Address Space Size. This field selects the size, in address bits, of the address space for the corresponding BAR or BAR pair when 64-bit addressing is selected. Assuming the size field is set to a valid value, the size of the address space requested by the BADDR field in the corresponding BAR is equal to 2^{SIZE} or 2^{64} when this field is zero. Bits in the BAR BADDR field correspond to PCI Express address bits. For example, bit 0 or the BAR BADDR field corresponds to PCI Express Address bit 4. Setting this field to zero allows all bits in the corresponding BAR BADDR field to be modified (i.e., selects entire 64-bit address space). Otherwise, setting this SIZE field to a non-zero value allows bits in the BAR BADDR field that correspond to PCI Express address bits greater than or equal to the SIZE field to be modified. Corresponding bits less than the SIZE field and greater than or equal to four always return a value of zero when read and cannot be modified. Setting the SIZE field to a value less than four results in all bits in the corresponding BAR BADDR field to take on a read-only zero value that effectively disables the BAR. The smallest memory size that may be requested by PCI Express is 128 (i.e., SIZE equal to 7) and the largest is 2^{32} bytes for 32-bit address space. The smallest I/O size that may be requested by the PES12NT3 is 16 bytes (i.e., SIZE equal to 4) while the largest allowed by PCI express is 256 bytes. The PES12NT3 does not enforce the minimum memory size or the maximum I/O size in hardware. Therefore, it 128 is the responsibility of the user to ensure that these requirements are met. Setting the SIZE field to a value greater than 32 when then MEMSI and TYPE fields in this register select I/O space or 32-bit memory space, results in bits greater than 32 being ignored (i.e., only the TYPE field can enable 64-bit addressing).
30:10	Reserved	RO	0x0	Reserved field.
31	EN	RW	0x0[1]	BAR Enable. When cleared, the corresponding BAR is disabled and returns a zero when read. 0x0 - (disabled) disabled. 0x1 - (enabled) enabled.

1. Not reset by external fundamental reset or internal/external hot reset

PCEE_BARTBASE1 - BAR 1 Translated Base Address (0x088)

When the MEMSI field in BARSETUP0 is set to memory space (i.e., zero) and the TYPE field is set to 64-bit addressing, BARTBASE1 takes on the function of the upper 32-bits of the TBADDR field in BARTBASE0. In this mode, all 32-bits of BARTBASE1 may be read and written.

Bit Field	Field Name	Type	Default Value	Description
3:0	Reserved	RO	0x0	Reserved field.

Notes

Bit Field	Field Name	Type	Default Value	Description
31:4	TBADDR	RW	0x0[1]	Translated Base Address. This field specifies the translated base address for transactions that map through BAR1 of the non-transparent bridge.

1. Not reset by external fundamental reset or internal/external hot reset

PCEE_BARSETUP2 - BAR 2 Setup (0x08C)

Bit Field	Field Name	Type	Default Value	Description
0	MEMSI	RW	0x0[1]	MEMSI Select. This field determines the MEMSI type returned in the MEMSI field of the corresponding BAR. 0x0 - (memory) memory space. 0x1 - (io) I/O space.
2:1	TYPE	RW	0x0[1]	Address Select. This field determines the value reported in the TYPE field of the corresponding BAR and selects the address space decoding used when memory space is selected in the MEMSI field in this register. When the MEMSI field indicates I/O space, this field is always zero. 0x0 -(addr32) 32-bit addressing. Located in lower 4 GB address space. 0x1 -(reserved) reserved. 0x2 -(addr64) 64-bit addressing. 0x3 -(reserved) reserved.
3	PREF	RW	0x0[1]	Prefetchable Select. This field determines the value reported in the PREF field of the corresponding BAR. 0x0 - (nonprefetch) non-prefetchable. 0x1 - (prefetch) prefetchable.

Notes

Bit Field	Field Name	Type	Default Value	Description
9:4	SIZE	RW	0x0[1]	Address Space Size. This field selects the size, in address bits, of the address space for the corresponding BAR or BAR pair when 64-bit addressing is selected. Assuming the size field is set to a valid value, the size of the address space requested by the BADDR field in the corresponding BAR is equal to 2^{SIZE} or 2^{64} when this field is zero. Bits in the BAR BADDR field correspond to PCI Express address bits. For example, bit 0 or the BAR BADDR field corresponds to PCI Express Address bit 4. Setting this field to zero allows all bits in the corresponding BAR BADDR field to be modified (i.e., selects entire 64-bit address space). Otherwise, setting this SIZE field to a non-zero value allows bits in the BAR BADDR field that correspond to PCI Express address bits greater than or equal to the SIZE field to be modified. Corresponding bits less than the SIZE field and greater than or equal to four always return a value of zero when read and cannot be modified. Setting the SIZE field to a value less than four results in all bits in the corresponding BAR BADDR field to take on a read-only zero value that effectively disables the BAR. The smallest memory size that may be requested by PCI Express is 128 (i.e., SIZE equal to 7) and the largest is 2^{32} bytes for 32-bit address space and 2^{64} bytes for 64-bit address space. The smallest I/O size that may be requested by the PES12NT3 is 16 bytes (i.e., SIZE equal to 4) while the largest allowed by PCI express is 256 bytes. The PES12NT3 does not enforce the minimum memory size or the maximum I/O size in hardware. Therefore, it 128 is the responsibility of the user to ensure that these requirements are met. Setting the SIZE field to a value greater than 32 when then MEMSI and TYPE fields in this register select I/O space or 32-bit memory space, results in bits greater than 32 being ignored (i.e., only the TYPE field can enable 64-bit addressing).
30:10	Reserved	RO	0x0	Reserved field.
31	EN	RW	0x0[1]	BAR Enable. When cleared, the corresponding BAR is disabled and returns a zero when read. 0x0 - (disabled) disabled. 0x1 - (enabled) enabled.

1. Not reset by external fundamental reset or internal/external hot reset

PCEE_BARTBASE2 - BAR 2 Translated Base Address (0x090)

Bit Field	Field Name	Type	Default Value	Description
3:0	Reserved	RO	0x0	Reserved field.

Notes

Bit Field	Field Name	Type	Default Value	Description
31:4	TBADDR	RW	0x0[1]	Translated Base Address. This field specifies the translated base address for transactions that map through BAR2 of the non-transparent bridge. When 64-bit addressing is selected, the translated base address consists of the value in this field together with the upper 32 bits of the address contained in the BARTBASE1 register.

1. Not reset by external fundamental reset or internal/external hot reset

PCEE_BARSETUP3 - BAR 3 Setup (0x094)

When the MEMSI field in BARSETUP2 is set to memory space (i.e., zero) and the TYPE field is set to 64-bit addressing, BAR3 takes on the function of the upper 32-bits of the BADDR field in BAR2. In this mode, the BARSETUP3 register takes on a read-only value of zero.

Bit Field	Field Name	Type	Default Value	Description
0	MEMSI	RW	0x0[1]	MEMSI Select. This field determines the MEMSI type returned in the MEMSI field of the corresponding BAR. 0x0 - (memory) memory space. 0x1 - (io) I/O space.
2:1	TYPE	RW	0x0[1]	Address Select. This field determines the value reported in the TYPE field of the corresponding BAR and selects the address space decoding used when memory space is selected in the MEMSI field in this register. When the MEMSI field indicates I/O space, this field is always zero. 0x0 -(addr32) 32-bit addressing. Located in lower 4 GB address space. 0x1 - (reserved) reserved. 0x2 - (reserved) reserved. 0x3 - (reserved) reserved.
3	PREF	RW	0x0[1]	Prefetchable Select. This field determines the value reported in the PREF field of the corresponding BAR. 0x0 - (nonprefetch) non-prefetchable. 0x1 - (prefetch) prefetchable.

Notes

Bit Field	Field Name	Type	Default Value	Description
9:4	SIZE	RW	0x0[1]	Address Space Size. This field selects the size, in address bits, of the address space for the corresponding BAR or BAR pair when 64-bit addressing is selected. Assuming the size field is set to a valid value, the size of the address space requested by the BADDR field in the corresponding BAR is equal to 2^{SIZE} or 2^{64} when this field is zero. Bits in the BAR BADDR field correspond to PCI Express address bits. For example, bit 0 or the BAR BADDR field corresponds to PCI Express Address bit 4. Setting this field to zero allows all bits in the corresponding BAR BADDR field to be modified (i.e., selects entire 64-bit address space). Otherwise, setting this SIZE field to a non-zero value allows bits in the BAR BADDR field that correspond to PCI Express address bits greater than or equal to the SIZE field to be modified. Corresponding bits less than the SIZE field and greater than or equal to four always return a value of zero when read and cannot be modified. Setting the SIZE field to a value less than four results in all bits in the corresponding BAR BADDR field to take on a read-only zero value that effectively disables the BAR. The smallest memory size that may be requested by PCI Express is 128 (i.e., SIZE equal to 7) and the largest is 2^{32} bytes for 32-bit address space. The smallest I/O size that may be requested by the PES12NT3 is 16 bytes (i.e., SIZE equal to 4) while the largest allowed by PCI express is 256 bytes. The PES12NT3 does not enforce the minimum memory size or the maximum I/O size in hardware. Therefore, it 128 is the responsibility of the user to ensure that these requirements are met.
30:10	Reserved	RO	0x0	Reserved field.
31	EN	RW	0x0[1]	BAR Enable. When cleared, the corresponding BAR is disabled and returns a zero when read. 0x0 - (disabled) disabled. 0x1 - (enabled) enabled.

1. Not reset by external fundamental reset or internal/external hot reset

PCEE_BARTBASE3 - BAR 3 Translated Base Address (0x098)

When the MEMSI field in BARSETUP2 is set to memory space (i.e., zero) and the TYPE field is set to 64-bit addressing, BARTBASE3 takes on the function of the upper 32-bits of the TBADDR field in BARTBASE2. In this mode, all 32-bits of BARTBASE3 may be read and written.

Bit Field	Field Name	Type	Default Value	Description
3:0	Reserved	RO	0x0	Reserved field.

Notes

Bit Field	Field Name	Type	Default Value	Description
31:4	TBADDR	RW	0x0[1]	Translated Base Address. This field specifies the translated base address for transactions that map through BAR3 of the non-transparent bridge. When a transaction address is translated, the PCI address bits from bit 31 through the bit specified by the SIZE field are replaced by the corresponding bits in this field.

1. Not reset by external fundamental reset or internal/external hot reset

PCEE_BARSETUP4 - BAR 4 Setup (0x09C)

Bit Field	Field Name	Type	Default Value	Description
0	MEMSI	RO	0x0	MEMSI Select. This field determines the MEMSI type returned in the MEMSI field of the corresponding BAR. Memory space is always selected. 0x0 - (memory) memory space. 0x1 - (io) I/O space.
2:1	TYPE	RO	0x0	Address Select. This field determines the value reported in the TYPE field of the corresponding BAR. 32-bit addressing is always selected.
3	PREF	RO	0x0	Prefetchable Select. This field determines the value reported in the PREF field of the corresponding BAR. Non-prefetchable space is always selected.
9:4	SIZE	RO	0xC	Address Space Size. This field selects the size, in address bits, of the address space for the corresponding BAR. A 4KB address space is always requested.
30:10	Reserved	RO	0x0	Reserved field.
31	EN	RW	0x0[1]	BAR Enable. When cleared, the corresponding BAR is disabled and returns a zero when read. 0x0 - (disabled) disabled. 0x1 - (enabled) enabled.

1. Not reset by external fundamental reset or internal/external hot reset

PCEE_PTCCFG - Punch Through Configuration Control (0x0A0)

Bit Field	Field Name	Type	Default Value	Description
1:0	Reserved	RO	0x0	Reserved field.
7:2	REG	RW	0x0[1]	Register Number. This field selects the configuration register number as defined by Section 7.2.2 of the PCI Express Base Specification, Rev. 1.0a
11:8	EREG	RW	0x0[1]	Extended Register Number. This field selects the extended configuration register number as defined by Section 7.2.2 of the PCI Express Base Specification, Rev. 1.0a

Notes

Bit Field	Field Name	Type	Default Value	Description
14:12	FUNC	RW	0x0[1]	Function Number. This field selects the function number as defined by Section 7.2.2 of the PCI Express Base Specification, Rev. 1.0a
19:15	DEV	RW	0x0[1]	Device Number. This field selects the device number as defined by Section 7.2.2 of the PCI Express Base Specification, Rev. 1.0a
27:20	BUS	RW	0x0[1]	Bus Number. This field selects the bus number as defined by Section 7.2.2 of the PCI Express Base Specification, Rev. 1.0a
29:28	Reserved	RO	0x0	Reserved field.
30	CFGTYPE	RW	0x0	Configuration Access Type. This field selects the type of configuration access generated using the punch through mechanism. 0x0 - (type0) type 0 configuration access 0x1 - (type1) type 1 configuration access
31	OP	RW	0x0[1]	Operation Select. This field selects the type of configuration operation to be performed when the PTCDATA register is written 0x0 - (read) configuration read 0x1 - (write) configuration write

1. Not reset by external fundamental reset or internal/external hot reset

PCEE_PTCDATA - Punch Through Configuration Data (0x0A4)

Bit Field	Field Name	Type	Default Value	Description
31:0	DATA	RW	0x0[1]	Configuration Data. A write to this field will generate a configuration read or write transaction, as selected by the OP field in the PTCCFG register, on the opposite side of the non-transparent bridge. The byte enables in the generated transaction on the opposite side of the non-transparent bridge match those of the write to this register. When a configuration write operation is selected, the value written to this field is the value used in the configuration write transaction. When a configuration read operation is selected, the value written to this field is ignored and the value returned by the read may be read from this field when the DONE bit is set in the PTCSTS register. Status for the generated transaction is reported in the PTCSTS register.

1. Not reset by external fundamental reset or internal/external hot reset

Notes

PCEE_PTCSTS - Punch Through Configuration Status (0x0A8)

Bit Field	Field Name	Type	Default Value	Description
0	BUSY	ROS	0x0	Punch Through Configuration Interface Busy. This bit is set when a punch through configuration transaction is in progress. 0x0 - (idle) configuration transaction interface is idle 0x1 - (busy) configuration transaction in progress
1	DONE	RW1C	0x0[1]	Punch Through Configuration Transaction Completed. This bit is set when a punch through configuration transaction has completed and the STATUS field is valid. Writing a one to this bit clears the status bit or aborts a punch through operation in progress. 0x0 -(notdone) configuration transaction interface is idle or transaction in flight. 0x1 -(done) configuration transaction completed
4:2	STATUS	RO	0x0	Punch Through Configuration Transaction Status. This field contains the completion status of the last punch through configuration transaction and is valid only when the DONE bit in this register is set. 0x0 - sc) successful completion 0x1 - (ur) unsupported request 0x2 - (crs) configuration request retry 0x3 - (ca) completer abort 0x4 - (ra) requester abort 0x5 through 0x7 - reserved
5	PTABORT	RO	0x0	Punch Through Abort Status. This bit is set if the last punch through configuration transaction was aborted (i.e., the STATUS field in this register is set to requester abort). This bit will remain set until the next punch through configuration transaction is initiated.
6:30	Reserved	RO	0x0	Reserved field.
31	PTC	RO	0x1	Punch Through Capable. This field indicates whether or not punch through transactions are supported by the non-transparent bridge endpoint. 0x0 -(unsupported) punch through configuration transactions are not supported. In this configuration all other fields in the PTCCFG, PTCDATA and PTCSTS register are hardwired to zero. 0x1 -(supported) punch through configuration transactions are supported as defined in the PTCCFG, PTCDATA, and PTCSTS registers.

1. Not reset by external fundamental reset or internal/external hot reset

PCEE_MTADDR - Mapping Table Address (0x0AC)

Bit Field	Field Name	Type	Default Value	Description
1:0	Reserved	RO	0x0	Reserved field.

Notes

Bit Field	Field Name	Type	Default Value	Description
5:2	ADDR	RW	0x0[1]	Mapping Table Address. This field contains the DWord address of a mapping table entry.
31:6	Reserved	RO	0x0	Reserved field.

1. Not reset by external fundamental reset or internal/external hot reset

PCEE_MTDATA - Mapping Table DATA (0x0B0)

Bit Field	Field Name	Type	Default Value	Description
0	V	RW	0x0[1]	Mapping Table Entry Valid. Reading this field returns the mapping table entry pointed to by the ADDR field in the MTADDR register. Writing this field updates the mapping table entry pointed to by the ADDR field. Only DWord accesses are supported to this register. Non DWord accesses result in an unsupported request completion. When set, this field indicates if the table entry is valid.
15:1	Reserved	RO	0x0	Reserved field.
18:16	FUNC	RW	0x0[1]	Mapping Table Function Number. Reading this field returns the mapping table entry pointed to by the ADDR field in the MTADDR register. Writing this field updates the mapping table entry pointed to by the ADDR field. Only DWord accesses are supported to this register. Non DWord accesses result in an unsupported request completion. This field contains the mapping table entry function number.
23:19	DEV	RW	0x0[1]	Mapping Table Device Number. Reading this field returns the mapping table entry pointed to by the ADDR field in the MTADDR register. Writing this field updates the mapping table entry pointed to by the ADDR field. Only DWord accesses are supported to this register. Non DWord accesses result in an unsupported request completion. This field contains the mapping table entry device number.
31:24	BUS	RW	0x0[1]	Mapping Table Bus Number. Reading this field returns the mapping table entry pointed to by the ADDR field in the MTADDR register. Writing this field updates the mapping table entry pointed to by the ADDR field. Only DWord accesses are supported to this register. Non DWord accesses result in an unsupported request completion. This field contains the mapping table entry bus number.

1. Not reset by external fundamental reset or internal/external hot reset

Notes

Non-Transparent Bridge Communications Capability Structure

PCEE_NTBCOMC - Non-Transparent Bridge Communications Capability (0x0B4)

Bit Field	Field Name	Type	Default Value	Description
7:0	VSID	RO	0x9	Vendor Specific Capability ID. The value of 0x9 identifies this capability as a vendor specific ID.
15:8	NXTPTR	RO	0xF0	Next Pointer. This field contains a pointer to the next capability structure.
23:16	CLENGTH	RO	0x3C	Capability Length. This field defines the length in bytes of the capability. It includes the VSID and NXTPTR fields.
31:24	IDTCAP	RO	0x2	IDT Capability. This field defines an IDT proprietary PCI, PCI-X or PCI Express capability. The value of 0x2 identifies this as a non-transparent bridge communications capability structure

PCEE_INMSG[0\|1\|2\|3] - Inbound Message [0\|1\|2\|3] (0x0B8-0C4)

Bit Field	Field Name	Type	Default Value	Description
31:0	INMSG	RO	0x0	Inbound Message. This read only field contains the value written by an agent to the corresponding Outbound Message [0|1|2|3] (OUTMSG[0|1|2|3]) register located in PCI configuration space on the opposite side of the non-transparent bridge.

PCEE_OUTMSG[0\|1\|2\|3] - Outbound Message [0\|1\|2\|3] (0x0C8-0D4)

Bit Field	Field Name	Type	Default Value	Description
31:0	OUTMSG	RW	0x0	Outbound Message. When written, the value in this field and that of the corresponding Inbound Message [0|1|2|3] (INMSG[0|1|2|3]) register located in PCI configuration space on the opposite side of the non-transparent bridge are modified with the value written. In addition, the corresponding Inbound Message (INMSG[0|1|2|3]) bit is set in the Interrupt Status (INTSTS) register located in PCI configuration space on the opposite side of the non-transparent bridge.

Notes

PCEE_SCRATCHPAD[0..1] - Scratchpad [0..1] (0x0D8-ODC)

Bit Field	Field Name	Type	Default Value	Description
31:0	SCRATCHPAD	RW	0x0	Scratchpad Value. This scratchpad register may be read and written from both sides of the non-transparent bridge. Scratchpad registers may not be accessed using the Extended Configuration Space Data (ECFGDATA) register. The behavior of scratchpad register accesses using this mechanism is undefined.

PCEE_INDBELL - Inbound Doorbell (0x0E0)

Bit Field	Field Name	Type	Default Value	Description
31:0	INDBELL	RW1C	0x0	Inbound Doorbell. Each bit in this field corresponds to status of one of the 32 inbound doorbells.The state of these bits is determined by the value written by an agent to the Outbound Doorbell (OUTDBELL) register located in PCI configuration space on the opposite side of the of the non-transparent bridge.

PCEE_OUTDBELL - Outbound Doorbell (0x0E4)

Bit Field	Field Name	Type	Default Value	Description
31:0	OUTDBELL	RW	0x0	Outbound Doorbell. Each bit in this field corresponds to status of one of the 32 outbound doorbells. Setting a bid in this register results in the corresponding bit being set in the Inbound Doorbell (INDBELL) register located in PCI configuration space on the opposite side of the non-transparent bridge.

PCEE_INTSTS - Interrupt Status (0x0E8)

Bit Field	Field Name	Type	Default Value	Description
0	INMSG0	RW1C	0x0	Inbound Message 0. This bit is set whenever a value is written to the OUTMSG0 register located in PCI configuration space on the opposite side of the non-transparent bridge. The action taken when this bit is set is determined by the Interrupt Control 0 (INTCTL0) register.
1	INMSG1	RW1C	0x0	Inbound Message 1. This bit is set whenever a value is written to the OUTMSG1 register located in PCI configuration space on the opposite side of the non-transparent bridge. The action taken when this bit is set is determined by the Interrupt Control 0 (INTCTL0) register.

Notes

Bit Field	Field Name	Type	Default Value	Description
2	INMSG2	RW1C	0x0	Inbound Message 2. This bit is set whenever a value is written to the OUTMSG2 register located in PCI configuration space on the opposite side of the non-transparent bridge. The action taken when this bit is set is determined by the Interrupt Control 0 (INTCTL0) register.
3	INMSG3	RW1C	0x0	Inbound Message 3. This bit is set whenever a value is written to the OUTMSG3 register located in PCI configuration space on the opposite side of the non-transparent bridge. The action taken when this bit is set is determined by the Interrupt Control 0 (INTCTL0) register.
4	INDBELL	RO	0x0	Inbound Doorbell. This bit is set whenever a bit is set in the Inbound Doorbell (INDBELL) register. The action taken when this bit is set is determined by the Interrupt Control 0 (INTCTL0) register.
5	OSRD	RW1C	depends on reset condition Sticky	Opposite Side Reset Detected. This bit is set whenever a fundamental or hot reset is detected on the opposite side of the non-transparent bridge. The action taken when this bit is set is determined by the Interrupt Control 0 (INTCTL0) register.
6	OSPSTATEM	RW1C	0x0	Opposite Side Power State Modification. This bit is set whenever a modification is made to the PSTATE field in the PMCSR register on the opposite side of the non-transparent bridge.
7	PALINKUP	RW1C	Undefined Sticky	Port A Link Up. This bit is set whenever the port A data link layer transitions from a DL_Down to a DL_Up state. The action taken when this bit is set is determined by the Interrupt Control 1 (INTCTL1) register.
8	PALINKDN	RW1C	Undefined Sticky	Port A Link Down. This bit is set whenever the port A data link layer transitions from a DL_up to a DL_Down state. The action taken when this bit is set is determined by the Interrupt Control 1 (INTCTL1) register.
9	PBLINKUP	RW1C	Undefined Sticky	Port B Link Up. This bit is set whenever the port B data link layer transitions from a DL_Down to a DL_Up state. The action taken when this bit is set is determined by the Interrupt Control 1 (INTCTL1) register.
10	PBLINKDN	RW1C	Undefined Sticky	Port B Link Down. This bit is set whenever the port B data link layer transitions from a DL_up to a DL_Down state. The action taken when this bit is set is determined by the Interrupt Control 1 (INTCTL1) register.
11	PCLINKUP	RW1C	Undefined Sticky	Port C Link Up. This bit is set whenever the port C data link layer transitions from a DL_Down to a DL_Up state. The action taken when this bit is set is determined by the Interrupt Control 1 (INTCTL1) register.
12	PCLINKDN	RW1C	Undefined Sticky	Port C Link Down. This bit is set whenever the port C data link layer transitions from a DL_up to a DL_Down state. The action taken when this bit is set is determined by the Interrupt Control 1 (INTCTL1) register.
31:13	Reserved	RO	0x0	Reserved field.

Notes

PCEE_INTCTL0 - Interrupt Control 0 (0x0EC)

Bit Field	Field Name	Type	Default Value	Description
2:0	INMSG0	RW	0x0	Inbound Message 0 Configuration. This field encodes the action taken when the INMSG0 bit in the INTSTS register is set, or cleared when INTx interrupt signalling is enabled. Regardless of the value of this field, an MSI is only sent when Enable (EN) bit is set in the MSICAP register. Similarly, and INTx message is only sent if not disabled by the INTXD bit in the PCICMD register. The action (i.e., this field) should not be modified while the corresponding bit is set. Modifying the action when the corresponding bit is set produces undefined results. 0x0 -(disabled) interrupt is masked/disabled. 0x1 -(msi) send a Message Signalled Interrupt (MSI) as specified by the MSI capability structure. 0x2 -(int_a) generate INTA assertion and negation messages. 0x3 -(int_b) generate INTB assertion and negation messages. 0x4 -(int_c) generate INTC assertion and negation messages. 0x5 -(int_d) generate INTD assertion and negation messages. 0x6 though 0x8 -(reserved) reserved.
5:3	INMSG1	RW	0x0	Inbound Message 1 Configuration. This field encodes the action taken when the INMSG1 bit in the INTSTS register is set, or cleared when INTx interrupt signalling is enabled. Regardless of the value of this field, an MSI is only sent when Enable (EN) bit is set in the MSICAP register. Similarly, and INTx message is only sent if not disabled by the INTXD bit in the PCICMD register. The action (i.e., this field) should not be modified while the corresponding bit is set. Modifying the action when the corresponding bit is set produces undefined results. 0x0 -(disabled) interrupt is masked/disabled. 0x1 -(msi) send a Message Signalled Interrupt (MSI) as specified by the MSI capability structure. 0x2 -(int_a) generate INTA assertion and negation messages. 0x3 -(int_b) generate INTB assertion and negation messages. 0x4 -(int_c) generate INTC assertion and negation messages. 0x5 -(int_d) generate INTD assertion and negation messages. 0x6 though 0x8 -(reserved) reserved.

Notes

Bit Field	Field Name	Type	Default Value	Description
8:6	INMSG2	RW	0x0	Inbound Message 2 Configuration. This field encodes the action taken when the INMSG2 bit in the INTSTS register is set, or cleared when INTx interrupt signalling is enabled. Regardless of the value of this field, an MSI is only sent when Enable (EN) bit is set in the MSICAP register. Similarly, and INTx message is only sent if not disabled by the INTXD bit in the PCICMD register. The action (i.e., this field) should not be modified while the corresponding bit is set. Modifying the action when the corresponding bit is set produces undefined results. 0x0 -(disabled) interrupt is masked/disabled. 0x1 -(msi) send a Message Signalled Interrupt (MSI) as specified by the MSI capability structure. 0x2 -(int_a) generate INTA assertion and negation messages. 0x3 -(int_b) generate INTB assertion and negation messages. 0x4 -(int_c) generate INTC assertion and negation messages. 0x5 -(int_d) generate INTD assertion and negation messages. 0x6 though 0x8 -(reserved) reserved.
11:9	INMSG3	RW	0x0	Inbound Message 3 Configuration. This field encodes the action taken when the INMSG3 bit in the INTSTS register is set, or cleared when INTx interrupt signalling is enabled. Regardless of the value of this field, an MSI is only sent when Enable (EN) bit is set in the MSICAP register. Similarly, and INTx message is only sent if not disabled by the INTXD bit in the PCICMD register. The action (i.e., this field) should not be modified while the corresponding bit is set. Modifying the action when the corresponding bit is set produces undefined results. 0x0 -(disabled) interrupt is masked/disabled. 0x1 -(msi) send a Message Signalled Interrupt (MSI) as specified by the MSI capability structure. 0x2 -(int_a) generate INTA assertion and negation messages. 0x3 -(int_b) generate INTB assertion and negation messages. 0x4 -(int_c) generate INTC assertion and negation messages. 0x5 -(int_d) generate INTD assertion and negation messages. 0x6 though 0x8 -(reserved) reserved.

Notes

Bit Field	Field Name	Type	Default Value	Description
14:12	INDBELL	RW	0x0	Inbound Doorbell Configuration. This field encodes the action taken when the INMSG1 bit in the INTSTS register is set, or cleared when INTx interrupt signalling is enabled. Regardless of the value of this field, an MSI is only sent when Enable (EN) bit is set in the MSICAP register. Similarly, and INTx message is only sent if not disabled by the INTXD bit in the PCICMD register. The action (i.e., this field) should not be modified while the corresponding bit is set. Modifying the action when the corresponding bit is set produces undefined results. 0x0 -(disabled) interrupt is masked/disabled. 0x1 -(msi) send a Message Signalled Interrupt (MSI) as specified by the MSI capability structure. 0x2 -(int_a) generate INTA assertion and negation messages. 0x3 -(int_b) generate INTB assertion and negation messages. 0x4 -(int_c) generate INTC assertion and negation messages. 0x5 -(int_d) generate INTD assertion and negation messages. 0x6 though 0x7 -(reserved) reserved.
17:15	OSRD	RW	0x0	Opposite Side Reset Detected Configuration. This field encodes the action taken when the OSRD bit in the INTSTS register is set, or cleared when INTx interrupt signalling is enabled. Regardless of the value of this field, an MSI is only sent when Enable (EN) bit is set in the MSICAP register. Similarly, and INTx message is only sent if not disabled by the INTXD bit in the PCICMD register. The action (i.e., this field) should not be modified while the corresponding bit is set. Modifying the action when the corresponding bit is set produces undefined results. 0x0 -(disabled) interrupt is masked/disabled. 0x1 -(msi) send a Message Signalled Interrupt (MSI) as specified by the MSI capability structure. 0x2 -(int_a) generate INTA assertion and negation messages. 0x3 -(int_b) generate INTB assertion and negation messages. 0x4 -(int_c) generate INTC assertion and negation messages. 0x5 -(int_d) generate INTD assertion and negation messages. 0x6 though 0x7 -(reserved) reserved.

Notes

Bit Field	Field Name	Type	Default Value	Description
20:18	OSPSTATEM	RW	0x0	Opposite Side Power State Modification Configuration. This field encodes the action taken when the OSPSTATEM bit in the INTSTS register is set, or cleared when INTx interrupt signalling is enabled. Regardless of the value of this field, an MSI is only sent when Enable (EN) bit is set in the MSICAP register. Similarly, and INTx message is only sent if not disabled by the INTXD bit in the PCICMD register. The action (i.e., this field) should not be modified while the corresponding bit is set. Modifying the action when the corresponding bit is set produces undefined results. 0x0 -(disabled) interrupt is masked/disabled. 0x1 -(msi) send a Message Signalled Interrupt (MSI) as specified by the MSI capability structure. 0x2 -(int_a) generate INTA assertion and negation messages. 0x3 -(int_b) generate INTB assertion and negation messages. 0x4 -(int_c) generate INTC assertion and negation messages. 0x5 -(int_d) generate INTD assertion and negation messages. 0x6 though 0x7 -(reserved) reserved.
28:21	Reserved	RO	0x0	Reserved field.
31:29	MSITC	RW	0x0	MSI Traffic Class. This field contains the traffic class to be used with MSI transaction. 0x0 -(tc0) traffic class 0 0x1 -(tc1) traffic class 1 0x2 -(tc2) traffic class 2 0x3 -(tc3) traffic class 3 0x4 -(tc4) traffic class 4 0x5 -(tc5) traffic class 5 0x6 -(tc6) traffic class 6 0x7 -(tc7) traffic class 7

Power Management Capability Structure

PCEE_PMCAP - PCI Power Management Capabilities (0x0F0)

Bit Field	Field Name	Type	Default Value	Description
7:0	CAPID	RO	0x1	Capability ID. The value of 0x1 identifies this capability as a PCI power management capability structure.
15:8	NXTPTR	RO	0x0	Next Pointer. This field contains 0x0 indicating that it is the last capability.
18:16	VER	RO	0x2	Power Management Capability Version. This field indicates compliance with version two of the specification.
19	PMECLK	RO	0x0	PME Clock. Does not apply to PCI Express.
20	Reserved	RO	0x0	Reserved field.

Notes

Bit Field	Field Name	Type	Default Value	Description
21	DEVSP	RWL	0x0	**Device Specific Initialization.** The value of zero indicates that no device specific initialization is required.
24:22	AUXI	RO	0x0	**AUX Current.** not used
25	D1	RO	0x0	**D1 Support.** This field indicates that the PES12NT3 does not support D1.
26	D2	RO	0x0	**D2 Support.** This field indicates that the PES12NT3 does not support D2.
31:27	PME	RO	0x0	**PME Support.** Non-transparent bridge endpoints never generate a PME message. This field indicates the power states in which the port may generate a PME.

PCEE_PMCSR - PCI Power Management Control and Status (0x0F4)

Bit Field	Field Name	Type	Default Value	Description
1:0	PSTATE	RW	0x0	**Power State.** This field is used to determine the current power state and to set a new power state. 0x0 - (d0) D0 state 0x1 -(d1) D1 state (not supported by the PES12NT3 and reserved) 0x2- (d2) D2 state (not supported by the PES12NT3 and reserved) 0x3 -(d3) $D3_{hot}$ state
7:2	Reserved	RO	0x0	Reserved field.
8	PMEE	RO	0x0	**PME Enable.** Non-transparent bridge endpoints never generate PM_PME messages. Therefore, this bit is hard-wired to zero.
12:9	DSEL	RO	0x0	**Data Select.** The optional data register is not implemented.
14:13	DSCALE	RO	0x0	**Data Scale.** The optional data register is not implemented.
15	PMES	RO	0x0	**PME Status.** Non-transparent bridge endpoints don't support PME notification. Therefore, this bit is hardwired to zero.
21:16	Reserved	RO	0x0	Reserved field.
22	B2B3	RO	0x0	**B2/B3 Support.** Does not apply to PCI Express.
23	BPCCE	RO	0x0	**Bus Power/Clock Control Enable.** Does not apply to PCI Express.
31:24	DATA	RO	0x0	**Data.** This optional field is not implemented.

Notes

Extended Configuration Space Access Registers

PCEE_ECFGADDR - Extended Configuration Space Access Address (0x0F8)

Bit Field	Field Name	Type	Default Value	Description
1:0	Reserved	RO	0x0	Reserved field.
7:2	REG	RW	0x0	Register Number. This field selects the configuration register number as defined by Section 7.2.2 of the PCI Express Base Specification, Rev. 1.0a
11:8	EREG	RW	0x0	Extended Register Number. This field selects the extended configuration register number as defined by Section 7.2.2 of the PCI Express Base Specification, Rev. 1.0a
31:12	Reserved	RO	0x0	Reserved field.

PCEE_ECFGDATA - Extended Configuration Space Access Data (0x0FC)

Bit Field	Field Name	Type	Default Value	Description
31:0	DATA	RW	0x0	Configuration Data. A read from this field will return the configuration space register value pointed to by the ECFGADDR register. A write to this field will update the contents of the configuration space register pointed to by the ECFGADDR register with the value written. For both reads and writes, the byte enables correspond to those used to access this field. When the ECFGADDR register points to the ECFGDATA register, then reads from ECFGDATA return zero and writes are ignored. When the ECFGADDR register points to itself, writes to the ECFGDATA register modify the contents of the ECFGADDR register. Note: Accessing the ECFGDATA or ECFGDATA data registers on the opposite side of the non-transparent bridge produces undefined results.

PCI Express Extended Capability Header

PCEE_PCIEECAP - PCI Express Extended Capability

Bit Field	Field Name	Type	Default Value	Description
15:0	CAPID	RO	0x0	Capability ID. The value of 0x0. indicates that the non-transparent bridge endpoint does not implement any extended capabilities.
19:16	CAPVER	RO	0x0	Capability Version. Not applicable.
31:20	NXTPTR	RO	0x0	Next Pointer. The value of 0x0 indicates that there are no extended capabilities.

Notes

Non-Transparent Bridge Control and Status Registers

PCEE_NTBCFG - Non-Transparent Bridge Configuration (0x200)

Bit Field	Field Name	Type	Default Value	Description
31:0	Reserved	RW	0x0	Reserved field.

PCEE_INTCTL1 - Interrupt Control 1 (0x210)

Bit Field	Field Name	Type	Default Value	Description
2:0	PALINKUP	RW	0x0	Port A Link Up Configuration. This field encodes the action taken when the PALINKUP bit in the INTSTS register is set, or cleared when INTx interrupt signalling is enabled. Regardless of the value of this field, an MSI is only sent when the Enable (EN) bit is set in the MSICAP register. Similarly, and INTx message is only sent if not disabled by the INTXD bit in the PCICMD register. The action (i.e., this field) should not be modified while the corresponding bit is set. Modifying the action when the corresponding bit is set produces undefined results. 0x0 -(disabled) interrupt is masked/disabled. 0x1 -(msi) send a Message Signalled Interrupt (MSI) as specified by the MSI capability structure. 0x2 -(int_a) generate INTA assertion and negation messages. 0x3 -(int_b) generate INTB assertion and negation messages. 0x4 -(int_c) generate INTC assertion and negation messages. 0x5 -(int_d) generate INTD assertion and negation messages. 0x6 though 0x8 -(reserved) reserved.

Notes

Bit Field	Field Name	Type	Default Value	Description
5:3	PALINKDN	RW	0x0	Port A Link Down Configuration. This field encodes the action taken when the PALINKDN bit in the INTSTS register is set, or cleared when INTx interrupt signalling is enabled. Regardless of the value of this field, an MSI is only sent when the Enable (EN) bit is set in the MSICAP register. Similarly, and INTx message is only sent if not disabled by the INTXD bit in the PCICMD register. The action (i.e., this field) should not be modified while the corresponding bit is set. Modifying the action when the corresponding bit is set produces undefined results. 0x0 -(disabled) interrupt is masked/disabled. 0x1 -(msi) send a Message Signalled Interrupt (MSI) as specified by the MSI capability structure. 0x2 -(int_a) generate INTA assertion and negation messages. 0x3 -(int_b) generate INTB assertion and negation messages. 0x4 -(int_c) generate INTC assertion and negation messages. 0x5 -(int_d) generate INTD assertion and negation messages. 0x6 though 0x8 -(reserved) reserved.
8:6	PBLINKUP	RW	0x0	Port B Link Up Configuration. This field encodes the action taken when the PBLINKUP bit in the INTSTS register is set, or cleared when INTx interrupt signalling is enabled. Regardless of the value of this field, an MSI is only sent when the Enable (EN) bit is set in the MSICAP register. Similarly, and INTx message is only sent if not disabled by the INTXD bit in the PCICMD register. The action (i.e., this field) should not be modified while the corresponding bit is set. Modifying the action when the corresponding bit is set produces undefined results. 0x0 -(disabled) interrupt is masked/disabled. 0x1 -(msi) send a Message Signalled Interrupt (MSI) as specified by the MSI capability structure. 0x2 -(int_a) generate INTA assertion and negation messages. 0x3 -(int_b) generate INTB assertion and negation messages. 0x4 -(int_c) generate INTC assertion and negation messages. 0x5 -(int_d) generate INTD assertion and negation messages. 0x6 though 0x8 -(reserved) reserved.

Notes

Bit Field	Field Name	Type	Default Value	Description
11:9	PBLINKDN	RW	0x0	Port B Link Down Configuration. This field encodes the action taken when the PBLINKDN bit in the INTSTS register is set, or cleared when INTx interrupt signalling is enabled. Regardless of the value of this field, an MSI is only sent when the Enable (EN) bit is set in the MSICAP register. Similarly, and INTx message is only sent if not disabled by the INTXD bit in the PCICMD register. The action (i.e., this field) should not be modified while the corresponding bit is set. Modifying the action when the corresponding bit is set produces undefined results. 0x0 -(disabled) interrupt is masked/disabled. 0x1 -(msi) send a Message Signalled Interrupt (MSI) as specified by the MSI capability structure. 0x2 -(int_a) generate INTA assertion and negation messages. 0x3 -(int_b) generate INTB assertion and negation messages. 0x4 -(int_c) generate INTC assertion and negation messages. 0x5 -(int_d) generate INTD assertion and negation messages. 0x6 though 0x8 -(reserved) reserved.
14:12	PCLINKUP	RW	0x0	Port C Link Up Configuration. This field encodes the action taken when the PCLINKUP bit in the INTSTS register is set, or cleared when INTx interrupt signalling is enabled. Regardless of the value of this field, an MSI is only sent when the Enable (EN) bit is set in the MSICAP register. Similarly, and INTx message is only sent if not disabled by the INTXD bit in the PCICMD register. The action (i.e., this field) should not be modified while the corresponding bit is set. Modifying the action when the corresponding bit is set produces undefined results. 0x0 -(disabled) interrupt is masked/disabled. 0x1 -(msi) send a Message Signalled Interrupt (MSI) as specified by the MSI capability structure. 0x2 -(int_a) generate INTA assertion and negation messages. 0x3 -(int_b) generate INTB assertion and negation messages. 0x4 -(int_c) generate INTC assertion and negation messages. 0x5 -(int_d) generate INTD assertion and negation messages. 0x6 though 0x8 -(reserved) reserved.

Notes

Bit Field	Field Name	Type	Default Value	Description
17:15	PCLINKDN	RW	0x0	Port C Link Down Configuration. This field encodes the action taken when the PCLINKDN bit in the INTSTS register is set, or cleared when INTx interrupt signalling is enabled. Regardless of the value of this field, an MSI is only sent when the Enable (EN) bit is set in the MSICAP register. Similarly, and INTx message is only sent if not disabled by the INTXD bit in the PCICMD register. The action (i.e., this field) should not be modified while the corresponding bit is set. Modifying the action when the corresponding bit is set produces undefined results. 0x0 -(disabled) interrupt is masked/disabled. 0x1 -(msi) send a Message Signalled Interrupt (MSI) as specified by the MSI capability structure. 0x2 -(int_a) generate INTA assertion and negation messages. 0x3 -(int_b) generate INTB assertion and negation messages. 0x4 -(int_c) generate INTC assertion and negation messages. 0x5 -(int_d) generate INTD assertion and negation messages. 0x6 though 0x8 -(reserved) reserved.
31:18	Reserved	RO	0x0	Reserved field.

Notes

PCEE_TLPPCTL - TLP Processing Control (0x214)

Bit Field	Field Name	Type	Default Value	Description
0	FRO	RW	0x0 Sticky	Force Relaxed Ordering. When this bit is set, all TLPs in which the relaxed attribute is applicable are modified as dictated by the Relaxed Ordering Modification (ROM) field in this register for TLPs flowing through the NTB from this side to the opposite side. When this bit is set, the state of the Enable Relaxed Ordering (ERO) bit in the PCI Express Device Control (PCIEDCTL) is ignored and has no functional affect on the operation of the device.
1	ROM	RW	0x0 Sticky	Relaxed Ordering Modification. When the FRO bit is set in this register, this field indicates the value that the relaxed ordering attribute should take on for all TLPs flowing through the NTB and in which the relaxed ordering attribute is applicable. 0x0 - (zero) Clear relaxed ordering attribute 0x1 - (one) Set relaxed ordering attribute
2	FNS	RW	0x0 Sticky	Force No-Snoop. When this bit is set, all TLPs in which the no-snoop attribute is applicable are modified as dictated by the No-Snoop Modification (NSM) field in this register for TLPs flowing through the NTB from this side to the opposite side.
3	NSM	RW	0x0 Sticky	No Snoop Modification. When the FNS bit is set in this register, this field indicates the value that the no-snoop attribute should take on for all TLPs flowing through the NTB and in which the no-snoop attribute is applicable. 0x0 - (zero) Clear no-snoop attribute 0x1 - (one) Set no-snoop attribute
31:4	Reserved	RO	0x0	Reserved field.

PCEE_BARTLIMIT0 - BAR 0 Translated Limit Address (0x218)

Bit Field	Field Name	Type	Default Value	Description
3:0	Reserved	RO	0x0	Reserved field.
31:4	TLADDR	RW	0xFFF_FFFF[1]	Translated Limit Address. This field specifies the translated limit address for transactions that map through BAR0 of the non-transparent bridge. When 64-bit addressing is selected, the translated limit address consists of the value in this field together with the upper 32 bits of the address contained in the BARTBASE1 register. A translation fails the limit test if the address is greater than the value specified in this field.

1. Not reset by external fundamental reset or internal/external hot reset

Notes

PCEE_BARTLIMIT1 - BAR 1 Translated Limit Address (0x21C)

When the MEMSI field in BARSETUP0 is set to memory space (i.e., zero) and the TYPE field is set to 64-bit addressing, BARTLIMIT1 takes on the function of the upper 32-bits of the TLADDR field in BARTLIMIT0. In this mode, all 32-bits of BARTLIMIT1 may be read and written.

Bit Field	Field Name	Type	Default Value	Description
3:0	Reserved	RO	0x0	Reserved field.
31:4	TLADDR	RW	0xFFF_FFFF[1]	Translated Limit Address. This field specifies the translated limit address for transactions that map through BAR1 of the non-transparent bridge. A translation fails the limit test if the address is greater than the value specified in this field.

1. Not reset by external fundamental reset or internal/external hot reset

PCEE_BARTLIMIT2 - BAR 2 Translated Limit Address (0x220)

Bit Field	Field Name	Type	Default Value	Description
3:0	Reserved	RO	0x0	Reserve field.
31:4	TLADDR	RW	0xFFF_FFFF[1]	Translated Limit Address. This field specifies the translated limit address for transactions that map through BAR2 of the non-transparent bridge. When 64-bit addressing is selected, the translated limit address consists of the value in this field together with the upper 32 bits of the address contained in the BARTBASE3 register. A translation fails the limit test if the address is greater than the value specified in this field.

1. Not reset by external fundamental reset or internal/external hot reset

PCEE_BARTLIMIT3 - BAR 3 Translated Limit Address (0x224)

When the MEMSI field in BARSETUP2 is set to memory space (i.e., zero) and the TYPE field is set to 64-bit addressing, BARTLIMIT3 takes on the function of the upper 32-bits of the TLADDR field in BARTLIMIT2. In this mode, all 32-bits of BARTLIMIT1 may be read and written.

Bit Field	Field Name	Type	Default Value	Description
3:0	Reserved	RO	0x0	Reserved field.
31:4	TLADDR	RW	0xFFF_FFFF[1]	Translated Limit Address. This field specifies the translated limit address for transactions that map through BAR3 of the non-transparent bridge. A translation fails the limit test if the address is greater than the value specified in this field.

1. Not reset by external fundamental reset or internal/external hot reset

Notes

PCEE_FOVRSTS - Failover Status (0x228)

Bit Field	Field Name	Type	Default Value	Description
0	CFMODE	RO	HWINIT	**Current Failover Mode.** This field indicates the current NTB upstream port failover mode. 0x0 -(normal) external port A associated with internal port A and external port C associated with internal port C. 0x1 - (failover) external port A associated with internal port C and external port C associated with internal port A.
1	FMODECC	RW1C	0x0 Sticky	**Failover Mode Change Completed.** This bit is set when a change in the NTB upstream port failover mode completes.
2	FMODECI	RW1C	0x0 Sticky	**Failover Mode Change Initiated.** This bit is set when a change is initiated in the NTB upstream port failover mode.
31:3	Reserved	RO	0x0	Reserved field.

PCEE_FOVRCTL - Failover Control (0x22C)

Bit Field	Field Name	Type	Default Value	Description
0	FOVRMSEL	RW	HWINIT Sticky	**NTB Upstream Port Failover Mode Select.** Modifying the value in this field initiates an NTB upstream port failover. When read, this field indicates the current NTB upstream port mode or the previous value written if an NTB upstream port failover is in progress. Modifying this field while an upstream port failover is in progress produces undefined results. The initial value of this field depends on the selected switch operating mode. The initial value is one if the SWMODE[3:0] field in the boot configuration vector is 5 or 6. The initial value is zero for all other SWMODE[3:0] field values. 0x0 -(normal) external port A associated with internal port A and external port C associated with internal port C. 0x1 - (failover) external port A associated with internal port C and external port C associated with internal port A.
1	SIGFEN	RW	0x0 Sticky	**Signal Failover Enable.** When this bit is set, an NTB upstream port failover is initiated when the state of the NTB Upstream Port Failover (FAILOVERP) signal does not match the current switch operating mode. The current switch operating mode is reported in the CNUSPM field in the NTB Upstream Port Failover Status (NUSPFSTS) register. Assertion of the FAILOVERP signal indicates failover mode while negation indicates normal mode. The FAILOVERP signal is a GPIO alternate function.
2	TIMFEN	RW	0x0 Sticky	**Timer Failover Enable.** When this bit is set, an NTB upstream port failover is initiated whenever the Count (COUNT) field in the NTB Upstream Port Failover Watchdog Timer (NUSPFTIMER) register reaches zero (i.e., the watchdog timer expires).

Notes

Bit Field	Field Name	Type	Default Value	Description
3	DFHRST	RW	0x0 Sticky	Disable Failover Hot Reset. When this bit is set, hot resets due to the data link layer of the upstream or NTB ports transitioning to the DL_Down caused by a failover are disabled.
4	IDLDHRST	RW	0x0 Sticky	Internal Hierarchy Disable Link Down Hot Reset. When this bit is set, hot resets due to the data link layer of the upstream port transitioning to the DL_Down state are disabled.
5	EDLDHRST	RW	0x0 Sticky	External Hierarchy Disable Link Down Hot Reset. When this bit is set, hot resets due to the data link layer of the NTB port transitioning to the DL_Down state are disabled.
6	IDHRSTPROP	RW	0x0 Sticky	Internal Hierarchy Disable Hot Reset Propagation. When this bit is set, hot resets received on the upstream port are ignored.
7	EDHRSTPROP	RW	0x0 Sticky	External Hierarchy Disable Hot Reset Propagation. When this bit is set, hot resets received on the NTB port are ignored.
31:8	Reserved	RO	0x0	Reserved field.

PCEE_FOVRTIMER - Failover Watchdog Timer (0x230)

Bit Field	Field Name	Type	Default Value	Description
31:0	COUNT	RW	0x0 Sticky	Watchdog Timer Count. This field contains the current watchdog timer count value. The value in this field is decremented by one every microsecond (1 uS). When this field reaches zero, it stops decrementing and the timer is said to have expired. When the value of this field transitions from one to zero, the Upstream Port Timer Failover Enable (TIMFEN) bit is set in the NTB Upstream Port Failover Control (NUSPFCTL) register, then an NTB upstream failover is initiated.

Notes

JTAG Boundary Scan

Notes

Introduction

The JTAG Boundary Scan interface provides a way to test the interconnections between integrated circuit pins after they have been assembled onto a circuit board.

There are two pin types present in the PES12NT3: AC-coupled and DC-coupled (also called AC and DC pins). The Boundary Scan interface in the PES12NT3 is IEEE 1149.1 compliant to allow testing of the DC pins. The DC pins are those “normal” pins that do not require AC-coupling.

The presence of AC-coupling capacitors on some of the PES12NT3 pins prevents DC values from being driven between a driver and receiver. An AC Boundary Scan methodology, as described in IEEE 1149.6, is available to provide a time-varying signal to pass through the AC-coupling when in AC test mode; however, IEEE 1149.6 is not supported in the PES12NT3.

Test Access Point

The system logic utilizes a 16-state, TAP controller, a six-bit instruction register, and five dedicated pins to perform a variety of functions. The primary use of the JTAG TAP Controller state machine is to allow the five external JTAG control pins to control and access the PES12NT3's many external signal pins. The JTAG TAP Controller can also be used for identifying the device part number. The JTAG logic of the PES12NT3 is depicted in Figure 10.1.

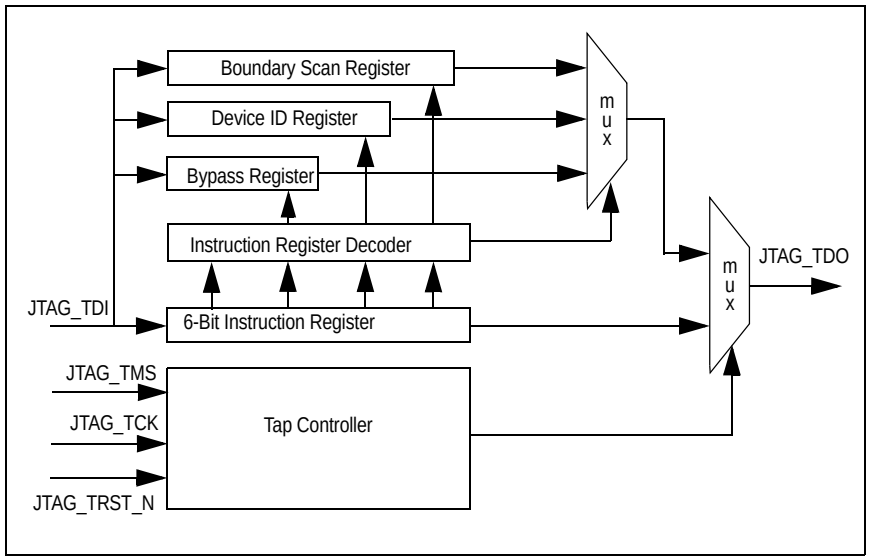

Figure 10.1 Diagram of the JTAG Logic

Refer to the IEEE 1149.1 document for an operational description of the Boundary Scan and TAP controller.

Signal Definitions

JTAG operations such as reset, state-transition control, and clock sampling are handled through the signals listed in Table 10.1. A functional overview of the TAP Controller and Boundary Scan registers is provided in the sections following the table.

Notes

Pin Name	Type	Description
JTAG_TRST_N	Input	JTAG RESET (active low) Asynchronous reset for JTAG TAP controller (internal pull-up)
JTAG_TCK	Input	JTAG Clock Test logic clock. JTAG_TMS and JTAG_TDI are sampled on the rising edge. JTAG_TDO is output on the falling edge.
JTAG_TMS	Input	JTAG Mode Select. Requires an external pull-up. Controls the state transitions for the TAP controller state machine (internal pull-up)
JTAG_TDI	Input	JTAG Input Serial data input for BSC chain, Instruction Register, IDCODE register, and BYPASS register (internal pull-up)
JTAG_TDO	Output	JTAG Output Serial data out. Tri-stated except when shifting while in Shift-DR and SHIFT-IR TAP controller states.

Table 10.1 JTAG Pin Descriptions

The TAP controller transitions from state to state, according to the value present on JTAG_TMS, as sampled on the rising edge of JTAG_TCK. The Test-Logic Reset state can be reached either by asserting JTAG_TRST_N or by applying a 1 to JTAG_TMS for five consecutive cycles of JTAG_TCK. A state diagram for the TAP controller appears in Figure 10.2. The value next to state represent the value that must be applied to JTAG_TMS on the next rising edge of JTAG_TCK, to transition in the direction of the associated arrow.

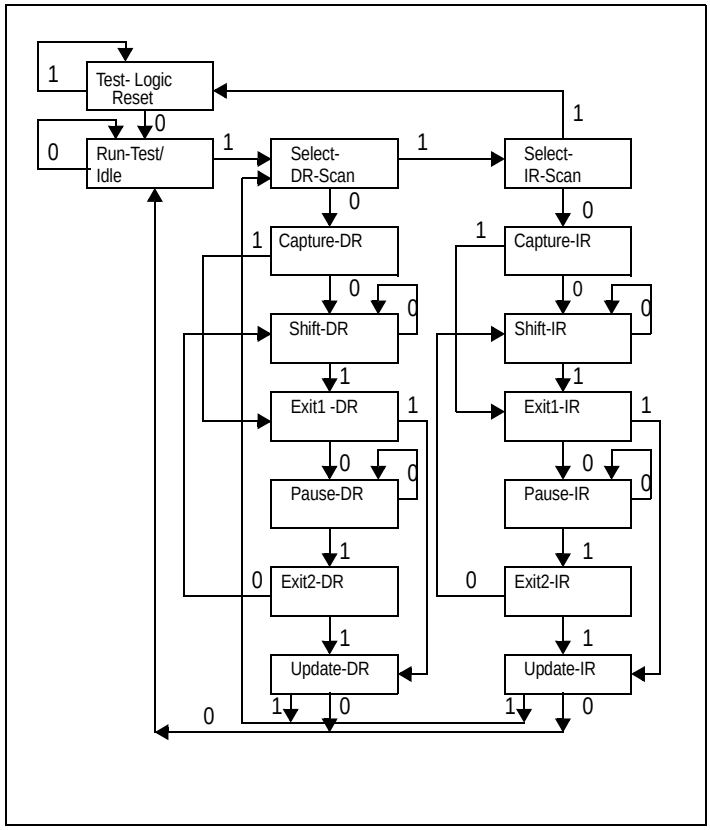

Figure 10.2 State Diagram of PES12NT3's TAP Controller

Notes

Boundary Scan Chain

Function	Pin Name	Type	Boundary Cell
PCI Express Interface	PEALREV	I	
	PEARN[3:0]	I	
	PEARP[3:0]	I	
	PEATN[3:0]	O	
	PEATP[3:0]	O	
	PECLREV	I	
	PECRN[3:0]	I	
	PECRP[3:0]	I	
	PECTN[3:0]	O	
	PECTP[3:0]	O	
	PEREFCLKN[1:0]	I	
	PEREFCLKP[1:0]	I	
	REFCLKM	I	
SMBus	MSMBADDR[4:1]	I	
	MSMBCLK	I/O	
	MSMBDAT	I/O	
	SSMBADDR[5,3:1]	I	
	SSMBCLK	I/O	
	SSMBDAT	I/O	
General Purpose I/O	GPIO[7:0]	I/O	
System Pins	CCLKDS	I	
	CCLKUS	I	
	MSMBSMODE	I	
	PENTBRSTN	I	
	PERSTN	I	
	RSTHALT	I	
	SWMODE[3:0]	I	
JTAG	JTAG_TCK	I	
	JTAG_TDI	I	
	JTAG_TDO	O	
	JTAG_TMS	I	
	JTAG_TRST_N	I	

Table 10.2 Boundary Scan Chain

Test Data Register (DR)

The Test Data register contains the following:

- Bypass register
- Boundary Scan registers
- Device ID register

Notes

These registers are connected in parallel between a common serial input and a common serial data output and are described in the following sections. For more detailed descriptions, refer to IEEE Standard Test Access Port (IEEE Std. 1149.1).

Boundary Scan Registers

This boundary scan chain is connected between JTAG_TDI and JTAG_TDO when EXTEST or SAMPLE/PRELOAD instructions are selected. Once EXTEST is selected and the TAP controller passes through the UPDATE-IR state, whatever value that is currently held in the boundary scan register's output latches is immediately transferred to the corresponding outputs or output enables.

Therefore, the SAMPLE/PRELOAD instruction must first be used to load suitable values into the boundary scan cells, so that inappropriate values are not driven out onto the system pins. All of the boundary scan cells feature a negative edge latch, which guarantees that clock skew cannot cause incorrect data to be latched into a cell. The input cells are sample-only cells. The simplified logic configuration is shown in Figure 10.3.

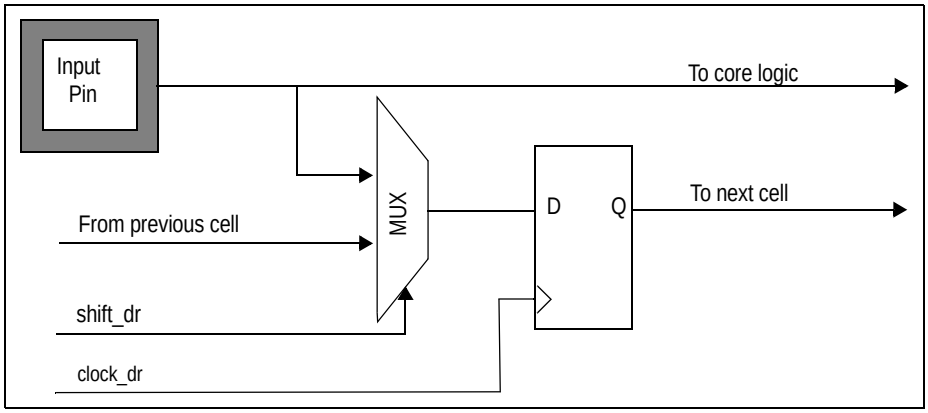

Figure 10.3 Diagram of Observe-only Input Cell

The simplified logic configuration of the output cells is shown in Figure 10.4.

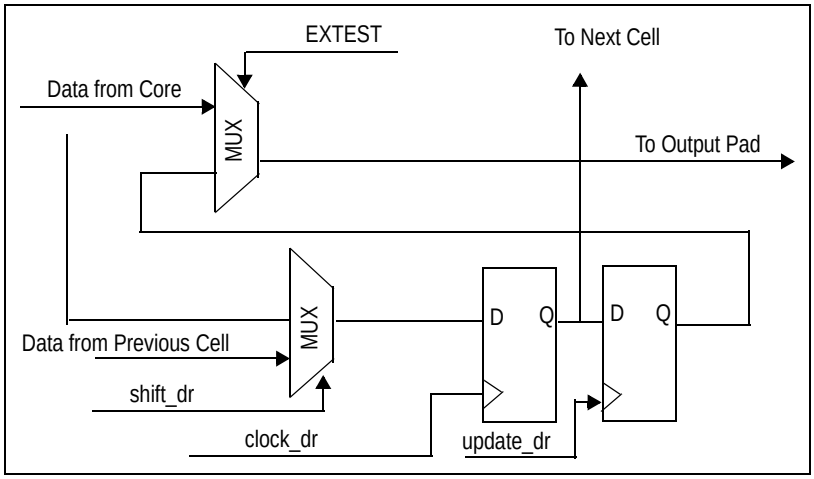

Figure 10.4 Diagram of Output Cell

The output enable cells are also output cells. The simplified logic is shown in Figure 10.5.

Notes

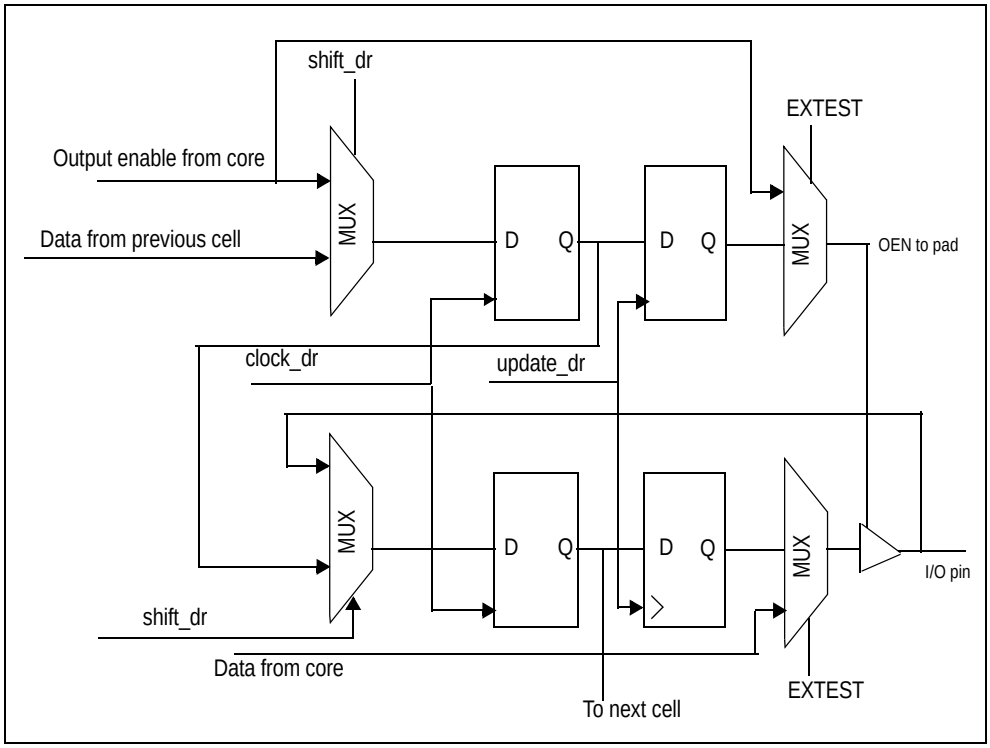

Figure 10.5 Diagram of Bidirectional Cell

The bidirectional cells are composed of only two boundary scan cells. They contain one output enable cell and one capture cell, which contains only one register. The input to this single register is selected via a mux that is selected by the output enable cell when EXTEST is disabled. When the Output Enable Cell is driving a high out to the pad (which enables the pad for output) and EXTEST is disabled, the Capture Cell will be configured to capture output data from the core to the pad.

However, in the case where the Output Enable Cell is low (signifying a tri-state condition at the pad) or EXTEST is enabled, the Capture Cell will capture input data from the pad to the core. The configuration is shown graphically in Figure 10.5.

Instruction Register (IR)

The Instruction register allows an instruction to be shifted serially into the device at the rising edge of JTAG_TCK. The instruction is then used to select the test to be performed or the test register to be accessed, or both. The instruction shifted into the register is latched at the completion of the shifting process, when the TAP controller is at the Update-IR state.

The Instruction register contains six shift-register-based cells that can hold instruction data. This register is decoded to perform the following functions:

- To select test data registers that may operate while the instruction is current. The other test data registers should not interfere with chip operation and selected data registers.
- To define the serial test data register path used to shift data between JTAG_TDI and JTAG_TDO during data register scanning.

The Instruction register is comprised of 6 bits to decode instructions, as shown in Table 10.3.

Notes

Instruction	Definition	Opcode
EXTEST	Mandatory instruction allowing the testing of board level interconnections. Data is typically loaded onto the latched parallel outputs of the boundary scan shift register using the SAMPLE/PRELOAD instruction prior to use of the EXTEST instruction. EXTEST will then hold these values on the outputs while being executed. Also see the CLAMP instruction for similar capability.	000000
SAMPLE/ PRELOAD	Mandatory instruction that allows data values to be loaded onto the latched parallel output of the boundary scan shift register prior to selection of the other boundary scan test instruction. The Sample instruction allows a snapshot of data flowing from the system pins to the on-chip logic or vice versa.	000001
IDCODE	Provided to select Device Identification to read out manufacturer's identity, part, and version number.	000010
HIGHZ	Tri-states all output and bidirectional boundary scan cells.	000011
RESERVED		000100 — 101100
VALIDATE	Automatically loaded into the instruction register whenever the TAP controller passes through the CAPTURE-IR state. The lower two bits '01' are mandated by the IEEE Std. 1149.1 specification.	101101
RESERVED		101110 — 111101
CLAMP	Provides JTAG users with the option to bypass the part's JTAG controller while keeping the part outputs controlled similar to EXTEST.	111110
BYPASS	The BYPASS instruction is used to truncate the boundary scan register as a single bit in length.	111111

Table 10.3 Instructions Supported by PES12NT3's JTAG Boundary Scan

EXTEST

The external test (EXTEST) instruction is used to control the boundary scan register, once it has been initialized using the SAMPLE/PRELOAD instruction. Using EXTEST, the user can then sample inputs from or load values onto the external pins of the PES12NT3. Once this instruction is selected, the user then uses the SHIFT-DR TAP controller state to shift values into the boundary scan chain. When the TAP controller passes through the UPDATE-DR state, these values will be latched onto the output pins or into the output enables.

SAMPLE/PRELOAD

The sample/preload instruction has a dual use. The primary use of this instruction is for preloading the boundary scan register prior to enabling the EXTEST instruction. Failure to preload will result in unknown random data being driven onto the output pins when EXTEST is selected. The secondary function of SAMPLE/PRELOAD is for sampling the system state at a particular moment. Using the SAMPLE function, the user can halt the device at a certain state and shift out the status of all of the pins and output enables at that time.

BYPASS

The BYPASS instruction is used to truncate the boundary scan register to a single bit in length. During system level use of the JTAG, the boundary scan chains of all the devices on the board are connected in series. In order to facilitate rapid testing of a given device, all other devices are put into BYPASS mode.

Notes

Therefore, instead of having to shift many times to get a value through the PES12NT3, the user only needs to shift one time to get the value from JTAG_TDI to JTAG_TDO. When the TAP controller passes through the CAPTURE-DR state, the value in the BYPASS register is updated to be 0.

CLAMP

This instruction, listed as optional in the IEEE 1149.1 JTAG Specifications, allows the boundary scan chain outputs to be clamped to fixed values. When the clamp instruction is issued, the bypass register is selected between TDI and TDO and the scan chain passes through this register to devices further downstream.

IDCODE

The IDCODE instruction is automatically loaded when the TAP controller state machine is reset either by the use of the JTAG_TRST_N signal or by the application of a '1' on JTAG_TMS for five or more cycles of JTAG_TCK as per the IEEE Std. 1149.1 specification. The least significant bit of this value must always be 1. Therefore, if a device has a Device ID register, it will shift out a 1 on the first shift if it is brought directly to the SHIFT-DR TAP controller state after the TAP controller is reset. The board- level tester can then examine this bit and determine if the device contains a Device ID register (the first bit is a 1), or if the device only contains a BYPASS register (the first bit is 0).

However, even if the device contains a Device ID register, it must also contain a BYPASS register. The only difference is that the BYPASS register will not be the default register selected during the TAP controller reset. When the IDCODE instruction is active and the TAP controller is in the Shift-DR state, the thirty-two bit value that will be shifted out of the Device ID register is shown in Figure 10.6.

Bit(s)	Mnemonic	Description	R/W	Reset
0	Reserved	Reserved	R	0x1
11:1	Manuf_ID	**Manufacturer Identity** (11 bits) This field identifies the manufacturer as IDT.	R	0x33
27:12	Part_number	**Part Number** (16 bits) This field identifies the silicon as PES12NT3.	R	0x8058
31:28	Version	**Version** (4 bits) This field identifies the silicon revision of the PES12NT3.	R	silicon-dependent

Table 10.4 System Controller Device Identification Register

Version	Part Number	Mnfg. ID	LSB
xxxx	1000|0000|0101|1000	0000|0011|011	1

Figure 10.6 Device ID Register Format

VALIDATE

The VALIDATE instruction is automatically loaded into the instruction register whenever the TAP controller passes through the CAPTURE-IR state. The lower two bits '01' are mandated by the IEEE Std. 1149.1 specification.

RESERVED

Reserved instructions implement various test modes used in the device manufacturing process. The user should not enable these instructions.

Usage Considerations

As previously stated, there are internal pull-ups on JTAG_TRST_N, JTAG_TMS, and JTAG_TDI. However, JTAG_TCK also needs to be driven to a known value. It is best to either drive a zero on the JTAG_TCK pin when it is not being used or to use an external pull-down resistor. In order to guarantee that

Notes

the JTAG does not interfere with normal system operation, the TAP controller should be forced into the Test-Logic-Reset controller state by continuously holding JTAG_TRST_N low and/or JTAG_TMS high when the chip is in normal operation. If JTAG will not be used, externally pull-down JTAG_TRST_N low to disable it.