Integrated Dual RF Transmitter and Observation Receiver

Preliminary Technical Data

ADRV9008-2

FEATURES

Dual transmitters
Dual input shared observation receiver
Maximum tunable transmitter synthesis bandwidth: 450 MHz
Maximum observation receiver bandwidth: 450 MHz
Fully integrated fractional-N RF synthesizers
Fully integrated clock synthesizer
Multichip phase synchronization for RF LO and baseband clocks
JESD204B datapath interface
Tuning range (center frequency): 75 MHz to 6000 MHz

APPLICATIONS

2G/3G/4G/5G macro cell base stations
Active antenna systems
Massive MIMO
Phased array radar
Electronic warfare
Military communications
Portable test equipment

GENERAL DESCRIPTION

The ADRV9008-2 is a highly integrated, RF agile transmit subsystem offering dual channel transmitters, observation path receiver, integrated synthesizers, and digital signal processing functions. The IC delivers a versatile combination of high performance and low power consumption demanded by 2G, 3G, 4G and 5G macro cell base stations, and active antenna applications.

The transmitters use an innovative direct conversion modulator that achieves multicarrier macro base station quality performance and low power. In 3G/4G mode, the maximum large signal bandwidth is 200 MHz. In multicarrier global system for mobile communications (MC-GSM) mode, which has higher in-band spurious-free dynamic range (SFDR), the maximum large signal bandwidth is 75 MHz.

The observation path consists of a wide bandwidth direct conversion receiver with state of the art dynamic range. The complete receive subsystem includes dc offset correction, quadrature correction, and digital filtering, thus eliminating the need for these functions in the digital baseband. Several auxiliary functions such as analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and general-purpose inputs/outputs (GPIOs) for PA and RF front-end control are also integrated.

The fully integrated phase locked loops (PLLs) provide high performance, low power fractional-N RF frequency synthesis for the transmitter and receiver sections. An additional synthesizer is used to generate the clocks needed for the converters, digital circuits, and the serial interface. Special precautions have been taken to provide the isolation demanded in high performance base station applications. All VCO and loop filter components are integrated.

The high speed JESD204B interface supports up to 12.288 Gbps lane rates, resulting in two lanes per transmitter in the widest bandwidth mode and two lanes for the observation path receiver in the widest bandwidth mode.

The core of the ADRV9008-2 can be powered directly from 1.3 V regulators and 1.8 V regulators and is controlled via a standard 4-wire serial port. Comprehensive power-down modes are included to minimize power consumption in normal use. The ADRV9008-2 is packaged in a 12 mm × 12 mm 196-ball chip scale ball grid array (CSP_BGA).

Rev. PrA Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

Technical Support www.analog.com

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FUNCTIONAL BLOCK DIAGRAM

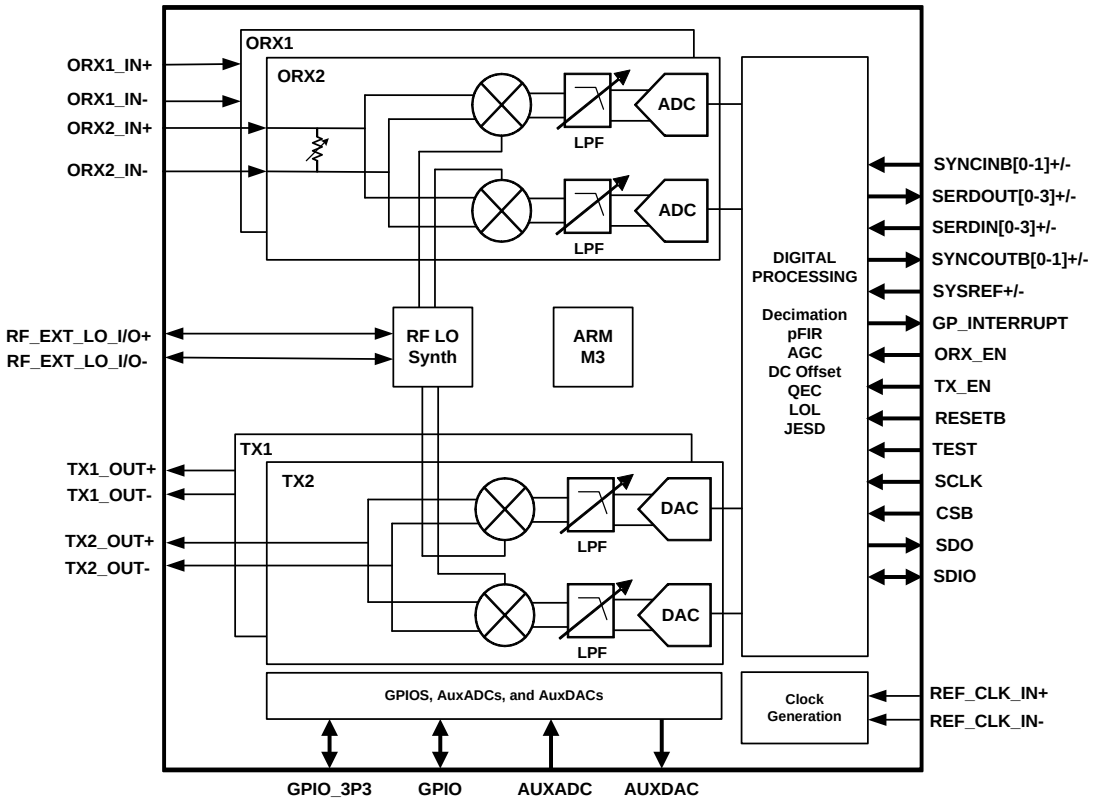


Figure 1.

SPECIFICATIONS

Electrical characteristics at VDDA1P3[1] = 1.3 V, VDDD1P3_DIG = 1.3 V, VDDA1P8_TX = 1.8 V, T_J = full operating temperature range. Local oscillator frequency (f_{LO}) = 1800 MHz, unless otherwise noted. The specifications in Table 1 are not de-embedded. Refer to the Typical Performance Characteristics section for input/output circuit path loss. The device configuration profile, unless otherwise specified, is as follows: Transmitter = 200 MHz/450 MHz (IQ rate = 491.52 MHz), observation receiver = 450 MHz (IQ rate = 491.52 MHz), JESD204B rate = 9.8304 GSPS, and device clock = 245.76 MHz.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
TRANSMITTERS						
Center Frequency		75		6000	MHz	
Transmitter (Tx) Synthesis Bandwidth (BW)				450	MHz	
Transmitter Large Signal Bandwidth				200	MHz	
Transmitter Large Signal Bandwidth (MC-GSM)				75	MHz	Low IF mode
Peak-to-Peak Gain Deviation			1.0		dB	450 MHz bandwidth, compensated by programmable finite impulse response (FIR) filter
Gain Slope			±0.1		dB	Any 20 MHz bandwidth span, compensated by programmable FIR filter
Deviation from Linear Phase			1		Degrees	450 MHz bandwidth
Transmitter Attenuation Power Control Range		0		32	dB	Signal-to-noise ratio (SNR) maintained for attenuation between 0 dB and 20 dB
Transmitter Attenuation Power Control Resolution			0.05		dB	
Transmitter Attenuation Integral Nonlinearity	INL		0.1		dB	For any 4 dB step
Transmitter Attenuation Differential Nonlinearity	DNL		±0.04		dB	Monotonic
Transmitter Attenuation Serial Peripheral Interface-2 (SPI-2) Timing						See Figure 4
Time from $\overline{CS}$ Going High to Change in Transmitter Attenuation	t_{SCH}	19.5		24	ns	
Time Between Consecutive Micro Attenuation Steps	t_{ACH}	6.5		8.1	ns	A large change in attenuation can be broken up into a series of smaller attenuation changes
Time Required to Reach Final Attenuation Value	t_{DCH}			800	ns	Time required to complete the change in attenuation from start attenuation to final attenuation value
Maximum Attenuation Overshoot During Transition		−1.0		+0.5	dB	
Change in Attenuation per Micro Step				0.5	dB	
Maximum Attenuation Change when $\overline{CS}$ Goes High			32		dB	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Adjacent Channel Leakage Ratio (ACLR) (LTE)						20 MHz LTE at −12 dBFS
			−67		dB	75 MHz < f ≤ 2800 MHz
			−64		dB	2800 MHz < f ≤ 4800 MHz
			−60		dB	4800 MHz < f ≤ 6000 MHz
In Band Noise Floor						0 dB attenuation, in-band noise falls 1 dB for each dB of attenuation for attenuation between 0 dB and 20 dB
			−148		dBm/Hz	600 MHz < f ≤ 3000 MHz
			−149		dBm/Hz	3000 MHz < f ≤ 4800 MHz
			−150.5		dBm/Hz	4800 MHz < f ≤ 6000 MHz
Out of Band Noise Floor						0 dB attenuation; 3 × bandwidth/2 offset
			−153		dBm/Hz	600 MHz < f ≤ 3000 MHz
			−154		dBm/Hz	3000 MHz < f ≤ 4800 MHz
			−155.5		dBm/Hz	4800 MHz < f ≤ 6000 MHz
Interpolation Images						
GSM Mode			−95		dBc	
3G/4G			−80		dBc	
Transmitter to Transmitter Isolation			85		dB	75 MHz < f ≤ 600 MHz
			75		dB	600 MHz < f ≤ 2800 MHz
			70		dB	2800 MHz < f ≤ 4800 MHz
			65		dB	4800 MHz < f ≤ 5700 MHz
			56		dB	5700 MHz < f ≤ 6000 MHz
Image Rejection						
Within Large Signal Bandwidth						QEC active
			70		dB	75 MHz < f ≤ 600 MHz
			65		dB	600 MHz < f ≤ 4000 MHz
			62		dB	4000 MHz < f ≤ 4800 MHz
			60		dB	4800 MHz < f ≤ 6000 MHz
Beyond Large Signal Bandwidth			40		dB	Assumes that distortion power density is 25 dB below desired power density
Maximum Output Power						0 dBFS, continuous wave (CW) tone into 50 Ω load, 0 dB transmitter attenuation
			9		dBm	75 MHz < f ≤ 600 MHz
			7		dBm	600 MHz < f ≤ 3000 MHz
			6		dBm	3000 MHz < f ≤ 4800 MHz
			4.5		dBm	4800 MHz < f ≤ 6000 MHz
Third-Order Output Intermodulation Intercept Point	OIP3					0 dB transmitter attenuation
			29		dBm	75 MHz < f ≤ 600 MHz
			27		dBm	600 MHz < f ≤ 4000 MHz
			23		dBm	4000 MHz < f ≤ 6000 MHz
Third-Order Intermodulation	IM3		−70		dBc	2 × GSMK carriers, ΣP_{OUT} = −12dBFS rms
						The 2 carriers can be placed anywhere within the transmitter band such that the IM3 products fall within the transmitter band or within 10 MHz of the band edges

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Carrier Leakage						With LO leakage correction active, 0 dB attenuation, scales decibel for decibel with attenuation, measured in 1 MHz bandwidth, resolution bandwidth, and video bandwidth = 100 kHz, rms detector, 100 trace average
Carrier Offset from Local Oscillator (LO)			−84		dBFS	75 MHz < f ≤ 600 MHz
			−82		dBFS	600 MHz < f ≤ 4800 MHz
			−80		dBFS	4800 MHz < f ≤ 6000 MHz
Carrier on LO			−71		dBFS	
Error Vector Magnitude (Third Generation Partnership Project (3GPP) Test Signals)	EVM					
75 MHz LO			0.5		%	300 kHz RF PLL loop bandwidth
1900 MHz LO			0.7		%	50 kHz RF PLL loop bandwidth
3800 MHz LO			0.7		%	300 kHz RF PLL loop bandwidth
5900 MHz LO			1.1		%	300 kHz RF PLL loop bandwidth
Output Impedance	Z_{OUT}		50		Ω	Differential (see Figure 268)
OBSERVATION RECEIVER	ORx					
Center Frequency		75		6000	MHz	ADRV9008-2
Gain Range			30		dB	Third-order input intermodulation intercept point (IIP3) improves decibel for decibel for the first 18 dB of gain attenuation, QEC performance optimized for 0 dB to 6 dB of attenuation only
Analog Gain Step			0.5		dB	For attenuator steps from 0 dB to 6 dB
Peak-to-Peak Gain Deviation			1		dB	450 MHz bandwidth, compensated by programmable FIR filter
Gain Slope			±0.1		dB	Any 20 MHz bandwidth span, compensated by programmable FIR filter
Deviation from Linear Phase			1		Degrees	450 MHz RF bandwidth
Receiver Bandwidth				450	MHz	
Receiver Alias Band Rejection		60			dB	Due to digital filters
Maximum Useable Input Level	P_{HIGH}					0 dB attenuation, increases decibel for decibel with attenuation, continuous wave corresponds to −1 dBFS at ADC
			−11		dBm	75 MHz < f ≤ 3000 MHz
			−9.5		dBm	3000 MHz < f ≤ 4800 MHz
			−8		dBm	4800 MHz < f ≤ 6000 MHz
Integrated Noise			−58.5		dBFS	450 MHz integration bandwidth
			−57.5		dBFS	491.52 MHz integration bandwidth
Second-Order Input Intermodulation Intercept Point	IIP2		62		dBm	Maximum observation receiver gain, P_{HIGH} − 14 dB per tone (see the Terminology section), 75 MHz < f ≤ 600 MHz
			62		dBm	Maximum observation gain, P_{HIGH} − 8 dB per tone (see the Terminology section), 600 MHz < f ≤ 3000 MHz

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Third-Order Input Intermodulation Intercept Point	IIP3					
Narrow Band			11		dBm	300 MHz < f ≤ 600 MHz, test condition: (P_{HIGH} − 14) dB per tone
						IM3 product < 130 MHz at baseband, test condition: (P_{HIGH} − 8) dB per tone
			12		dBm	600 MHz < f ≤ 3000 MHz
			12		dBm	3000 MHz < f ≤ 4800 MHz
			11		dBm	4800 MHz < f ≤ 6000 MHz
Wide Band						
			7		dBm	600 MHz < f ≤ 3000 MHz
			7		dBm	3000 MHz < f ≤ 4800 MHz
			6		dBm	4800 MHz < f ≤ 6000 MHz
Third-Order Intermodulation Product	IM3					IM3 product < 130 MHz at baseband, two tones, each at (P_{HIGH} − 12) dB
			−70		dBc	600 MHz < f ≤ 3000 MHz
			−67		dBc	3000 MHz < f ≤ 4800 MHz
			−62		dBc	4800 MHz < f ≤ 6000 MHz
Fifth-Order Intermodulation Product (1800 MHz)	IM5		−80		dBc	IM5 product < 50 MHz at baseband, two tones, each at (P_{HIGH} − 14) dB
Seventh-Order Intermodulation Product (1800 MHz)	IM7		−80		dBc	IM7 product < 50 MHz at baseband, two tones, each at (P_{HIGH} − 14) dB
Spurious-Free Dynamic Range	SFDR		70		dB	Non IMx related spurs, does not include HDx, (P_{HIGH} − 11) dB input signal
Harmonic Distortion						(P_{HIGH} − 11) dB input signal
Second-Order Harmonic Distortion Product	HD2		−80		dBc	In band HD falls within ±25 MHz
			−80		dBc	Out of band HD falls within ±50 MHz
Third-Order Harmonic Distortion Product	HD3		−70		dBc	In band HD falls within ±25 MHz
			−60		dBc	Out of band HD falls within ±50 MHz
Image Rejection						QEC active
Within Large Signal Bandwidth			65		dB	
Outside Large Signal Bandwidth			55		dB	
Input Impedance			100		Ω	Differential (see Figure 269)
Isolation						
Transmitter 1 (Tx1) to Observation Receiver 1 (ORx1) and Transmitter 2 (Tx2) to Observation Receiver 2 (ORx2)			65		dB	600 MHz < f ≤ 5300 MHz
			55		dB	5300 MHz < f ≤ 6000 MHz
Tx1 to ORx2 and Tx2 to ORx 1			65		dB	600 MHz < f ≤ 5300 MHz
			55		dB	5300 MHz < f ≤ 6000 MHz

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
LO SYNTHESIZER						
LO Frequency Step			2.3		Hz	1.5 GHz to 2.8 GHz, 76.8 MHz phase frequency detector (PFD) frequency
LO Spur			−85		dBc	Excludes integer boundary spurs
Integrated Phase Noise						2 kHz to 18 MHz
1900 MHz LO			0.2		°rms	Narrow PLL loop bandwidth (50 kHz)
3800 MHz LO			0.36		°rms	Wide PLL loop bandwidth (300 kHz)
5900 MHz LO			0.54		°rms	Wide PLL loop bandwidth (300 kHz)
Spot Phase Noise						
1900 MHz LO						Narrow PLL loop bandwidth
100 kHz Offset			−100		dBc/Hz	
200 kHz Offset			−115		dBc/Hz	
400 kHz Offset			−120		dBc/Hz	
600 kHz Offset			−129		dBc/Hz	
800 kHz Offset			−132		dBc/Hz	
1.2 MHz Offset			−135		dBc/Hz	
1.8 MHz Offset			−140		dBc/Hz	
6 MHz Offset			−150		dBc/Hz	
10 MHz Offset			−153		dBc/Hz	
3800 MHz LO						Wide PLL loop bandwidth
100 kHz Offset			−104		dBc/Hz	
1.2 MHz Offset			−125		dBc/Hz	
10 MHz Offset			−145		dBc/Hz	
5900 MHz LO						Wide PLL loop bandwidth
100 kHz Offset			−99		dBc/Hz	
1.2 MHz Offset			−119.7		dBc/Hz	
10 MHz Offset			−135.4		dBc/Hz	
LO PHASE SYNCHRONIZATION						
Phase Deviation			1.6		ps/°C	Change in LO delay per temperature change
EXTERNAL LO INPUT						
Input Frequency	f_{EXTLO}	150		8000	MHz	Input frequency must be 2× the desired LO frequency
Input Signal Power		0		12	dBm	50 Ω matching at the source
			3		dBm	f_{EXTLO} ≤ 2 GHz, add 0.5 dBm/GHz above 2 GHz
			6		dBm	f_{EXTLO} = 8 GHz
External LO Input Signal Differential						To ensure adequate QEC
Phase Error				3.6	ps	
Amplitude Error				1	dB	
Duty Cycle Error				2	%	
Even-Order Harmonics				−50	dBc	
CLOCK SYNTHESIZER						
Integrated Phase Noise						1 kHz to 100 MHz
1966.08 MHz LO			0.4		°rms	PLL optimized for close in phase noise
Spot Phase Noise						
1966.08 MHz						
100 kHz Offset			−109		dBc/Hz	
1 MHz Offset			−129		dBc/Hz	
10 MHz Offset			−149		dBc/Hz	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
REFERENCE CLOCK (REF_CLK_IN)						
Frequency Range		10		1000	MHz	
Signal Level		0.3		2.0	V p-p	AC-coupled, common-mode voltage (V_{CM}) = 618 mV, for best spurious performance, use <1 V p-p input clock
AUXILIARY CONVERTERS						
ADC						
Resolution			12		Bits	
Input Voltage						
Minimum			0.05		V	
Maximum			VDDA_3P3 − 0.05		V	
DAC						
Resolution			10		Bits	Includes four offset levels
Output Voltage						
Minimum			0.7		V	1 V V_{REF}
Maximum			VDDA_3P3 − 0.3		V	2.5 V V_{REF}
Output Drive Capability			10		mA	
DIGITAL SPECIFICATIONS (CMOS)—SPI, GPIO_x, TXx_ENABLE, ORXx_ENABLE						
Logic Inputs						
Input Voltage						
High Level		VDD_INTERFACE × 0.8		VDD_INTERFACE	V	
Low Level		0		VDD_INTERFACE × 0.2	V	
Input Current						
High Level		−10		+10	µA	
Low Level		−10		+10	µA	
Logic Outputs						
Output Voltage						
High Level		VDD_INTERFACE × 0.8			V	
Low Level				VDD_INTERFACE × 0.2	V	
Drive Capability			3		mA	
DIGITAL SPECFICATIONS (CMOS)—GPIO_3P3_x						
Logic Inputs						
Input Voltage						
High Level		VDDA_3P3 × 0.8		VDDA_3P3	V	
Low Level		0		VDDA_3P3 × 0.2	V	
Input Current						
High Level		−10		+10	µA	
Low Level		−10		+10	µA	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Logic Outputs						
Output Voltage						
High Level		VDDA_ 3P3 × 0.8			V	
Low Level				VDDA_ 3P3 × 0.2	V	
Drive Capability			4		mA	
DIGITAL SPECIFICATIONS (LVDS)						
Logic Inputs (SYSREF_IN±, SYNCINx±)						
Input Voltage Range		825		1675	mV	Each differential input in the pair
Input Differential Voltage Threshold		−100		+100	mV	
Receiver Differential Input Impedance			100		Ω	Internal termination enabled
Logic Outputs (SYNCOUTx±)						
Output Voltage						
High				1375	mV	
Low		1025			mV	
Output Differential Voltage			225		mV	Programmable in 75 mV steps
Output Offset Voltage			1200		mV	
SPI TIMING						
SCLK Period	t_{CP}	20			ns	
SCLK Pulse Width	t_{MP}	10			ns	
$\overline{CS}$ Setup to First SCLK Rising Edge	t_{SC}	3			ns	
Last SCLK Falling Edge to $\overline{CS}$ Hold	t_{HC}	0			ns	
SDIO Data Input Setup to SCLK	t_S	2			ns	
SDIO Data Input Hold to SCLK	t_H	0			ns	
SCLK Rising Edge to Output Data Delay (3-Wire or 4-Wire Mode)	t_{CO}	3		8	ns	
Bus Turnaround Time, Read After Bits per Pixel (BBP) Drives Last Address Bit	t_{HZM}	t_H		t_{CO}	ns	
Bus Turnaround Time, Read After ADRV9008-2 Drives Last Data Bit	t_{HZS}	0		t_{CO}	ns	
JESD204B DATA OUTPUT TIMING						AC-coupled
Unit Interval	UI	81.38		320	ps	
Data Rate per Channel (NRZ)		3125		12288	Mbps	
Rise Time	t_R	24	39.5		ps	20% to 80% in 100 Ω load
Fall Time	t_F	24	39.4		ps	20% to 80% in 100 Ω load
Output Common-Mode Voltage	V_{CM}	0		1.8	V	AC-coupled
Differential Output Voltage	V_{DIFF}	360	600	770	mV	
Short-Circuit Current	I_{DSHORT}	−100		+100	mA	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Differential Termination Impedance		80	94.2	120	Ω	
Total Jitter			15.13		ps	Bit error rate (BER) = 10^{-15}
Uncorrelated Bounded High Probability Jitter	UBHPJ		0.56		ps	
Duty Cycle Distortion	DCD		0.369		ps	
SYSREF_IN± Setup Time to REF_CLK_IN_x		2.5			ns	See Figure 2
SYSREF_IN± Hold Time to REF_CLK_IN_x		−1.5			ns	See Figure 2
Latency	T_{LAT_FRM}					REF_CLK_IN = 245.76 MHz
			116.5		Clock cycles	Observation receiver bandwidth = 450 MHz, IQ rate = 491.52 MHz, lane rate = 9830.4 MHz, number of converters (M) = 4, number of lanes (L) = 2, converter resolution (N) = 16, number of samples per converter (S) = 1
			237.02		ns	
			89.4		Clock cycles	Receiver bandwidth = 200 MHz, IQ rate = 245.76 MHz, lane rate = 9830.4 MHz, M = 2, L = 2, N = 16, S = 1
			364.18		ns	
JESD204B DATA INPUT TIMING						AC-coupled
Unit Interval	UI	81.38		320	ps	
Data Rate per Channel (NRZ)		3125		12288	Mbps	
Differential Voltage	V_{DIFF}	125		750	mV	
V_{TT} Source Impedance	Z_{TT}		8.9	30	Ω	
Differential Impedance	Z_{RDIFF}	80	105.1	120		
Termination Voltage	V_{TT}					
AC-Coupled		1.267		1.33	V	
Latency	t_{LAT_DEFRM}		74.45		Clock cycles	Device clock = 245.76 MHz, transmitter bandwidth = 200 MHz, IQ rate = 491.52 MHz, lane rate = 9830.4 MHz, M = 2, L = 2, N = 16, S = 1
			153.5		ns	

[1] VDDA1P3 refers to all analog 1.3 V supplies, including: VDDA1P3_RF_SYNTH, VDDA1P3_BB, VDDA1P3_RX_RF, VDDA1P3_RX_TX, VDDA1P3_RF_VCO_LDO, VDDA1P3_RF_LO, VDDA1P3_DES, VDDA1P3_SER, VDDA1P3_CLOCK_SYNTH, VDDA1P3_CLOCK_VCO_LDO, VDDA1P3_AUX_SYNTH, and VDDA1P3_AUX_VCO_LDO.

CURRENT AND POWER CONSUMPTION SPECIFICATIONS

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CHARACTERISTICS					
VDDA1P3[1] Analog Supply	1.267	1.3	1.33	V	
VDDD1P3_DIG Supply	1.267	1.3	1.33	V	
VDDA1P8_TX Supply	1.71	1.8	1.89	V	
VDDA1P8_BB Supply	1.71	1.8	1.89	V	
VDD_INTERFACE Supply	1.71	1.8	2.625	V	CMOS and LVDS supply, 1.8 V to 2.5 V nominal range
VDDA_3P3 Supply	3.135	3.3	3.465	V	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POSITIVE SUPPLY CURRENT					LO at 2600 MHz
450 MHz Transmitter Bandwidth, Observation Receiver Disabled					Two transmitters enabled
VDDA1P3[1] Analog Supply		1978		mA	
VDDD1P3_DIG Supply		611		mA	Transmitter QEC active
VDDA1P8_TX Supply		455		mA	Transmitter RF attenuation = 0 dB, full scale CW
		135		mA	Transmitter RF attenuation = 15 dB, full scale continuous wave
VDD_INTERFACE Supply		8		mA	VDD_INTERFACE = 2.5V
VDDA1P8_BB Supply		68		mA	
VDDA_3P3 Supply		3		mA	No AUXDAC_x or AUXADC_x enabled; if enabled, AUXADC_x adds 2.7 mA and each AUXDAC_x adds 1.5 mA
Total Power Dissipation		4.34		W	Typical supply voltages, 0 dB transmitter attenuation, transmitter QEC active
		3.76		W	Typical supply voltages, 15 dB transmitter attenuation, transmitter QEC active
450 MHz Transmitter Bandwidth, Observation Receiver Enabled					Two transmitters enabled
VDDA1P3[1] Analog Supply		2059		mA	
VDDD1P3_DIG Supply		1501		mA	Transmitter QEC tracking active, observation receiver QEC enabled
VDDA1P8_TX Supply		455		mA	Transmitter RF attenuation = 0 dB, full scale continuous wave
		135		mA	Transmitter RF attenuation = 15 dB, full scale continuous wave
VDD_INTERFACE Supply		8		mA	VDD_INTERFACE = 2.5 V
VDDA1P8_BB Supply		63		mA	
VDDA_3P3 Power Supply		3		mA	No AUXDAC_x or AUXADC_x enabled, if enabled, AUXADC_x adds 2.7 mA and each AUXDAC_x adds 1.5 mA
Total Power Dissipation		5.59		W	Typical supply voltages, 0 dB transmitter attenuation, transmitter QEC active
		5.01		W	Typical supply voltages, 15 dB transmitter attenuation, transmitter QEC active

[1] VDDA1P3 refers to all analog 1.3 V supplies, including: VDDA1P3_RF_SYNTH, VDDA1P3_BB, VDDA1P3_RX_RF, VDDA1P3_RX_TX, VDDA1P3_RF_VCO_LDO, VDDA1P3_RF_LO, VDDA1P3_DES, VDDA1P3_CLOCK, VDDA1P3_TX_LO_BUFFER, and VDDA1P3_CLOCK_SYNTH.

TIMING DIAGRAMS

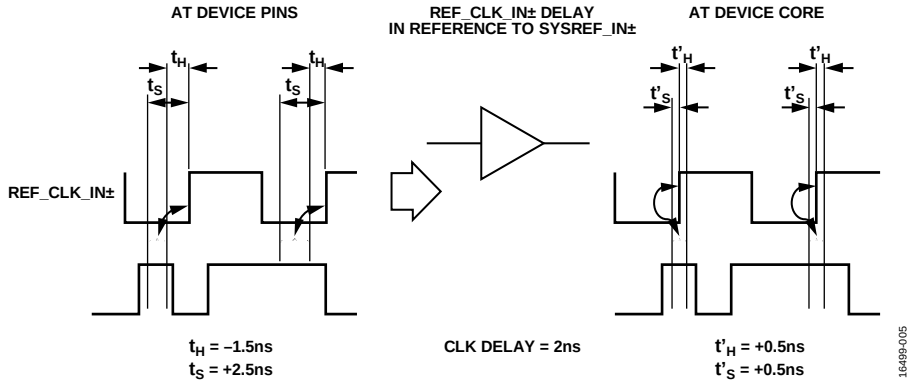


Figure 2. SYSREF_IN± Setup and Hold Timing

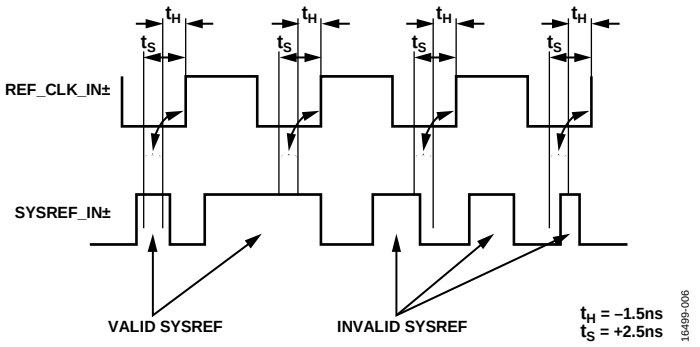


Figure 3. SYSREF_IN± Setup and Hold Timing Examples, Relative to Device Clock

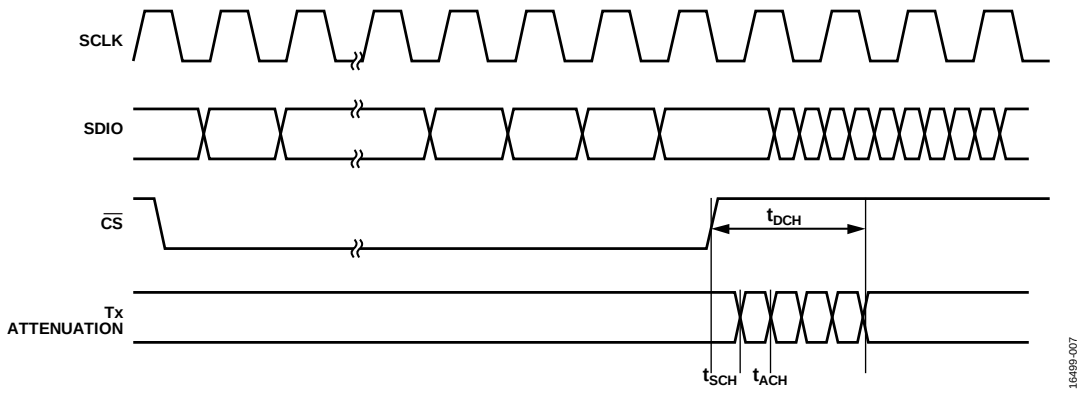


Figure 4. Transmitter Attenuation Update via SPI-2 Port

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
VDDA1P3[1] to VSSA	−0.3 V to +1.4 V
VDDD1P3_DIG to VSSD	−0.3 V to +1.4 V
VDD_INTERFACE to VSSA	−0.3 V to +3.0 V
VDDA_3P3 to VSSA	−0.3 V to +3.9 V
VDDA1P8_TX to VSSA	−0.3 V to +2.0 V
VDD_INTERFACE Logic Inputs and Outputs to VSSD	−0.3 V to VDD_INTERFACE + 0.3 V
JESD204B Logic Outputs to VSSA	−0.3 V to VDDA1P3_SER
JESD204B Logic Inputs to VSSA	−0.3 V to VDDA1P3_DES +0.3 V
Input Current to any Pin Except Supplies	±10 mA
Reflow Profile	260°C
Maximum Input Power into RF Port	23 dBm (peak)
Maximum Transmitter Voltage Standing Wave Ratio (VSWR)	3:1
Maximum Junction Temperature	110°C
Storage Temperature Range	−65°C to +150°C

[1] VDDA1P3 refers to all analog 1.3 V supplies, including: VDDA1P3_RF_SYNTH, VDDA1P3_BB, VDDA1P3_RX_RF, VDDA1P3_RX_TX, VDDA1P3_RF_VCO_LDO, VDDA1P3_RF_LO, VDDA1P3_DES, VDDA1P3_CLOCK, VDDA1P3_TX_LO_BUFFER, and VDDA1P3_CLOCK_SYNTH.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

REFLOW PROFILE

The ADRV9008-2 reflow profile is in accordance with the JEDEC JESD204B criteria for Pb-free devices. The maximum reflow temperature is 260°C.

THERMAL MANAGEMENT

The ADRV9008-2 is a high power device that can dissipate over 3 W depending on the user application and configuration. Because of the power dissipation, the ADRV9008-2 uses an exposed die package to provide the customer with the most effective method of controlling the die temperature. The exposed die allows cooling of the die directly. Figure 5 shows the profile view of the device mounted to a user printed circuit board (PCB) and a heat sink (typically the aluminum case) to keep the junction (exposed die) below the maximum junction temperature shown in Table 3. The device is designed for a lifetime of 10 years when operating at the maximum junction temperature.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction-to-case thermal resistance.

Thermal resistance data for the ADRV9008-2 mounted on both a JEDEC 2S2P test board and a 10-layer Analog Devices, Inc., evaluation board are listed in Table 4. Do not exceed the absolute maximum junction temperature rating in Table 3. 10-layer PCB entries refer to the 10-layer Analog Devices, Inc. evaluation board, which more accurately reflects the PCB used in customer applications.

Table 4. Thermal Resistance[1, 2]

Package Type	θ_{JA}	θ_{JC_TOP}	θ_{JB}	Ψ_{JT}	Ψ_{JB}	Unit
BC-196-13	21.1	0.04	4.9	0.3	4.9	°C/W

[1] For the θ_{JC} test, 100 µm thermal interface material (TIM) is used. TIM is assumed to have 3.6 thermal conductivity watts/(meter × Kelvin).
[2] Using enhanced heat removal techniques such as PCB, heat sink, airflow, and so on, improves the thermal resistance values.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

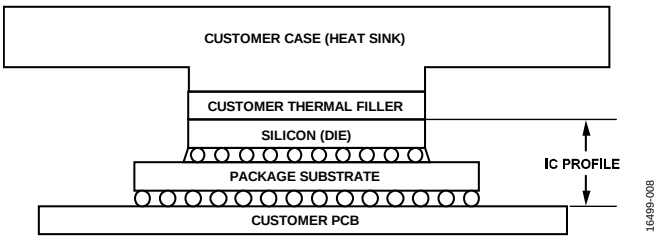


Figure 5. Typical Thermal Management Solution

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	VSSA	ORX2_IN+	ORX2_IN-	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	ORX1_IN+	ORX1_IN-	VSSA
B	VDDA1P3_ RX_RF	VSSA	VSSA	VSSA	VSSA	VSSA	RF_EXT_ LO_I/O-	RF_EXT_ LO_I/O+	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA
C	GPIO_3p3_0	GPIO_3p3_3	VDDA1P3_ RX_TX	VSSA	VDDA1P3_ RF_VCO_LDO	VDDA1P3_ RF_VCO_LDO	VDDA1P1_ RF_VCO	VDDA1P3_ RF_LO	VSSA	VDDA1P3_ AUX_VCO_ LDO	VSSA	VDDA_3P3	GPIO_3p3_9	RBIAS
D	GPIO_3p3_1	GPIO_3p3_4	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VDDA1P1_ AUX_VCO	VSSA	VSSA	GPIO_3p3_8	GPIO_3p3_10
E	GPIO_3p3_2	GPIO_3p3_5	GPIO_3p3_6	VDDA1P8_BB	VDDA1P3_BB	VSSA	REF_CLK_IN+	REF_CLK_IN-	VSSA	AUX_SYNTH_ OUT	AUXADC_3	VDDA1P8_TX	GPIO_3p3_7	GPIO_3p3_11
F	VSSA	VSSA	AUXADC_0	AUXADC_1	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	AUXADC_2	VSSA	VSSA	VSSA
G	VSSA	VSSA	VSSA	VSSA	VDDA1P3_ CLOCK_ SYNTH	VSSA	VDDA1P3_ RF_SYNTH	VDDA1P3_ AUX_SYNTH	RF_SYNTH_ VTUNE	VSSA	VSSA	VSSA	VSSA	VSSA
H	TX2_OUT-	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	GPIO_12	GPIO_11	VSSA	TX1_OUT+
J	TX2_OUT+	VSSA	GPIO_18	RESETB	GP_ INTERRUPT	TEST	GPIO_2	GPIO_1	SDIO	SDO	GPIO_13	GPIO_10	VSSA	TX1_OUT-
K	VSSA	VSSA	SYSREF_IN+	SYSREF_IN-	GPIO_5	GPIO_4	GPIO_3	GPIO_0	SCLK	CSB	GPIO_14	GPIO_9	VSSA	VSSA
L	VSSA	VSSA	SYNCINB1-	SYNCINB1+	GPIO_6	GPIO_7	VSSD	VDDD1P3_ DIG	VDDD1P3_ DIG	VSSD	GPIO_15	GPIO_8	SYNCOUTB1-	SYNCOUTB1+
M	VDDA1P1_ CLOCK_VCO	VSSA	SYNCINB0-	SYNCINB0+	ORX1_ENABLE	TX1_ENABLE	ORX2_ENABLE	TX2_ENABLE	VSSA	GPIO_17	GPIO_16	VDD_ INTERFACE	SYNCOUTB0-	SYNCOUTB0+
N	VDDA1P3_ CLOCK_VCO_LDO	VSSA	SERDOUT3-	SERDOUT3+	SERDOUT2-	SERDOUT2+	VSSA	VDDA1P3_ SER	VDDA1P3_ DES	SERDIN1-	SERDIN1+	SERDIN0-	SERDIN0+	VSSA
P	AUX_SYNTH_ VTUNE	VSSA	VSSA	SERDOUT1-	SERDOUT1+	SERDOUT0-	SERDOUT0+	VDDA1P3_ SER	VDDA1P3_ DES	VSSA	SERDIN3-	SERDIN3+	SERDIN2-	SERDIN2+

Figure 6. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Type	Mnemonic	Description
A1, A4 to A11, A14, B2 to B6, B9 to B14, C4, C9, C11, D3 to D9, D11, D12, E6, E9, F1, F2, F5 to F10, F12 to F14, G1 to G4, G6, G10 to G14, H2 to H10, H13, J2, J13, K1, K2, K13, K14, L1, L2, M2, M9, N2, N7, N14, P2, P3, P10	Input	VSSA	Analog Supply Voltage (V_{SS}).
A12	Input	ORX1_IN+	Differential Input for Observation Receiver 1. When this pin is unused, connect to GND.
A13	Input	ORX1_IN−	Differential Input for Observation Receiver 1. When this pin is unused, connect to GND.
A2	Input	ORX2_IN+	Differential Input for Observation Receiver 2. When this pin is unused, connect to GND.
A3	Input	ORX2_IN−	Differential Input for Observation Receiver 2. When this pin is unused, connect to GND.
B1	Input	VDDA1P3_RX_RF	Observation Receiver Supply.
B8	Input	RF_EXT_LO_I/O+	Differential External LO Input/Output. If this pin is used for the external LO, the input frequency must be 2× desired carrier frequency. When this pin is unused, do not connect.
B7	Input	RF_EXT_LO_I/O−	Differential External LO Input/Output. If this pin is used for the external LO, the input frequency must be 2× desired carrier

Pin No.	Type	Mnemonic	Description
			frequency. When this pin is unused, do not connect.
C1	Input/ output	GPIO_3p3_0	General-Purpose Inputs and Outputs (GPIO) Pin Referenced to 3.3 V Supply. The alternative function is AUXDAC_4. Because this pin contains an input stage, control the voltage on the pin. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration) or this pin can be left floating, programmed as outputs, and driven low.
C2	Input/ output	GPIO_3p3_3	General-Purpose Inputs and Outputs Pin Referenced to 3.3 V Supply. Because this pin contains an input stage, control the voltage on the pin. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration) or this pin can be left floating, programmed as outputs, and driven low.
C13	Input/ output	GPIO_3p3_9	General-Purpose Inputs and Outputs Pin Referenced to 3.3 V Supply. The alternative function is AUXDAC_9. Because this pin contains an input stage, control the voltage on the pin. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration) or this pin can be left floating, programmed as outputs, and driven low.
D1	Input/ output	GPIO_3p3_1	General-Purpose Inputs and Outputs Pin Referenced to 3.3 V Supply. The alternative function is AUXDAC_5. Because this pin contains an input stage, control the voltage on the pin. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration) or this pin can be left floating, programmed as outputs, and driven low.
D2	Input/ output	GPIO_3p3_4	General-Purpose Inputs and Outputs Pin Referenced to 3.3 V Supply. The alternative function is AUXDAC_6. Because this pin contains an input stage, control the voltage on the pin. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration) or this pin can be left floating, programmed as outputs, and driven low.
D13	Input/ output	GPIO_3p3_8	General-Purpose Inputs and Outputs Pin Referenced to 3.3 V Supply. The alternative function is AUXDAC_1. Because this pin contains an input stage, control the voltage on the pin. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration) or this pin can be left floating, programmed as outputs, and driven low.
D14	Input/ output	GPIO_3p3_10	General-Purpose Inputs and Outputs Pin Referenced to 3.3 V Supply. The alternative function is AUXDAC_0. Because this pin contains an input stage, control the voltage on the pin. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration) or this pin can be left floating, programmed as outputs, and driven low.
E1	Input/ output	GPIO_3p3_2	General-Purpose Inputs and Outputs Pin Referenced to 3.3 V Supply. Because this pin contains an input stage, control the voltage on the pin. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration) or this pin can be left floating, programmed as outputs, and driven low.
E2	Input/ output	GPIO_3p3_5	General-Purpose Inputs and Outputs Pin Referenced to 3.3 V Supply. The alternative function is AUXDAC_7. Because this pin contains an input stage, control the voltage on the pin. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration) or this pin can be left floating, programmed as outputs, and driven low.
E3	Input/ output	GPIO_3p3_6	General-Purpose Inputs and Outputs Pin Referenced to 3.3 V Supply. The alternative function is AUXDAC_8. Because this pin contains an input stage, control the voltage on the pin. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration) or this pin can be left floating, programmed as outputs, and driven low.

Pin No.	Type	Mnemonic	Description
E13	Input/ output	GPIO_3p3_7	General-Purpose Inputs and Outputs Pin Referenced to 3.3 V Supply. The alternative function is AUXDAC_2. Because this pin contains an input stage, control the voltage on the pin. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration) or this pin can be left floating, programmed as outputs, and driven low.
E14	Input/ output	GPIO_3p3_11	General-Purpose Inputs and Outputs Pin Referenced to 3.3 V Supply. The alternative function is AUXDAC_3. Because this pin contains an input stage, control the voltage on the pin. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration) or this pin can be left floating, programmed as outputs, and driven low.
C10	Input	VDDA1P3_AUX_VCO_LDO	1.3 V Supply.
C12	Input	VDDA_3P3	General-Purpose Output Pull-Up Voltage and Auxiliary DAC Supply Voltage.
C14	Input/ output	RBIAS	Bias Resistor. Tie this pin to ground using a 14.3 kΩ resistor. This pin generates an internal current based on an external 1% resistor.
C3	Input	VDDA1P3_RX_TX	1.3 V supply for transmitter/receiver baseband circuits. TIA/TX GM/BB FILTERS/AUXDACs.
C5, C6	Input	VDDA1P3_RF_VCO_LDO	RF VCO LDO Supply Inputs. Connect Pin C5 and Pin C6. Then separate trace to common supply point.
C7	Input	VDDA1P1_RF_VCO	1.1 V VCO Supply. Decouple this pin with a 1 µF capacitor.
C8	Input	VDDA1P3_RF_LO	1.3 V LO Generator for RF Synthesizer. This pin is sensitive to supply noise.
D10	Input	VDDA1P1_AUX_VCO	1.1 V VCO Supply. Decouple this pin with 1 µF capacitor.
E10	Output	AUX_SYNTH_OUT	AUX PLL Output. When this pin is unused, do not connect.
E12	Input	VDDA1P8_TX	1.8 V Supply for transmitter.
E4	Input	VDDA1P8_BB	1.8 V Supply for ADC and DAC.
E5	Input	VDDA1P3_BB	1.3 V Supply for ADC, DAC, and AUXADC.
E7	Input	REF_CLK_IN+	Device Clock Differential Input.
E8	Input	REF_CLK_IN−	Device Clock Differential Input Negative.
F3, F4, F11, E11	Input	AUXADC_0 through AUXADC_3	Auxiliary ADC Input. When this pin is unused, connect to GND with a pull down resistor or directly to GND.
G5	Input	VDDA1P3_CLOCK_SYNTH	1.3 V Supply Input for Clock Synthesizer. Use a separate trace on the PCB back to a common supply point.
G7	Input	VDDA1P3_RF_SYNTH	1.3 V RF Synthesizer Supply Input. This pin is very sensitive to aggressors.
G8	Input	VDDA1P3_AUX_SYNTH	1.3 V AUX Synthesizer Supply Input.
G9	Output	RF_SYNTH_VTUNE	RF Synthesizer PLL Output Voltage Level (VTUNE) Output.
H11	Input/ output	GPIO_12	Digital GPIO, 1.8 V to 2.5 V. Because this pin contains an input stage, control the voltage on the pin. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration) or the pin can be left floating, programmed as outputs and driven low.
H12	Input/ output	GPIO_11	Digital GPIO, 1.8 V to 2.5 V. Because this pin contains an input stage, control the voltage on the pin. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration) or the pin can be left floating, programmed as outputs and driven low.
J11	Input/ output	GPIO_13	Digital GPIO, 1.8 V to 2.5 V. Because this pin contains an input stage, control the voltage on the pin. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration) or the pin can be left floating, programmed as outputs and driven low.

Pin No.	Type	Mnemonic	Description
J12	Input/ output	GPIO_10	Digital GPIO, 1.8 V to 2.5 V. Because this pin contains an input stage, control the voltage on the pin. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration) or the pin can be left floating, programmed as outputs and driven low.
J3	Input/ output	GPIO_18	Digital GPIO, 1.8 V to 2.5 V. The JTAG function is TCLK. Because this pin contains an input stage, control the voltage on the pin. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration) or the pin can be left floating, programmed as outputs and driven low.
J7	Input/ output	GPIO_2	Digital GPIO, 1.8 V to 2.5 V. The user sets the JTAG function to 0. Because this pin contains an input stage, control the voltage on the pin. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration) or the pin can be left floating, programmed as outputs and driven low.
J8	Input/ output	GPIO_1	Digital GPIO, 1.8 V to 2.5 V. The user sets the JTAG function to 0. Because this pin contains an input stage, control the voltage on the pin. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration) or the pin can be left floating, programmed as outputs and driven low.
K5	Input/ output	GPIO_5	Digital GPIO, 1.8 V to 2.5 V. The JTAG function is TDO. Because this pin contains an input stage, control the voltage on the pin. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration) or the pin can be left floating, programmed as outputs and driven low.
K6	Input/ output	GPIO_4	Digital GPIO, 1.8 V to 2.5 V. The JTAG function is $\overline{\text{TRST}}$. Because this pin contains an input stage, control the voltage on the pin. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration) or the pin can be left floating, programmed as outputs and driven low.
K7	Input/ output	GPIO_3	Digital GPIO, 1.8 V to 2.5 V. The user sets the JTAG function to 1. Because this pin contains an input stage, control the voltage on the pin. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration) or the pin can be left floating, programmed as outputs and driven low.
K8	Input/ output	GPIO_0	Digital GPIO, 1.8 V to 2.5 V. The user sets the JTAG function to 1. Because this pin contains an input stage, control the voltage on the pin. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration) or the pin can be left floating, programmed as outputs and driven low.
K11	Input/ output	GPIO_14	Digital GPIO, 1.8 V– 2.5 V. Because this pin contains an input stage, control the voltage on the pin. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration) or the pin can be left floating, programmed as outputs and driven low.
K12	Input/ output	GPIO_9	Digital GPIO, 1.8 V to 2.5 V. Because this pin contains an input stage, control the voltage on the pin. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration) or the pin can be left floating, programmed as outputs and driven low.
L5	Input/ output	GPIO_6	Digital GPIO, 1.8 V to 2.5 V. The JTAG function is TDI. Because this pin contains an input stage, control the voltage on the pin. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration) or the pin can be left floating, programmed as outputs and driven low.
L6	Input/ output	GPIO_7	Digital GPIO, 1.8 V to 2.5 V. The JTAG function is TMS. Because this pin contains an input stage, control the voltage on the pin. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration) or the pin can be left floating, programmed as outputs and driven low.

Pin No.	Type	Mnemonic	Description
L11	Input/ output	GPIO_15	Digital GPIO, 1.8 V to 2.5 V. Because this pin contains an input stage, control the voltage on the pin. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration) or the pin can be left floating, programmed as outputs and driven low.
L12	Input/ output	GPIO_8	Digital GPIO, 1.8 V to 2.5 V. Because this pin contains an input stage, control the voltage on the pin. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration) or the pin can be left floating, programmed as outputs and driven low.
M10	Input/ output	GPIO_17	Digital GPIO, 1.8 V to 2.5 V. Because this pin contains an input stage, control the voltage on the pin. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration) or the pin can be left floating, programmed as outputs and driven low.
M11	Input/ output	GPIO_16	Digital GPIO, 1.8 V to 2.5 V. Because this pin contains an input stage, control the voltage on the pin. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration) or the pin can be left floating, programmed as outputs and driven low.
H14	Output	TX1_OUT+,	Transmitter 1 Positive Output. When unused, do not connect this pin.
J14	Output	TX1_OUT–	Transmitter 1 Negative Output. When unused, do not connect this pin.
J1	Output	TX2_OUT+	Transmitter 2 Positive Output. When unused, do not connect this pin.
H1	Output	TX2_OUT–	Transmitter 2 Negative Output. When unused, do not connect this pin.
J10	Output	SDO	Serial Data Output. In SPI 3-wire mode, do not connect this pin.
J4	Input	$\overline{\text{RESET}}$	Active Low Chip Reset.
J5	Output	GP_INTERRUPT	General-Purpose Digital Interrupt Output Signal. When unused, do not connect this pin.
J6	Input	TEST	Pin Used for JTAG Boundary Scan. When unused, connect this pin to GND.
J9	Input/ output	SDIO	Serial Data Input in 4-Wire Mode or Input/Output in 3-Wire Mode.
K10	Input	CSB	Serial Data Bus Chip Select, Active Low.
K3	Input	SYSREF_IN+	LVDS Input.
K4	Input	SYSREF_IN–	LVDS Input.
K9	Input	SCLK	Serial Data Bus Clock.
L14	Output	$\overline{\text{SYNCOUT1+}}$	LVDS Output. When unused, do not connect this pin.
L13	Output	$\overline{\text{SYNCOUT1–}}$	LVDS Output. When unused, do not connect this pin.
L4	Input	$\overline{\text{SYNCIN1+}}$	LVDS Input. When unused, connect this pin to GND with a pull-down resistor or directly to GND.
L3	Input	$\overline{\text{SYNCIN1–}}$	LVDS Input. When unused, connect this pin to GND with a pull-down resistor or directly to GND.
L7, L10	Input	VSSD	Digital Supply.
L8, L9	Input	VDDD1P3_DIG	1.3 V Digital Core. Connect L8 and L9 separate trace to common supply point.
M1	Input	VDDA1P1_CLOCK_VCO	1.1 V VCO supply, decouple with 1 µF.
M12	Input	VDD_INTERFACE	Input/Output Interface Supply, 1.8 V to 2.5 V.
M14	Output	$\overline{\text{SYNCOUT0+}}$	JESD204B Transmitter Channel Data Link LVDS Output. This pin forms the sync signal associated with transmitter channel data on the JESD204B interface. When unused, do not connect this pin.
M13	Output	$\overline{\text{SYNCOUT0–}}$	JESD204B Transmitter Channel Data Link LVDS Output. This pin forms the sync signal associated with transmitter channel data on the JESD204B interface. When unused, do not connect this pin.

Pin No.	Type	Mnemonic	Description
M4	Input	SYNCIN0+	JESD204B Receiver Channel 1 Data Link LVDS Input. This pin forms the sync signal associated with receiver channel data on the JESD204B interface. When unused, connect this pin to GND with a pull-down resistor or directly to GND.
M3	Input	SYNCIN0–	JESD204B Receiver Channel 1 Data Link LVDS Input. This pin forms the sync signal associated with receiver channel data on the JESD204B interface. When unused, connect this pin to GND with a pull-down resistor or directly to GND.
M5	Input	ORX1_ENABLE	Observation Receiver 1 Enable Pin. When unused, connect this pin to GND with a pull-down resistor or directly to GND.
M6	Input	TX1_ENABLE	Transmitter 1 Enable Pin. When unused, connect this pin to GND with a pull-down resistor or directly to GND.
M7	Input	ORX2_ENABLE	Observation Receiver 2 Enable Pin. When unused, connect this pin to GND with a pull-down resistor or directly to GND.
M8	Input	TX2_ENABLE	Transmitter 2 Enable Pin. When unused, connect this pin to GND with a pull-down resistor or directly to GND.
N1	Input	VDDA1P3_CLOCK_VCO_LDO	1.3 V Separate Trace to Common Supply Point.
N4	Output	SERDOUT3+	RF Current Mode Logic (CML) Differential Output 3. When unused, do not connect this pin.
N3	Output	SERDOUT3–	RF CML Differential Output 3. When unused, do not connect this pin.
N6	Output	SERDOUT2+	RF CML Differential Output 2. When unused, do not connect this pin.
N5	Output	SERDOUT2–	RF CML Differential Output 2. When unused, do not connect this pin.
N11	Input	SERDIN1+	RF CML Differential Input 1. When unused, do not connect this pin.
N10	Input	SERDIN1–	RF CML Differential Input 1. When unused, do not connect this pin.
N13	Input	SERDIN0+	RF CML Differential Input 0. When unused, do not connect this pin.
N12	Input	SERDIN0–	RF CML Differential Input 0. When unused, do not connect this pin.
N8, P8	Input	VDDA1P3_SER	1.3 V Supply for JESD204B Serializer.
N9, P9	Input	VDDA1P3_DES	1.3 V Supply for JESD204B Deserializer.
P1	Output	AUX_SYNTH_VTUNE	Auxiliary Synthesizer VTUNE Output.
P5	Output	SERDOUT1+	RF CML Differential Output 1. When unused, do not connect this pin.
P4	Output	SERDOUT1–	RF CML Differential Output 1. When unused, do not connect this pin.
P7	Output	SERDOUT0+	RF CML Differential Output 0. When unused, do not connect this pin.
P6	Output	SERDOUT0–	RF CML Differential Output 0. When unused, do not connect this pin.
P12	Input	SERDIN3+	RF CML Differential Input 3. When unused, do not connect this pin.
P11	Input	SERDIN3–	RF CML Differential Input 3. When unused, do not connect this pin.
P14	Input	SERDIN2+	RF CML Differential Input 2. When unused, do not connect this pin.
P13	Input	SERDIN2–	RF CML Differential Input 2. When unused, do not connect this pin.

TYPICAL PERFORMANCE CHARACTERISTICS

The temperature settings refer to the die temperature

75 MHz TO 525 MHz BAND

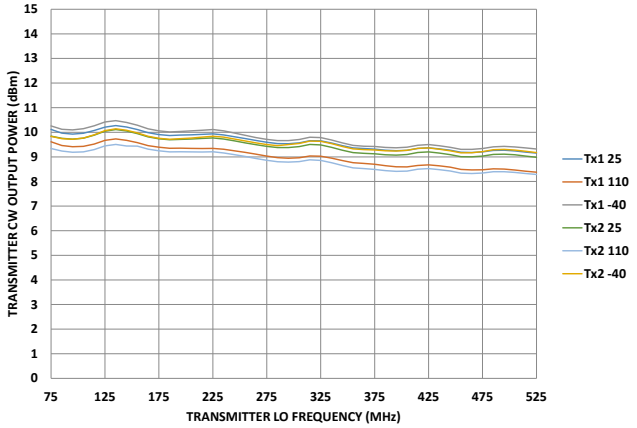


Figure 7. Transmitter Continuous Wave Output Power vs. Transmitter LO Frequency, Transmitter QEC and External LO Leakage Active, Transmitter 50 MHz/100 MHz Bandwidth Mode, IQ Rate = 122.88 MHz, Attenuation = 0 dB, Not De-Embedded

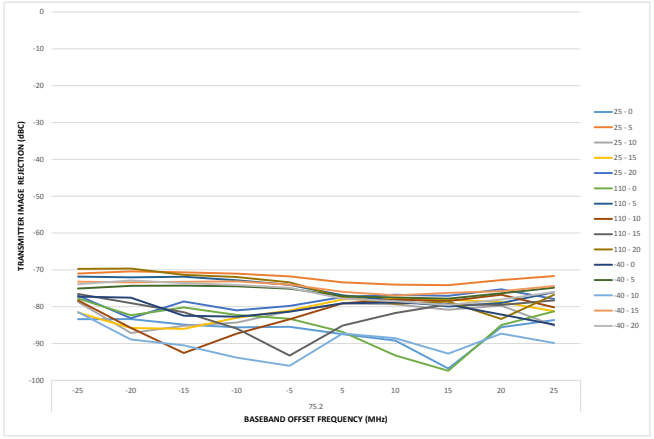


Figure 8. Transmitter Image Rejection Across Large Signal Bandwidth vs. Baseband Offset Frequency and Transmitter Attenuation, QEC Trained with Three Tones Placed at 10 MHz, 48 MHz, and 100 MHz (Tracking On), Total Combined Power = −10 dBFS. Correction Then Frozen (Tracking Turned Off), Continuous Wave Tone Swept Across Large Signal Bandwidth, LO = 75 MHz

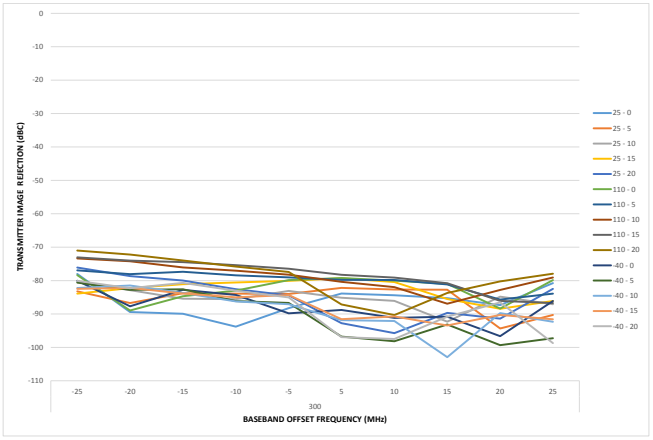


Figure 9. Transmitter Image Rejection Across Large Signal Bandwidth vs. Baseband Offset Frequency and Transmitter Attenuation, QEC Trained with Three Tones Placed at 10 MHz, 48 MHz, and 100 MHz (Tracking On), Total Combined Power = −10 dBFS, Correction Then Frozen (Tracking Turned Off), Continuous Wave Tone Swept Across Large Signal Bandwidth, LO = 300 MHz

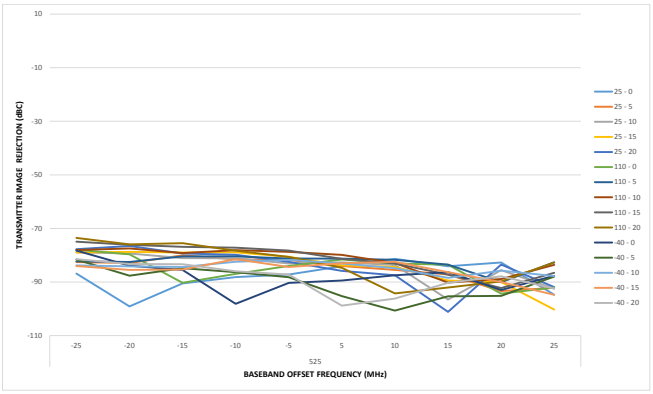


Figure 10. Transmitter Image Rejection Across Large Signal Bandwidth vs. Baseband Offset Frequency and Transmitter Attenuation, QEC Trained with Three Tones Placed at 10 MHz, 48 MHz, and 100 MHz (Tracking On), Total Combined Power = −10 dBFS, Correction Then Frozen (Tracking Turned Off), Continuous Wave Tone Swept Across Large Signal Bandwidth, LO = 525 MHz

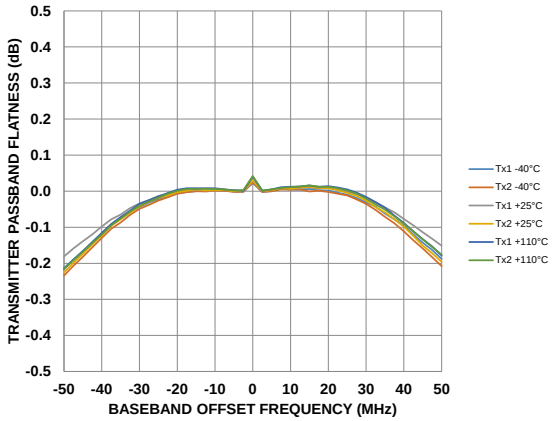


Figure 11. Transmitter Passband Flatness vs. Baseband Offset Frequency, Off Chip Match Response De-Embedded, LO = 300 MHz, Calibrated at 25°C

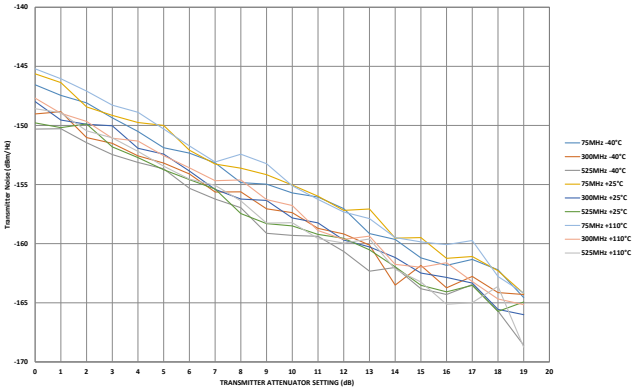


Figure 14. Transmitter Noise vs. Transmitter Attenuation Setting, 50 MHz Offset

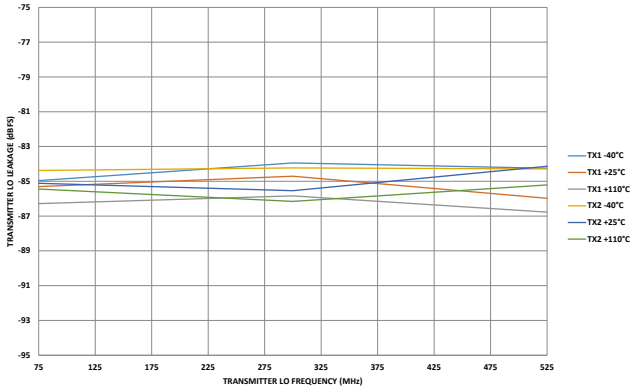


Figure 12. Transmitter LO Leakage vs. Transmitter LO Frequency, Transmitter Attenuation = 0 dB, Baseband Tone Frequency = 10 MHz, Tracked

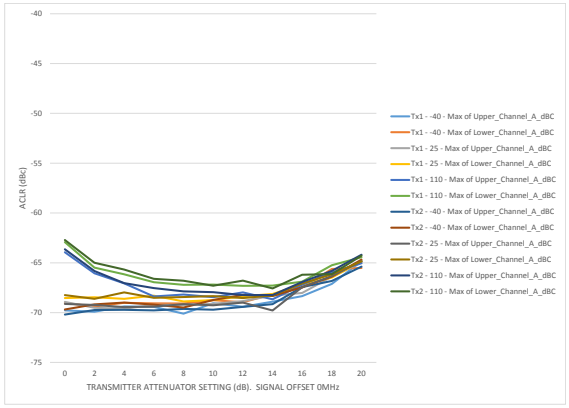


Figure 15. Transmitter Adjacent Channel Leakage Ratio vs. Transmitter Attenuation Setting, LO = 75 MHz, LTE 20 MHz Peak to Average Ratio (PAR) = 12 dB, DAC Boost Normal, Upper Side and Lower Side, Performance Limited by Spectrum Analyzer at Higher Attenuation Settings

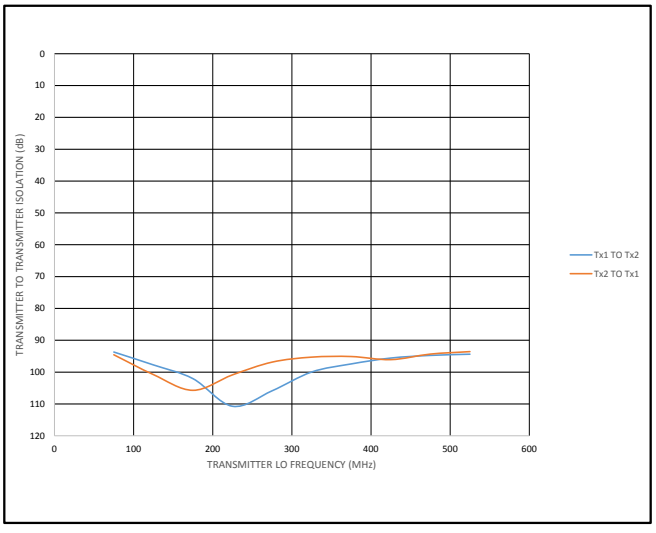


Figure 13. Transmitter to Transmitter Isolation vs. Transmitter LO Frequency, Temperature: 25°C

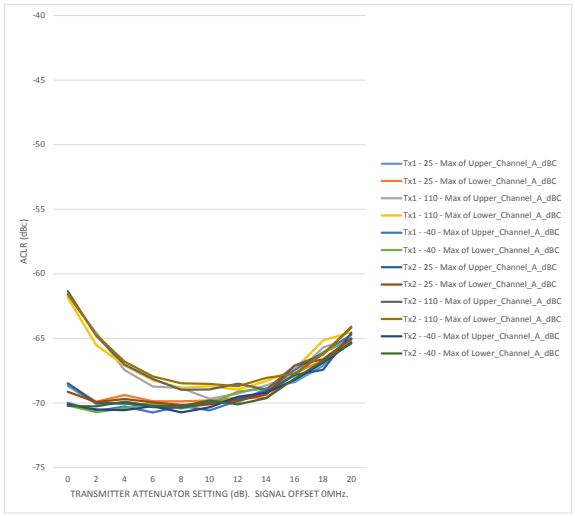


Figure 16. Transmitter Adjacent Channel Leakage Ratio vs. Transmitter Attenuation Setting, LO = 300 MHz, LTE 20 MHz PAR = 12 dB, DAC Boost Normal, Upper Side and Lower Side, Performance Limited by Spectrum Analyzer at Higher Attenuation Settings

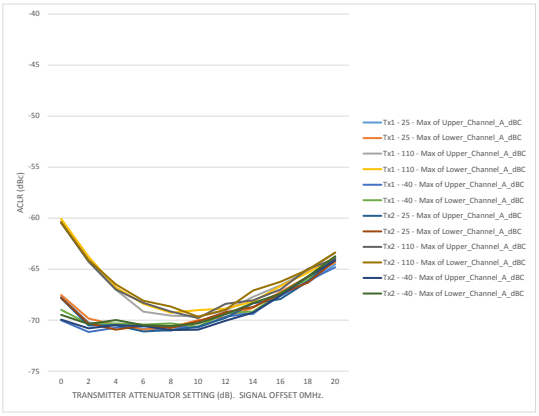


Figure 17. Transmitter Adjacent Channel Leakage Ratio vs. Transmitter Attenuation Setting, LO = 525 MHz, LTE 20 MHz PAR = 12 dB, DAC Boost Normal, Upper Side and Lower Side, Performance Limited by Spectrum Analyzer at Higher Attenuation Settings

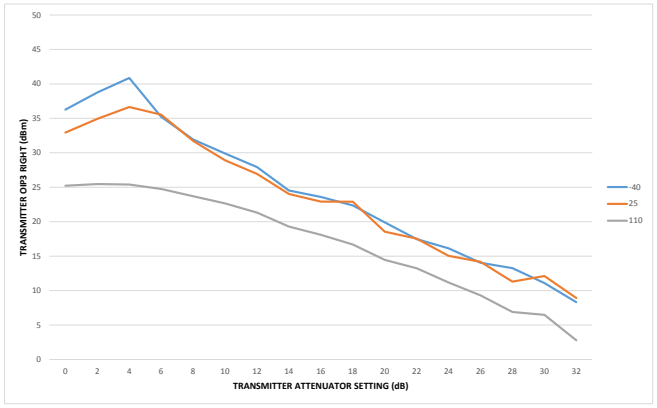


Figure 20. Transmitter OIP3 Right vs. Transmitter Attenuation Setting, LO = 525 MHz, Total RMS Power = −12 dBFS, 20 MHz/25 MHz Tones

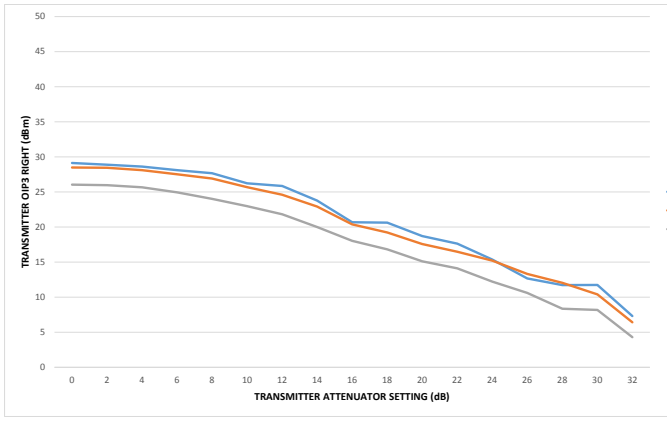


Figure 18. Transmitter OIP3 Right vs. Transmitter Attenuation Setting, LO = 75 MHz, Total Root Mean Square (RMS) Power = −12 dBFS, 20 MHz/25 MHz Tones

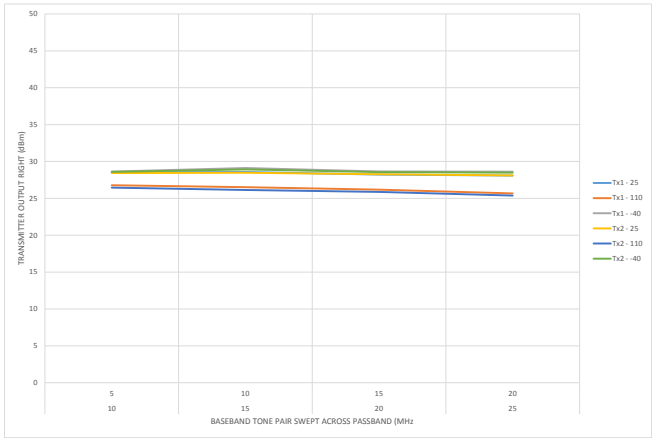


Figure 21. Transmitter OIP3 Right vs. Baseband Tone Pair Swept Across Passband, LO = 75 MHz, Total RMS Power = −12 dBFS, 4 dB Transmitter Attenuation

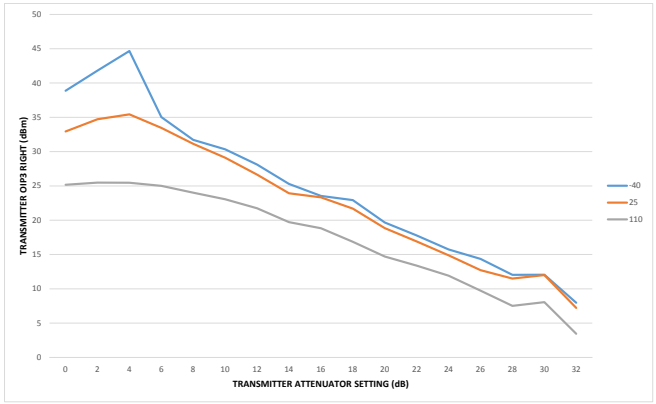


Figure 19. Transmitter OIP3 Right vs. Transmitter Attenuation Setting, LO = 300 MHz, Total RMS Power = −12 dBFS, 20 MHz/25 MHz Tones

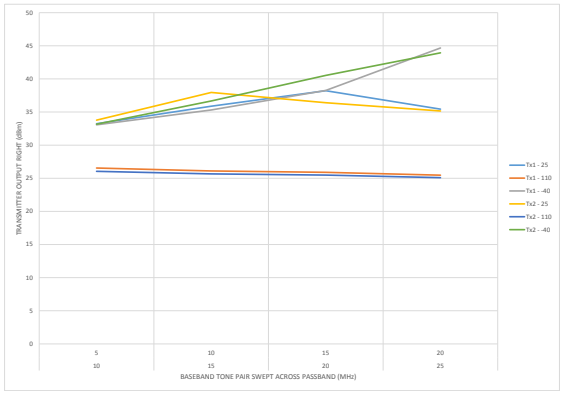


Figure 22. Transmitter OIP3 Right vs. Baseband Frequency Offset, LO = 300 MHz, Total RMS Power = −12 dBFS, 4 dB Transmitter Attenuation

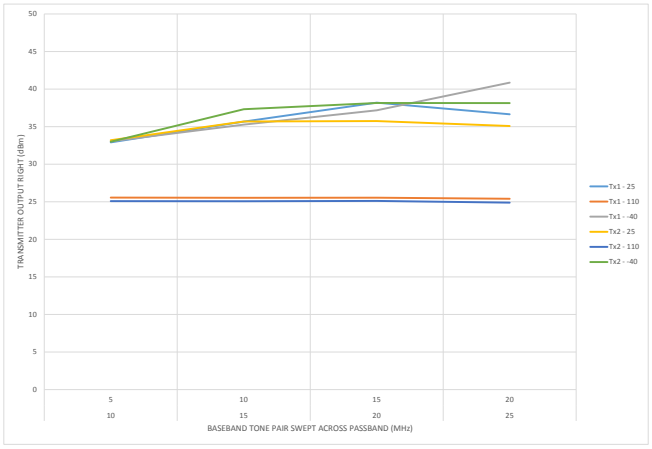


Figure 23. Transmitter OIP3 Right vs. Baseband Frequency Offset, LO = 525 MHz, Total RMS Power = −12 dBFS, 4 dB Transmitter Attenuation

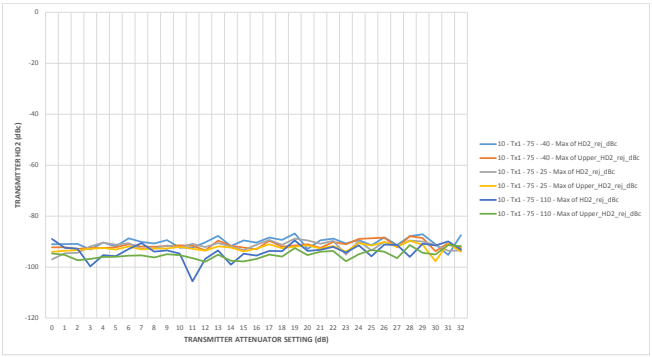


Figure 24. Transmitter HD2 vs. Transmitter Attenuation Setting, Baseband Frequency = 10 MHz, LO = 75 MHz, Continuous Wave = −15 dBFS

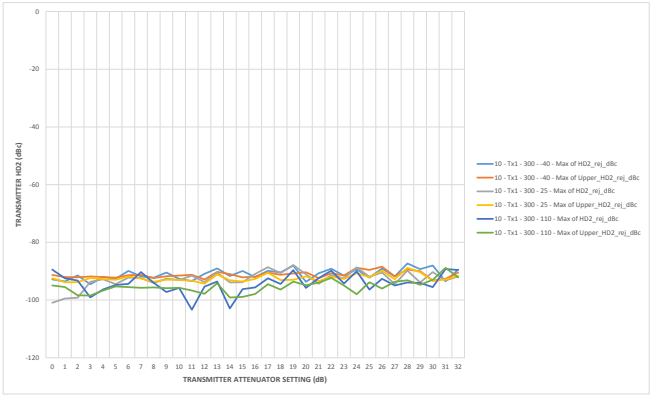


Figure 25. Transmitter HD2 vs. Transmitter Attenuation Setting, Baseband Frequency = 10 MHz, LO = 300 MHz, Continuous Wave = −15 dBFS

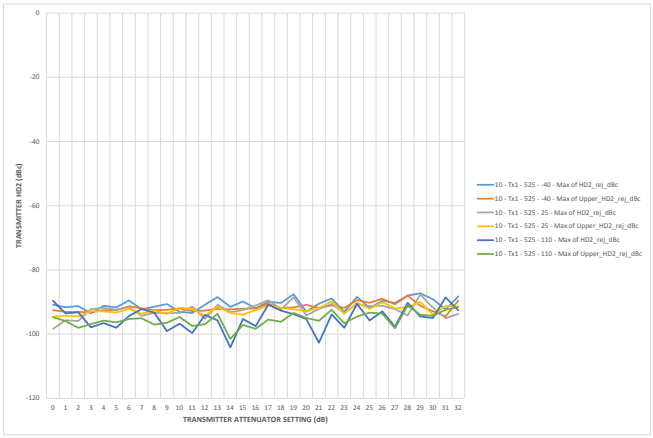


Figure 26. Transmitter HD2 vs. Transmitter Attenuation Setting, Baseband Frequency = 10 MHz, LO = 525 MHz, Continuous Wave = −15 dBFS

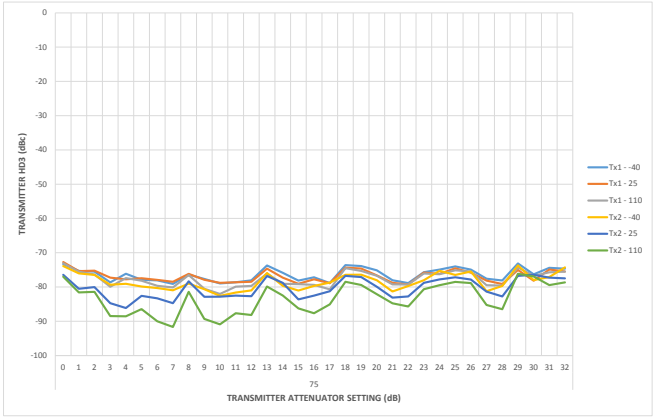


Figure 27. Transmitter HD3 vs. Transmitter Attenuation Setting, LO = 75 MHz, Continuous Wave = −15 dBFS, Baseband Frequency = 10 MHz

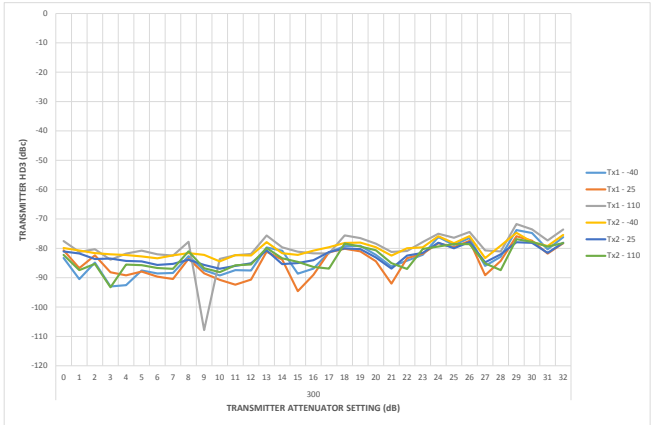


Figure 28. Transmitter HD3 vs. Transmitter Attenuation Setting, LO = 300 MHz, Continuous Wave = −15 dBFS, Baseband Frequency = 10 MHz

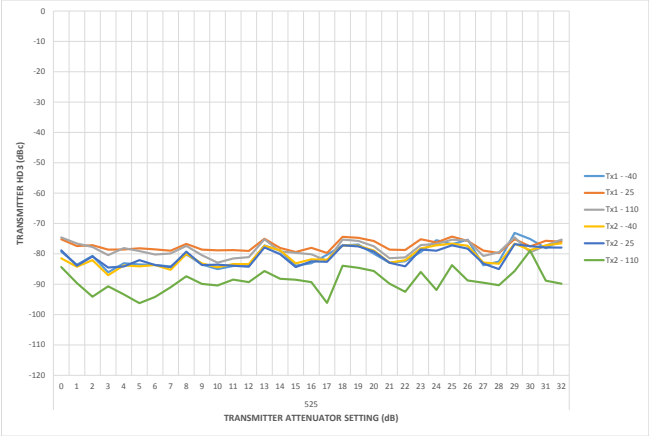


Figure 29. Transmitter HD3 vs. Transmitter Attenuation Setting, LO = 525 MHz, Continuous Wave = −15 dBFS, Baseband Frequency = 10 MHz

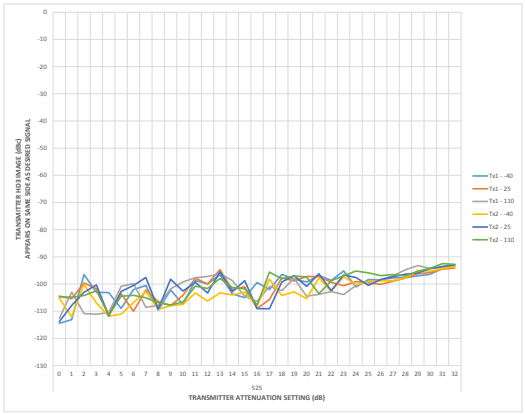


Figure 32. Transmitter HD3 Image Appears on Same Side as Desired Signal vs. Transmitter Attenuation Setting, LO = 525 MHz, Continuous Wave = −15 dBFS

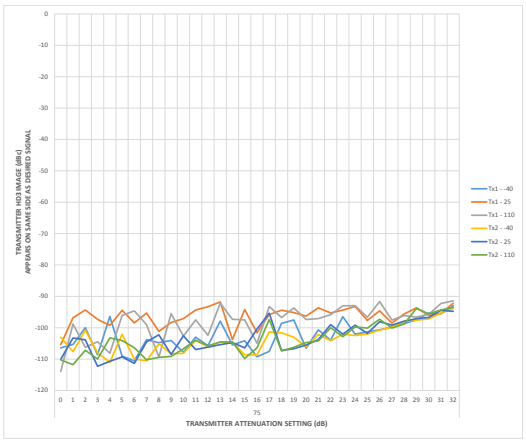


Figure 30. Transmitter HD3 Image Appears on Same Side as Desired Signal vs. Transmitter Attenuation Setting, LO = 75 MHz, Continuous Wave = −15 dBFS

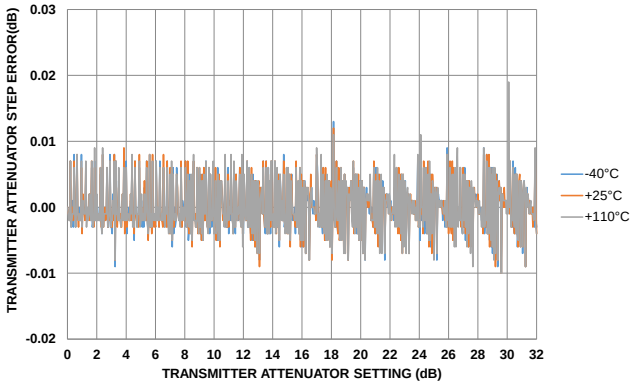


Figure 33. Transmitter Attenuator Step Error vs. Transmitter Attenuation Setting, LO = 75 MHz, Baseband Frequency = 10 MHz, Backoff = 15 dBFS

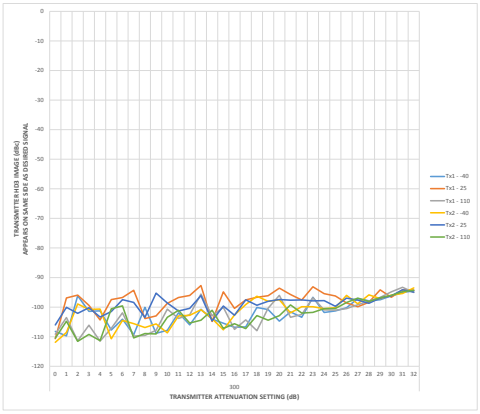


Figure 31. Transmitter HD3 Image Appears on Same Side as Desired Signal vs. Transmitter Attenuation Setting, LO = 300 MHz, Continuous Wave = −15 dBFS

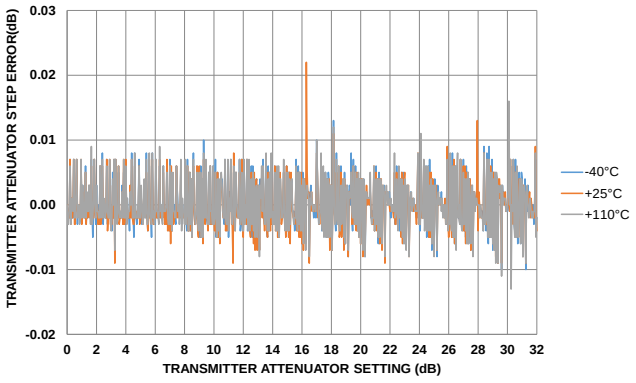


Figure 34. Transmitter Attenuator Step Error vs. Transmitter Attenuation Setting, LO = 300 MHz, Baseband Frequency = 10 MHz, Backoff = 15 dBFS

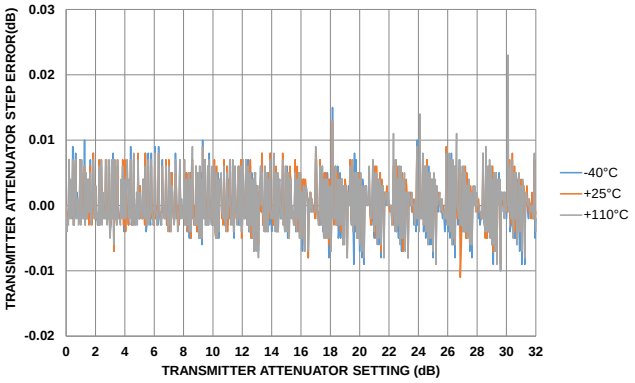


Figure 35. Transmitter Attenuator Step Error vs. Transmitter Attenuation Setting, LO = 525 MHz, Baseband Frequency = 10 MHz, Backoff = 15 dBFS

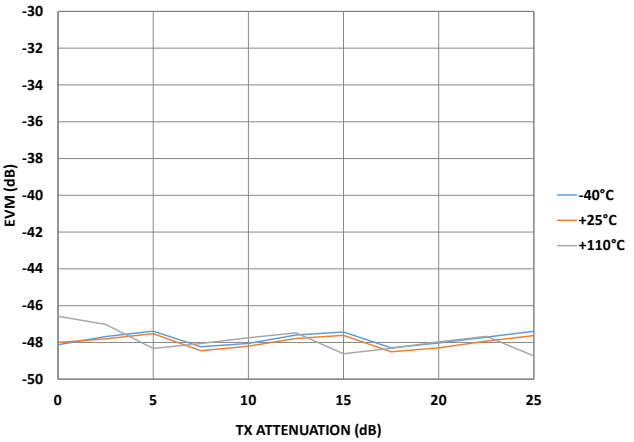


Figure 38. Transmitter EVM vs. Transmitter Attenuation, 20 MHz LTE Signal Centered on DC, LO = 525 MHz

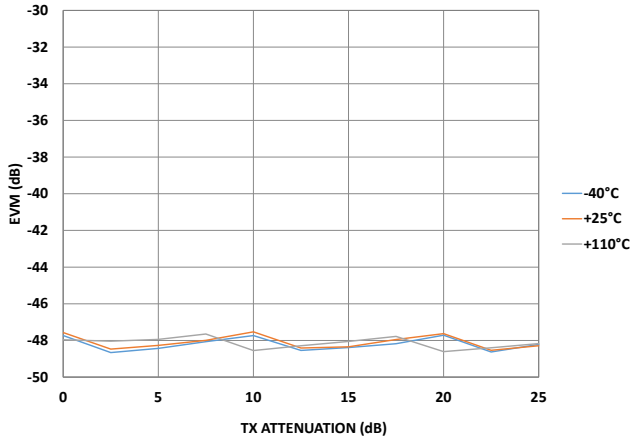


Figure 36. Transmitter EVM vs. Transmitter Attenuation, 20 MHz LTE Signal Centered on DC, LO = 75 MHz

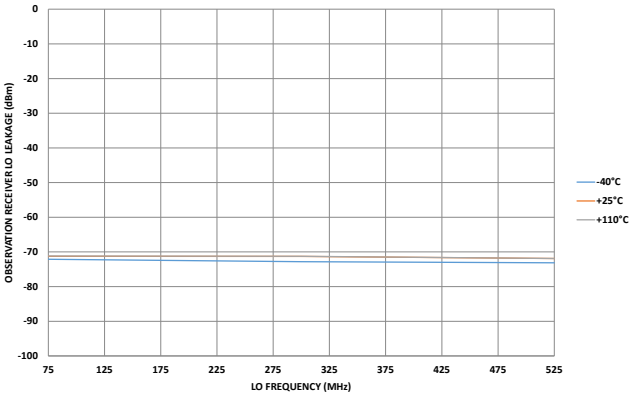


Figure 39. Observation Receiver LO Leakage vs. LO Frequency, 75 MHz, 300 MHz, 525 MHz, Attenuation = 0 dB

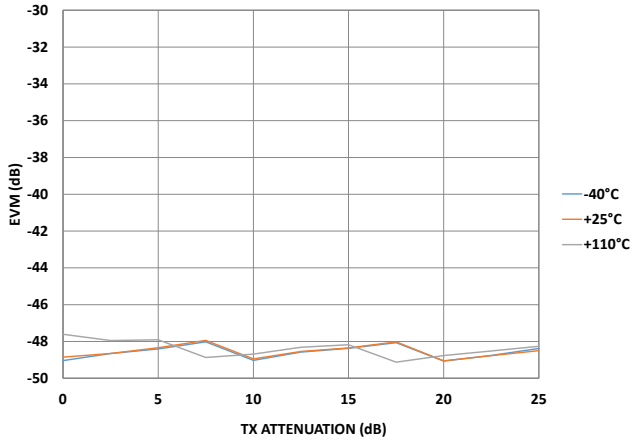


Figure 37. Transmitter EVM vs. Transmitter Attenuation, 20 MHz LTE Signal Centered on DC, LO = 300 MHz

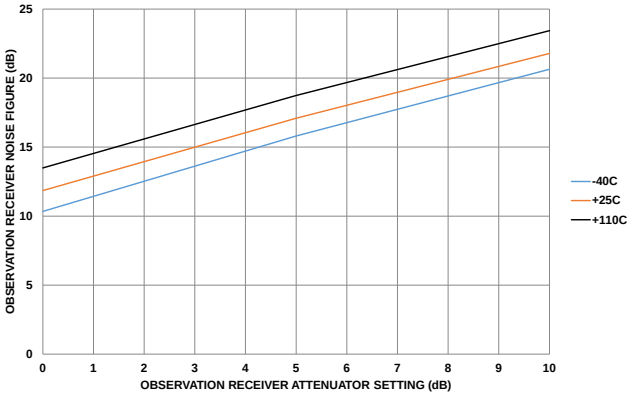


Figure 40. Observation Receiver Noise Figure vs. Observation Receiver Attenuator Setting, LO = 75 MHz, Total Nyquist Integration Bandwidth

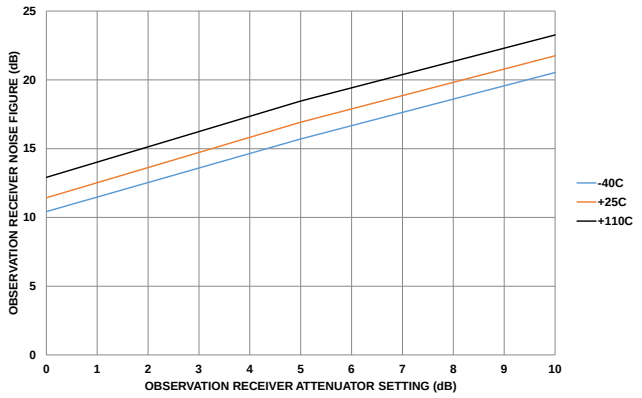


Figure 41. Observation Receiver Noise Figure vs. Observation Receiver Attenuator Setting, LO = 300 MHz, Total Nyquist Integration Bandwidth

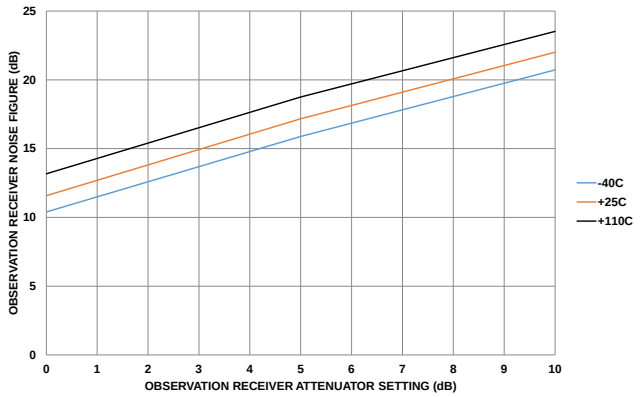


Figure 42. Observation Receiver Noise Figure vs. Observation Receiver Attenuator Setting, LO = 525 MHz, Total Nyquist Integration Bandwidth

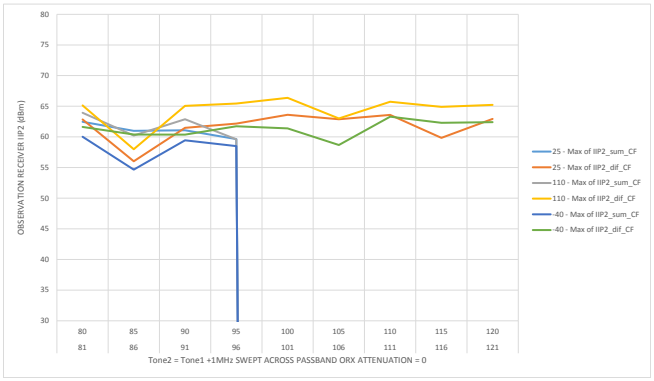


Figure 43. Observation Receiver IIP2, Sum and Difference Products vs. f1 Offset Frequency, Tones Separated by 1 MHz Swept Across Passband at −25 dBm Each, LO = 75 MHz, Attenuation = 0 dB

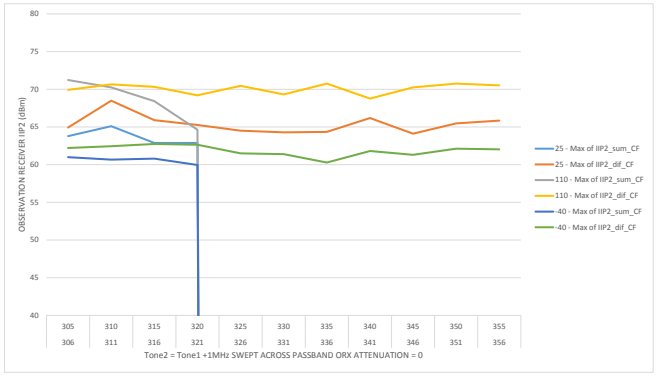


Figure 44. Observation Receiver IIP2, Sum and Difference Products vs. f1 Offset Frequency, Tones Separated by 1 MHz Swept Across Passband at −25 dBm Each, LO = 300 MHz, Attenuation = 0 dB

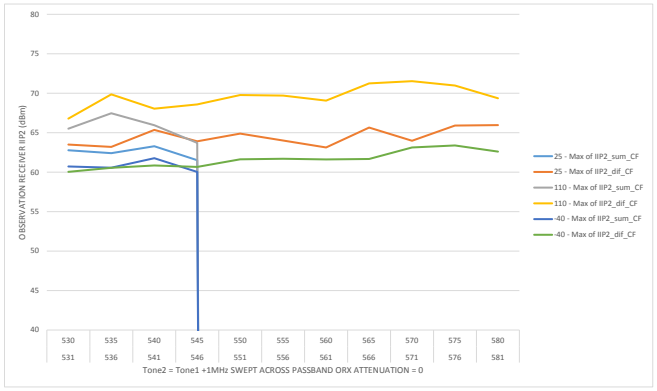


Figure 45. Observation Receiver IIP2, Sum and Difference Products vs. f1 Offset Frequency, Tones Separated by 1 MHz Swept Across Passband at −25 dBm Each, LO = 525 MHz, Attenuation = 0 dB

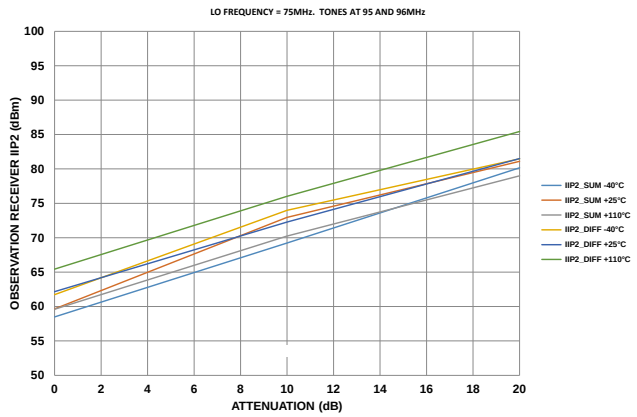


Figure 46. Observation Receiver IIP2, Sum and Difference Products vs. Attenuation, LO = 75 MHz, Tone 1 = 95 MHz, Tone 2 = 96 MHz at −25 dBm Plus Attenuation

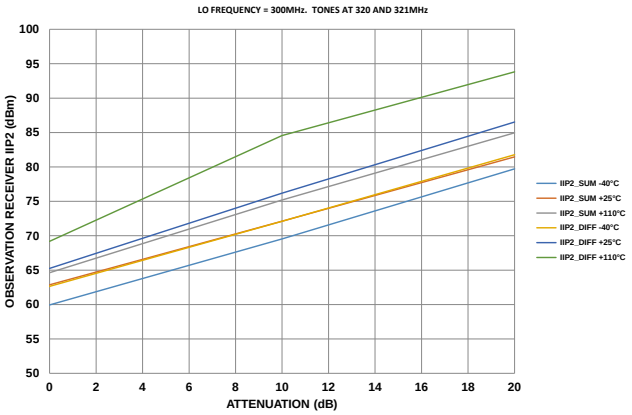


Figure 47. Observation Receiver IIP2, Sum and Difference Products vs. Attenuation, LO = 300 MHz, Tone 1 = 320 MHz, Tone 2 = 321 MHz at −25 dBm Plus Attenuation

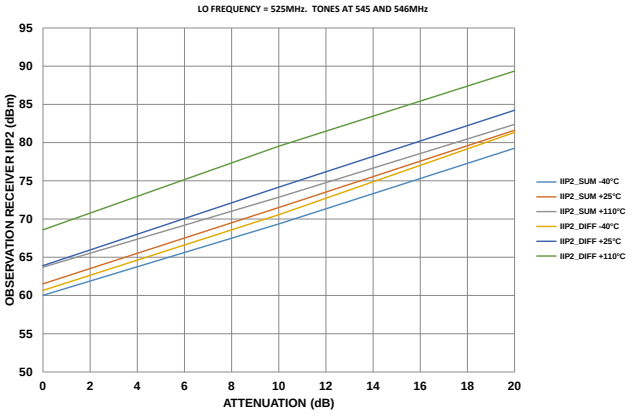


Figure 48. Observation Receiver IIP2, Sum and Difference Products vs. Attenuation, LO = 525 MHz, Tone 1 = 545 MHz, Tone 2 = 546 MHz at −25 dBm Plus Attenuation

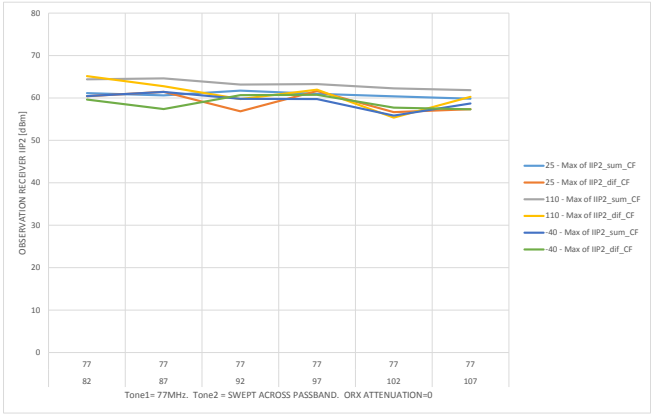


Figure 49. Observation Receiver IIP2, f1 to f2 vs. Intermod Frequency, LO = 75 MHz, Tone 1 = 77 MHz, Tone 2 = Swept, −25 dBm Each, Attenuation = 0 dB

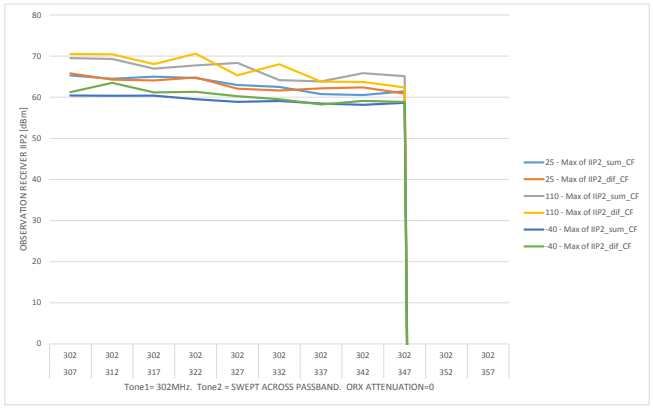


Figure 50. Observation Receiver IIP2, f1 to f2 vs. Intermod Frequency, LO = 300 MHz, Tone 1 = 302 MHz, Tone 2 = Swept, −25 dBm Each, Attenuation = 0 dB

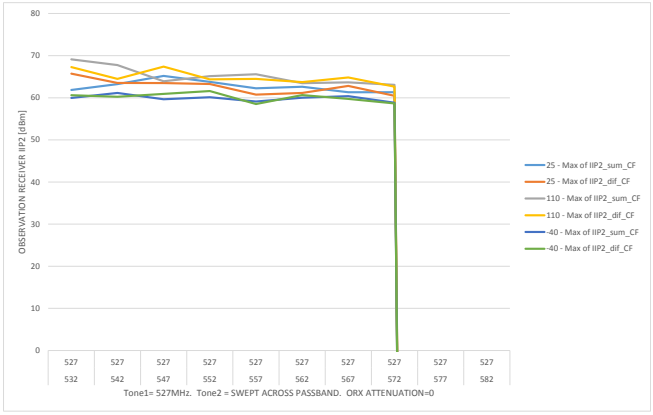


Figure 51. Observation Receiver IIP2, f1 to f2 vs. Intermod Frequency, LO = 525 MHz, Tone 1 = 527 MHz, Tone 2 = Swept, −25 dBm Each, Attenuation = 0 dB

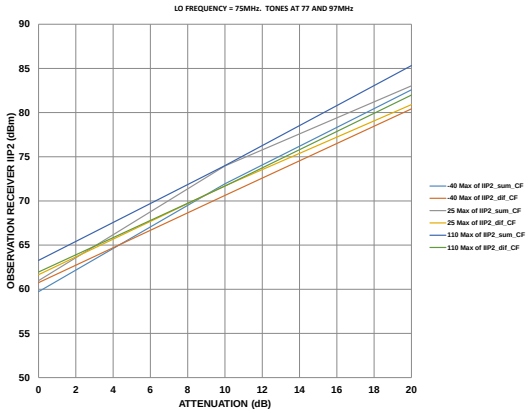


Figure 52. Observation Receiver IIP2, f1 to f2 vs. Attenuation, LO = 75 MHz, Tone 1 = 77 MHz, Tone 2 = 97 MHz at −25 dBm Plus Attenuation

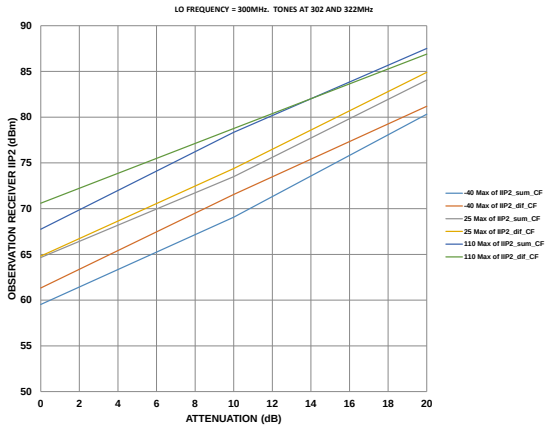


Figure 53. Observation Receiver IIP2, f1 to f2 vs. Attenuation, LO = 300 MHz, Tone 1 = 302 MHz, Tone 2 = 322 MHz at –25 dBm Plus Attenuation

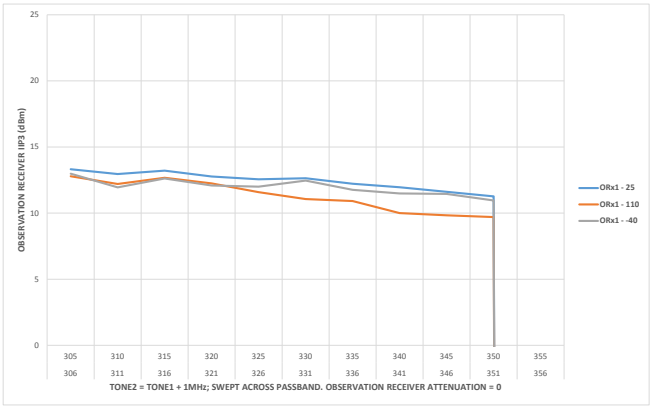


Figure 56. Observation Receiver IIP3, 2 f1 to f2 vs. f1 Offset Frequency, LO = 300 MHz, Attenuation = 0 dB, Tones Separated By 1 MHz Swept Across Passband at –25 dBm Each

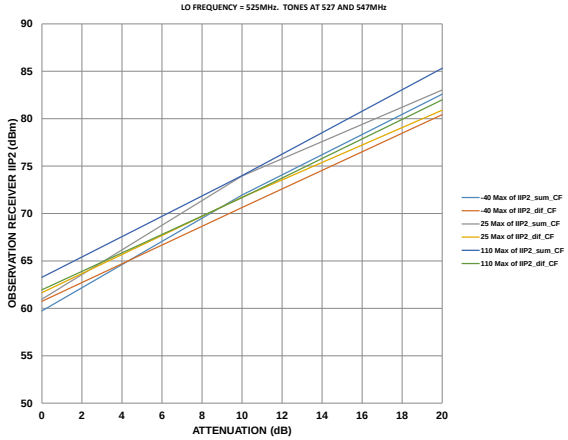


Figure 54. Observation Receiver IIP2, f1 to f2 vs. Attenuation, LO = 525 MHz, Tone 1 = 527 MHz, Tone 2 = 547 MHz at –25 dBm Plus Attenuation

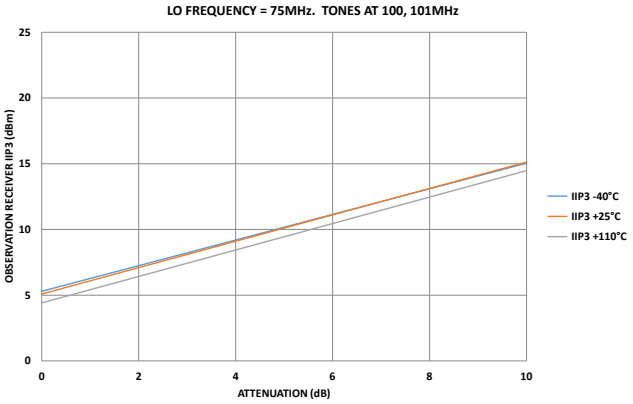


Figure 57. Observation Receiver IIP3, 2 f1 to f2 vs. Attenuation, LO = 75 MHz, Tone 1 = 100 MHz, Tone 2 = 101 MHz at –24 dBm Plus Attenuation

Figure 55. Observation Receiver IIP3, 2f1 to f2 vs. Intermod Frequency, LO = 75 MHz, Attenuation = 0 dB, Tones Separated By 1 MHz Swept Across Passband at –25 dBm Each

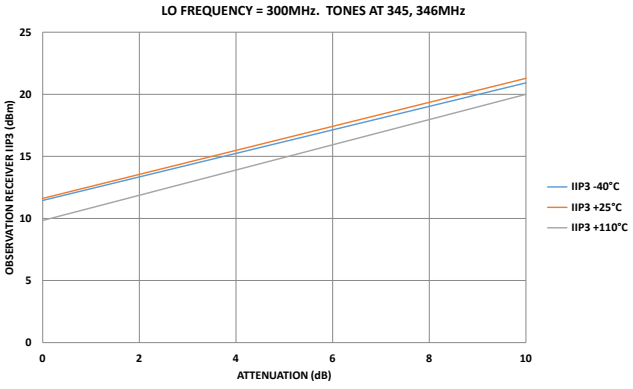


Figure 58. Observation Receiver IIP3, 2f1 to f2 vs. Attenuation, LO = 300 MHz, Tone 1 = 345 MHz, Tone 2 = 346 MHz at – 24 dBm Plus Attenuation

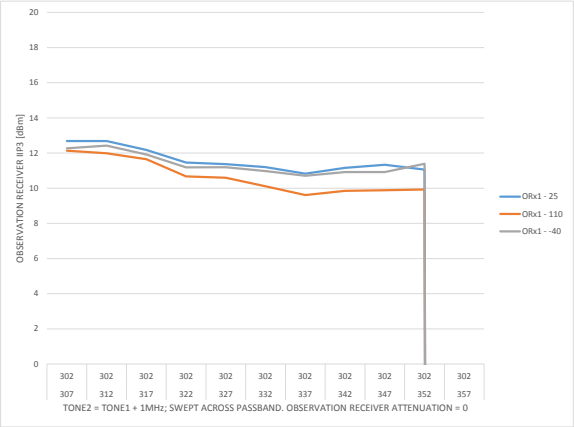


Figure 59. Observation Receiver IIP3, 2f1 to f2 vs. f1 Offset Frequency, LO = 300 MHz, Attenuation = 0 dB, Tones Separated by 1 MHz Swept Across Passband at −19 dBm Each

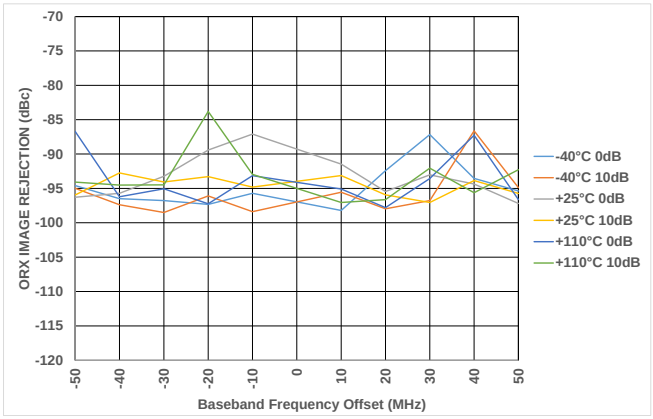


Figure 62. Observation Receiver Image Rejection vs. Baseband Frequency Offset and Attenuation, Continuous Wave Signal Swept Across the Band, LO = 300 MHz

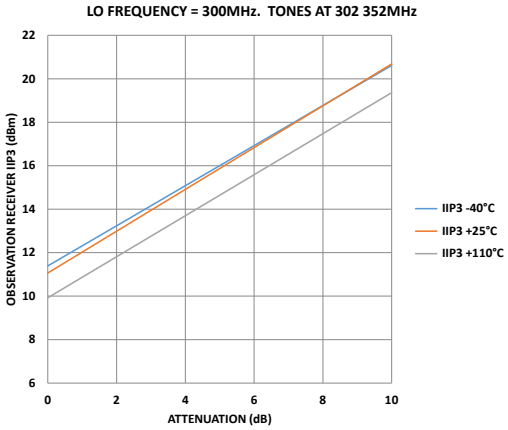


Figure 60. Observation Receiver IIP3, 2f1 to f2 vs. Attenuation, LO = 300 MHz, Tone 1 = 302 MHz, Tone 2 = 352 MHz at −19 dBm Plus Attenuation

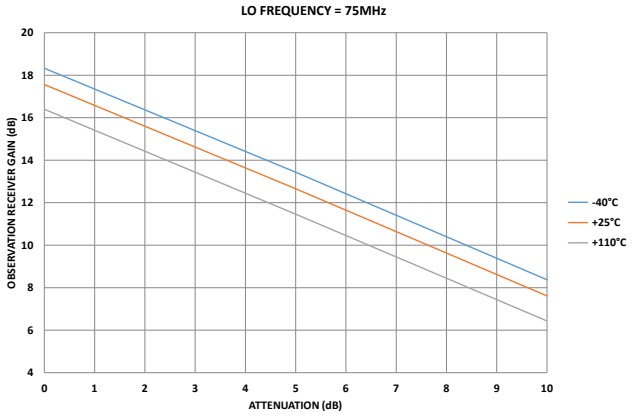


Figure 63. Observation Receiver Gain vs. Observation Receiver Attenuation, LO = 75 MHz

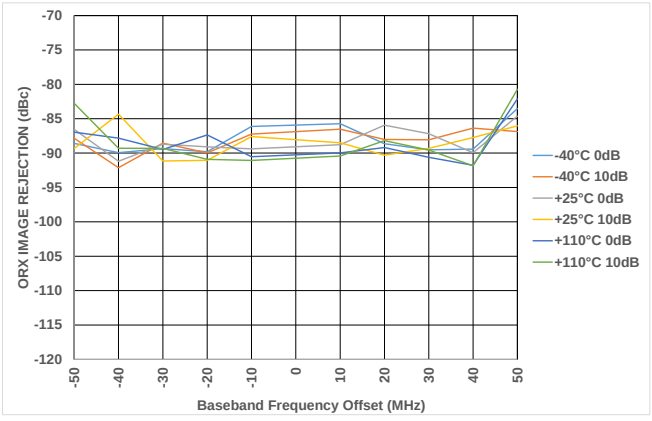


Figure 61. Observation Receiver Image Rejection vs. Baseband Frequency Offset and Attenuation, Continuous Wave Signal Swept Across the Band, LO = 75 MHz

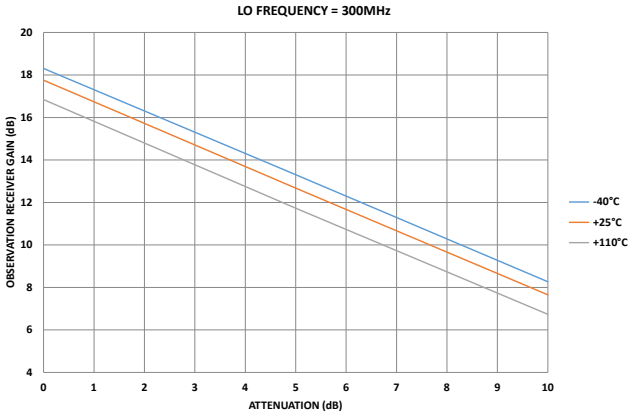


Figure 64. Observation Receiver Gain vs. Observation Receiver Attenuation, LO = 300 MHz

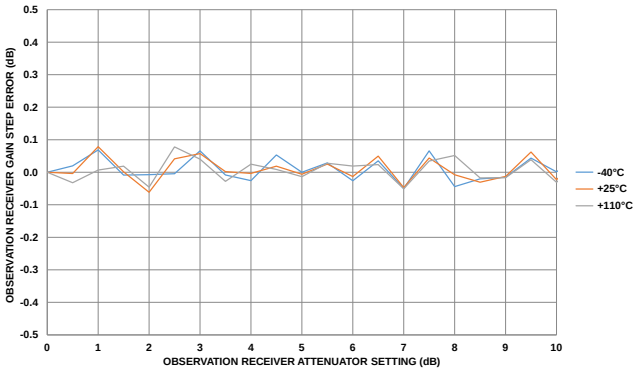


Figure 65. Observation Receiver Gain Step Error vs. Observation Receiver Attenuator, LO = 75 MHz

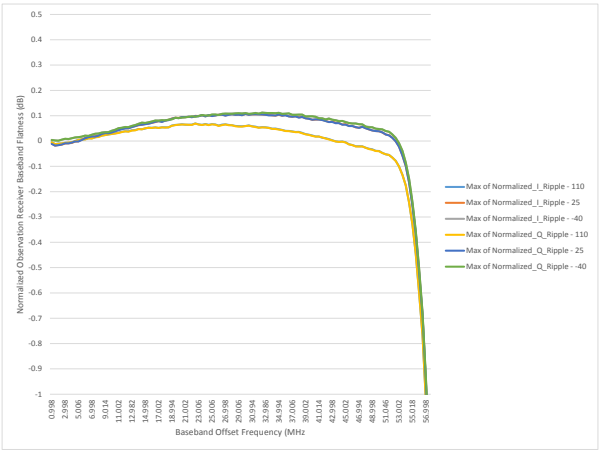


Figure 68. Normalized Observation Receiver Baseband Flatness vs. Baseband Offset Frequency, LO = 75 MHz, Attenuation = 0 dB

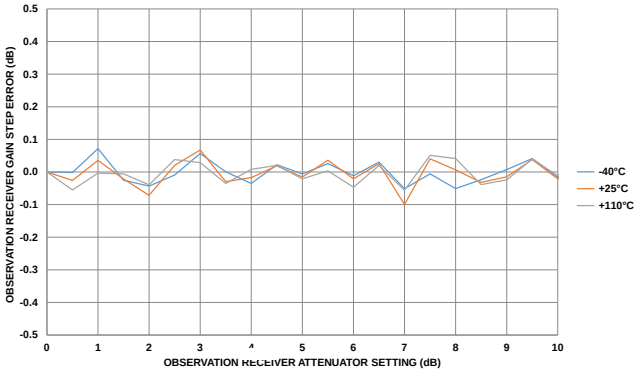


Figure 66. Observation Receiver Attenuator Gain Step Error vs. Observation Receiver Attenuator, LO = 325 MHz

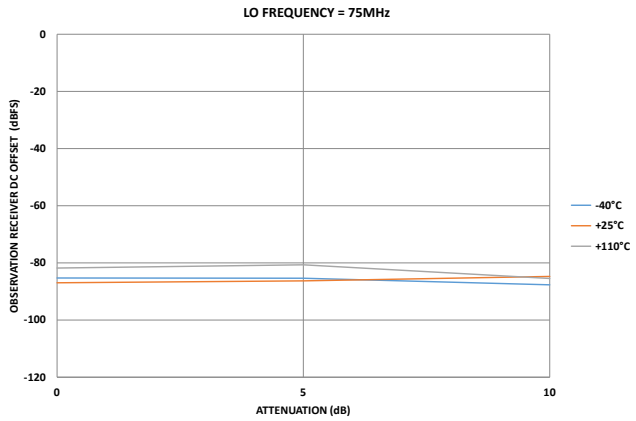


Figure 69. Observation Receiver DC Offset vs. Attenuation, LO = 75 MHz, Baseband Frequency = 50 MHz

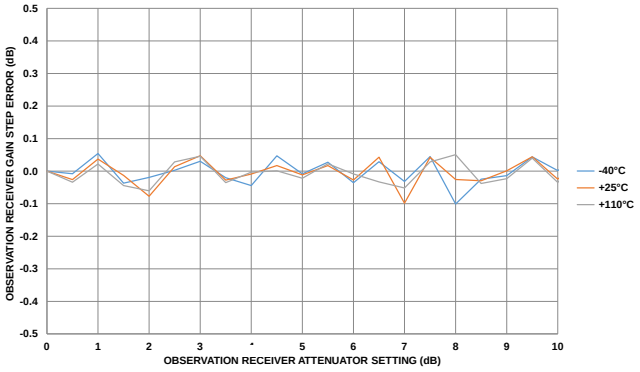


Figure 67. Observation Receiver Attenuator Gain Step Error vs. Observation Receiver Attenuator, LO = 525 MHz

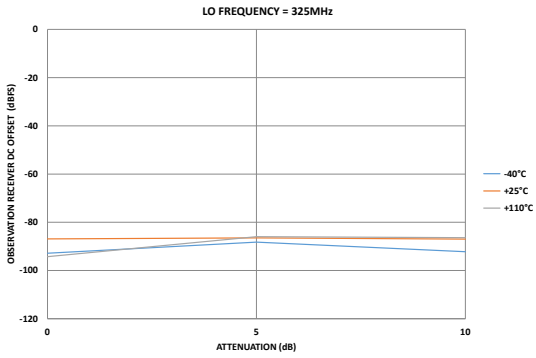


Figure 70. Observation Receiver DC Offset vs. Attenuation, LO = 325 MHz, Baseband Frequency = 50 MHz

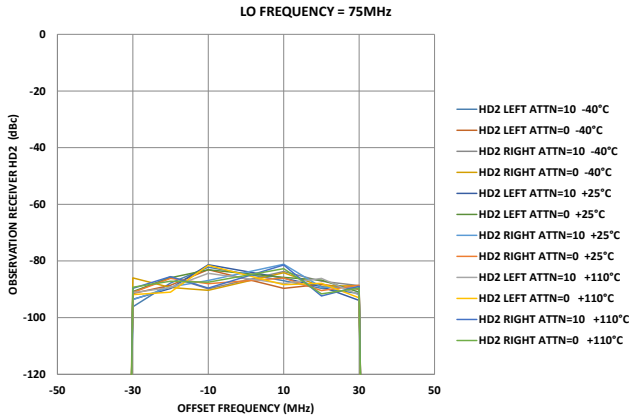


Figure 71. Observation Receiver HD2 vs. Offset Frequency and Attenuation, LO = 75 MHz, Tone Level = –21 dBm Plus Attenuation

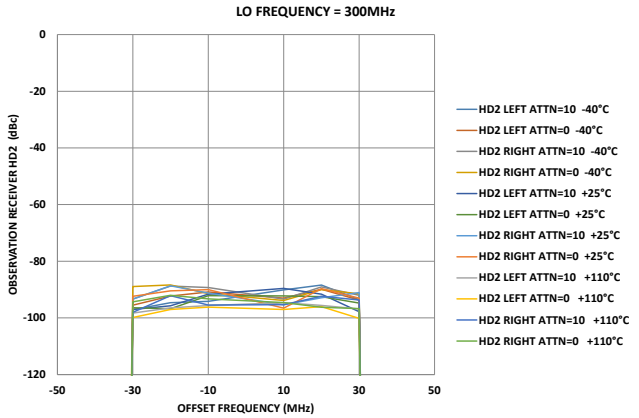


Figure 72. Observation Receiver HD2 vs. Offset Frequency and Attenuation, LO = 300 MHz, Tone Level = –22 dBm Plus Attenuation

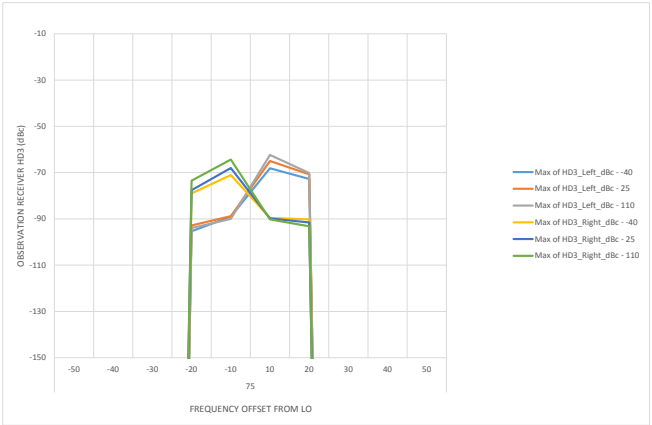


Figure 73. Observation Receiver HD3 Left and Right vs. Frequency Offset from LO, Tone Level = –21 dBm at Attenuation = 0 dB, LO = 75 MHz

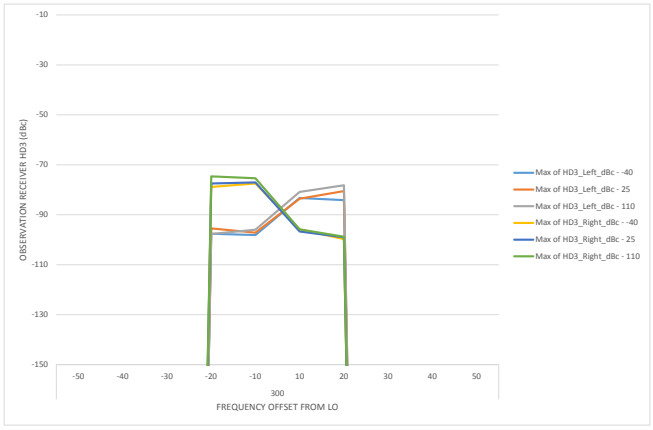


Figure 74. Observation Receiver HD3 Left and Right vs. Frequency Offset from LO, Tone Level = –22 dBm at Attenuation = 0 dB, LO = 300 MHz

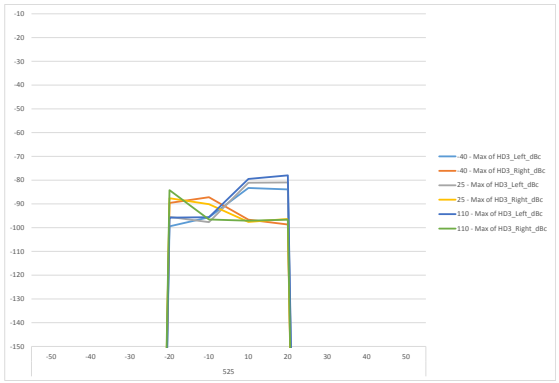


Figure 75. Observation Receiver HD3 Left and Right vs. Frequency Offset from LO, Tone Level –22 dBm at Attenuation = 0 dB, LO = 525 MHz

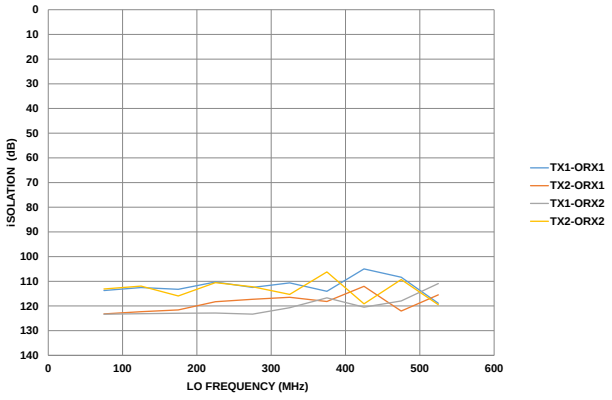


Figure 76. Transmitter to Observation Receiver Isolation vs. LO Frequency, Temperature = 25°C

Fig 77. LO Phase Noise vs. Frequency Offset, LO = 75 MHz, RMS Phase Error Integrated from 2 kHz to 18 MHz, PLL Loop Bandwidth = 300 kHz

Fig 79. LO Phase Noise vs. Frequency Offset, LO = 525 MHz, RMS Phase Error Integrated from 2 kHz to 18 MHz, PLL Loop Bandwidth = 300 kHz

Fig 78. LO Phase Noise vs. Frequency Offset, LO = 300 MHz, RMS Phase Error Integrated from 2 kHz to 18 MHz, PLL Loop Bandwidth = 300 kHz

650 MHz TO 3000 MHz BAND

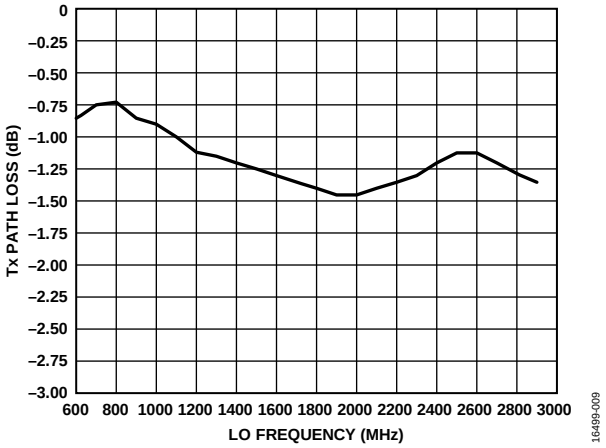


Figure 80. Transmitter Matching Circuit Path Loss vs. LO Frequency (Can Be Used for De-Embedding Performance Data)

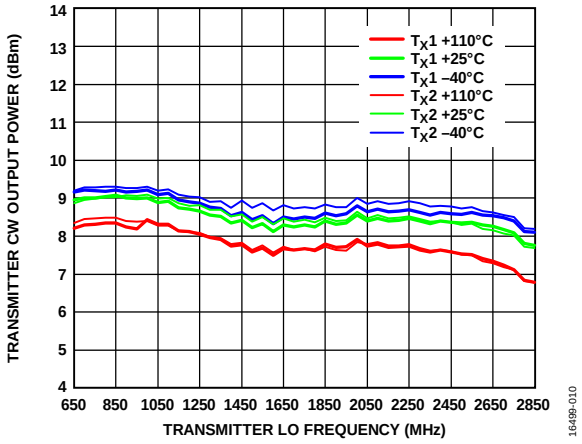


Figure 81. Transmitter Continuous Wave Output Power vs. Transmitter Frequency, Transmitter QEC and External LO Leakage Active, Transmitter in 200 MHz/450 MHz Bandwidth Mode, IQ Rate = 491.52 MHz, Attenuation = 0 dB (Not De-Embedded)

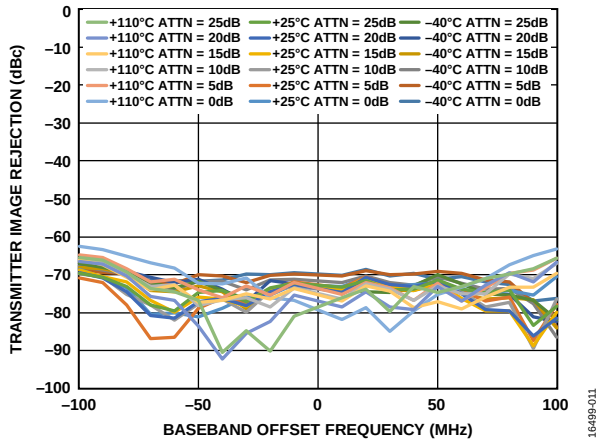


Figure 82. Transmitter Image Rejection Across Large Signal Bandwidth vs. Offset Frequency and Attenuation, QEC Trained with Three Tones Placed at 10 MHz, 50 MHz, and 100 MHz (Tracking On), Total Combined Power = –6 dBFS, Correction Then Frozen (Tracking Turned Off), Continuous Wave Tone Swept Across Large Signal Bandwidth

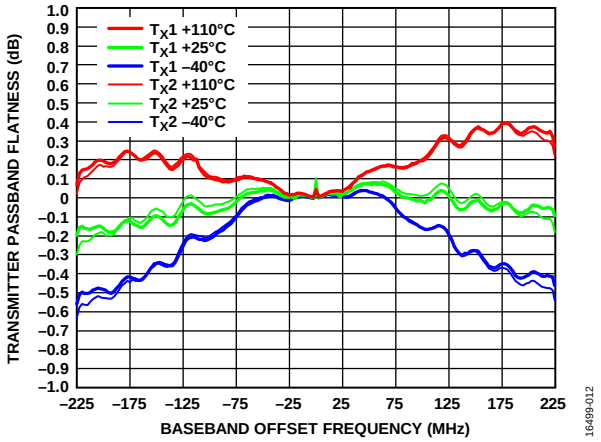


Figure 83. Transmitter Passband Flatness vs. Baseband Offset Frequency, LO = 2600 MHz

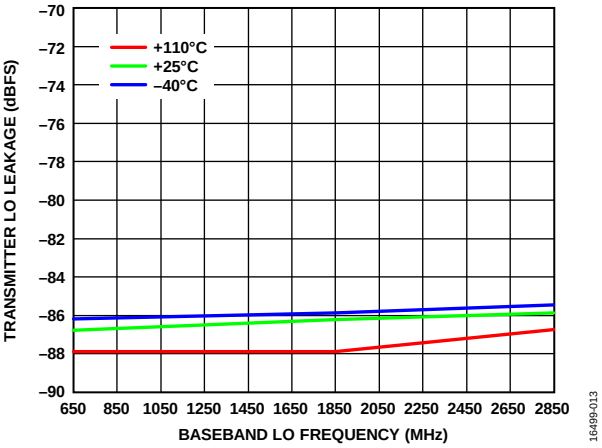


Figure 84. Transmitter LO Leakage vs. Baseband LO Frequency, Transmitter Attenuation = 0 dB

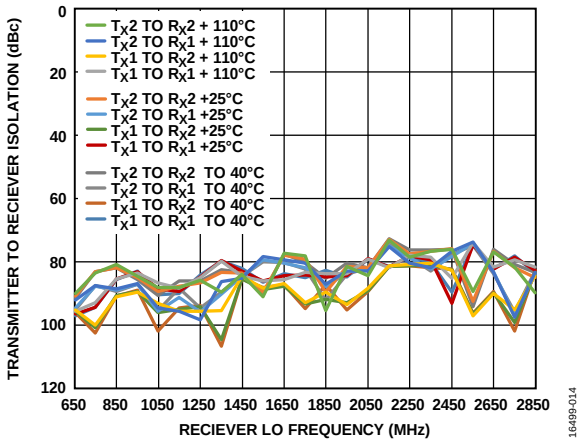


Figure 85. Transmitter to Receiver Isolation vs. Receiver LO Frequency

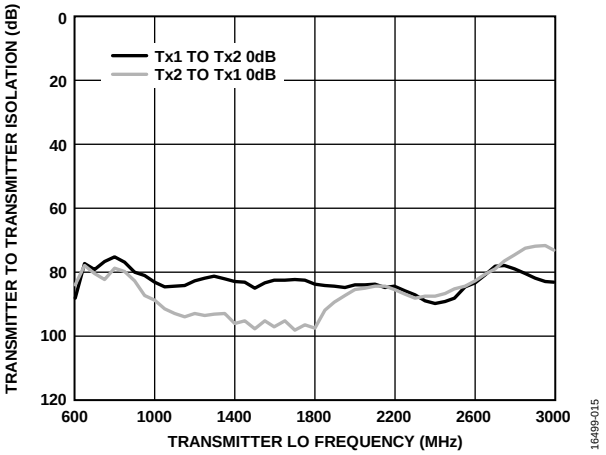


Figure 86. Transmitter to Transmitter Isolation vs. Transmitter LO Frequency, Temperature = 25°C

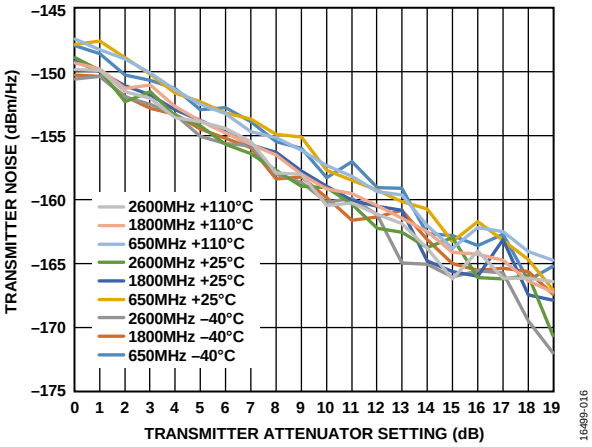


Figure 87. Transmitter Noise vs. Transmitter Attenuation Setting

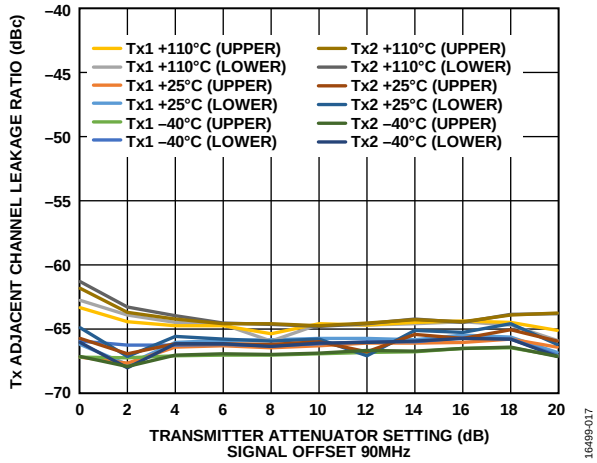


Figure 88. Transmitter Adjacent Channel Leakage Ratio vs. Transmitter Attenuation Setting, Signal Offset = 90 MHz, LO = 650 MHz, LTE 20 MHz PAR = 12 dB, Upper Side and Lower Side

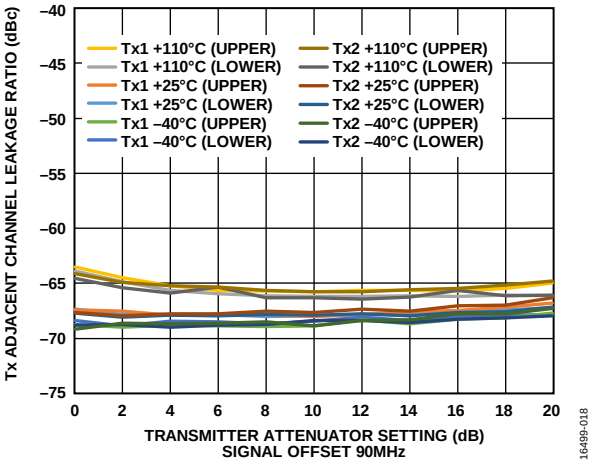


Figure 89. Transmitter Adjacent Channel Leakage Ratio vs. Transmitter Attenuation Setting, Signal Offset = 90 MHz, LO = 1850 MHz, LTE 20 MHz PAR = 12 dB, Upper Side and Lower Side

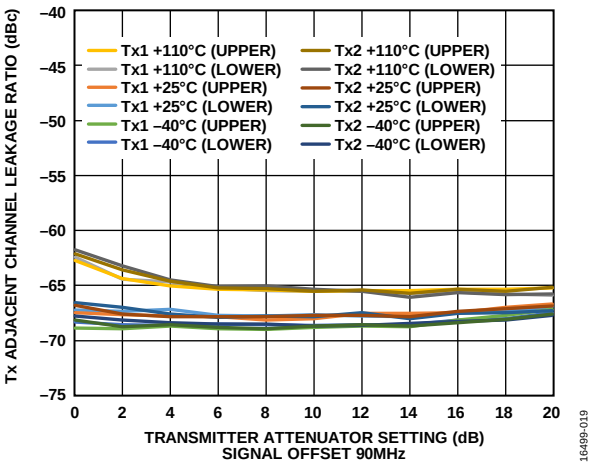


Figure 90. Transmitter Adjacent Channel Leakage Ratio vs. Transmitter Attenuation Setting, Signal Offset = 90 MHz, LO = 2850 MHz, LTE 20 MHz PAR = 12 dB, Upper Side and Lower Side

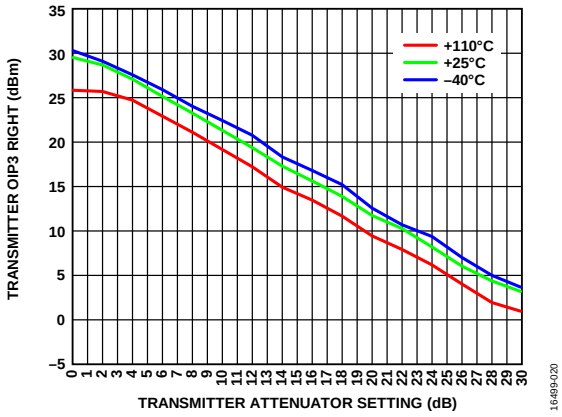


Figure 91. Transmitter OIP3, Right or Upper Sideband Response vs. Transmitter Attenuation Setting, LO = 850 MHz, 15 dB Digital Backoff per Tone

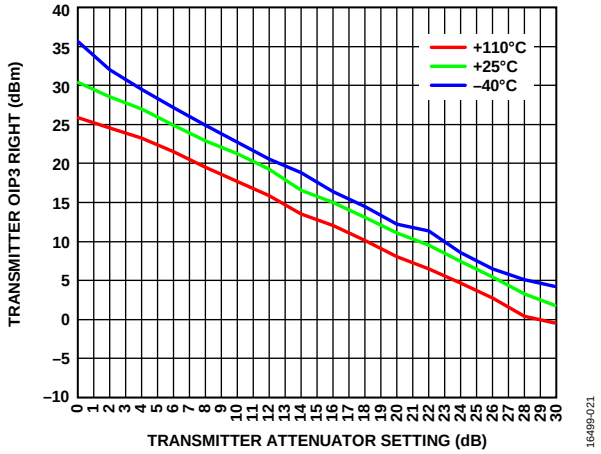


Figure 92. Transmitter OIP3, Right vs. Transmitter Attenuation, LO = 1850 MHz, 15 dB Digital Backoff per Tone

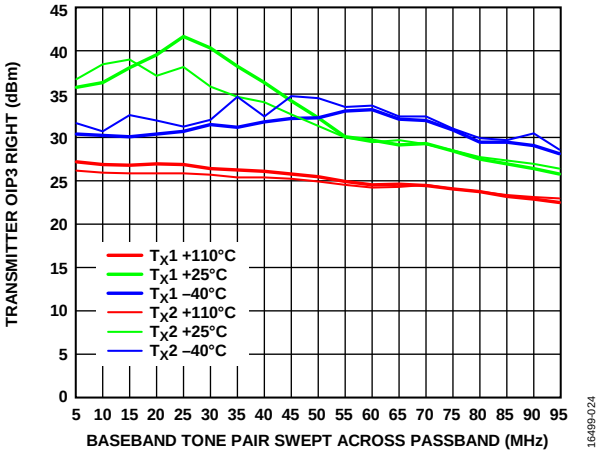


Figure 95. Transmitter OIP3, Right vs. Baseband Tone Pair Swept Across Passband, LO = 1850 MHz, 15 dB Digital Backoff per Tone

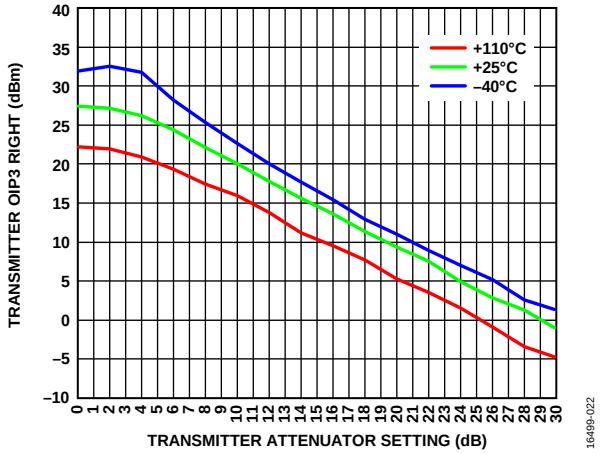


Figure 93. Transmitter OIP3, Right vs. Transmitter Attenuation Setting, LO = 2650 MHz, 15 dB Digital Backoff per Tone

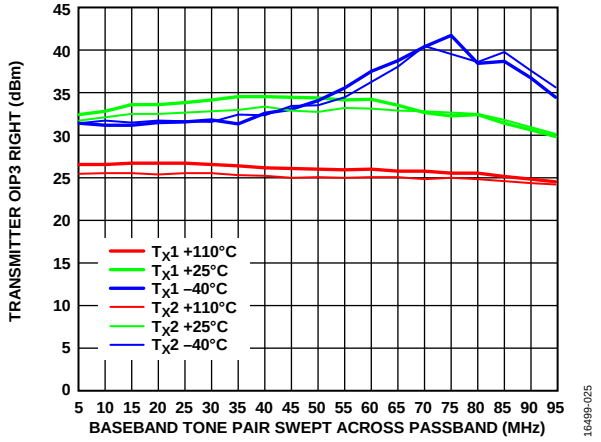


Figure 96. Transmitter OIP3, Right vs. Baseband Tone Pair Swept Across Passband, LO = 2850 MHz,15 dB Digital Backoff per Tone,

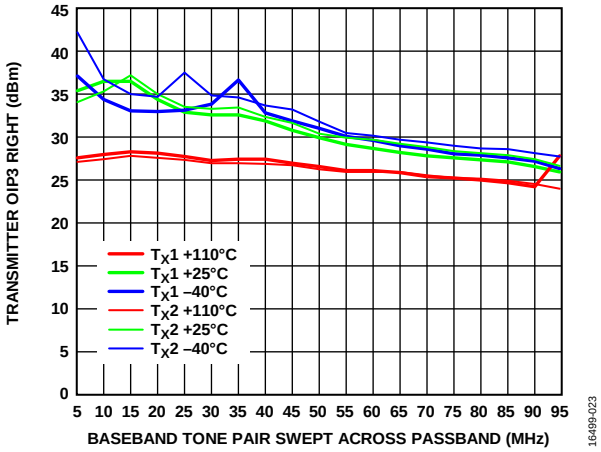


Figure 94. Transmitter OIP3, Right vs. Baseband Tone Pair Swept Across Passband, LO = 850 MHz, 15 dB Digital Backoff per Tone

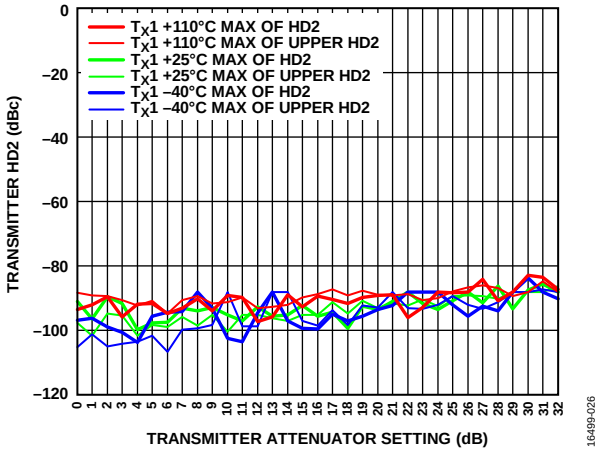


Figure 97. Transmitter HD2 vs. Transmitter Attenuation Setting, Baseband Frequency = 10 MHz, LO = 1850 MHz, 15 dB Digital Backoff

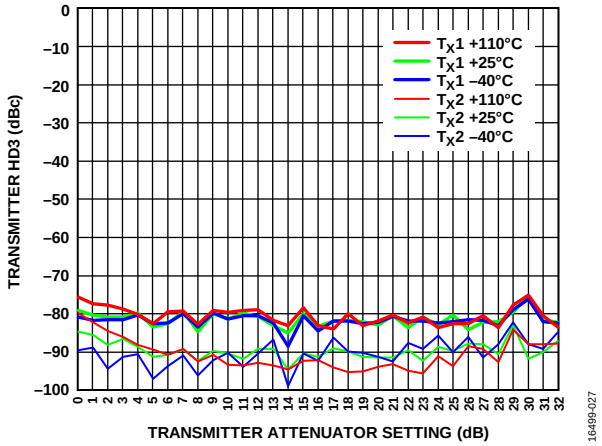


Figure 98. Transmitter HD3 vs. Transmitter Attenuation Setting, LO = 650 MHz, Digital Backoff = 15 dB

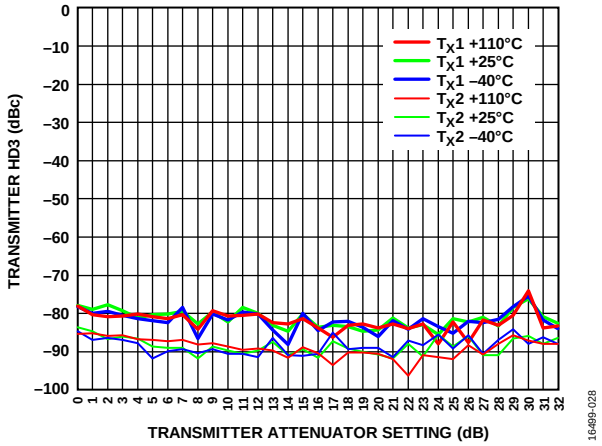


Figure 99. Transmitter HD3 vs. Transmitter Attenuation Setting, LO = 1850 MHz, Digital Backoff = 15 dB,

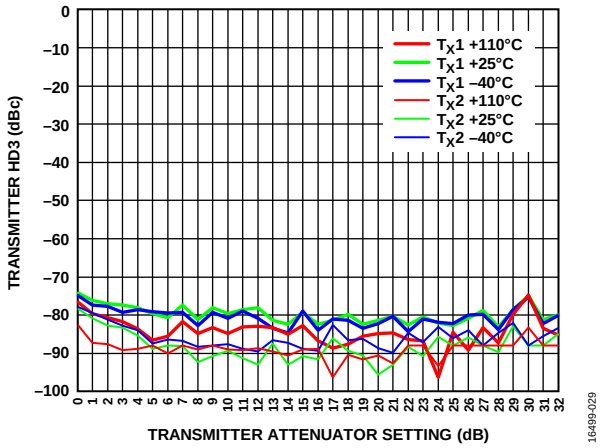


Figure 100. Transmitter HD3 vs. Transmitter Attenuation Setting, LO = 2850 MHz, Digital Backoff = 15 dB

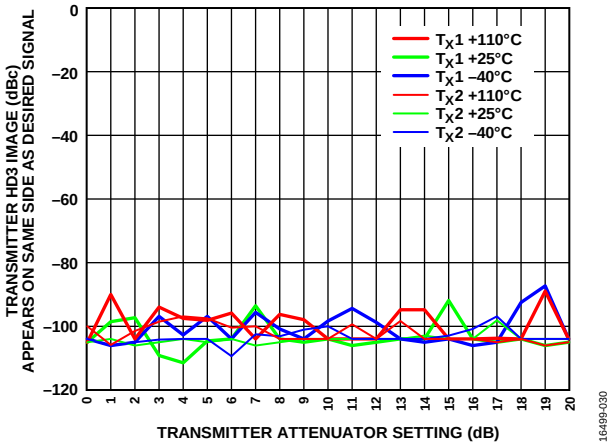


Figure 101. Transmitter HD3 on Same Side as Desired Signal vs. Transmitter Attenuation Setting, LO = 2850 MHz, Digital Backoff = 15 dB

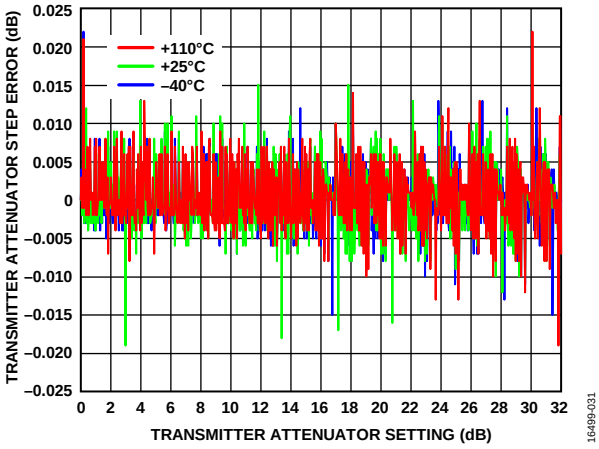


Figure 102. Transmitter Attenuation Step Error vs. Transmitter Attenuation Setting, LO = 650 MHz

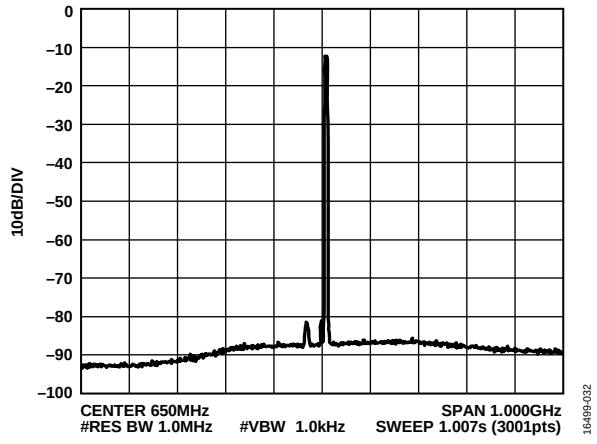


Figure 103. Transmitter Output Spurious, Transmitter 1 = 650 MHz, 5 MHz LTE, Offset = 10 MHz, RMS = –12 dBFS, Temperature = 25°C

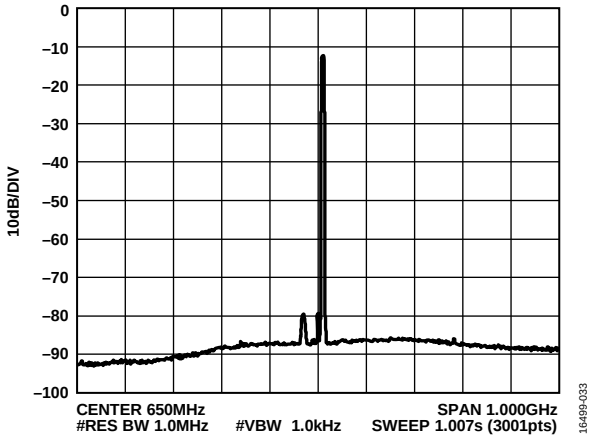


Figure 104. Transmitter Output Spurious, Transmitter 2 = 650 MHz, LTE = 5 MHz, Offset = 10 MHz, RMS = −12 dBFS, Temperature = 25°C

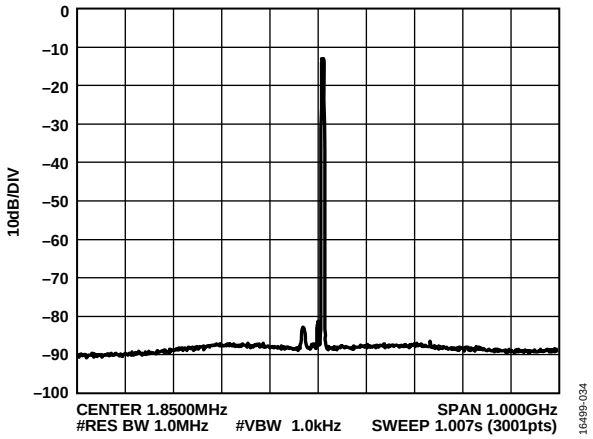


Figure 105. Transmitter Output Spurious, Transmitter 1 = 1850 MHz, LTE = 5 MHz, Offset = 10 MHz, RMS = −12 dBFS, Temperature = 25°C

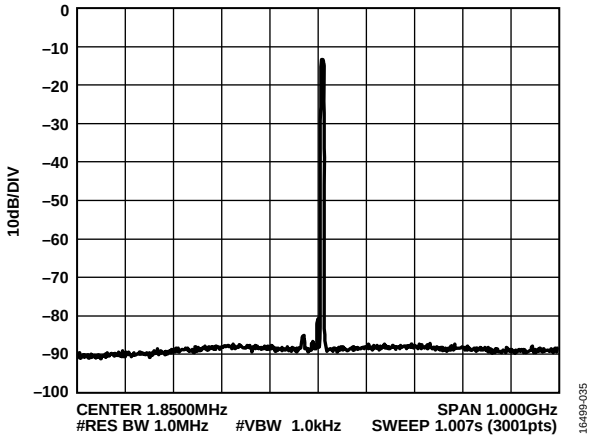


Figure 106. Transmitter Output Spurious, Transmitter 2 = 1850 MHz, LTE = 5 MHz, Offset = 10 MHz, RMS = −12 dBFS, Temperature = 25°C

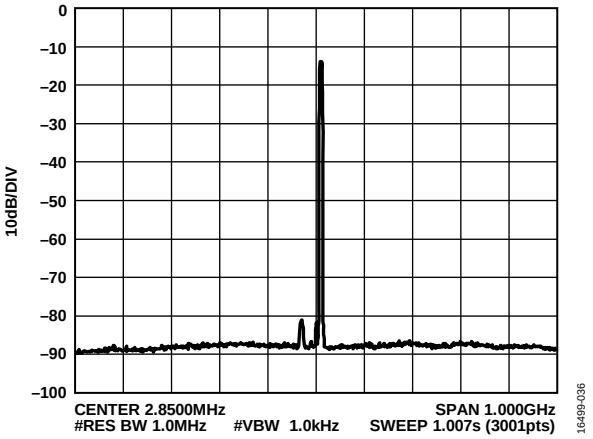


Figure 107. Transmitter Output Spurious, Transmitter 1 = 2850 MHz, LTE = 5 MHz, Offset = 10 MHz, RMS = −12 dBFS, Temperature = 25°C

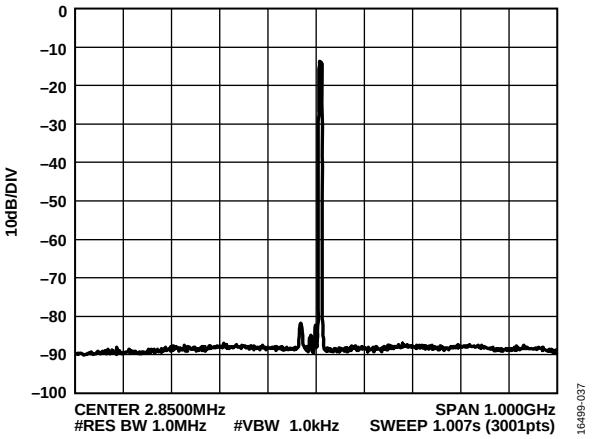


Figure 108. Transmitter Output Spurious, Transmitter 2 = 2850 MHz, LTE = 5 MHz, Offset = 10 MHz, RMS = −12 dBFS, Temperature = 25°C

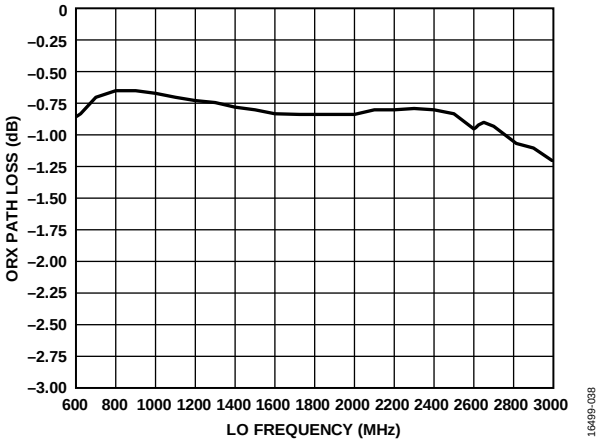


Figure 109 Observation Receiver Matching Circuit Path Loss vs. Frequency, Can Be Used for De-Embedding Performance Data

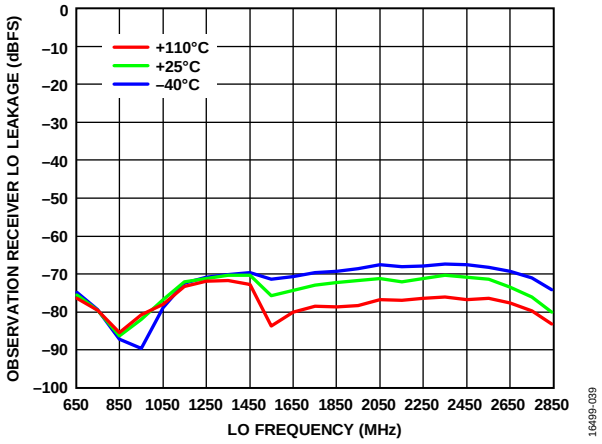


Figure 110. Observation Receiver LO Leakage vs. Transmitter LO Frequency

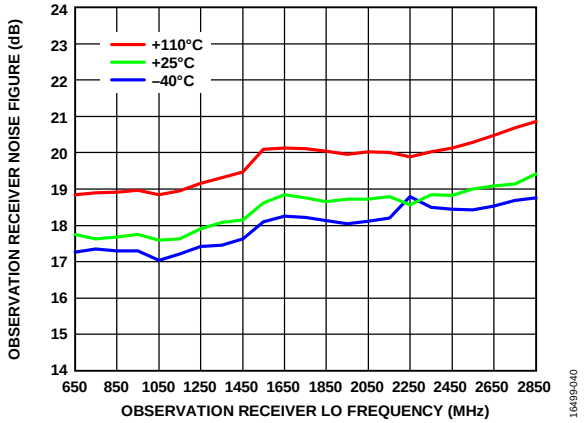


Figure 111. Observation Receiver Noise Figure vs. Observation Receiver LO Frequency, Total Nyquist Integration Bandwidth

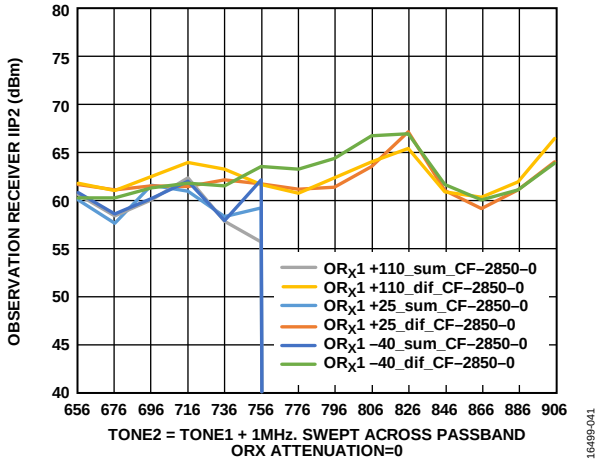


Figure 112. Observation Receiver IIP2, Sum and Difference Products vs. f1 Offset Frequency, Tones Separated by 1 MHz Swept Across Passband at –19 dBm Each, 650 MHz, Attenuation = 0 dB

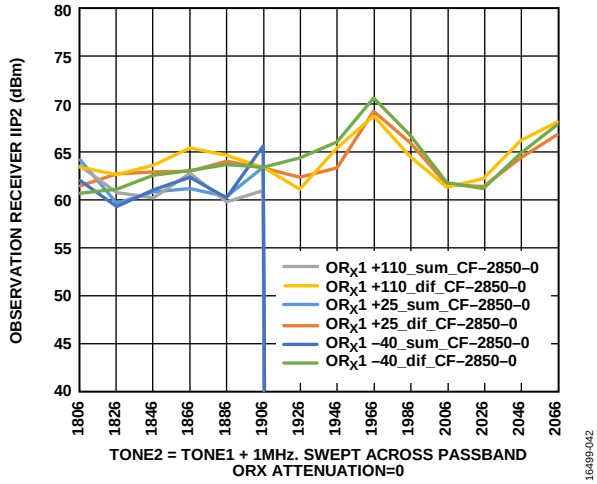


Figure 113. Observation Receiver IIP2, Sum and Difference Products vs. f1 Offset Frequency, Tones Separated by 1 MHz Swept Across Passband at –19 dBm Each, 1800 MHz, Attenuation = 0 dB

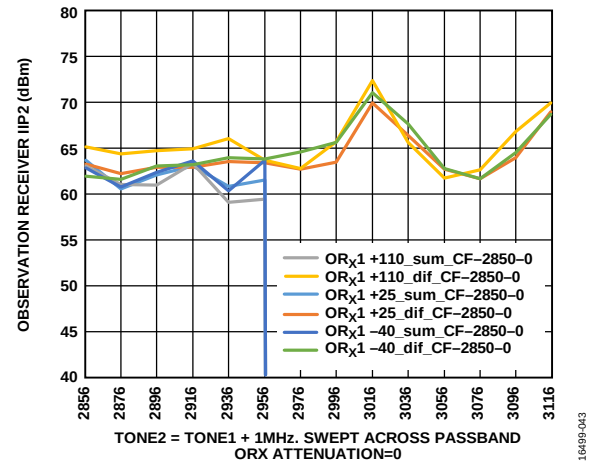


Figure 114. Observation Receiver IIP2, Sum and Difference Products vs. f1 Offset Frequency, Tones Separated by 1 MHz Swept Across Passband at –19 dBm Each, 2850 MHz, Attenuation = 0 dB

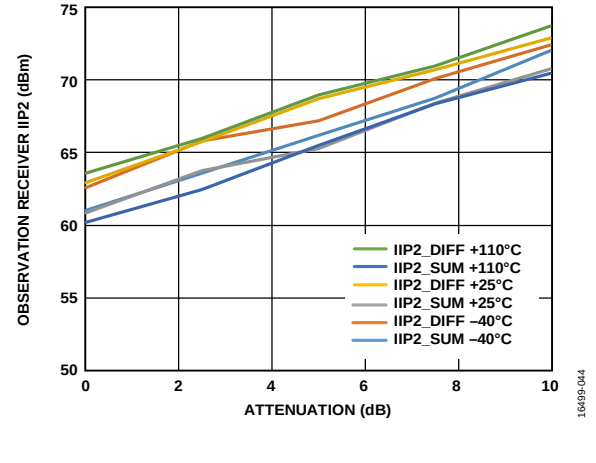


Figure 115. Observation Receiver IIP2, Sum and Difference Products vs. Attenuation, Tone 1 = 1845 MHz, Tone 2 = 1846 MHz at –19 dBm Plus Attenuation, LO = 1800 MHz

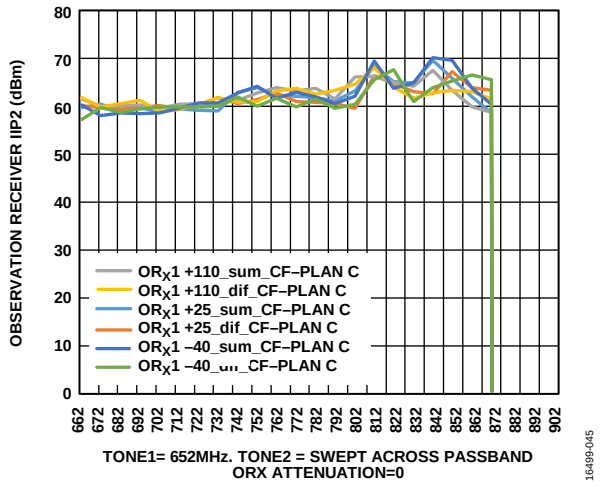


Figure 116. Observation Receiver IIP2, f1 to f2 vs. Intermodulation Frequency, LO = 650 MHz, Tone 1 = 652 MHz, Tone 2 Swept at −19 dBm Each, Attenuation = 0 dB

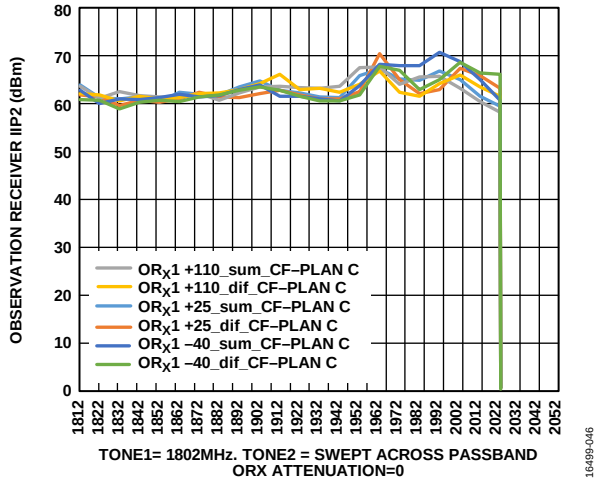


Figure 117. Observation Receiver IIP2, f1 to f2 vs. Intermodulation Frequency, LO = 1800 MHz, Tone 1 = 1802 MHz, Tone 2 Swept at −19 dBm Each, Attenuation = 0 dB

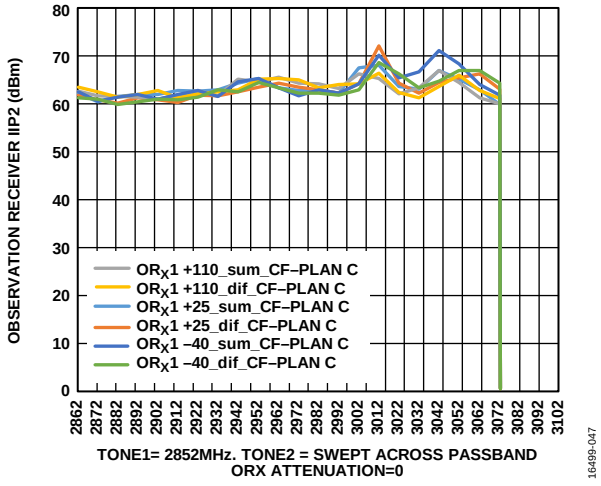


Figure 118. Observation Receiver IIP2, f1 to f2 vs. Intermodulation Frequency, LO = 2850 MHz, Tone 1 = 2852 MHz, Tone 2 Swept at −19 dBm Each, Attenuation = 0 dB

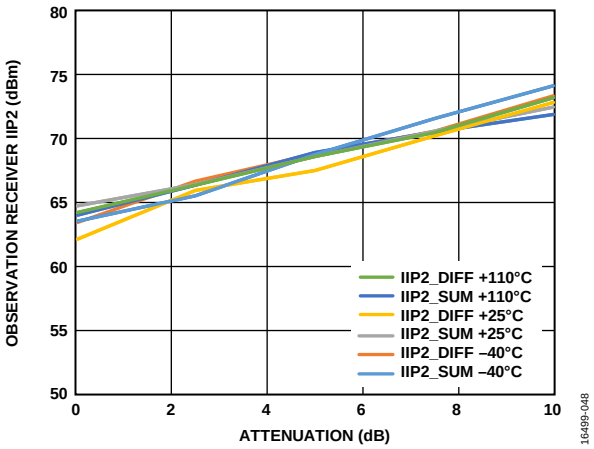


Figure 119. Observation Receiver IIP2, f1 to f2 vs. Attenuation, LO = 1800 MHz, Tone 1 = 1802 MHz, Tone 2 = 1902 MHz at −19 dBm Plus Attenuation

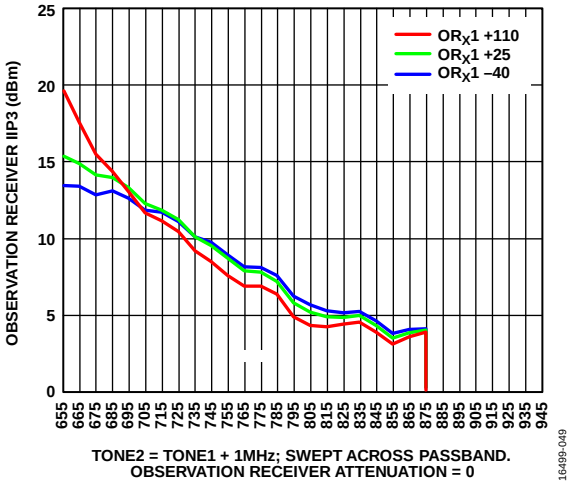


Figure 120. Observation Receiver IIP3, 2f1 to f2 vs. f1 Offset Frequency, 650 MHz, Attenuation = 0 dB, Tones Separated by 1 MHz Swept Across Passband at −19 dBm Each

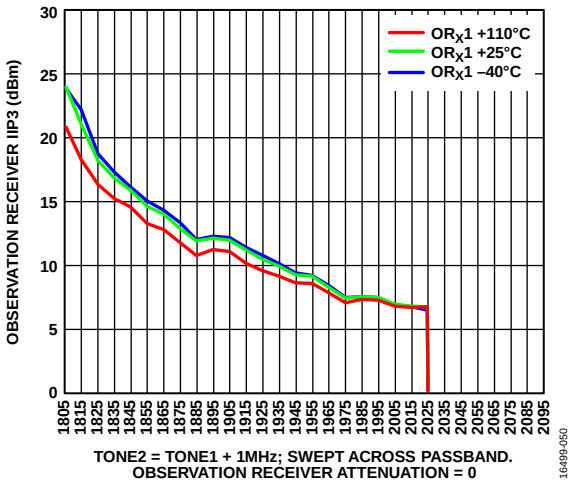


Figure 121. Observation Receiver IIP3, 2f1 to f2 vs. f1 Offset Frequency, 1800 MHz, Attenuation = 0 dB, Tones Separated by 1 MHz Swept Across Passband at −19 dBm Each

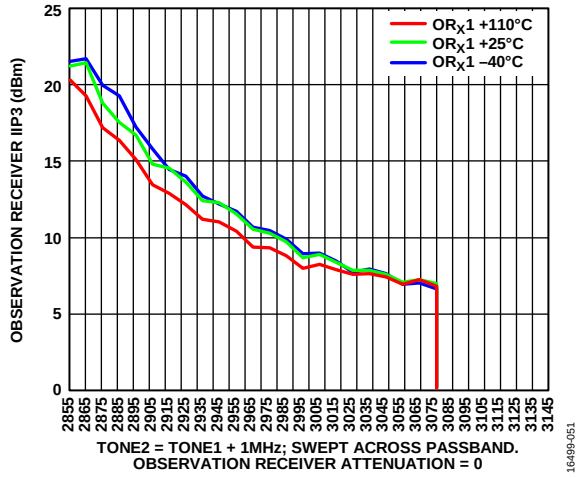


Figure 122. Observation Receiver IIP3, 2f1 to f2 vs. f1 Offset Frequency, LO = 2850 MHz, Attenuation = 0 dB, Tones Separated by 1 MHz Swept Across Passband at –19 dBm Each

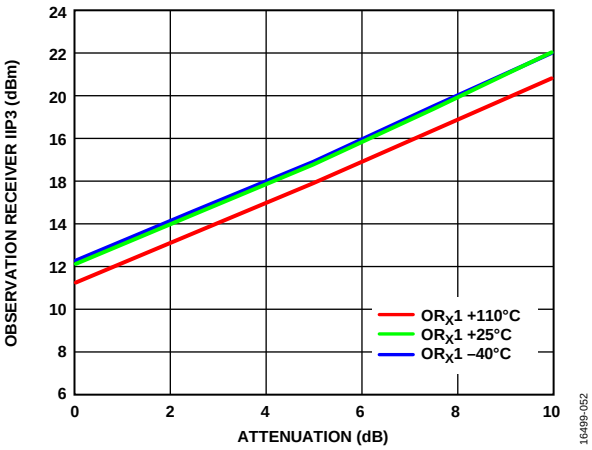


Figure 123. Observation Receiver IIP3, 2f1 to f2 vs. Attenuation, LO = 1800 MHz, Tone 1 = 1895 MHz, Tone 2 = 1896 MHz at –19 dBm Plus Attenuation

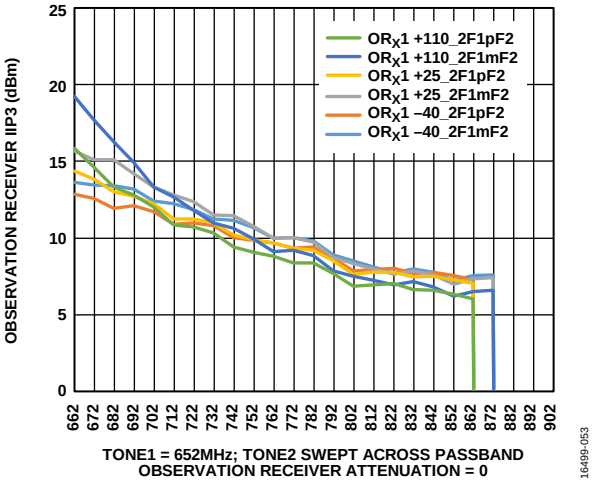


Figure 124. Observation Receiver IIP3, 2f1 to f2 vs. Intermodulation Frequency, LO = 650 MHz, Tone 1 = 652 MHz, Tone 2 Swept at –19 dBm Each

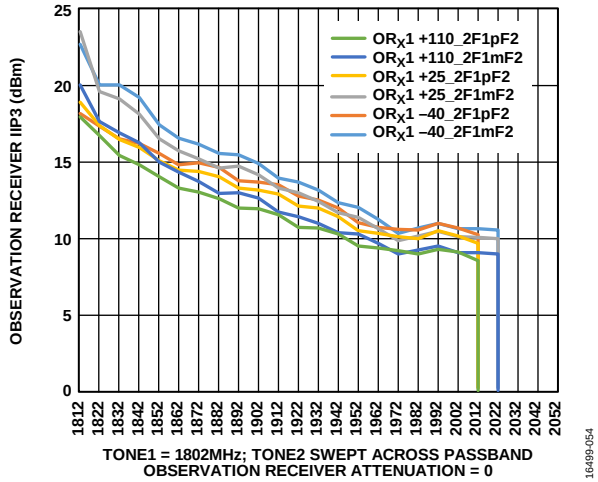


Figure 125. Observation Receiver IIP3, 2f1 to f2 vs. Intermodulation Frequency, LO = 1800 MHz, Tone 1 = 1802 MHz, Tone 2 Swept at –19 dBm Each

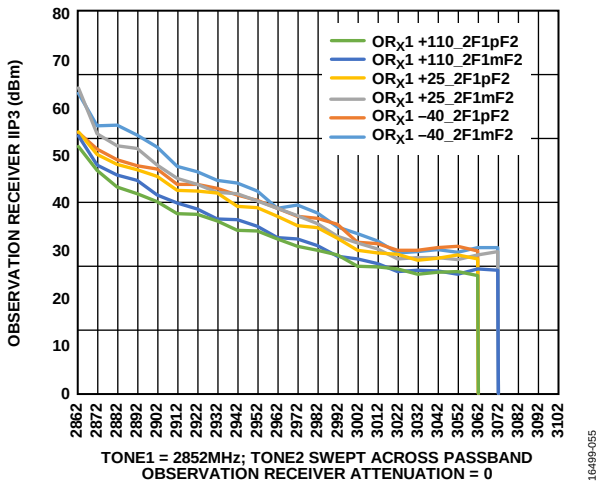


Figure 126. Observation Receiver IIP3, 2f1 to f2 vs. Intermodulation Frequency, LO = 2850 MHz, Tone 1 = 2852 MHz, Tone 2 Swept at –19 dBm Each

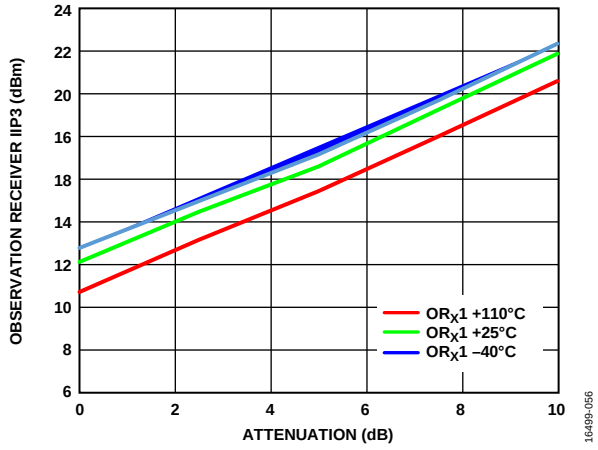


Figure 127. Observation Receiver IIP3, 2f1 to f2 vs. Attenuation, LO = 1800 MHz, Tone 1 = 1802 MHz, Tone 2 = 1922 MHz at –19 dBm Plus Attenuation

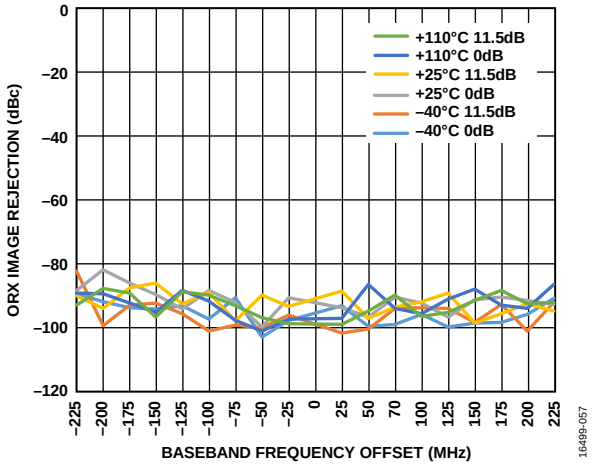


Figure 128. Observation Receiver Image Rejection vs. Baseband Frequency Offset, Continuous Wave Signal Swept Across the Band, LO = 650 MHz

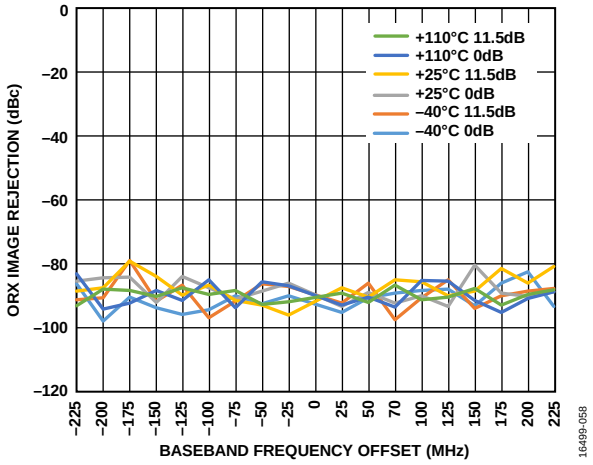


Figure 129. Observation Receiver Image Rejection vs. Baseband Frequency Offset, Continuous Wave Signal Swept Across the Band, LO = 1850 MHz

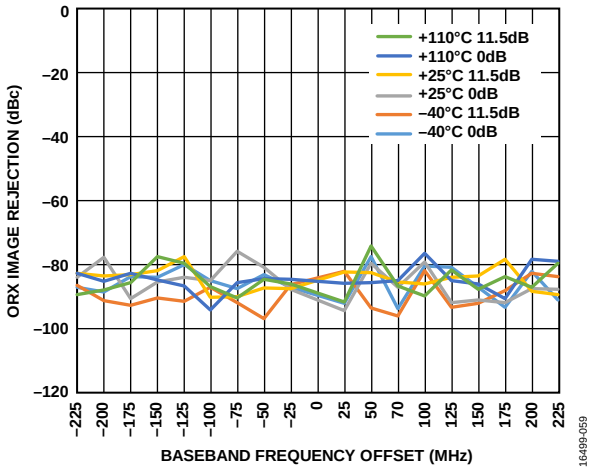


Figure 130. Observation Receiver Image Rejection vs. Baseband Frequency Offset, Continuous Wave Signal Swept Across the Band, LO = 2850 MHz

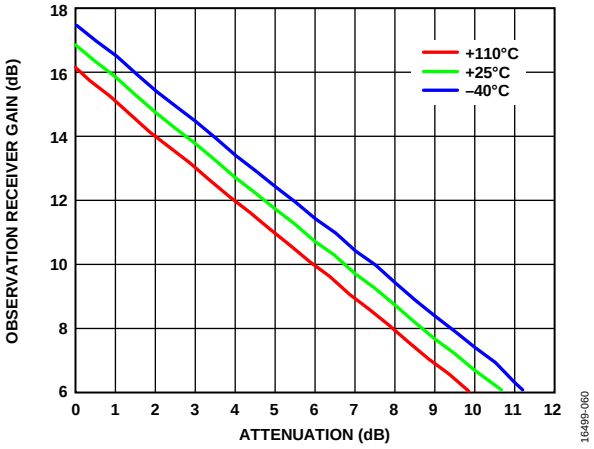


Figure 131. Observation Receiver Gain vs. Observation Receiver Attenuation, LO = 650 MHz

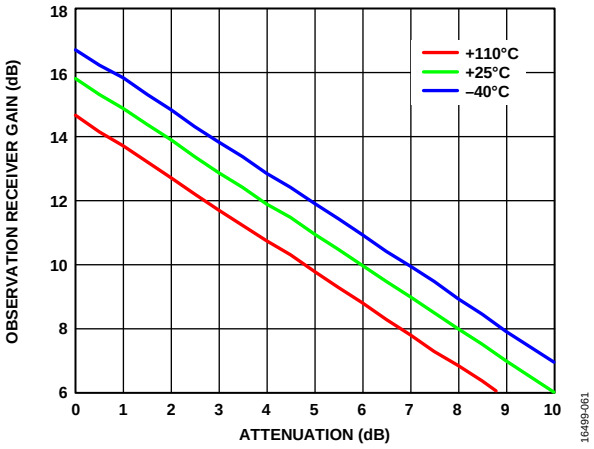


Figure 132. Observation Receiver Gain vs. Observation Receiver Attenuation, LO = 1800 MHz

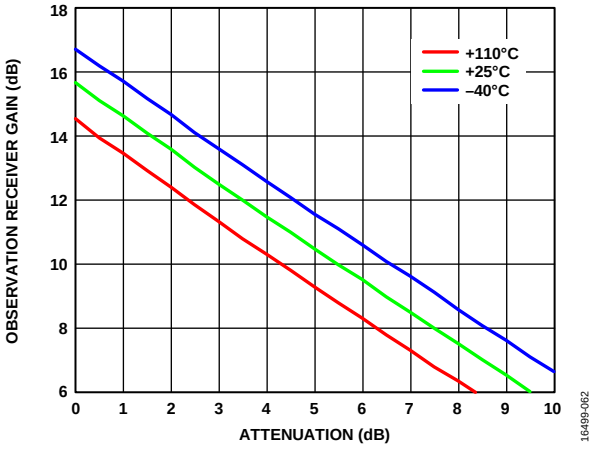


Figure 133. Observation Receiver Gain vs. Observation Receiver Attenuation, LO = 2800 MHz

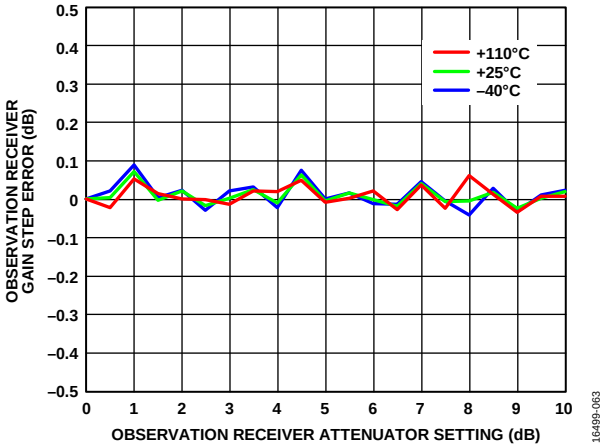


Figure 134. Observation Receiver Attenuator Step Accuracy vs. Observation Receiver Attenuator Setting, LO = 2600 MHz

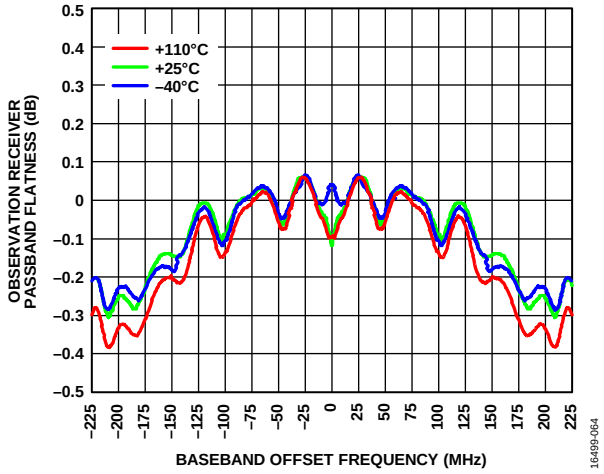


Figure 135. Observation Receiver Pass-Band Flatness, LO = 1800 MHz

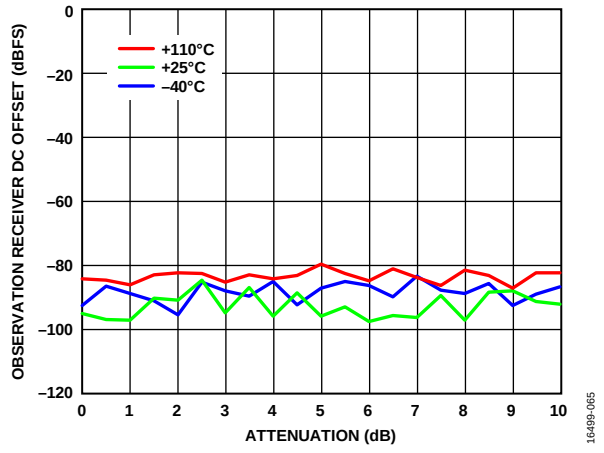


Figure 136. Observation Receiver DC Offset vs. Attenuation, LO = 1850 MHz

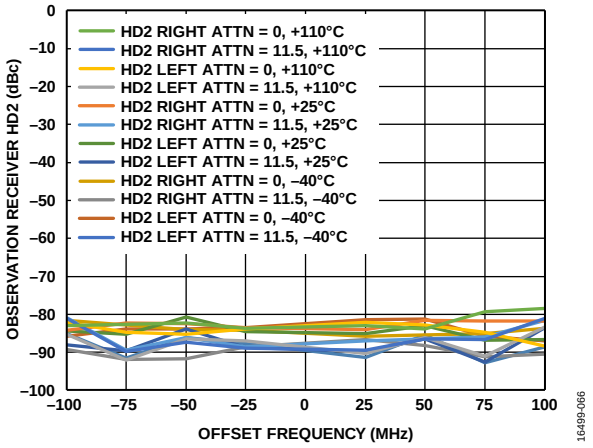


Figure 137. Observation Receiver HD2 vs. Offset Frequency and Attenuation, LO = 650 MHz Tone Level = –20 dBm at 0 dB Attenuation

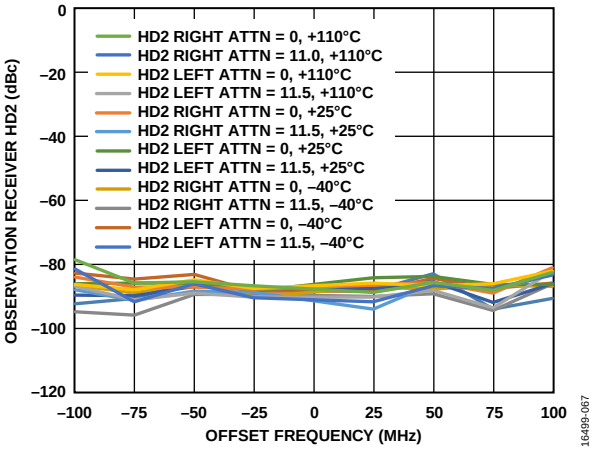


Figure 138. Observation Receiver HD2 vs. Offset Frequency and Attenuation, LO = 1850 MHz Tone Level = –20 dBm at 0 dB Attenuation

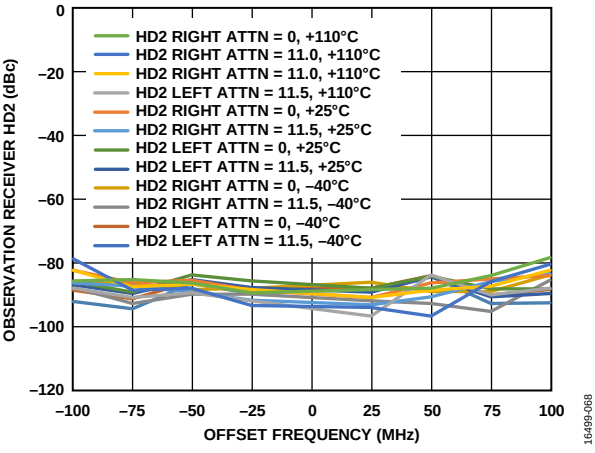


Figure 139. Observation Receiver HD2 vs. Offset Frequency and Attenuation, LO = 2850 MHz, Tone Level = –20 dBm at 0 dB Attenuation

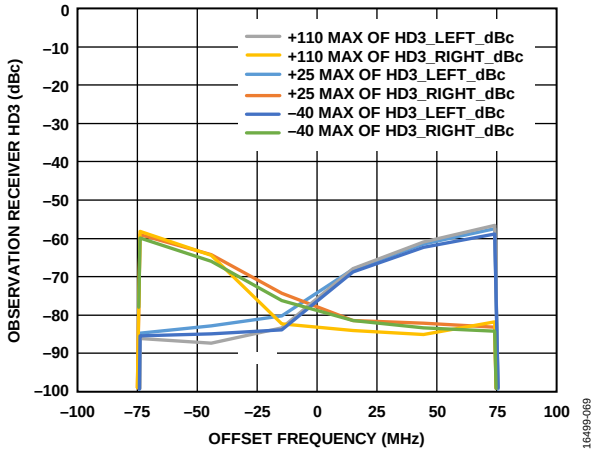


Figure 140. Observation Receiver HD3, Left and Right vs. Offset Frequency, LO = 650 MHz, Tone Level = –20 dBm at 0 dB Attenuation

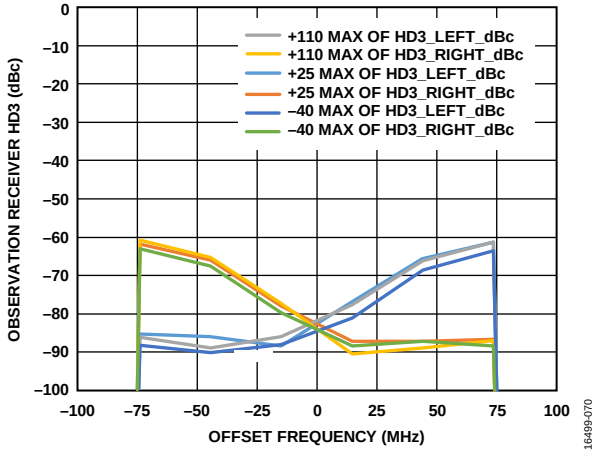


Figure 141. Observation Receiver HD3, Left and Right vs. Offset Frequency, LO = 1850 MHz, Tone Level = –20 dBm at 0 dB Attenuation

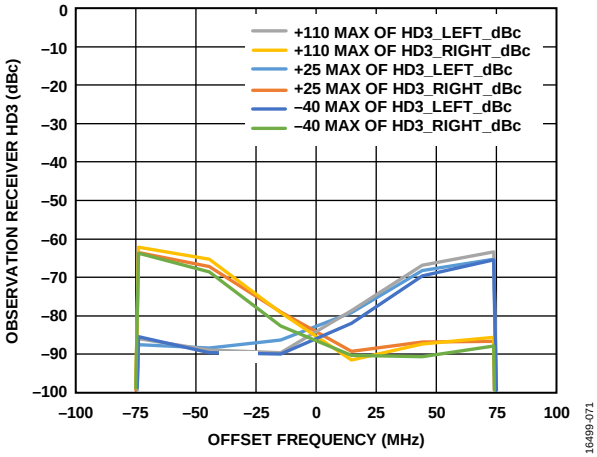


Figure 142. Observation Receiver HD3, Left and Right vs. Offset Frequency, LO = 2850 MHz, Tone Level = –20 dBm at 0 dB Attenuation

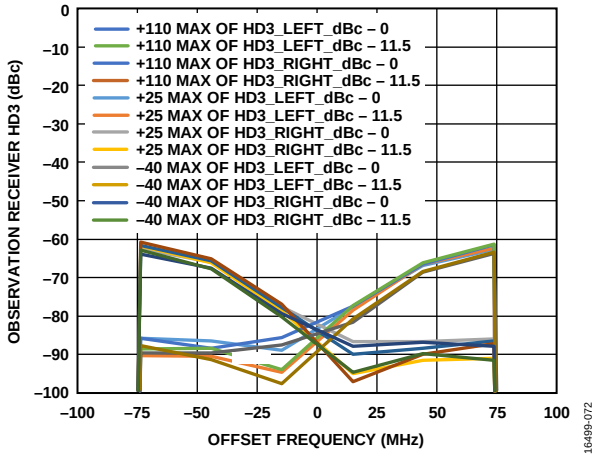


Figure 143. Observation Receiver HD3, Left and Right vs. Offset Frequency, LO = 1850 MHz, Observation Receiver Attenuation = 0 dB and 11.5 dB

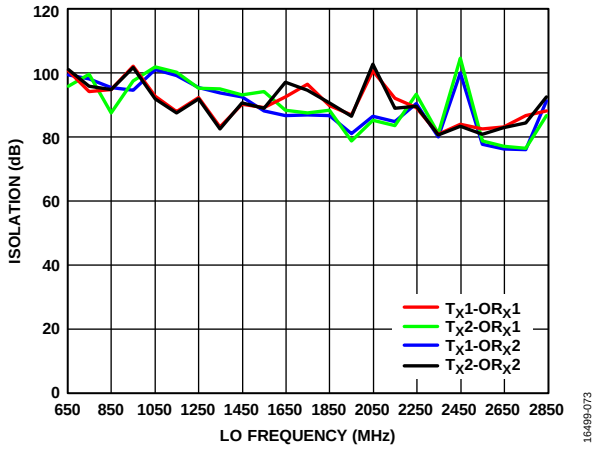


Figure 144. Transmitter to Observation Receiver Isolation vs. LO Frequency, Temperature = 25°C

Figure 145. LO Phase Noise vs. Frequency Offset, LO = 1900 MHz, RMS Phase Error Integrated from 2 kHz to 18 MHz, Spectrum Analyzer Limits Far Out Noise

3400 MHz TO 4800 MHz BAND

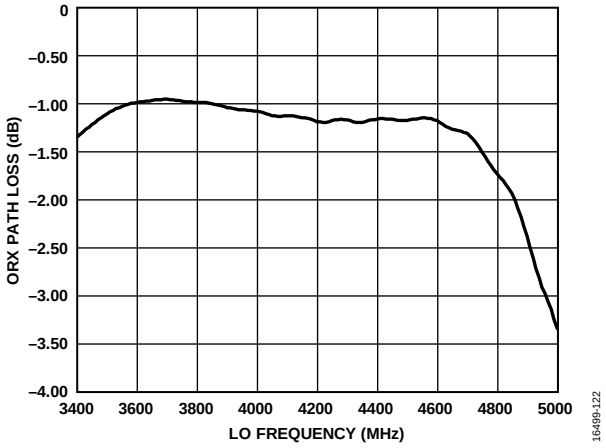


Figure 146. Transmitter Path Loss vs. LO Frequency (Simulation), Can Be Used for De-Embedding Performance Data

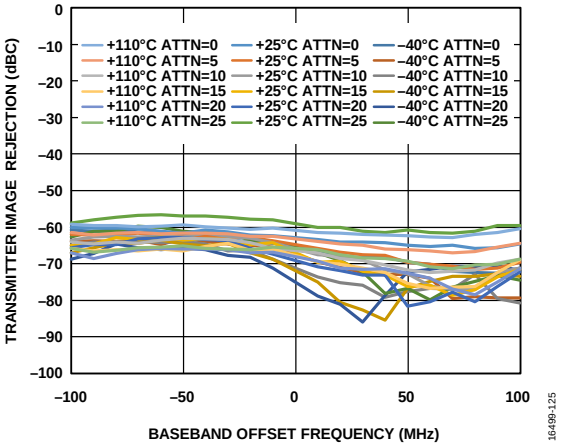


Figure 149. Transmitter Image Rejection Across Large Signal Bandwidth vs. Baseband Offset Frequency and Attenuation, QEC Trained with Three Tones (Tracking On), Total Combined Power = −6 dBFS, Correction Then Frozen (Tracking Turned Off), Continuous Wave Tone Swept Across Large Signal Bandwidth, LO = 4600 MHz

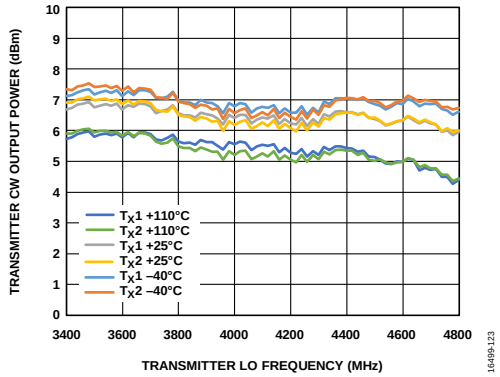


Figure 147. Transmitter Continuous Wave Output Power vs. Transmitter LO Frequency, Transmitter QEC and External LO Leakage Active, Transmitter in 200 MHz/450 MHz Bandwidth Mode, IQ Rate = 491.52 MHz, Attenuation =0 dB, Not De-Embedded

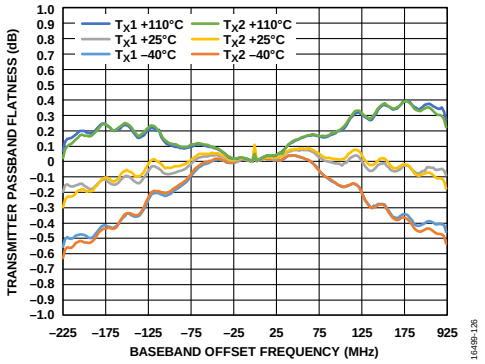


Figure 150. Transmitter Passband Flatness vs. Baseband Offset Frequency, Off-Chip Match Response De-Embedded, LO = 3600 MHz

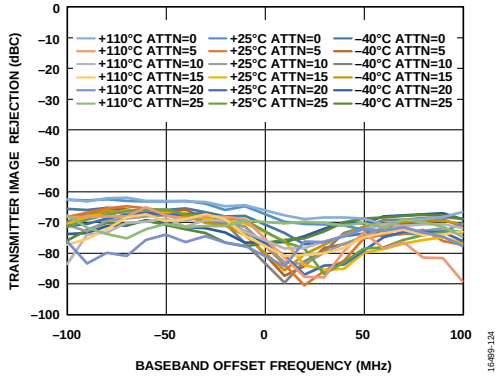


Figure 148. Transmitter Image Rejection Across Large Signal Bandwidth vs. Baseband Offset Frequency and Attenuation, QEC Trained with Three Tones Placed at 10 MHz, 50 MHz, and 100 MHz (Tracking On), Total Combined Power = −6 dBFS, Correction Then Frozen (Tracking Turned Off), Continuous Wave Tone Swept Across Large Signal Bandwidth, LO = 3700 MHz

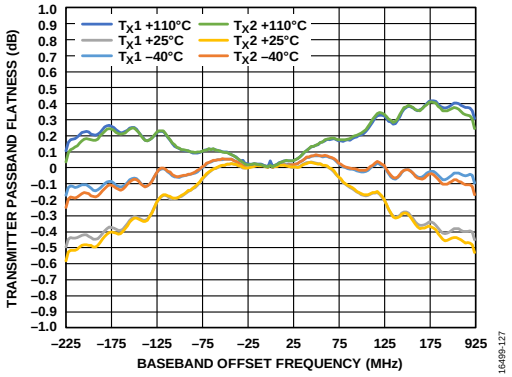


Figure 151. Transmitter Passband Flatness vs. Baseband Offset Frequency, Off-Chip Match Response De-Embedded, LO = 4600 MHz

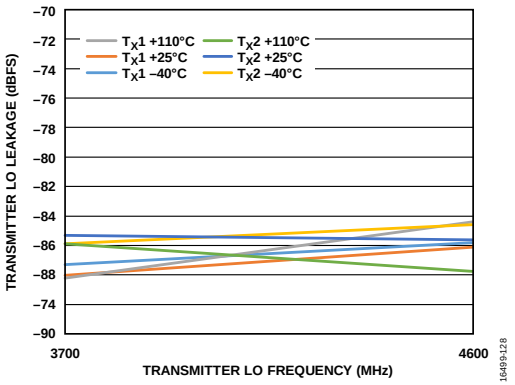


Figure 152. Transmitter LO Leakage vs. Transmitter LO Frequency, Transmitter Attenuation = 0 dB

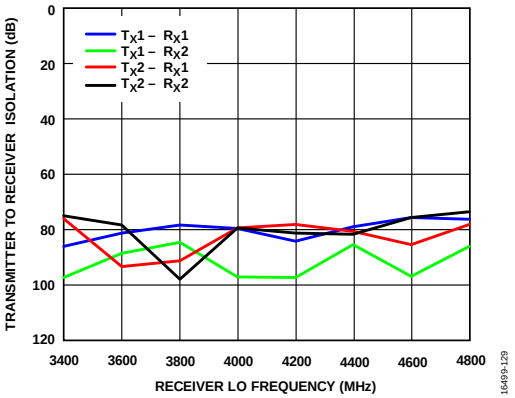


Figure 153. Transmitter to Receiver Isolation vs. Receiver LO Frequency, Temperature = –40°C, +25°C, and +110°C

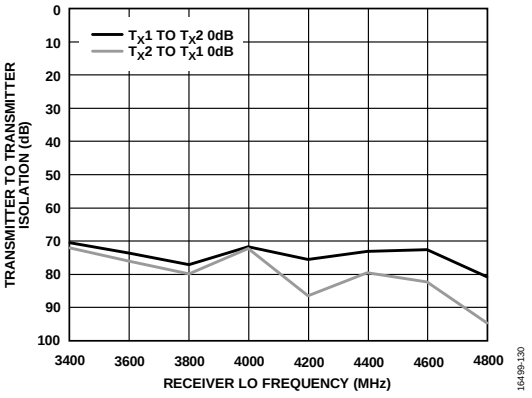


Figure 154. Transmitter to Transmitter Isolation vs. Transmitter LO Frequency, Temperature = 25°C

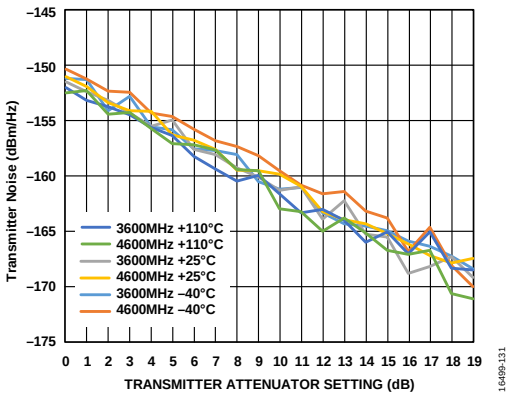


Figure 155. Transmitter Noise vs. Transmitter Attenuation Setting

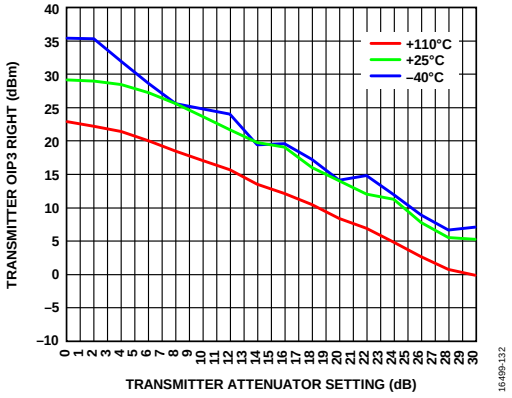


Figure 156. Transmitter OIP3, Right vs. Transmitter Attenuation Setting, LO = 3600 MHz, Total RMS Power = –12 dBFS

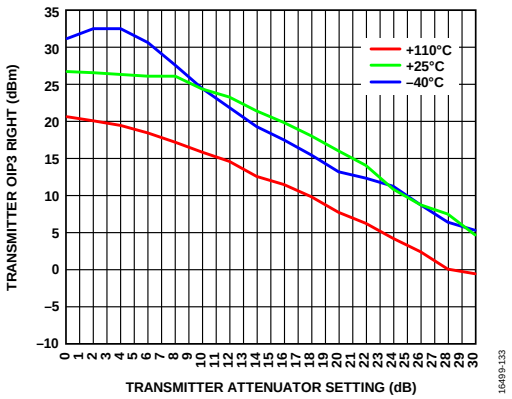


Figure 157. Transmitter OIP3, Right vs. Transmitter Attenuation Setting, LO = 4600 MHz, Total RMS Power = –12 dBFS

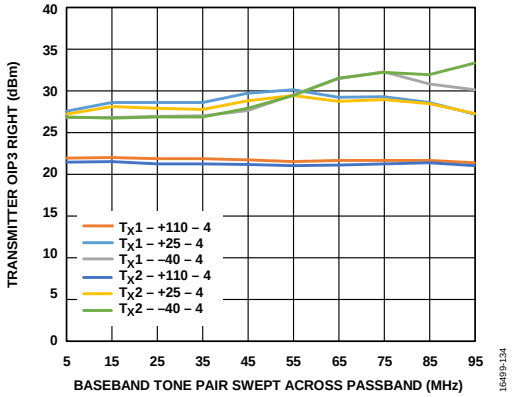


Figure 158. Transmitter OIP3, Right vs. Baseband Tone Pair Swept Across Passband, LO = 36000 MHz, Total RMS Power = −12 dBFS

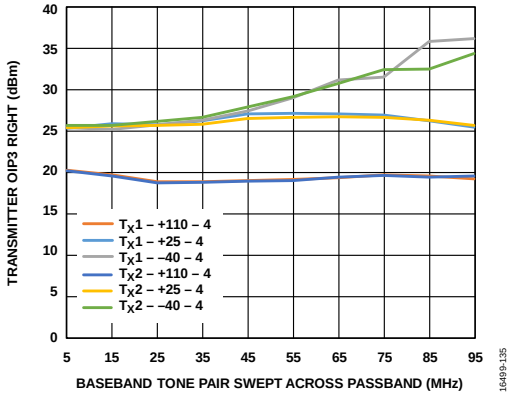


Figure 159. Transmitter OIP3, Right vs. Baseband Tone Pair Swept Across Passband, LO = 4600 MHz, Total RMS Power = −12 dBFS

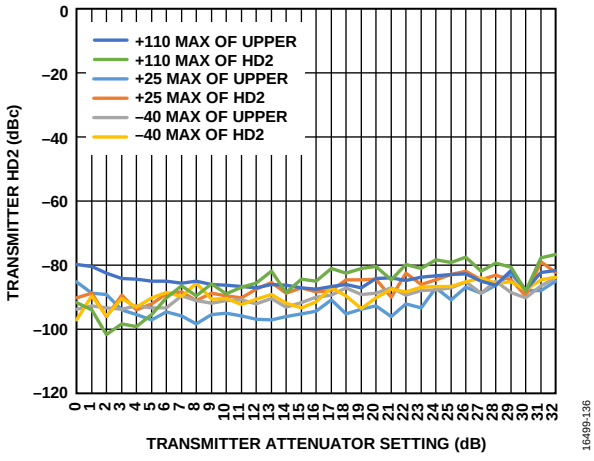


Figure 160. Transmitter HD2 vs. Transmitter Attenuation Setting, Baseband Frequency = 10 MHz, LO = 3600 MHz, Continuous Wave = −15 dBFS

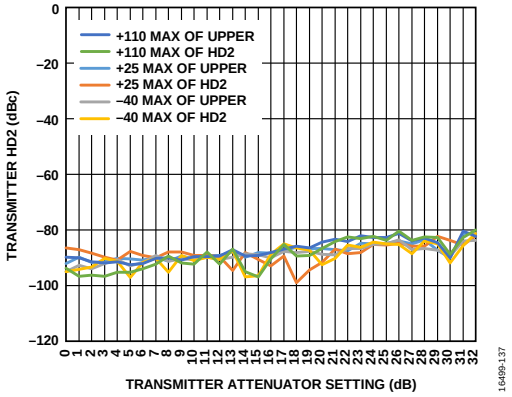


Figure 161. Transmitter HD2 vs. Transmitter Attenuation Setting, Baseband Frequency = 10 MHz, LO = 4600 MHz, Continuous Wave = −15 dBFS

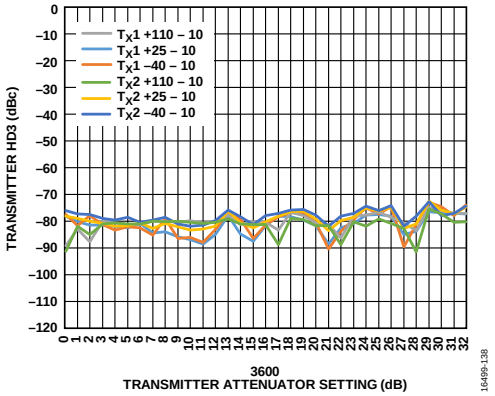


Figure 162. Transmitter HD3 vs. Transmitter Attenuation Setting, LO = 3600 MHz, Continuous Wave = −15 dBFS, Baseband Frequency = 10 MHz

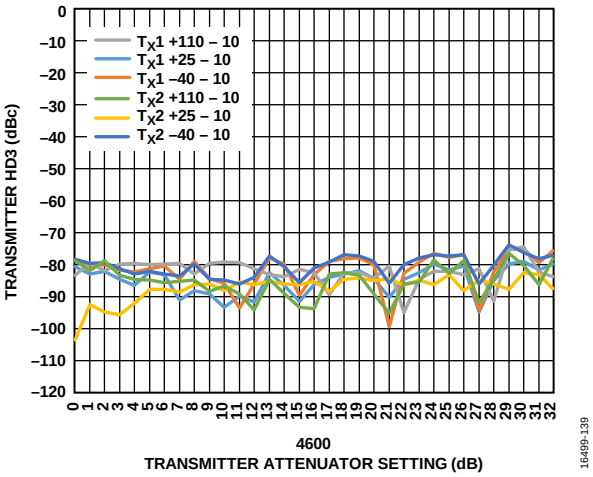


Figure 163. Transmitter HD3 vs. Transmitter Attenuation Setting, LO = 4600 MHz, Continuous Wave = −15 dBFS, Baseband Frequency = 10 MHz

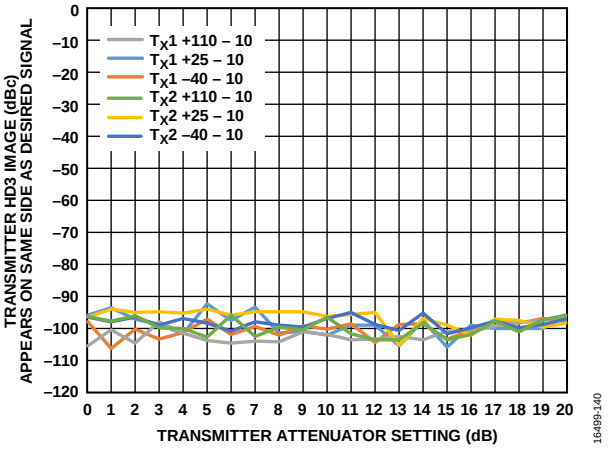


Figure 164. Transmitter HD3 Image Appears on Same Side as Desired Signal vs. Transmitter Attenuation Setting, LO = 3600 MHz, Continuous Wave = −15 dBFS

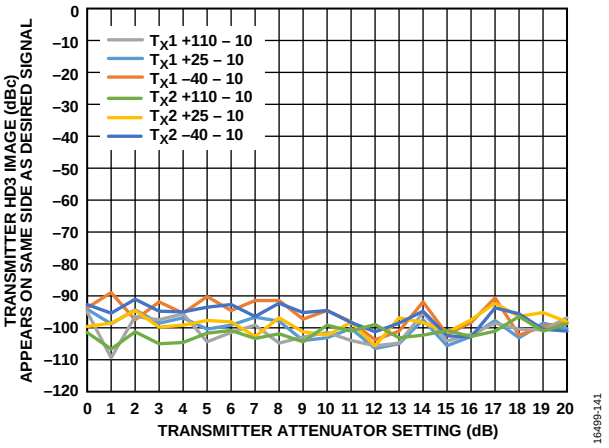


Figure 165. Transmitter HD3 Image Appears on Same Side as Desired Signal vs. Transmitter Attenuation Setting, LO = 4600 MHz, Continuous Wave = −15 dBFS

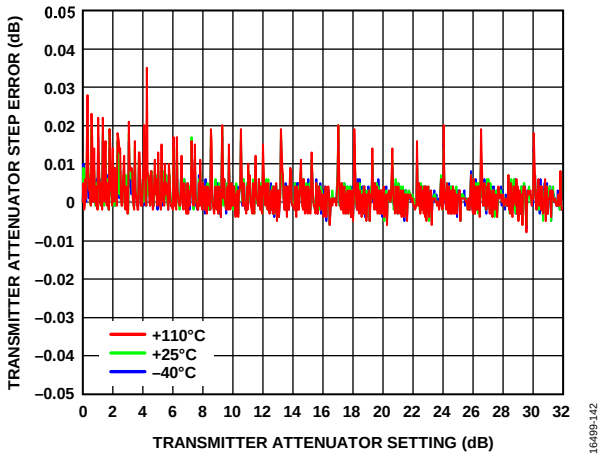


Figure 166. Transmitter Attenuator Step Error vs. Transmitter Attenuation Setting, LO = 3600 MHz

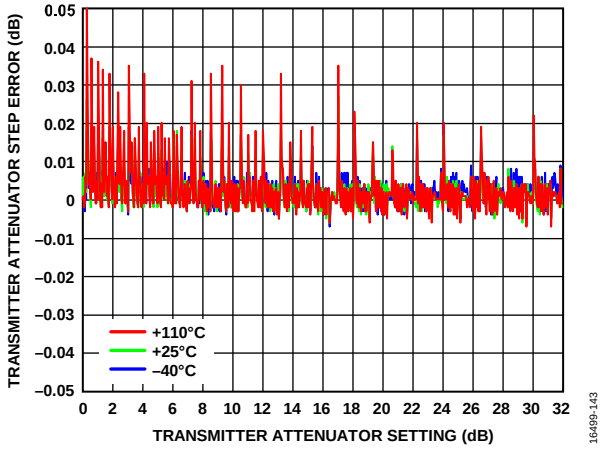


Figure 167. Transmitter Attenuator Step Error vs. Transmitter Attenuation Setting, LO = 4600 MHz

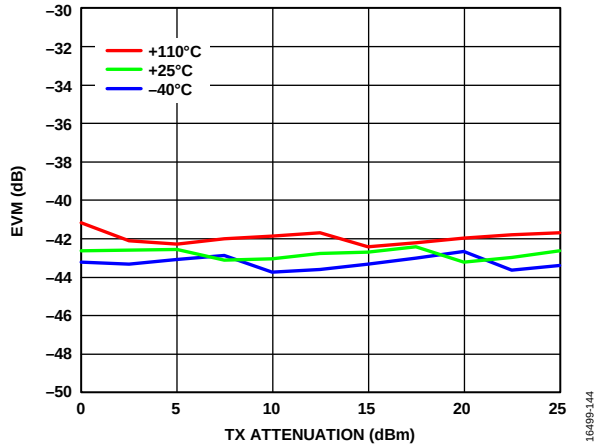


Figure 168. Transmitter EVM vs. Transmitter Attenuation, 20 MHz LTE Signal Centered on DC, LO = 3600 MHz

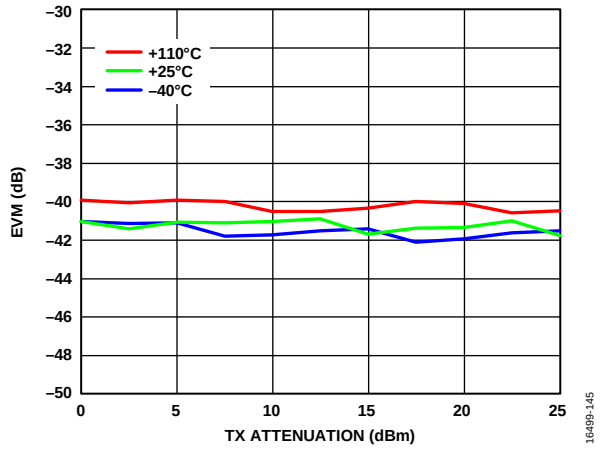


Figure 169. Transmitter EVM vs. Transmitter Attenuation, 20 MHz LTE Signal Centered on DC, LO = 4600 MHz

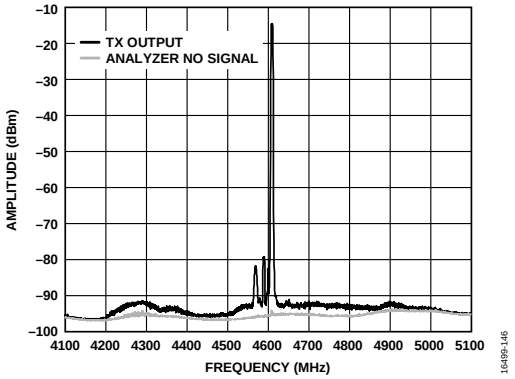


Figure 170. Amplitude vs. Frequency Transmitter Output Spurious, Transmitter 1 = 4600 MHz, LTE = 5 MHz, Offset = 10 MHz, RMS Ripple in Noise Floor Due to Spectrum Analyzer = −12 dBFS, Temperature = 25°C

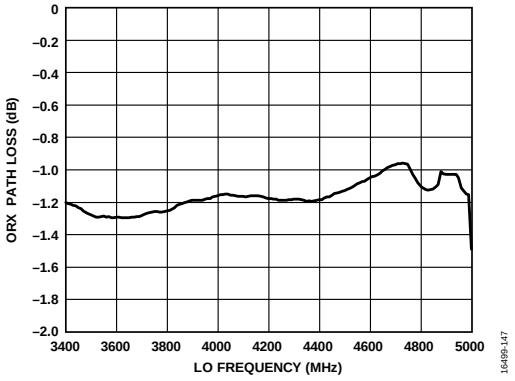


Figure 171. Observation Receiver Off Chip Matching Circuit Path Loss vs. LO Frequency (Simulation), Can Be Used for De-Embedding Performance Data

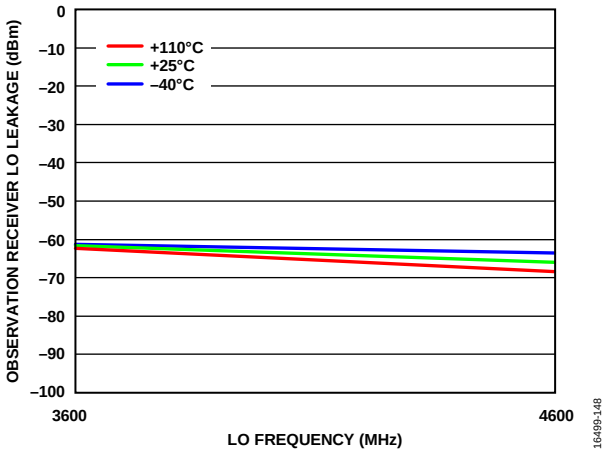


Figure 172. Observation Receiver LO Leakage vs. LO Frequency from 3600 MHz to 4600 MHz

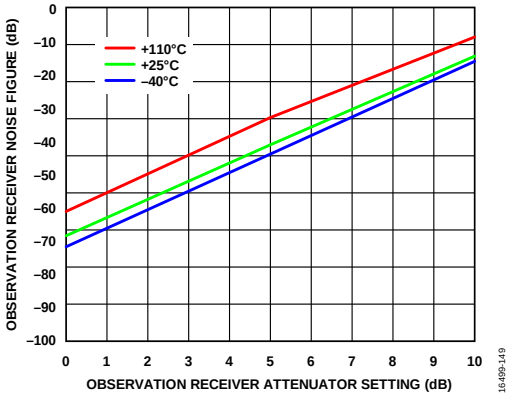


Figure 173. Observation Receiver Noise Figure vs. Observation Receiver Attenuator Setting, LO = 3600 MHz, Total Nyquist Integration Bandwidth

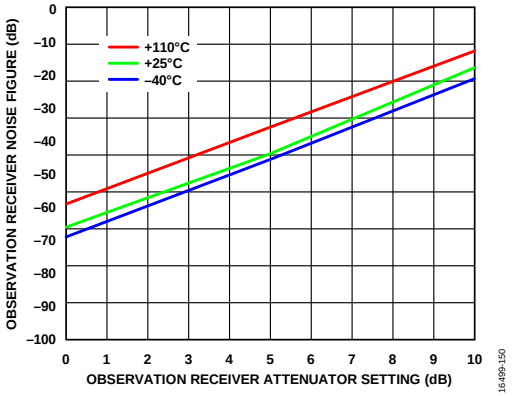


Figure 174. Observation Receiver Noise Figure vs. Observation Receiver Attenuator Setting, LO = 4600 MHz, Total Nyquist Integration Bandwidth

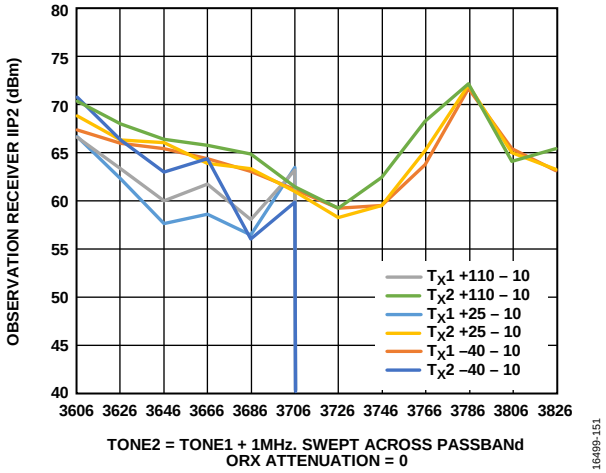


Figure 175. Observation Receiver IIP2, Sum and Difference Products vs. f1 Offset Frequency, Tones Separated by 1 MHz Swept Across Passband at −22 dBm Each, LO = 3600 MHz, Attenuation = 0 dB

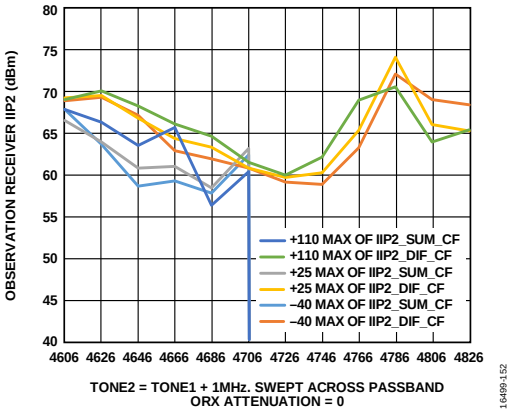


Figure 176. Observation Receiver IIP2, Sum and Difference Products vs. f1 Offset Frequency, Tones Separated By 1 MHz Swept Across Passband at –22 dBm Each, LO = 4600 MHz, Attenuation = 0 dB

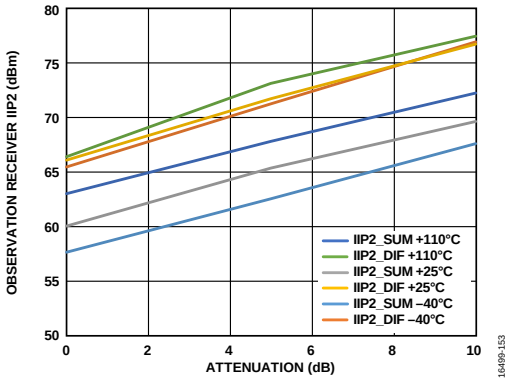


Figure 177. Observation Receiver IIP2, Sum and Difference Products vs. Attenuation, LO = 3600 MHz, Tone 1 = 3645 MHz, Tone 2 = 3646 MHz at –22 dBm Plus Attenuation

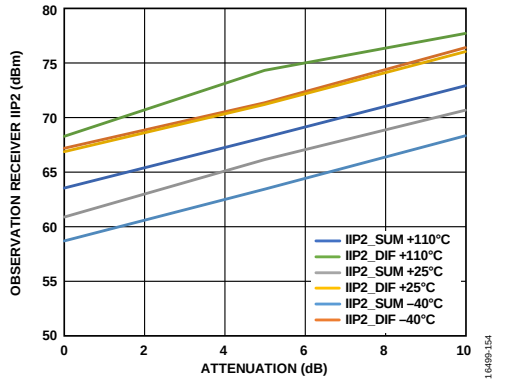


Figure 178. Observation Receiver IIP2, Sum and Difference Products vs. Attenuation, LO = 4600 MHz, Tone 1 = 4645 MHz, Tone 2 = 4646 MHz at –22 dBm Plus Attenuation

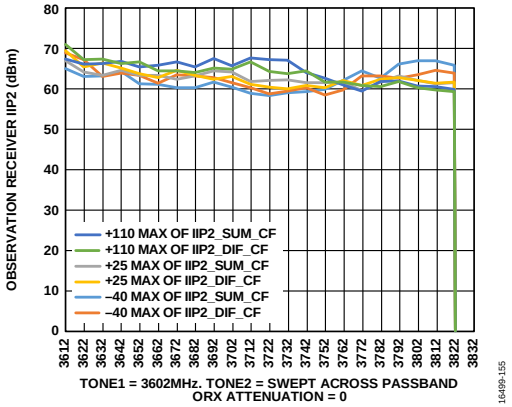


Figure 179. Observation Receiver IIP2, f1 to f2 vs. Intermodulation Frequency, LO = 3600 MHz, Tone 1 = 3602 MHz, Tone 2 Swept, –22 dBm Each, Attenuation = 0 dB

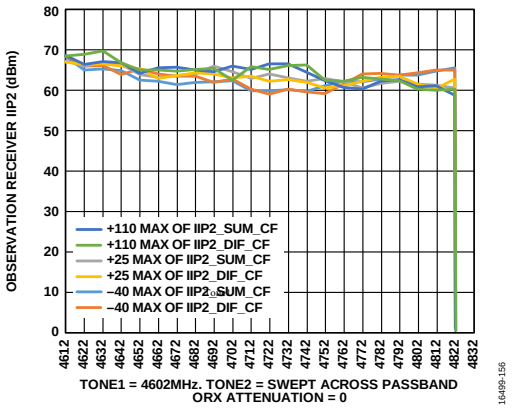


Figure 180. Observation Receiver IIP2, f1 to f2 vs. Intermodulation Frequency, LO = 4600 MHz, Tone 1 = 4602 MHz, Tone 2 Swept, –22 dBm Each, Attenuation = 0 dB

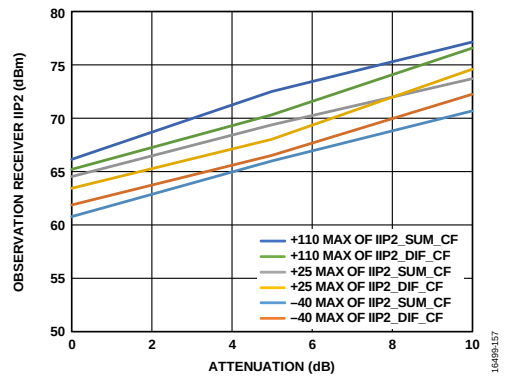


Figure 181. Observation Receiver IIP2, f1 to f2 vs. Attenuation, LO = 3600 MHz, Tone 1 = 3602 MHz, Tone 2 = 3702 MHz at –22 dBm Plus Attenuation

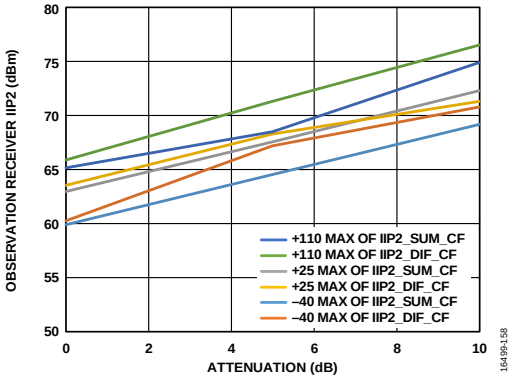


Figure 182. Observation Receiver IIP2, f1 to f2 vs. Attenuation, 4600 MHz, Tone 1 = 4602 MHz, Tone 2 = 4612 MHz at –22 dBm Plus Attenuation

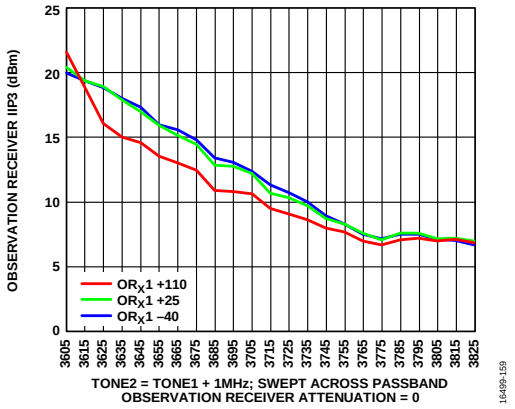


Figure 183. Observation Receiver IIP3, 2 f1 to f2 vs. f1 Offset Frequency, LO = 3600 MHz, Attenuation = 0 dB, Tones Separated by 1 MHz Swept Across Passband at –22dBm Each

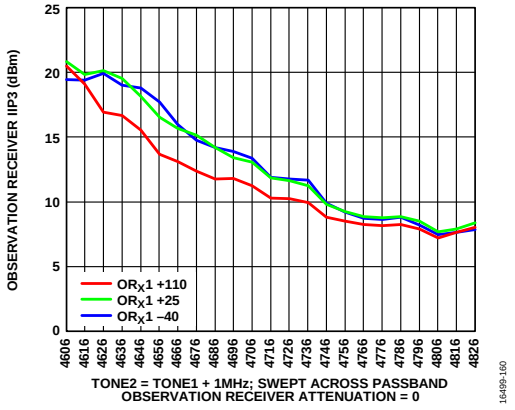


Figure 184. Observation Receiver IIP3, 2 f1 to f2vs. f1 Offset Frequency, LO = 4600 MHz, Attenuation = 0 dB, Tones Separated by 1 MHz Swept Across Passband at –22 dBm Each

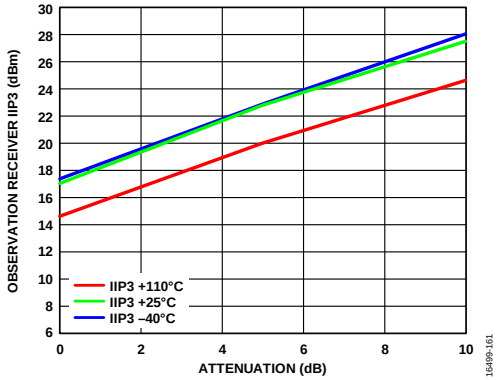


Figure 185. Observation Receiver IIP3, 2f1 to f2 vs. Attenuation, LO = 3600 MHz, Tone 1 = 3695 MHz, Tone 2 = 3696 MHz at –22 dBm Plus Attenuation

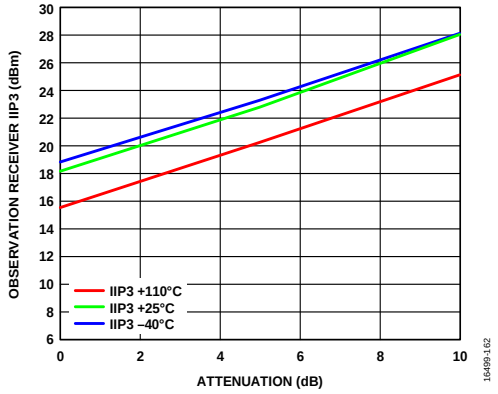


Figure 186. Observation Receiver IIP3, 2 f1 to f2 vs. Attenuation, LO = 4600 MHz, Tone 1 = 4695 MHz, Tone 2 = 4696 MHz at –22 dBm Plus Attenuation

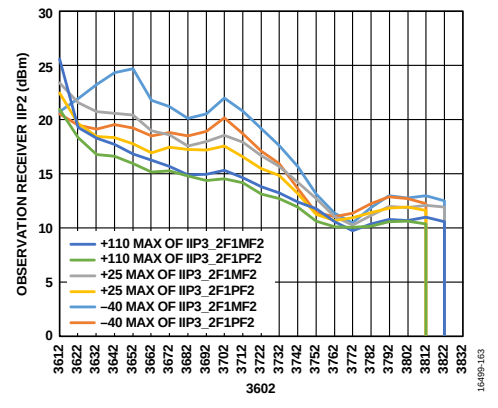


Figure 187. Observation Receiver IIP3, 2f1 to f2 vs. Intermodulation Frequency, LO = 3600 MHz, Tone 1 = 3602 MHz, Tone 2 Swept, –22 dBm Each

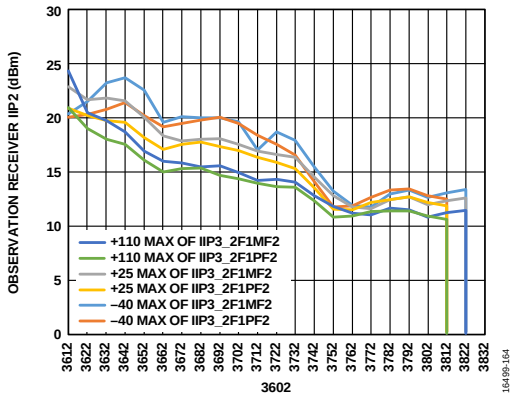


Figure 188. Observation Receiver IIP3, 2f1 to f2 vs. Intermodulation Frequency, LO = 4600 MHz, Tone 1 = 4602 MHz, Tone 2 Swept, −22 dBm Each

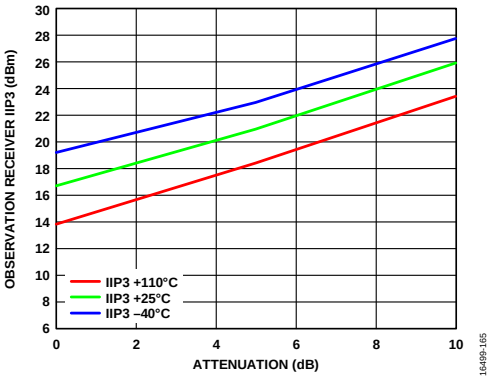


Figure 189. Observation Receiver IIP3, 2f1 to f2 vs. Attenuation, LO = 3600 MHz, Tone 1 = 3602 MHz, Tone 2 = 3722 MHz, −22 dBm Plus Attenuation Each

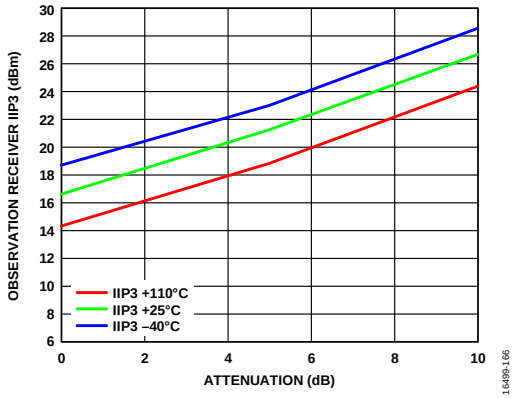


Figure 190. Observation Receiver IIP3, 2f1 to f2 vs. Attenuation, LO = 4600 MHz, Tone 1 = 4602 MHz, Tone 2 = 4722 MHz at −22 dBm Plus Attenuation Each

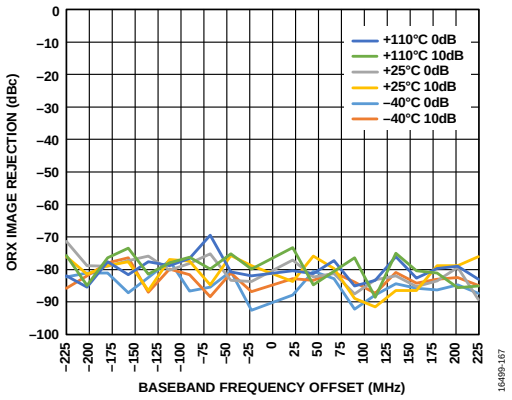


Figure 191. Observation Receiver Image Rejection vs. Baseband Frequency Offset, Continuous Wave Signal Swept Across the Band, LO = 3600 MHz

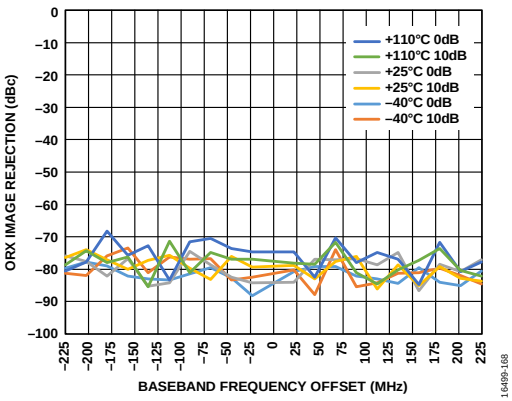


Figure 192. Observation Receiver Image Rejection vs. Baseband Frequency Offset, Continuous Wave Signal Swept Across the Band, LO = 4600 MHz

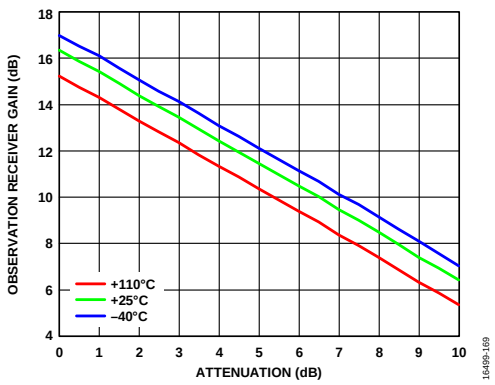


Figure 193. Observation Receiver Gain vs. Observation Receiver Attenuation, LO = 3600 MHz

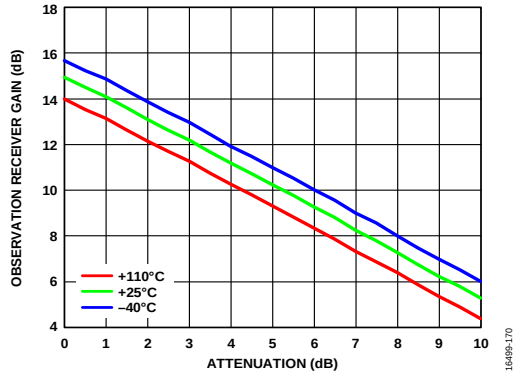


Figure 194. Observation Receiver Gain vs. Observation Receiver Attenuation, LO = 4600 MHz

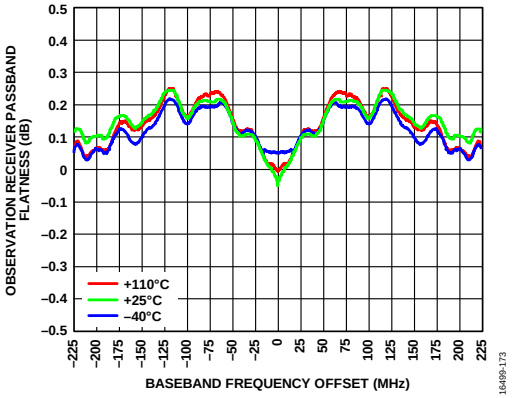


Figure 197. Observation Receiver Passband Flatness vs. Baseband Frequency Offset, LO = 3600 MHz

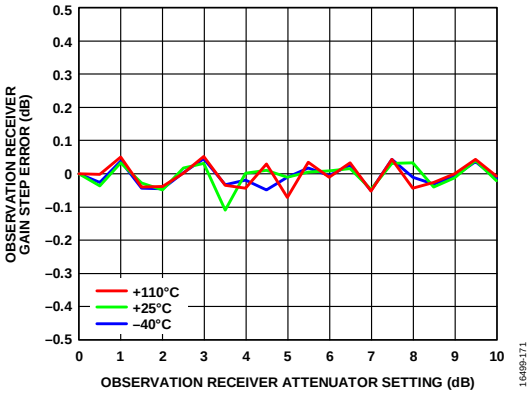


Figure 195. Observation Receiver Gain Step Error vs. Observation Receiver Attenuator Setting, LO = 3600 MHz

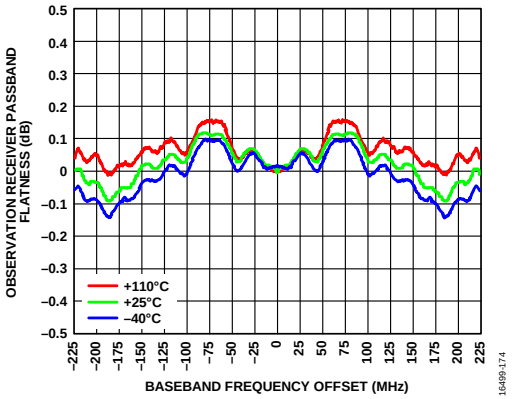


Figure 198. Observation Receiver Passband Flatness vs. Baseband Frequency Offset, LO = 4600 MHz

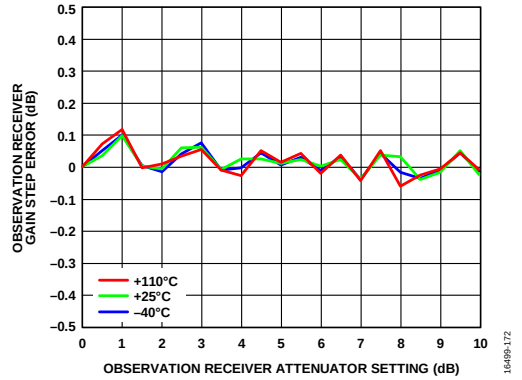


Figure 196. Observation Receiver Gain Step Error vs. Observation Receiver Attenuator Setting, LO = 4600 MHz

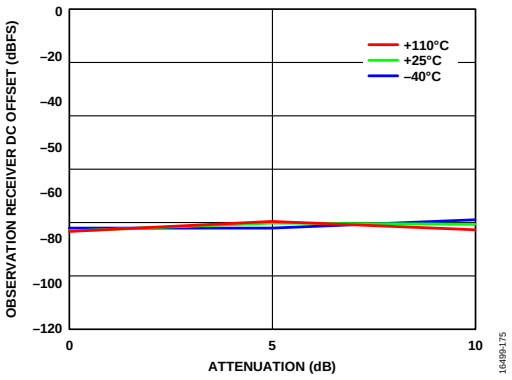


Figure 199. Observation Receiver DC Offset vs. Attenuation, LO = 3600 MHz

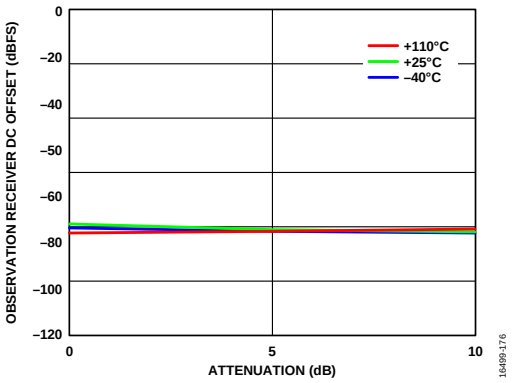


Figure 200. Observation Receiver DC Offset vs. Attenuation, LO = 4600 MHz

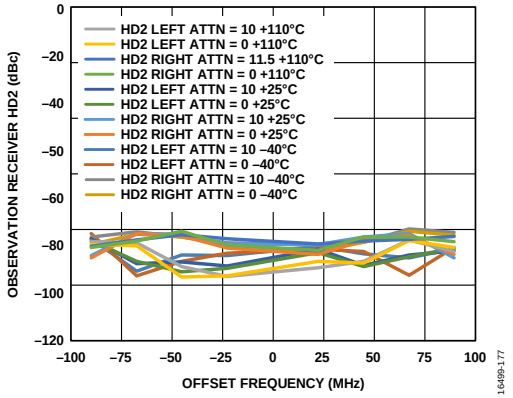


Figure 201. Observation Receiver HD2 vs. Offset Frequency, LO = 3600 MHz, Tone Level = –20 dBm Plus Attenuation

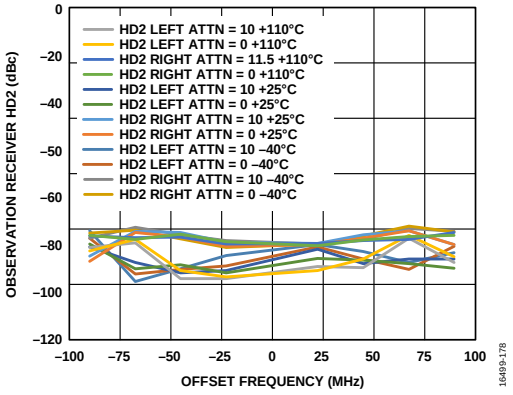


Figure 202. Observation Receiver HD2 vs. Offset Frequency, LO = 4600 MHz, Tone Level = –20 dBm Plus Attenuation

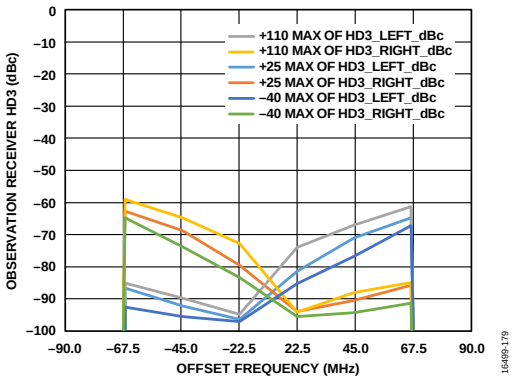


Figure 203. Observation Receiver HD3, Left and Right vs. Offset Frequency, LO = 3600 MHz, Tone Level = –20 dBm

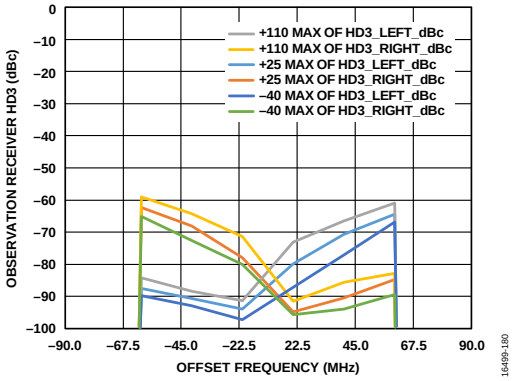


Figure 204. Observation Receiver HD3, Left and Right vs. Offset Frequency, LO = 4600 MHz, Tone Level = –20 dBm

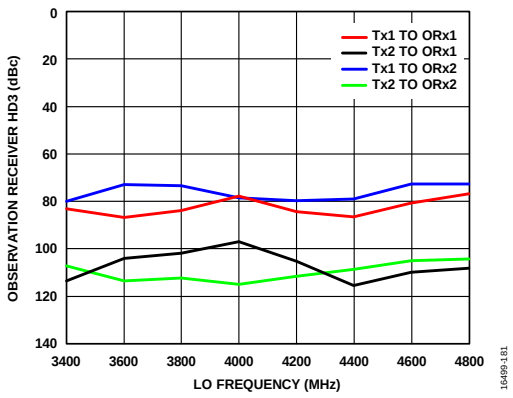


Figure 205. Transmitter to Observation Receiver Isolation vs. LO Frequency, Temperature = 25°C

Figure 206. LO Phase Noise vs. Frequency Offset, LO = 3800 MHz, RMS Phase Error Integrated from 2 kHz to 18 MHz, PLL Loop Bandwidth = 300 kHz, Spectrum Analyzer Limits Far Out Noise

5100 MHz TO 5900 MHz BAND

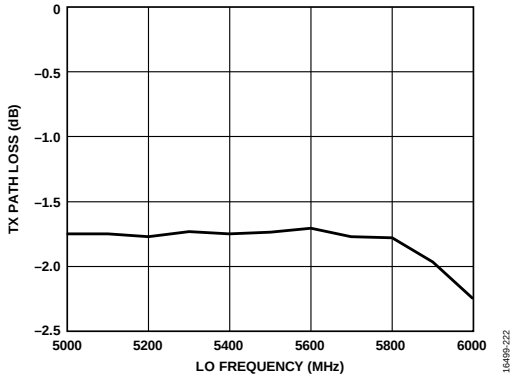


Figure 207. Transmitter Path Loss vs. LO Frequency (Simulation), Useful for De-Embedding Performance Data

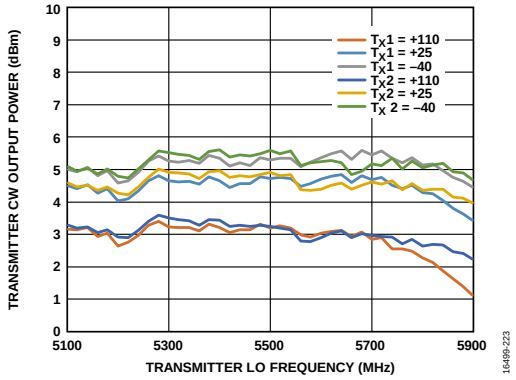


Figure 208. Transmitter Continuous Wave Output Power vs. Transmitter LO Frequency, Transmitter QEC, and External LO Leakage Active, Bandwidth Mode = 200 MHz/450 MHz, IQ Rate = 491.52 MHz, Attenuation = 0 dB, Not De-Embedded

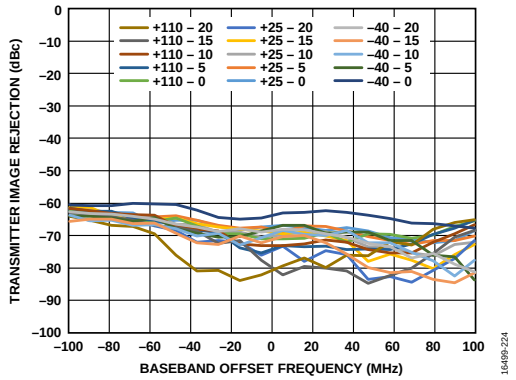


Figure 209. Transmitter Image Rejection Across Large Signal Bandwidth vs. Baseband Offset Frequency QEC Trained with Three Tones Placed at 10 MHz, 50 MHz, and 100 MHz (Tracking On), Total Combined Power = –6 dBFS, Correction Then Frozen (Tracking Turned Off), Continuous Wave Tone Swept Across Large Signal Bandwidth, LO = 5100 MHz

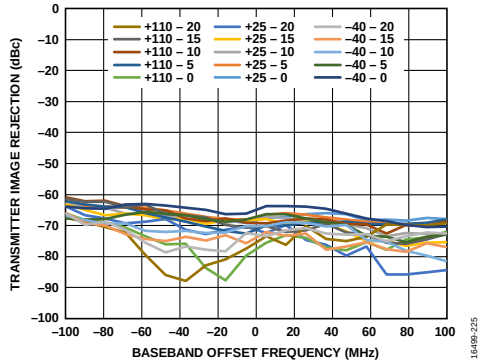


Figure 210. Transmitter Image Rejection Across Large Signal Bandwidth vs. Baseband Offset Frequency, QEC Trained with Three Tones Placed at 10 MHz, 50 MHz, and 100 MHz (Tracking On), Total Combined Power = –6 dBFS, Correction Then Frozen (Tracking Turned Off), Continuous Wave Tone Swept Across Large Signal Bandwidth, LO = 5500 MHz

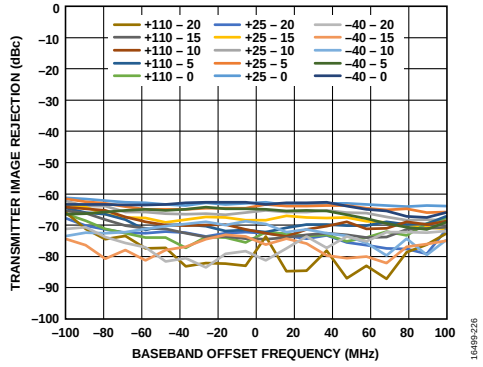


Figure 211. Transmitter Image Rejection Across Large Signal Bandwidth vs. Baseband Offset Frequency, QEC Trained with Three Tones Placed at 10 MHz, 50 MHz, and 100 MHz (Tracking On), Total Combined Power = –6 dBFS, Correction Then Frozen (Tracking Turned Off), Continuous Wave Tone Swept Across Large Signal Bandwidth, LO = 5900 MHz

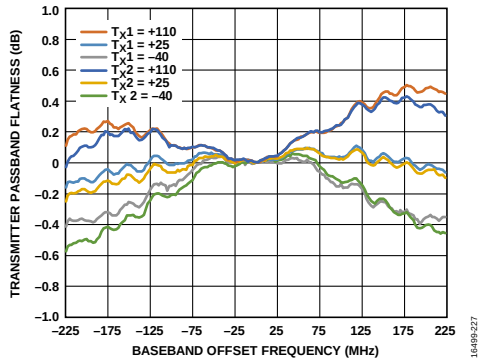


Figure 212. Transmitter Passband Flatness vs. Baseband Offset Frequency, Off-Chip Match Response De-Embedded, LO = 5700 MHz, Measurements Performed with Device Calibrated at 25°C

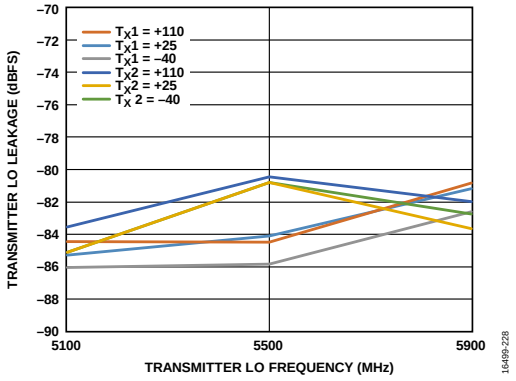


Figure 213. Transmitter LO Leakage vs. Transmitter LO Frequency, Transmitter Attenuation = 0 dB

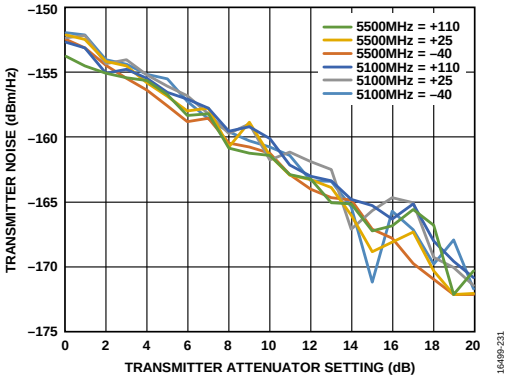


Figure 216. Transmitter Noise vs. Transmitter Attenuation Setting;

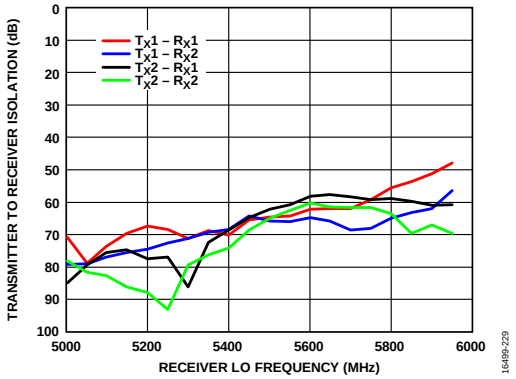


Figure 214. Transmitter to Receiver Isolation vs. Receiver LO Frequency, Temperature = 25°C

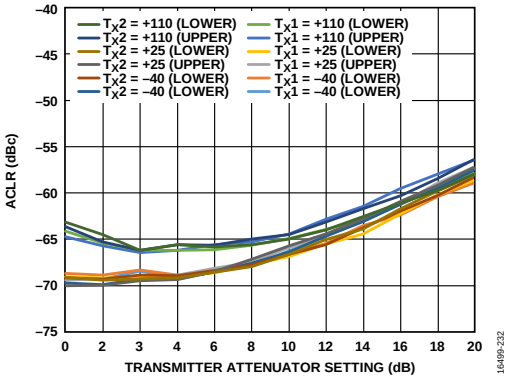


Figure 217. Transmitter Adjacent Channel Leakage Ratio (ACLR) vs. Transmitter Attenuation Setting, LO = 5100 MHz, LTE 20 MHz PAR = 12 dB, DAC Boost Normal, Upper Side and Lower Side, Decreasing ACLR at Higher Attenuation due to Spectrum Analyzer Noise Floor

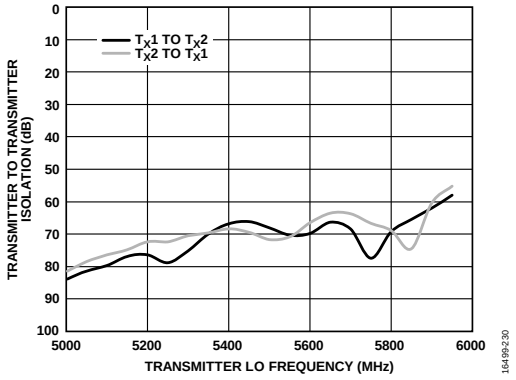


Figure 215. Transmitter to Transmitter Isolation vs. Transmitter LO Frequency; Temperature = 25°C

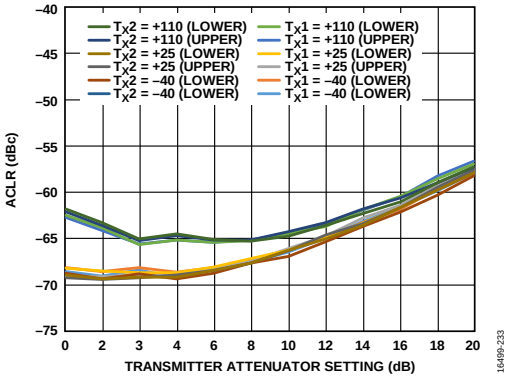


Figure 218. Transmitter Adjacent Channel Leakage Ratio (ACLR) vs. Transmitter Attenuation Setting, LO = 5500 MHz, LTE 20 MHz PAR = 12 dB, DAC Boost Normal; Upper Side and Lower Side, Decreasing ACLR at Higher Attenuation due to Spectrum Analyzer Noise Floor

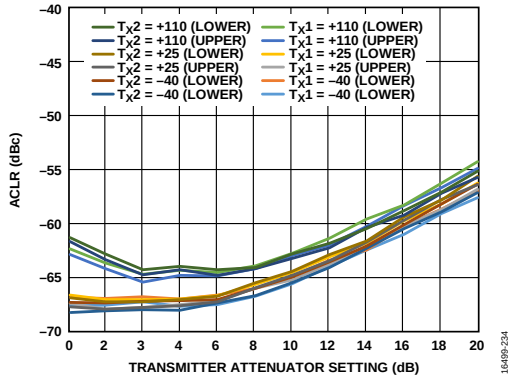


Figure 219. Transmitter Adjacent Channel Leakage Ratio vs. Transmitter Attenuation Setting, LO = 5900 MHz, LTE 20 MHz PAR = 12 dB, DAC Boost Normal, Upper Side and Lower Side, Decreasing ACLR at Higher Attenuation Due to Spectrum Analyzer Noise Floor

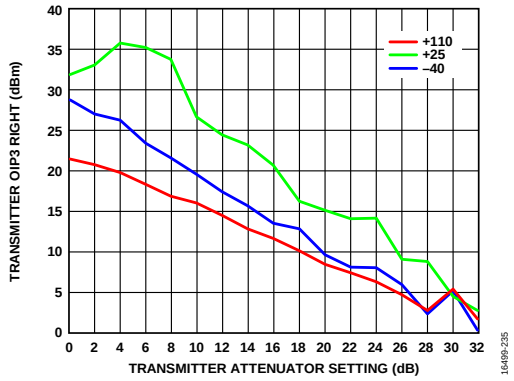


Figure 220. Transmitter OIP3, Right vs. Transmitter Attenuation Setting, LO = 5100 MHz, Total RMS Power = −12 dBFS

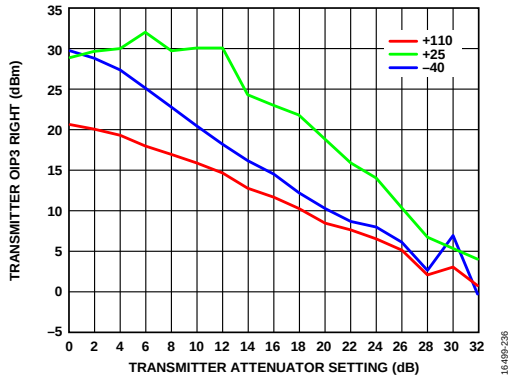


Figure 221. Transmitter OIP3, Right vs. Transmitter Attenuation Setting, LO = 5500 MHz, Total RMS Power = −12 dBFS

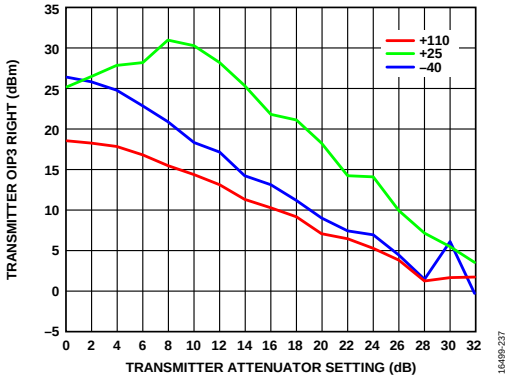


Figure 222. Transmitter OIP3, Right vs. Transmitter Attenuation Setting, LO = 5800 MHz, Total RMS Power = −12 dBFS

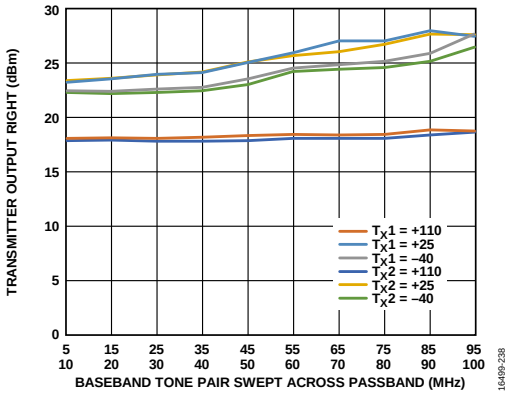


Figure 223. Transmitter OIP3, Right vs. Baseband Frequency Offset, LO = 5100 MHz, Total RMS Power = −12 dBFS Power, Transmitter Attenuation = 4 dB

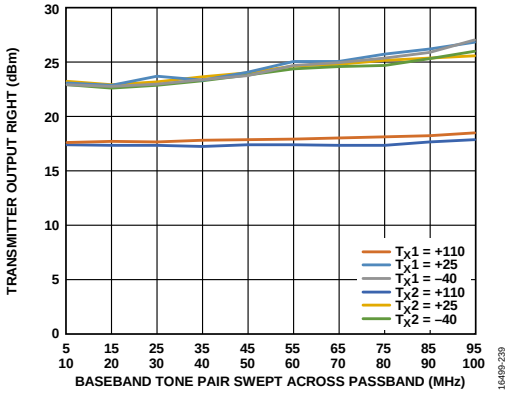


Figure 224. Transmitter OIP3, Right vs. Baseband Frequency Offset, LO = 5500 MHz, Total RMS Power = −12 dBFS, Transmitter Attenuation = 4 dB

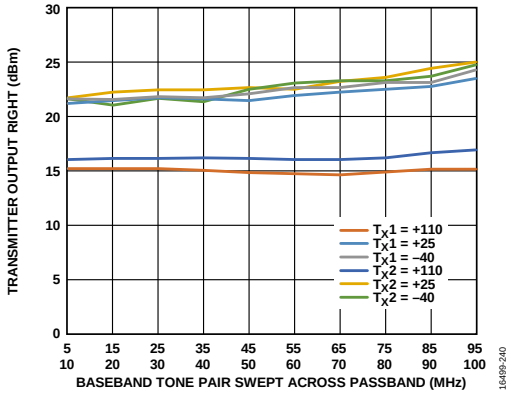


Figure 225. Transmitter Output, Right vs. Baseband Frequency Offset, LO = 5900 MHz, Total RMS Power = −12 dBFS, Transmitter Attenuation = 4 dB

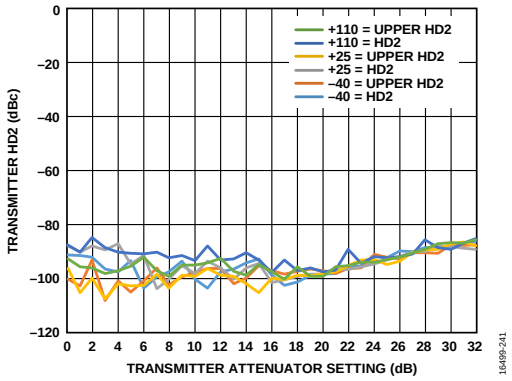


Figure 226. Transmitter HD2 vs. Transmitter Attenuation Setting, Baseband Frequency = 10 MHz, LO = 5100 MHz, Continuous Wave = −15 dBFS

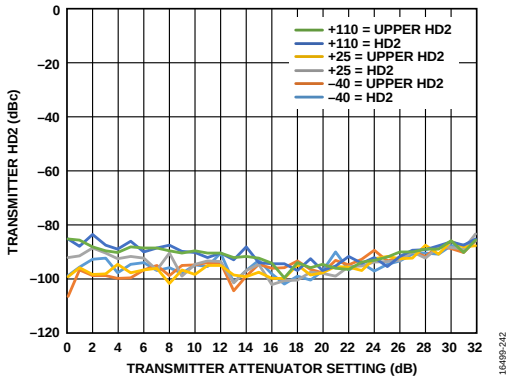


Figure 227. Transmitter HD2 vs. Transmitter Attenuation Setting, Baseband Frequency = 10 MHz, LO = 5500 MHz, Continuous Wave = −15 dBFS

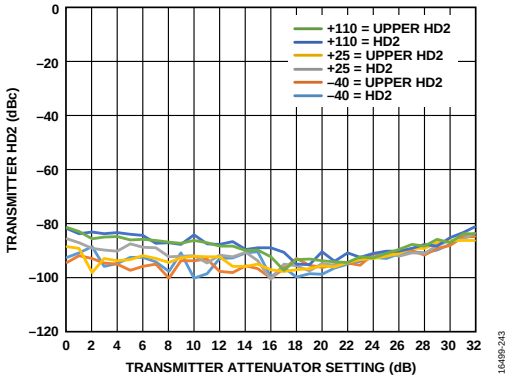


Figure 228. Transmitter HD2 vs. Transmitter Attenuation Setting, Baseband Frequency = 10 MHz, LO = 5900 MHz, Continuous Wave = −15 dBFS

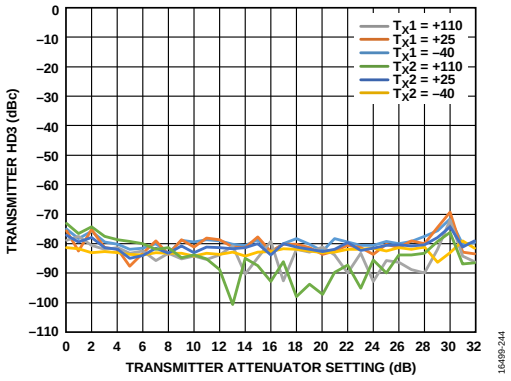


Figure 229. Transmitter HD3 on Opposite Sideband vs. Transmitter Attenuation Setting, LO = 5100 MHz, Continuous Wave = −15 dBFS, Baseband Frequency = 10 MHz

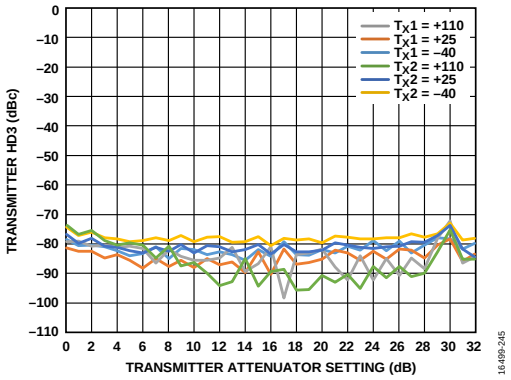


Figure 230. Transmitter HD3 on Opposite Sideband vs. Transmitter Attenuation Setting, LO = 5500 MHz, Continuous Wave = −15 dBFS, Baseband Frequency = 10 MHz

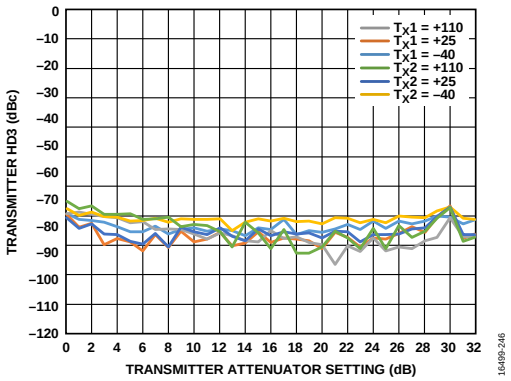


Figure 231. Transmitter HD3 on Opposite Sideband vs. Transmitter Attenuation Setting, LO = 5900 MHz, Continuous Wave = −15 dBFS, Baseband Frequency = 10 MHz

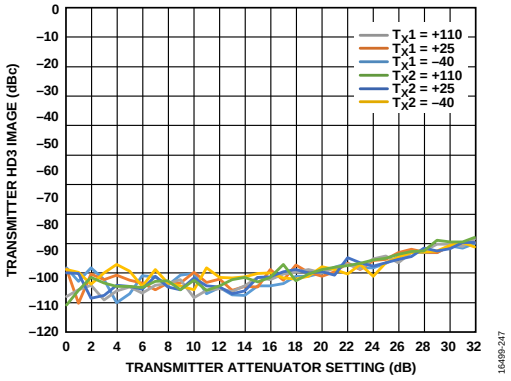


Figure 232. Transmitter HD3 on Same Sideband as Signal vs. Transmitter Attenuation Setting, LO = 5100 MHz, Continuous Wave = −15 dBFS

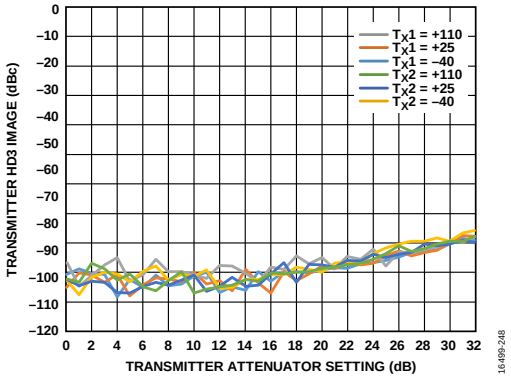


Figure 233. Transmitter HD3 on Same Sideband as Signal vs. Transmitter Attenuation Setting, LO = 5500 MHz, Continuous Wave = −15 dBFS

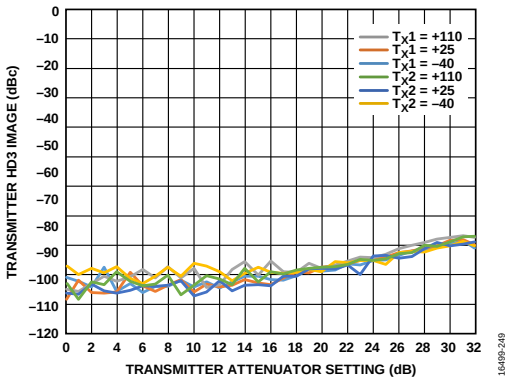


Figure 234. Transmitter HD3 on Same Sideband as Signal vs. Transmitter Attenuation Setting, LO = 5900 MHz, Continuous Wave = −15 dBFS

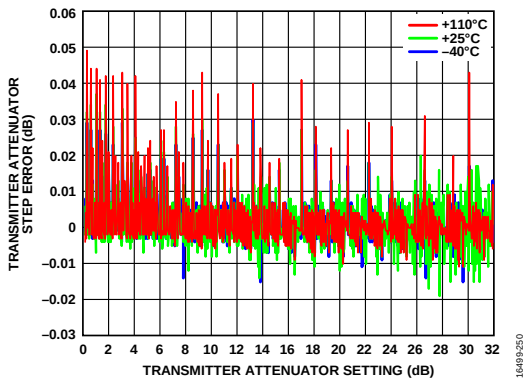


Figure 235. Transmitter Attenuation Step Error vs. Transmitter Attenuation Setting, LO = 5100 MHz

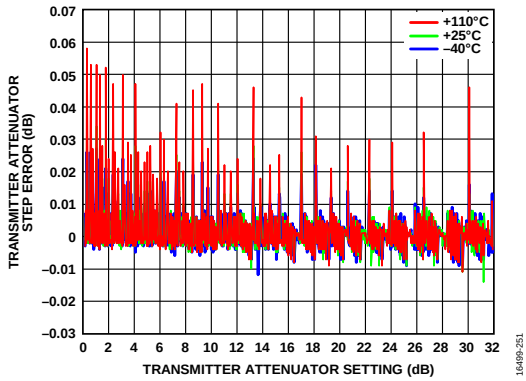


Figure 236. Transmitter Attenuation Step Error vs. Transmitter Attenuation Setting, LO = 5500 MHz

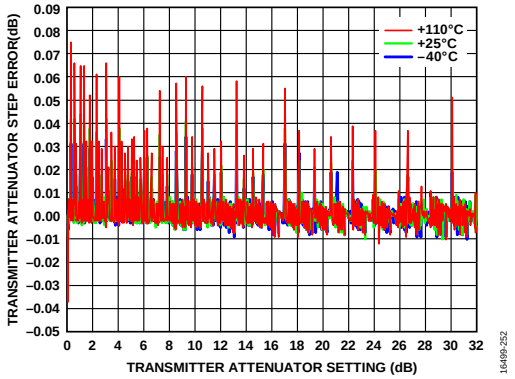


Figure 237. Transmitter Attenuator Step Error vs. Transmitter Attenuation Setting, LO = 5900 MHz

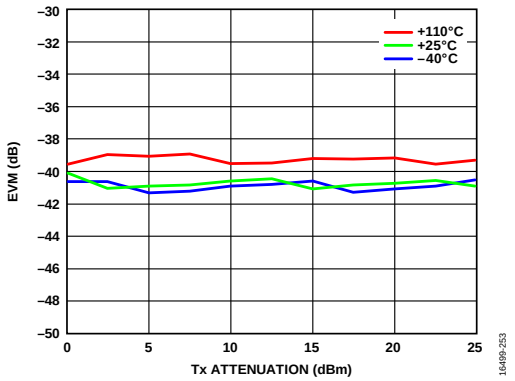


Figure 238. Transmitter EVM vs. Transmitter Attenuation, LTE Signal = 20 MHz Centered on DC, LO = 5100 MHz

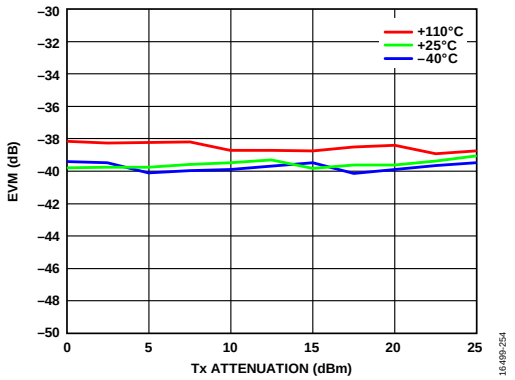


Figure 239. Transmitter EVM vs. Transmitter Attenuation, LTE Signal = 20 MHz, Centered on DC, LO = 5500 MHz

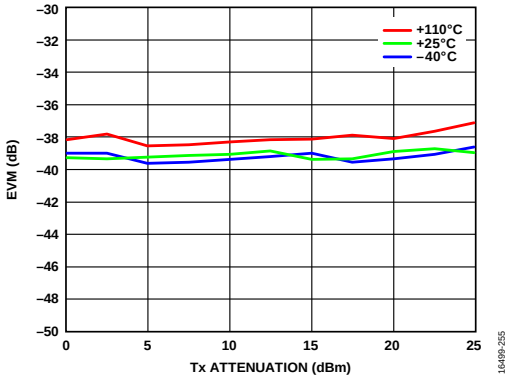


Figure 240. Transmitter EVM vs. Transmitter Attenuation, LTE Signal = 20 MHz, Centered on DC, LO = 5900 MHz

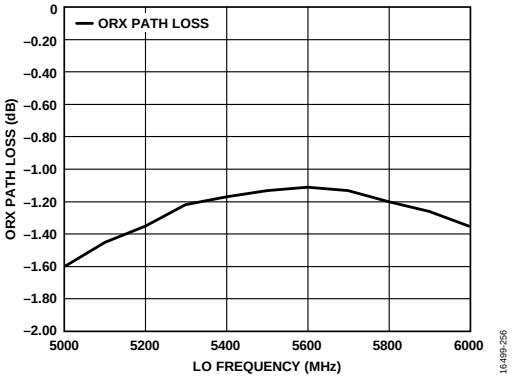


Figure 241. Observation Receiver Path Loss vs. LO Frequency (Simulation), Can Be Used for De-Embedding Performance Data

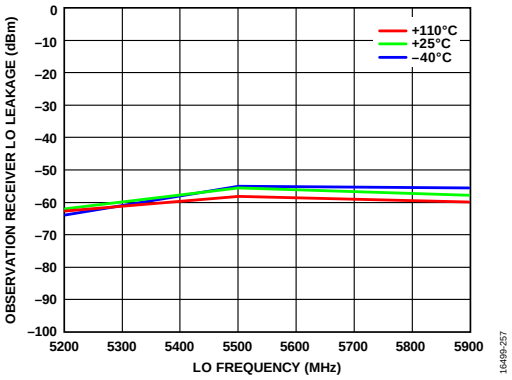


Figure 242. Observation Receiver LO Leakage vs. LO Frequency, 5200 MHz, 5500 MHz, and 5900 MHz

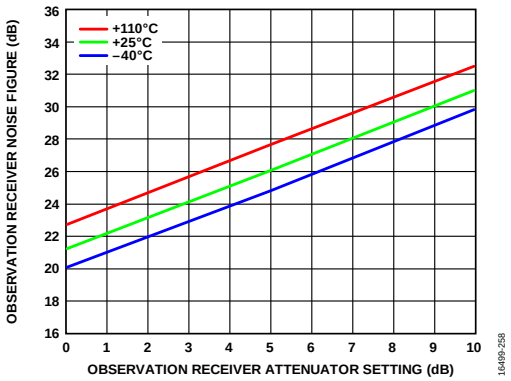


Figure 243. Observation Receiver Noise Figure vs. Observation Receiver Attenuator Setting, 5200 MHz, Total Nyquist Integration Bandwidth

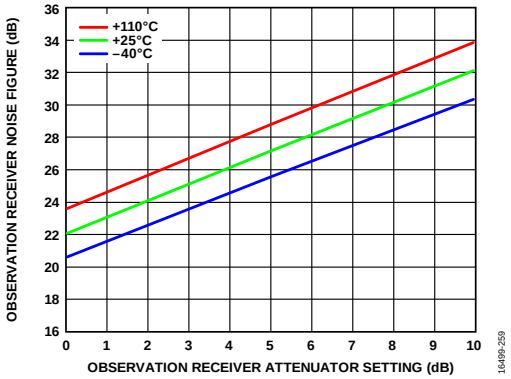


Figure 244. Observation Receiver Noise Figure vs. Observation Receiver Attenuator Setting, 5500 MHz, Total Nyquist Integration Bandwidth

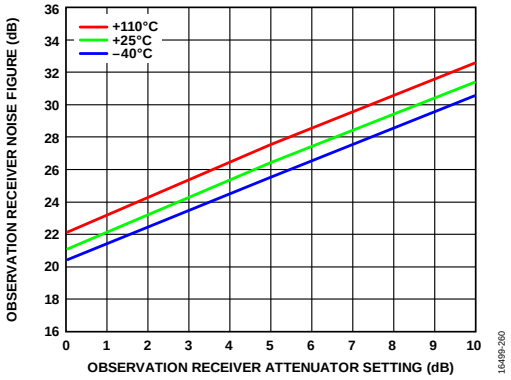


Figure 245. Observation Receiver Noise Figure vs. Observation Receiver Attenuator Setting, 5800 MHz, Total Nyquist Integration Bandwidth

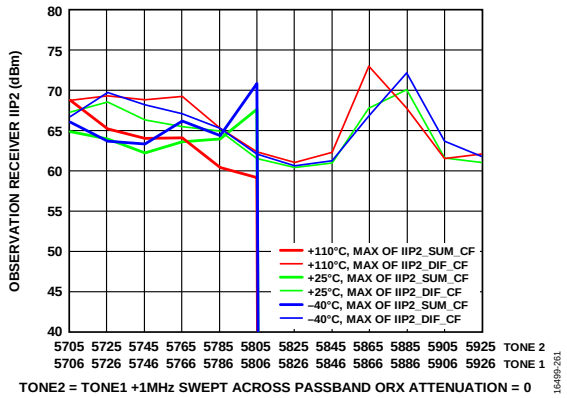


Figure 246. Observation Receiver IIP2, Sum and Difference Products vs. f1 Offset Frequency, Tones Separated By 1 MHz Swept Across Passband at –19 dBm Each, 5700 MHz, Attenuation = 0 dB

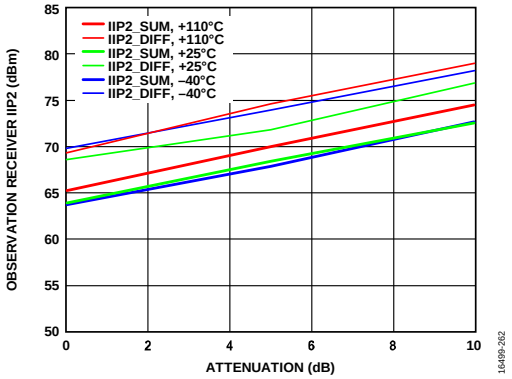


Figure 247. Observation Receiver IIP2, Sum and Difference Products vs. Attenuation, LO = 5700 MHz, Tone 1 =5725 MHz, Tone 2 = 5726 MHz at –19 dBm Plus Attenuation

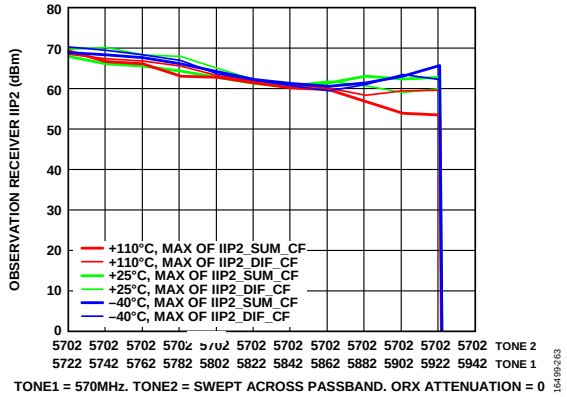


Figure 248. Observation Receiver IIP2, f1 to f2 vs. Intermodulation Frequency, LO = 5700 MHz, Tone 1 = 5702 MHz, Tone 2 Swept, –19 dBm Each, Attenuation = 0 dB

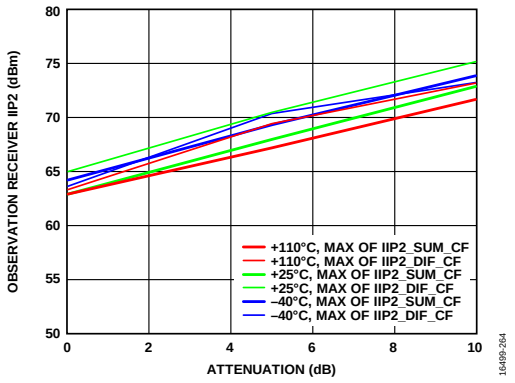


Figure 249. Observation Receiver IIP2, f1 to f2 vs. Attenuation, LO = 5700 MHz, Tone 1 = 5702 MHz, Tone 2 = 5802 MHz at –19 dBm Plus Attenuation

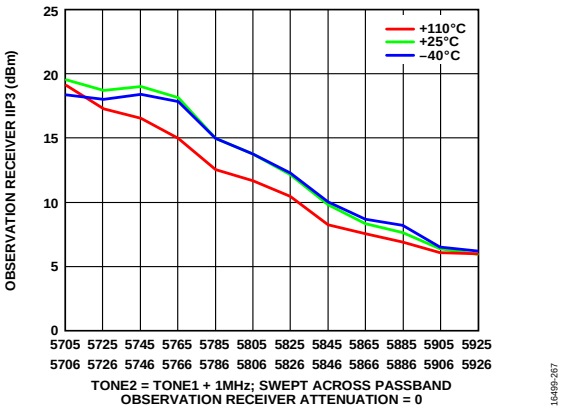


Figure 252. Observation Receiver IIP3, 2f1 to f2 vs. Attenuation, LO = 5700 MHz, Tone 1 = 5702 MHz, Tone 2 = 5722 MHz at –22 dBm Plus Attenuation Each

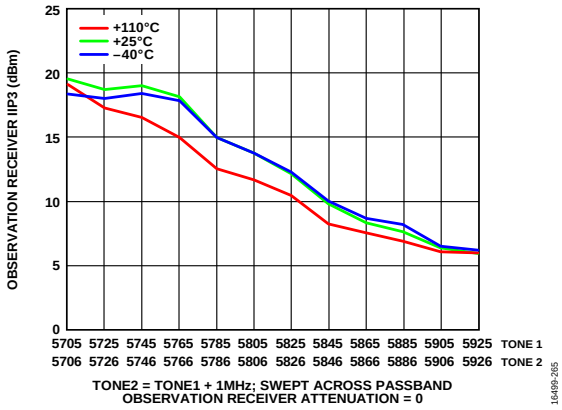


Figure 250. Observation Receiver IIP3, 2f1 to f2 vs. f1 Offset Frequency, LO = 5700 MHz, 0 dB Attenuation, Tones Separated by 1 MHz Swept Across Passband at –19 dBm Each

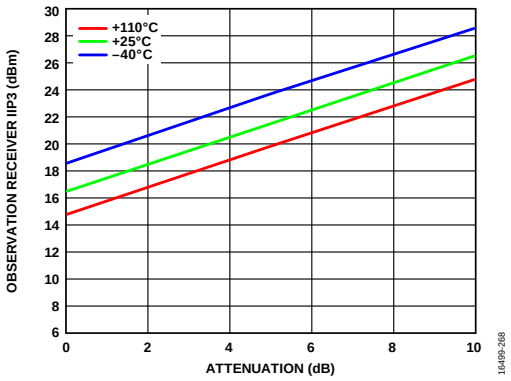


Figure 253. Observation Receiver IIP3, 2f1 to f2 vs. Attenuation, LO = 5700 MHz, Tone 1 = 5702 MHz, Tone 2 = 5822 MHz at –19 dBm Plus Attenuation

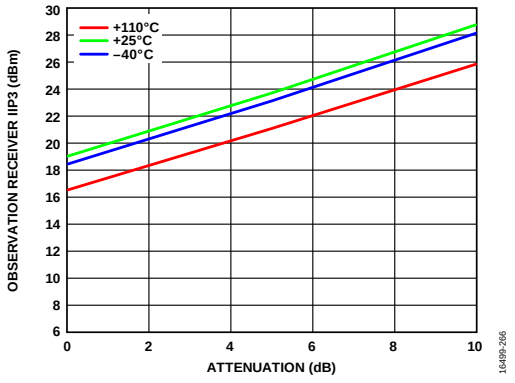


Figure 251. Observation Receiver IIP3, 2f1 to f2 vs. Attenuation, LO = 5700 MHz, Tone 1 = 5745 MHz, Tone 2 = 5746 MHz at –19 dBm Plus Attenuation

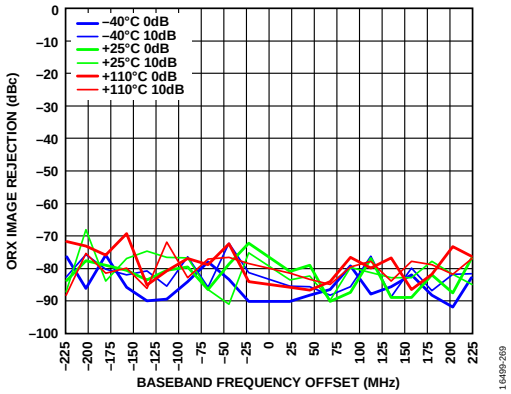


Figure 254. Observation Receiver Image Rejection vs. Observation Receiver Attenuation, Continuous Wave Signal Swept Across the Band, LO = 5200 MHz

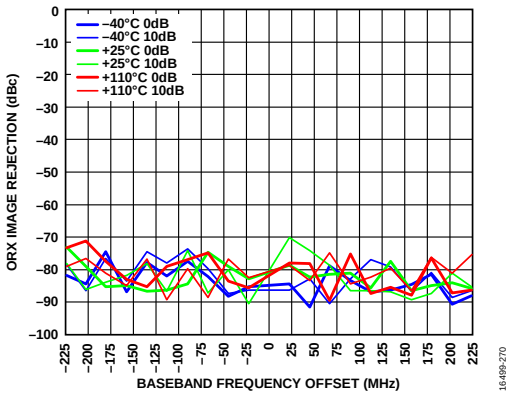


Figure 255. Observation Receiver Image Rejection vs. Baseband Frequency Offset and Observation Receiver Attenuation, Continuous Wave Signal Swept Across the Band, LO = 5700 MHz

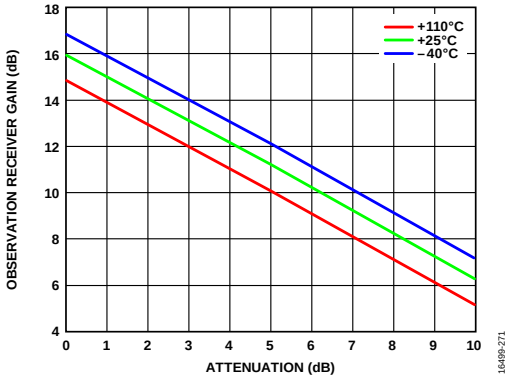


Figure 256. Observation Receiver Gain vs. Attenuation, LO = 5200 MHz

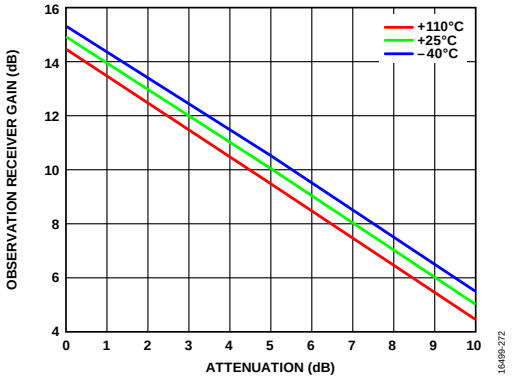


Figure 257. Observation Receiver Gain vs. Attenuation, LO = 5700 MHz

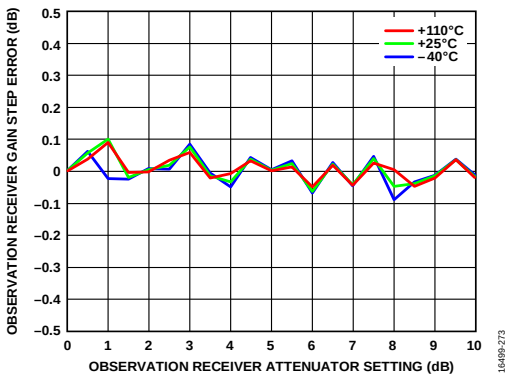


Figure 258. Observation Receiver Gain Step Error vs. Observation Receiver Attenuator Setting, LO = 5200 MHz

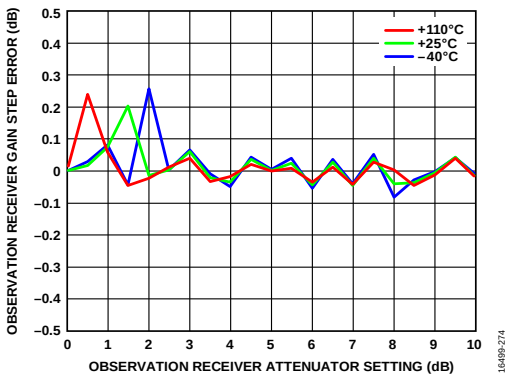


Figure 259. Observation Receiver Gain Step Error vs. Observation Receiver Attenuator Setting, LO = 5600 MHz

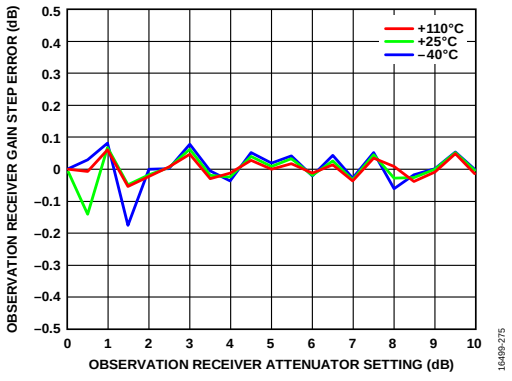


Figure 260. Observation Receiver Gain Step Error vs. Observation Receiver Attenuator Setting, LO = 5600 MHz

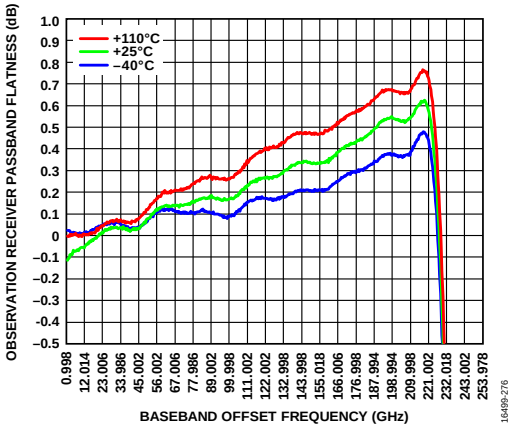


Figure 261. Observation Receiver Passband Flatness vs. Baseband Offset Frequency, LO = 5700 MHz

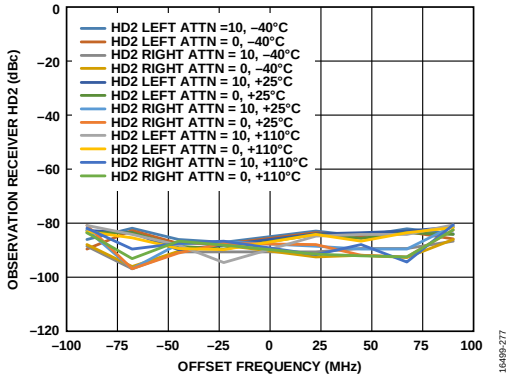


Figure 262. Observation Receiver HD2 vs. Offset Frequency, LO = 5200 MHz, Tone Level = –20 dBm Plus Attenuation

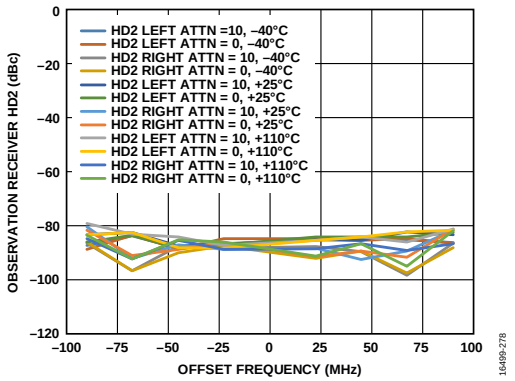


Figure 263. Observation Receiver HD2 vs. Offset Frequency, LO = 5700 MHz, Tone Level = –20 dBm Plus Attenuation

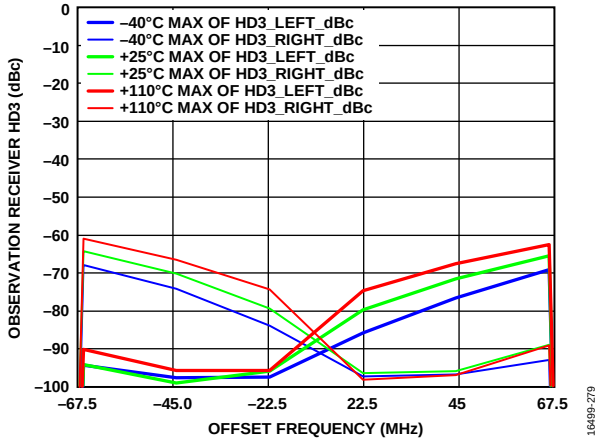


Figure 264. Observation Receiver HD3, Left and Right vs. Offset Frequency, LO = 5200 MHz, Tone Level = –20 dBm

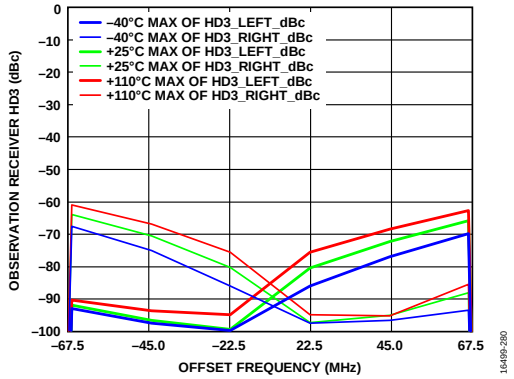


Figure 265. Observation Receiver HD3, Left and Right vs. Offset Frequency, LO = 5700 MHz, Tone Level = –20 dBm

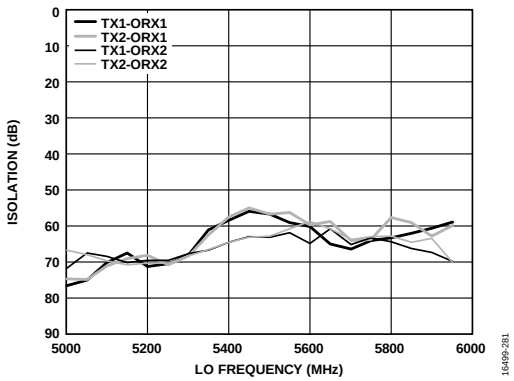


Figure 266. Transmitter to Observation Receiver Isolation vs. LO Frequency, Temperature = 25°C

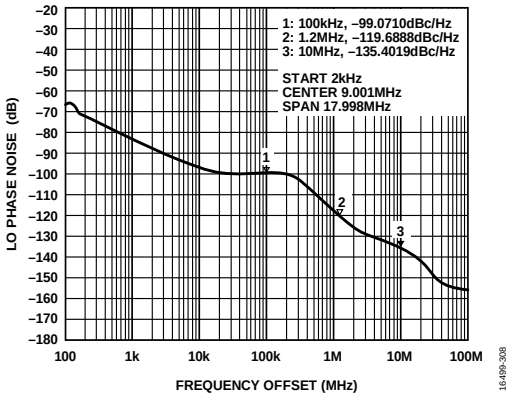


Figure 267. LO Phase Noise vs. Frequency Offset, LO = 5900 MHz, RMS Phase Error Integrated from 2 kHz to 18 MHz, PLL Loop Bandwidth > 300 kHz, Spectrum Analyzer Limits Far Out Noise

TRANSMITTER OUTPUT IMPEDANCE

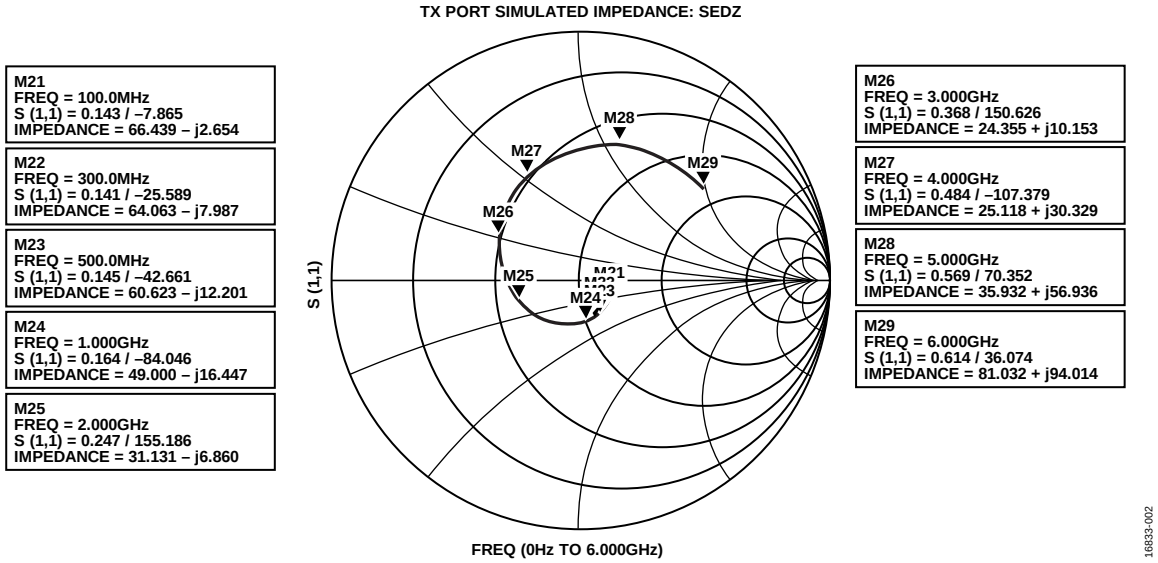


Figure 268. Transmitter Output Impedance Series Equivalent Differential Impedance (SEDZ)

OBSERVATION RECEIVER INPUT IMPEDANCE

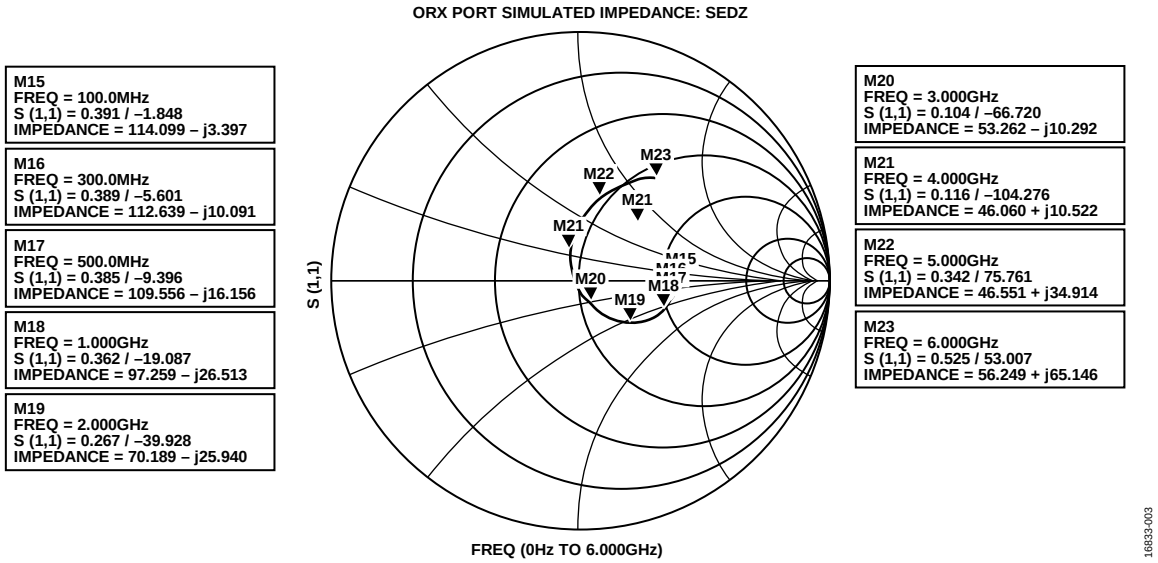


Figure 269. Observation Receiver Input Impedance SEDZ

TERMINOLOGY

Large Signal Bandwidth

Large signal bandwidth, otherwise known as instantaneous bandwidth or signal bandwidth, is the bandwidth over which there are large signals. For example, for Band 42 LTE, the large signal bandwidth is 200 MHz.

Occupied Bandwidth

Occupied bandwidth is the total bandwidth of the active signals. For example, three 20 MHz carriers have a 60 MHz occupied bandwidth, regardless of where the carriers are placed within the large signal bandwidth.

Synthesis Bandwidth

Synthesis bandwidth is the bandwidth over which digital predistortion (DPD) linearization is transmitted. Synthesis bandwidth is the 1 dB bandwidth of the transmitter. The power density of the signal outside the occupied bandwidth is assumed to be 25 dB below the signal in the occupied bandwidth. This assumes that the unlinearized power amplifier (PA) achieves 25 dB ACLR.

Observation Bandwidth

Observation bandwidth is the 1 dB bandwidth of the observation receiver. With the observation receiver sharing the transmitter LO, the observation receiver sees similar power densities, such as those in the occupied bandwidth and synthesis bandwidth of the transmitter.

Backoff

Backoff is the difference (in dB) between full scale and the rms signal power.

P_{HIGH}

P_{HIGH} is the largest signal that can be applied without overloading the ADC for the observation receiver input. Due to the nature of continuous time Σ-Δ ADCs, this input level results in slightly less than full scale at the digital output. This is because of the nature of the continuous time Σ-Δ ADCs, which, for example, exhibit a soft overload in contrast to the hard clipping of pipeline ADCs.

THEORY OF OPERATION

The ADRV9008-2 is a highly integrated RF transmitter subsystem capable of configuration for a wide range of applications. The device integrates all RF, mixed-signal, and digital blocks necessary to provide all transmitter traffic receiver, and DPD observation receiver functions in a single device. Programmability allows the transmitter to be adapted for use in many TDD and 3G/4G cellular standards. The ADRV9008-2 contains four high speed serial interface links for the transmitter chain, and two high speed links each for the receiver chain and observation receiver chain. The links are JESD204B, Subclass 1 compliant. The two receiver lanes can be reused for the observation receiver, providing a low pin count and a reliable data interface to field programmable gate arrays (FPGAs) or integrated baseband solutions.

The ADRV9008-2 also provides tracking correction of dc offset QEC errors, and transmitter LO leakage to maintain high performance under varying temperatures and input signal conditions. The device also includes test modes that allow system designers to debug designs during prototyping and to optimize radio configurations.

TRANSMITTER (Tx)

The ADRV9008-2 transmitter section consists of two identical and independently controlled channels that provide all digital processing, mixed-signal, and RF blocks necessary to implement a direct conversion system while sharing a common frequency synthesizer. The digital data from the JESD204B lanes pass through a fully programmable, 128-tap FIR filter with variable interpolation rates. The FIR output is sent to a series of interpolation filters that provide additional filtering and interpolation prior to reaching the DAC. Each 14-bit DAC has an adjustable sample rate.

When converted to baseband analog signals, the in phase (I) and quadrature (Q) signals are filtered to remove sampling artifacts and are fed to the upconversion mixers. Each transmitter chain provides a wide attenuation adjustment range with fine granularity to optimize signal-to-noise ratio (SNR).

OBSERVATION RECEIVER (ORx)

The ADRV9008-2 contains an independent DPD observation receiver (ORx) front end with two multiplexed inputs and a common digital back end that is shared with the traffic receiver. The innovative configuration enables a highly efficient shared receiver/observation receiver mode where the device can support fast switching between receiver and observation receiver mode in TDD applications. The observation receiver shares the common frequency synthesizer with the transmitter.

The observation receiver is a direct conversion system that contains a programmable attenuator stage, followed by matched I and Q mixers, baseband filters, and ADCs.

The continuous time Σ-Δ ADCs have inherent antialiasing that reduces the RF filtering requirement.

The ADC outputs can be conditioned further by a series of decimation filters and a programmable FIR filter with additional decimation settings. The sample rate of each digital filter block is adjustable by changing decimation factors to produce the desired output data rate.

CLOCK INPUT

The ADRV9008-2 requires a differential clock connected to the REF_CLK_IN_x pins. The frequency of the clock input must be between 10 MHz and 1000 MHz and must have very low phase noise because this signal generates the RF LO and internal sampling clocks.

SYNTHESIZERS

RF PLL

The ADRV9008-2 contains a fractional-N PLL to generate the RF LO for the signal paths. The PLL incorporates an internal VCO and loop filter, requiring no external components. The LOs on multiple chips can be phase synchronized to support active antenna systems and beam forming applications.

Clock PLL

The ADRV9008-2 contains a PLL synthesizer that generates all the baseband related clock signals and serialization/deserialization (SERDES) clocks. This PLL is programmed based on the data rate and sample rate requirements of the system.

SERIAL PERIPHERAL INTERFACE (SPI)

The ADRV9008-2 uses an SPI interface to communicate with the baseband processor (BBP). This interface can be configured as a 4-wire interface with dedicated receiver and transmitter ports, or it can be configured as a 3-wire interface with a bidirectional data communications port. This bus allows the BBP to set all device control parameters using a simple address data serial bus protocol.

Write commands follow a 24-bit format. The first five bits set the bus direction and the number of bytes to transfer. The next 11 bits set the address where data is written. The final 8 bits are the data transferred to the specific register address.

Read commands follow a similar format with the exception that the first 16 bits are transferred on the SDIO pin and the final eight bits are read from the ADRV9008-2, either on the SDO pin in 4-wire mode or on the SDIO pin in 3-wire mode.

JTAG BOUNDARY SCAN

The ADRV9008-2 provides support for JTAG boundary scan. There are five dual function pins associated with the JTAG interface. These pins, listed in Table 5, are used to access the on-chip test access port. To enable the JTAG functionality, set the GPIO_3 pin through the GPIO_0 pin to 1001, and then pull the TEST pin high.

POWER SUPPLY SEQUENCE

The ADRV9008-2 requires a specific power-up sequence to avoid undesired power-up currents. In the optimal power-up sequence, the VDDD1P3_DIG and the VDDA1P3_x supplies (VDDA1P3_x includes all 1.3 V domains) power up first and at the same time. If these supplies cannot be brought up simultaneously, then the VDDD1P3_DIG supply must come up first. Bring the VDDA_3P3, VDDA1P8_x, VDDA1P3_DES, and VDDA1P3_SER supplies up after the 1.3 V supplies. The VDD_INTERFACE supply can be brought up at any time. Note that no device damage occurs if this sequence is not followed. However, failure to follow this sequence may result in higher than expected power-up currents. It is also recommended to toggle the RESET signal after power stabilizes, prior to configuration. The power-down sequence is not critical. If a power-down sequence is followed, remove the VDDD1P3_DIG supply last to avoid any back biasing of the digital control lines.

GPIO_x PINS

The ADRV9008-2 provides 19, 1.8 V to 2.5 V GPIO signals that can be configured for numerous functions. When configured as outputs, certain pins can provide real-time signal information to the BBP, allowing the BBP to determine observation receiver performance. A pointer register selects the information that is output to these pins. Signals used for manual gain mode, calibration flags, state machine states, and various observation receiver parameters are among the outputs that can be monitored on these pins. Additionally, certain pins can be configured as inputs and used for various functions, such as setting the receiver gain in real time.

Twelve 3.3 V GPIO_x pins are also included on the device. These pins provide control signals to external components.

AUXILIARY CONVERTERS

AUXADC_x

The ADRV9008-2 contains an auxiliary ADC that is multiplexed to four input pins (AUXADC_x). The auxiliary ADC is 12 bits with an input voltage range of 0.05 V to VDDA_3P3 − 0.05 V. When enabled, the auxiliary ADC is free running. The SPI reads provide the last value latched at the ADC output. The auxiliary ADC can also be multiplexed to a built in, diode-based temperature sensor.

AUXDAC_x

The ADRV9008-2 contains 10 identical auxiliary DACs (AUXDAC_x) that can be used for bias or other system functionality. The auxiliary DACs are 10 bits, have an output voltage range of approximately 0.7 V to VDDA_3P3 − 0.3 V, and have a current drive of 10 mA.

JESD204B DATA INTERFACE

The digital data interface for the ADRV9008-2 uses JEDEC JESD204B Subclass 1. The serial interface operates at speeds of up to 12.288 Gbps. The benefits of the JESD204B interface include a reduction in required board area for data interface routing, resulting in smaller total system size. Four high speed serial lanes are provided for transmit and four high speed lanes are provided for observation receiver. The ADRV9008-2 supports single-lane or dual-lane interfaces as well as fixed and floating point data formats for observation receiver data.

Table 6. Observation Path Interface Rates

		JESD204B	
BW (MHz)	**Output Rate (MSPS)**	**Lane Rate (Mbps)**	**Number of Lanes**
200	245.76	9830.4	1
200	307.2	12288	1
250	307.2	12288	1
450	491.52	9830.4	2
450	491.52	4915.2	4

Table 7. Transmitter Interface Rates (Other Output Rates, Bandwidth, and JESD204B Lanes Also Supported)

		Single-Channel Operation		Dual-Channel Operation	
BW (MHz)	**Input Rate (MSPS)**	**JESD204B Lane Rate (Mbps)**	**JESD204B Number of Lanes**	**JESD204B Lane Rate (Mbps)**	**JESD204B Number of Lanes**
200	245.76	9830.4	1	9830.4	2
200	307.2	12288	1	12288	2
250	307.2	12288	1	12288	2
450	491.52	9830.4	2	9830.4	4

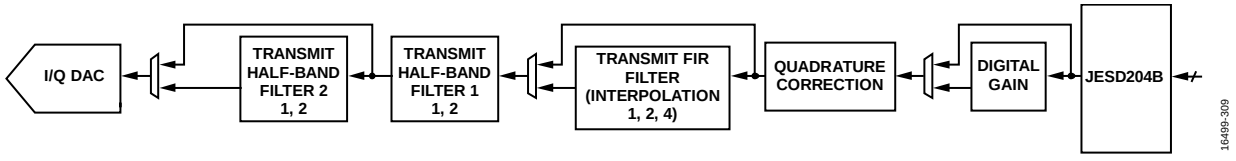


Figure 270. Transmitter Datapath Filter Implementation

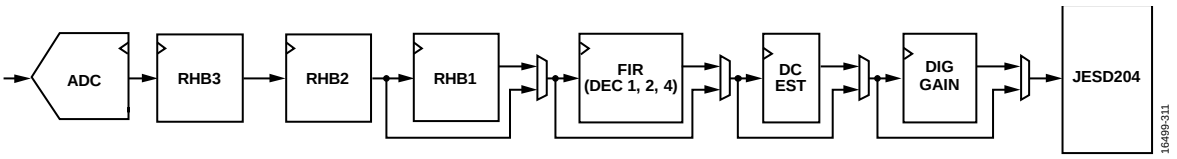


Figure 271. Observation Receiver Datapath Filter Implementation

APPLICATIONS INFORMATION

PCB LAYOUT AND POWER SUPPLY RECOMMENDATIONS

Overview

The ADRV9008-2 device is a highly integrated RF agile transceiver with significant signal conditioning integrated onto one chip. Due to the increased complexity of the device and its high pin count, careful printed circuit board (PCB) layout is important to get the optimal performance. This data sheet provides a checklist of issues to look for and guidelines on how to optimize the PCB to mitigate performance issues. The goal of this data sheet is to help achieve the optimal performance from the ADRV9008-2 while reducing board layout effort. This document assumes that the reader is an experienced analog and RF engineer who understands RF PCB layout and has an understanding of RF transmission lines. This data sheet discusses the following issues and provides guidelines for system designers to achieve the optimal performance performance for the ADRV9008-2:

- PCB material and stack up selection
- Fanout and trace space layout guidelines
- Components placement and routing guidelines
- RF and JESD transmission line layout
- Isolation techniques used on the ADRV9009 customer card
- Power management considerations
- Unused pin instructions

PCB MATERIAL AND STACKUP SELECTION

Figure 272 shows the PCB stackup used for the ADRV9008-2 customer evaluation boards. The dielectric material used on the top and the bottom layers is 8 mil Rogers 4350B. The remaining dielectric layers are FR4-370 HR. The board design uses the Rogers laminate for the top and the bottom layers for its low loss tangent at high frequencies. The ground planes under the Rogers laminate (Layer 2 and Layer 13) are the reference planes for the transmission lines routed on the outer surfaces. These layers are solid copper planes without any splits under the RF traces. Layer 2 and Layer 13 are crucial to maintaining the RF signal integrity and, ultimately, ADRV9008-2 performance. Layer 3 and Layer 12 are used to route power supply domains. To keep the RF section of the ADRV9008-2 isolated from the fast transients of the digital section, the JESD204B interface lines are routed on Layer 5 and Layer 10. Those layers have impedance control set to a 100 Ω differential. The remaining digital lines from ADRV9008-2 are routed on inner Layer 7 and inner Layer 8. RF traces on the outer layers need to be a controlled impedance to get the best performance from the device. 0.5 ounce copper or 1 ounce copper is used for the inner layers in this board. The outer layers use 1.5 ounce copper so that the RF traces are less prone to pealing. Ground planes on this board are full copper floods with no splits except for vias, through-hole components, and isolation structures. The ground planes must route entirely to the edge of the PCB under the surface-mount type A (SMA) connectors to maintain signal launch integrity. Power planes can be pulled back from the board edge to decrease the risk of shorting from the board edge.

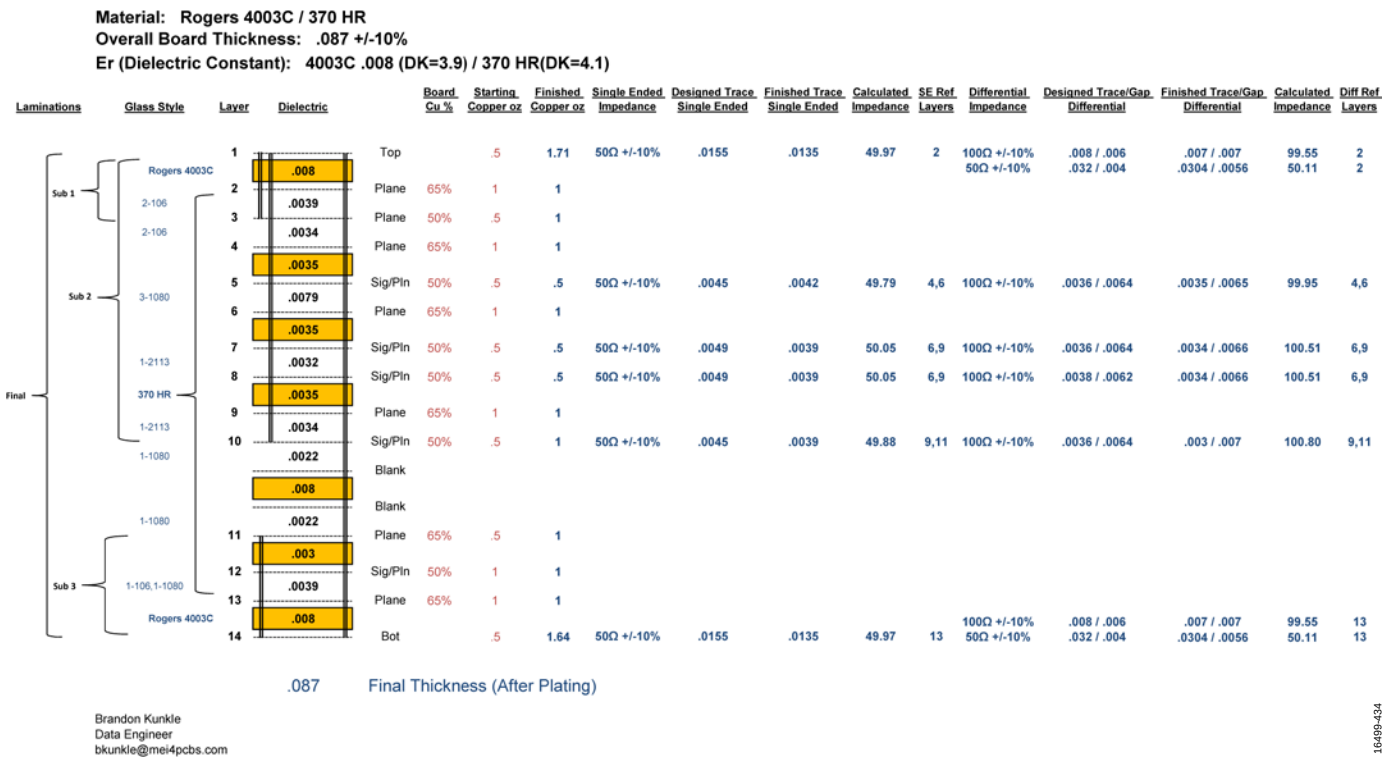


Figure 272. ADRV9009, ADRV9008-1, ADRV9008-2 Customer Evaluation Board Trace Impedance and Stackup

Table 8. Customer Evaluation Board Single Ended Impedance and Stackup

Layer	Board Copper %	Starting Copper (oz.)	Finished Copper (oz.)	Single Ended Impedance	Designed Trace Single Ended	Finished Trace Single Ended	Calculated Impedance	Single Ended Ref Layers
1	N/A[1]	0.5	1.71	50 Ω ±10%	0.0155	0.0135	49.97	2
	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
2	65	1	1	N/A	N/A	N/A	N/A	N/A
3	50	0.5	1	N/A	N/A	N/A	N/A	N/A
4	65	1	1	N/A	N/A	N/A	N/A	N/A
5	50	0.5	0.5	50 Ω ±10%	0.0045	0.0042	49.79	4, 6
6	65	1	1	N/A	N/A	N/A	N/A	N/A
7	50	0.5	0.5	50 Ω ±10%	0.0049	0.0039	50.05	6, 9
8	50	0.5	0.5	50 Ω ±10%	0.0049	0.0039	50.05	6, 9
9	65	1	1	N/A	N/A	N/A	N/A	N/A
10	50	0.5	1	50 Ω ±10%	0.0045	0.0039	49.88	9, 11
11	65	0.5	1	N/A	N/A	N/A	N/A	N/A
12	50	1	1	N/A	N/A	N/A	N/A	N/A
13	65	1	1	N/A	N/A	N/A	N/A	N/A
14		0.5	1.64	50 Ω ±10%	0.0155	0.0135	49.97	13

[1] N/A means not applicable.

Table 9. Customer Evaluation Board Differential Impedance and Stackup[1]

Layer	Differential Impedance	Designed Trace/Gap Differential	Finished Trace/Gap Differential	Calculated Impedance	Differential Reference Layers
1	100 Ω ±10%	0.008/0.006	0.007/0.007	99.55	2
	50 Ω ±10%	0.0032/0.004	0.0304/0.0056	50.11	2
2	N/A[1]	N/A	N/A	N/A	N/A
3	N/A	N/A	N/A	N/A	N/A
4	N/A	N/A	N/A	N/A	N/A
5	100 Ω ±10%	0.0036/0.0064	0.0034/0.0065	99.95	4, 6
6	N/A	N/A	N/A	N/A	N/A
7	100 Ω ±10%	0.0036/0.0064	0.0034/0.0066	100.51	6, 9
8	100 Ω ±10%	0.0038/0.0062	0.0034/0.0066	100.51	6, 9
9	N/A	N/A	N/A	N/A	N/A
10	100 Ω ±10%	0.0036/0.0064	0.003/0.007	100.80	9, 11
11	N/A	N/A	N/A	N/A	N/A
12	N/A	N/A	N/A	N/A	N/A
13	100 Ω ±10%	0.008/0.006	0.007/0.007	99.55	13
14	50 Ω ±10%	0.032	0.004	50.11	13

[1] N/A means not applicable.

FANOUT AND TRACE SPACE GUIDELINES

The ADRV9008-2 device uses a 196 ball chip scale package ball grid array (CSP_BGA), 12 × 12 mm package. The pitch between the pins is 0.8 mm. This small pitch makes it impractical to route all signals on a single layer. RF pins have been placed on the outer edges of the ADRV9008-2 package. The location of the pins helps in routing the critical signals without a fanout via. Each digital signal is routed from the BGA pad using a 4.5 mil trace. The trace is connected to the BGA using via in the pad structure. The signals are buried in the inner layers of the board for routing to other parts of the system.

The JESD204B interface signals are routed on two signal layers that utilize impedance control (Layer 5 and Layer 10). The spacing between the BGA pads is 17.5 mil. Once the signal is on the inner layers, a 3.6 mil trace (50 Ω) connects the JESD204B signal to the FPGA mezzanine card (FMC) connector. The recommended BGA land pad size is 15 mil.

Figure 273 shows the fanout scheme of the ADRV9008-2 evaluation card. As mentioned before, the ADRV9008-2 evaluation board uses via in the pad technique. This routing approach can be used for the ADRV9008-2 if there are no issues with manufacturing capabilities.

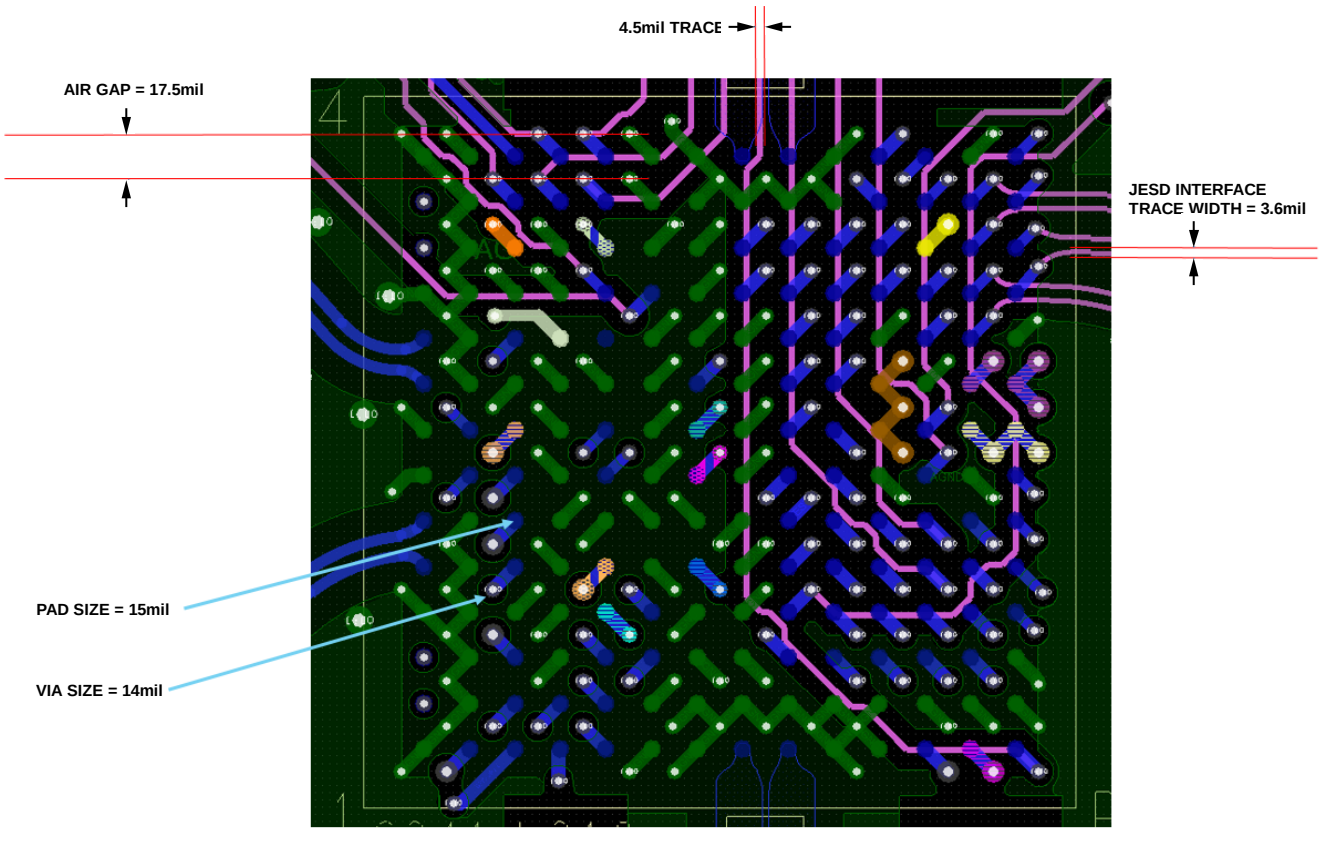


Figure 273. Trace Fanout Scheme on 8-2 Evaluation Card (PCB Layer Top and Layer 5 Enabled)

COMPONENT PLACEMENT AND ROUTING GUIDELINES

The ADRV9008-2 transceiver requires few external components to function, but those that are used require careful placement and routing to optimize performance. This section provides a checklist for properly placing and routing critical signals and components.

Signals with Highest Routing Priority

RF lines and JESD204B interface signals are the signals that are most critical and need to be routed with the highest priority.

Figure 274 shows the general directions in which each of the signals need to be routed so that they can be properly isolated from noisy signals.

The receiver and transmitter baluns and the matching circuits affect the overall RF performance of the ADRV9008-2 transceiver. Make every effort to optimize the component selection and placement to avoid performance degradation. The RF Routing Guidelines section describes proper matching circuit placement and routing in more detail. Refer to the RF Port Interface Information section for more information.

To achieve the desired level of isolation between RF signal paths, use the technique described in the ADRV9008-1 /ADRV9008-2/ADRV9009 Hardware Reference Manual in customer designs.

In cases in which ADRV9008-2 is used, install a 10 µF capacitor near the transmitter balun(s) VDDA1P8_TX dc feed(s) for RF transmitter outputs. This acts as a reservoir for the transmitter supply current. The Transmitter Balun DC Feed Supplies section discusses more details about the transmitter output power supply configuration.

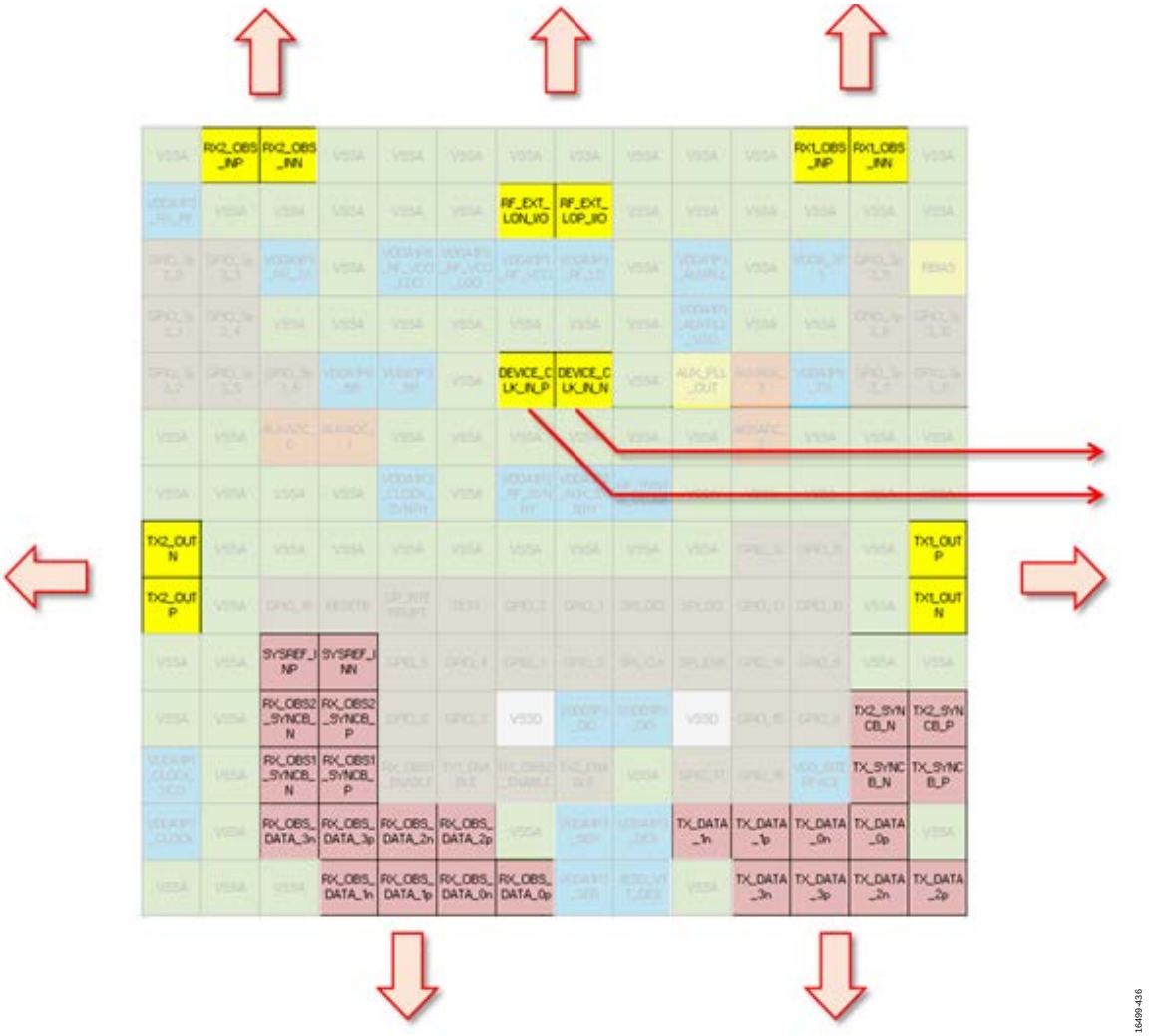


Figure 274. RF IO, DEV_CLK, and JESD204B Signal Routing Guidelines for ADRV9008-2

Figure 275 illustrates placement for ac coupling capacitors and a 100 Ω termination resistor near the ADRV9008-2 REF_CLK_IN± pins. Shield traces by ground surrounded with vias staggered along the edge of the trace pair. The trace pair creates a shielded channel that shields the reference clock from any interference from other signals. Refer to the ADRV9008-2 evaluation card layout, including board support files included with the evaluation board software, for exact details.

Route the JESD204B interface at the beginning of the PCB design and with the same priority as RF signals. The section outlines recommendations for JESD204B interface routing. Provide appropriate isolation between interface differential pairs. The Isolation Between JESD204B Lines section provides guidelines for optimizing isolation.

The RF_EXT_LO_I/O– (B7), RF_EXT_LO_I/O+ (B8) pins on all ADRV9008-2 variants are internally dc biased. If an external LO is used, connect it via ac coupling capacitors.

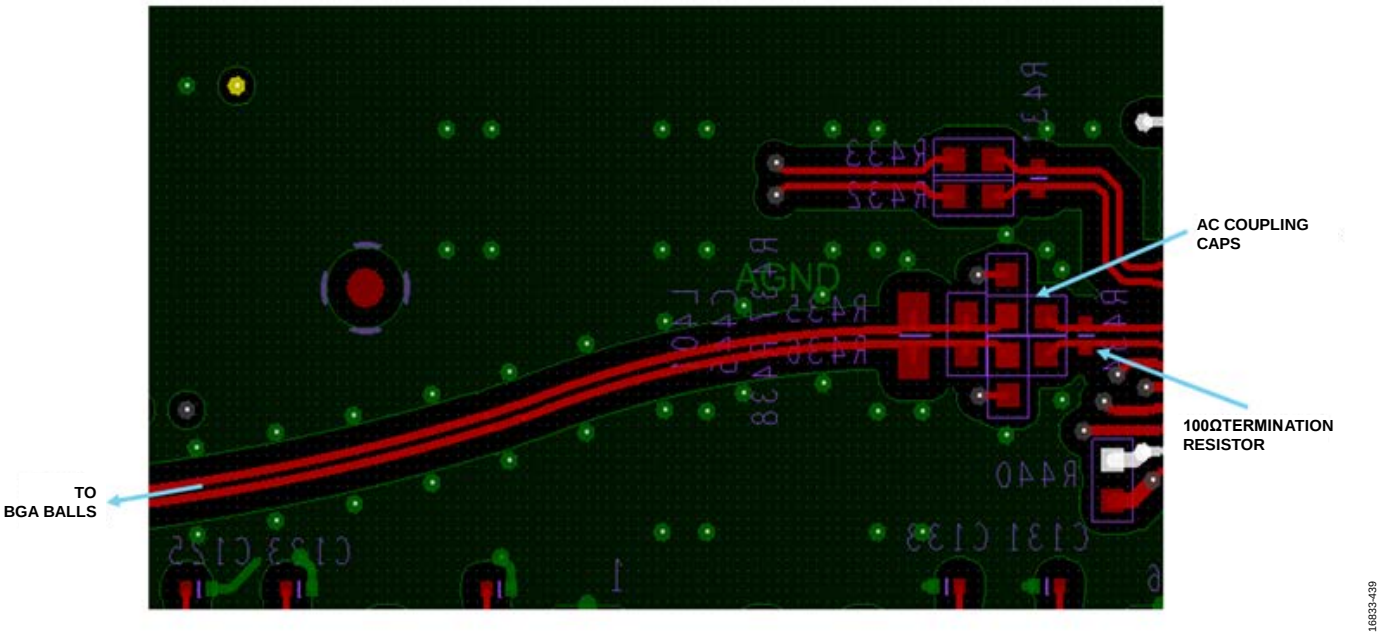


Figure 275. REF_CLK_IN Routing Recommendation

Signals with Second Routing Priority

Power supply quality has direct impact on overall system performance. To achieve optimal performance, users should follow recommendations regarding ADRV9008-2 power supply routing. The following recommendations outline how to route different power domains that can be connected together directly and that can be tied to the same supply, but are separated by a 0 Ω placeholder resistor or ferrite bead.

When the recommendation is to use a trace to connect power to a particular domain, make sure that this trace is surrounded by ground.

Figure 276 shows an example of such traces routed on the ADRV9008-2 evaluation card on Layer 12. Each trace is separated from any other signal by the ground plane and vias. Separating the traces from other signals is essential to providing necessary isolation between the ADRV9008-2 power domains.

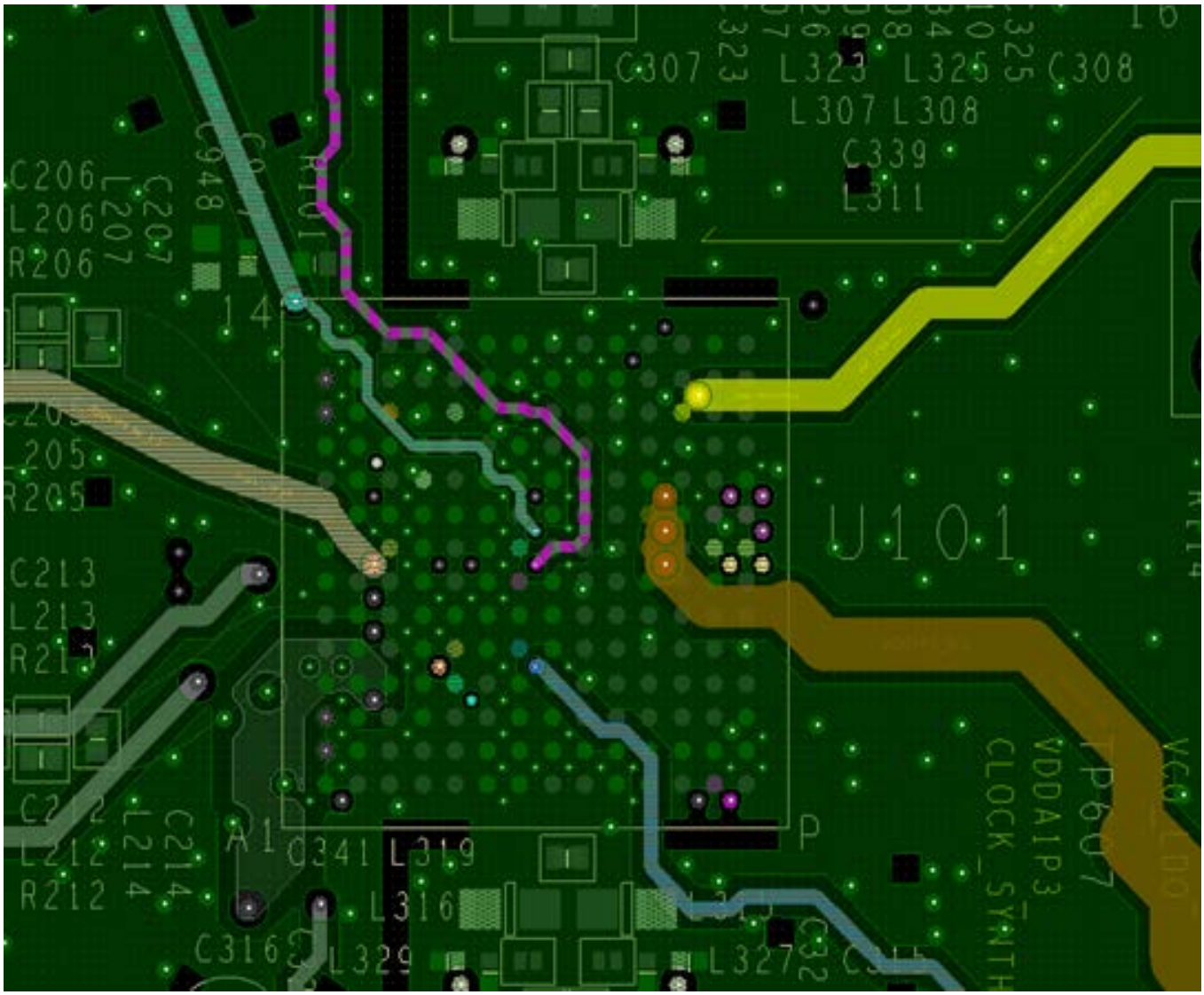


Figure 276. Layout Example of Power Supply Domains Routed with Ground Shielding (Layer 12 to Power)

Each power supply pin requires a 0.1 µF bypass capacitor near the pin at a minimum. Place the ground side of the bypass capacitor so that ground currents flow away from other power pins and their bypass capacitors.

For domains shown in Figure 277, like those domains that are powered through a 0 Ω placeholder resistor or ferrite bead (FB), place the 0 Ω placeholder resistors or ferrite beads further away from the device. Space 0 Ω placeholder resistors or ferrite beads apart from each other to ensure the electric fields on the ferrite beads do not influence each other. Figure 278 shows an example of how the ferrite beads, reservoir capacitors, and decoupling capacitors are placed. The recommendation is to connect a ferrite bead between a power plane and the ADRV9008-2 at a distance away from the device The ferrite bead supplies a trace with a reservoir capacitor connected to it. Then shield that trace with ground and provide power to the power pins on the ADRV9008-2 power pin. Place a 100 nF capacitor near the power supply pin with the ground side of the bypass capacitor placed so that ground currents flow away from other power pins and their bypass capacitors.

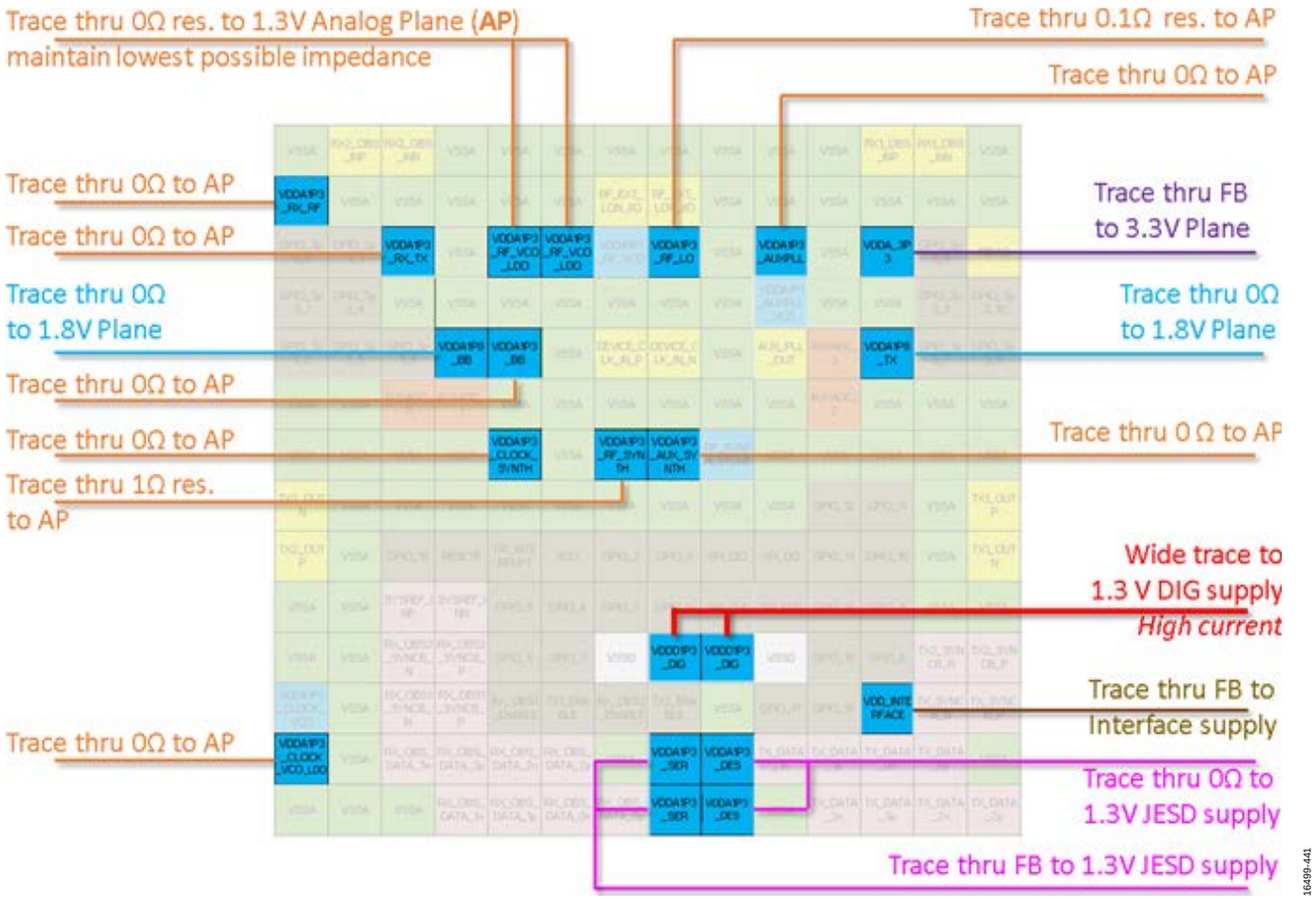


Figure 277. ADRV9008-2 Power Supply Domains Interconnection Guidelines

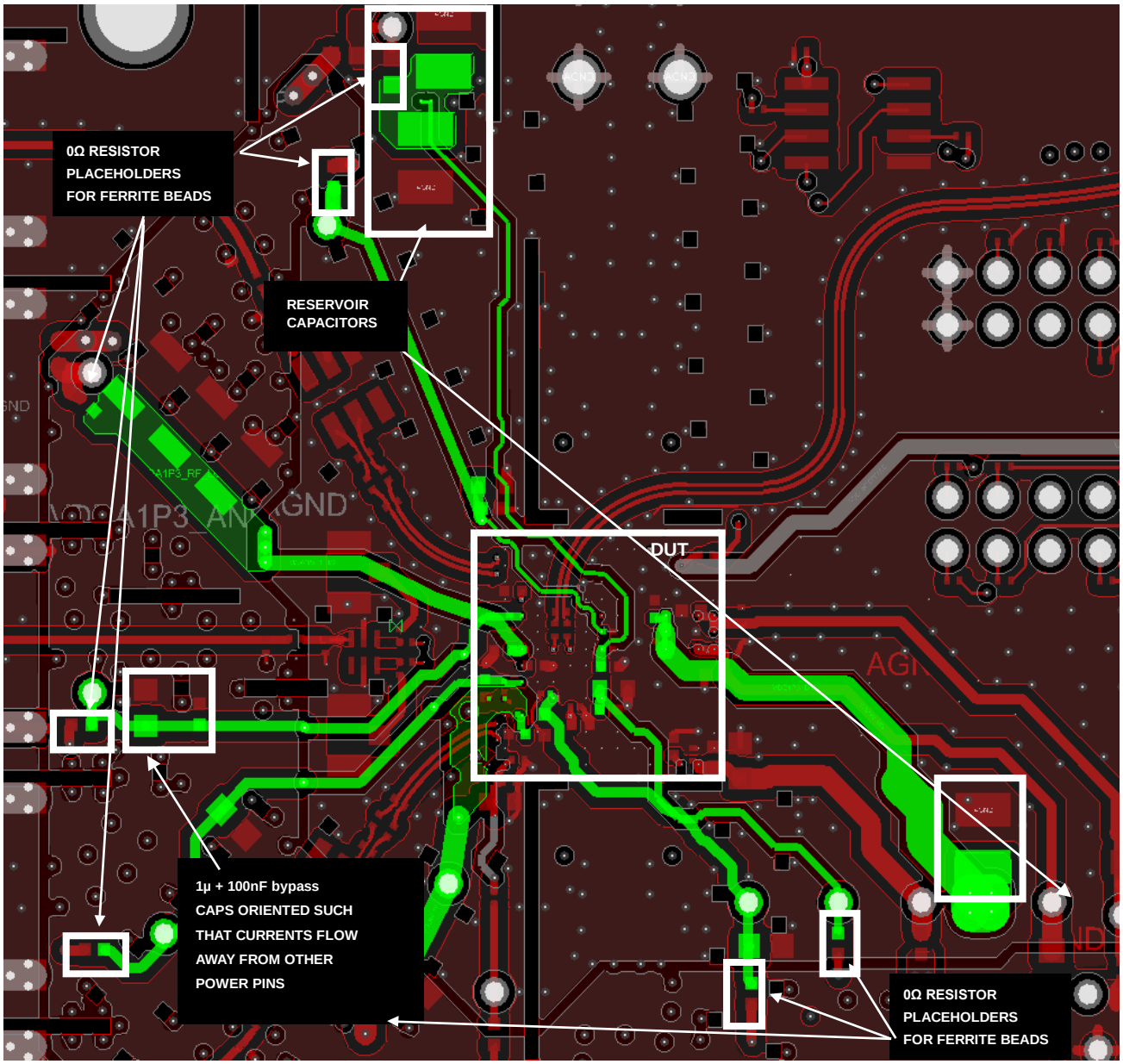


Figure 278. Placement Example of 0 Ω Resistor Placeholders for Ferrite Beads, Reservoir and Bypass Capacitors on ADRV90098-2 Customer Card (Layers: 12 to Power and Bottom)

Signals with Lowest Routing Priority

As a last step while designing the PCB layout, route signals shown in Figure 279. The following list outlines the recommended order of signal routing:

1. Use ceramic 1 µF bypass capacitors at the VDDA1P1_RF_VCO, VDDA1P1_AUX_VCO, and VDDA1P1_CLOCK_VCO pins. Place them as close as possible to the ADRV9008-2 device with the ground side of the bypass capacitor placed so that ground currents flow away from other power pins and their bypass capacitors, if at all possible.
2. Connect a 14.3 kΩ resistor to the RBIAS pin (C14). This resistor must have a 1% tolerance.
3. Pull the TEST (J6) pin to ground for normal operation. The device has support for JTAG boundary scan, and this pin is used to access that function. Refer to the **Error! Reference source not found.** section for JTAG boundary scan information.
4. Pull the $\overline{\text{RESET}}$ pin (J4) high with a 10 kΩ resistor to VDD_INTERFACE for normal operation. To reset the device, drive the $\overline{\text{RESET}}$ pin low.

When routing analog signals such as GPIO3P3_n/AUXDAC_n or AUXADC_n, it is recommended to route them away from the digital section (row H through row P). Do not cross the analog section of the ADRV9008-2 highlighted by a red-dotted line in Figure 279, by any digital signal routing.

When routing digital signals from rows H and below, it is important to route them away from the analog section (row A through row G). Do not cross the analog section of the ADRV9008-2 highlighted by a red-dotted line in Figure 279 by any digital signal routing.

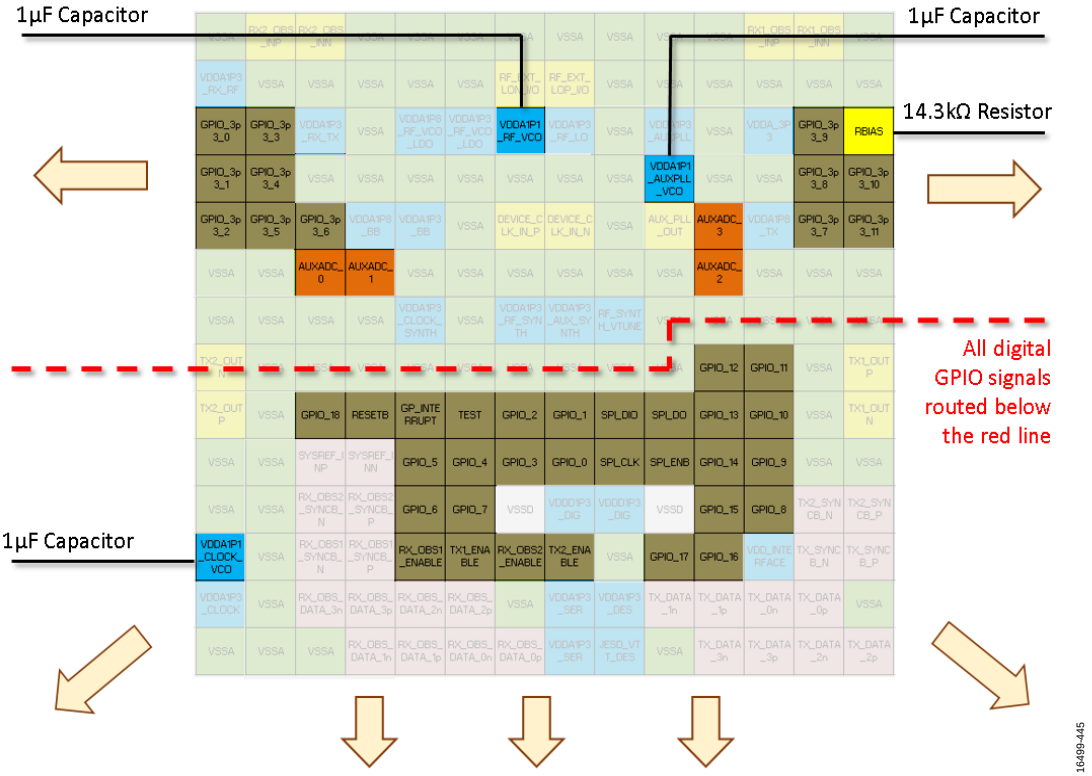


Figure 279. ADRV9008-2 Auxiliary ADC, Analog and Digital GPIO Signals Routing Guidelines

RF AND JESD204B TRANSMISSION LINE LAYOUT

RF Routing Guidelines

The ADRV9008-2 customer evaluation boards use microstrip type lines for receiver, observation receiver, and transmitter RF traces. In general, Analog Devices, Inc. does not recommend using vias to route RF traces unless a direct line route is not possible. Differential lines from the balun to the receiver, observation receiver, and transmitter pins need to be as short as possible. Make the length of the single-ended transmission line also short to minimize the effects of parasitic coupling. It is important to note that these traces are the most critical when optimizing performance and are, therefore, routed before any other routing. These traces have the highest priority if trade-offs are needed.

Figure 281 shows pi matching networks on the single-ended side of the baluns. The receiver front end is dc biased internally, so the differential side of the balun is ac-coupled. The system designer can optimize the RF performance with a proper selection of the balun, matching components, and ac coupling capacitors. The external LO traces and the REF_CLK_IN± traces may require matching components as well to ensure optimal performance.

All the RF signals mentioned above must have a solid ground reference under each trace. Do not run any of the critical traces over a section of the reference plane that is discontinuous. The ground flood on the reference layer must extend all the way to the edge of the board. This flood length ensures good signal integrity for the SMA launch when an edge-launch connector is used.

Refer to the RF Port Interface Information section for more information on RF matching recommendations for the device.

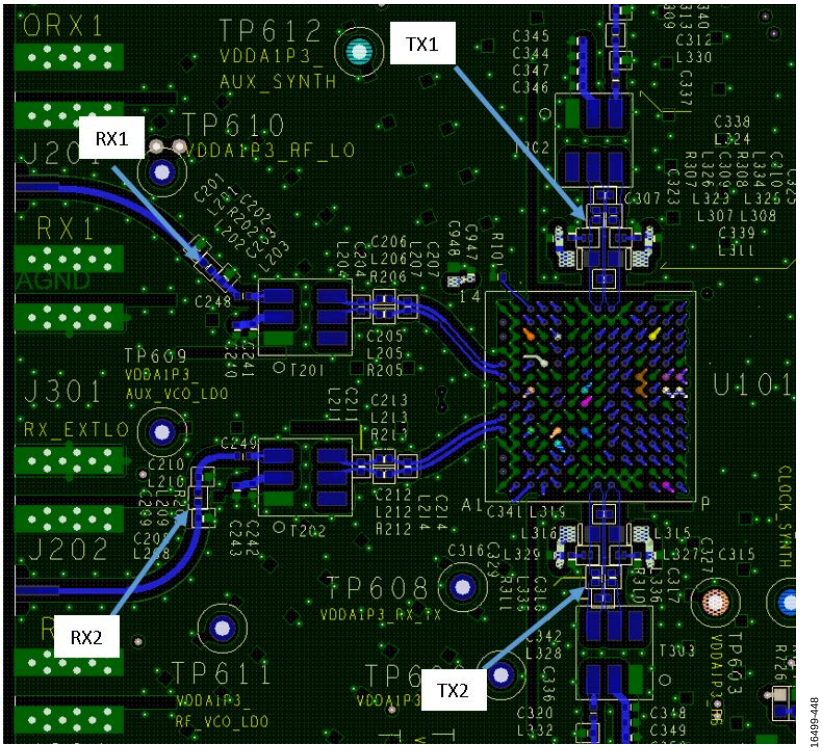


Figure 280. PI Network Matching Components Available on Different RF Nets (use the ADRV9008-2 Evaluation Card as an example)

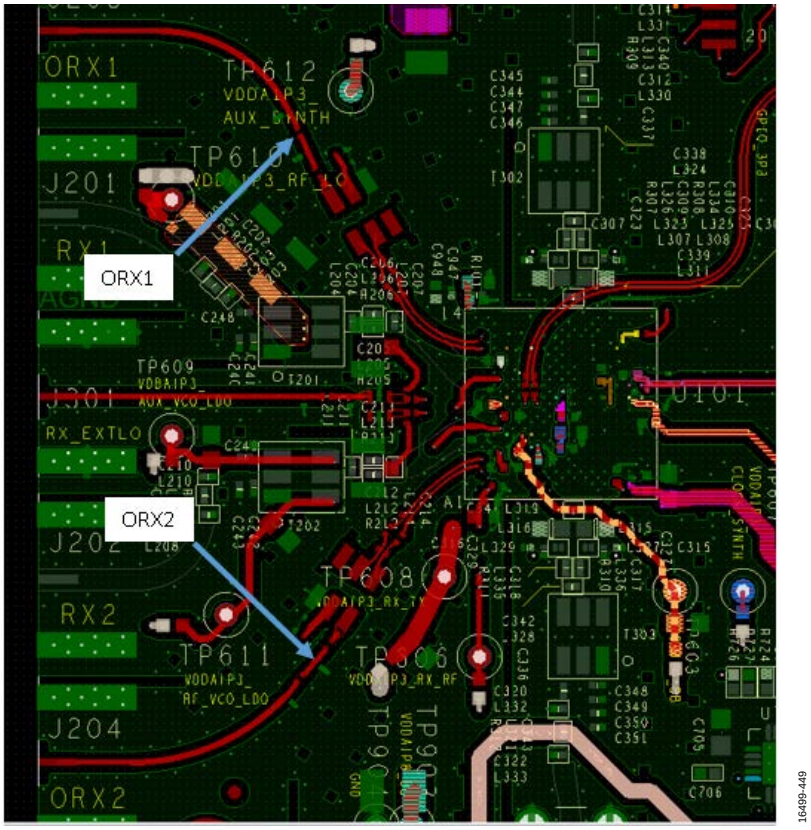


Figure 281. PI Network Matching Components Available on Different RF Nets (use ADRV9009 Evaluation Card as an example)

Transmitter Balun DC Feed Supplies

Each transmitter requires approximately 200 mA supplied through an external connection. On the ADRV9008-2 and ADRV9009 customer evaluation cards, bias voltages are supplied at the dc feed of the baluns. Layout of both boards allows the use of external chokes to provide a 1.8 V power domain to the ADRV9008-2 outputs. This is useful in scenarios where a balun used at the transmitter output is not capable to conduct the current necessary for transmitter outputs to operate. To reduce switching transients when attenuation settings change, power the balun dc feed or transmitter output chokes directly by the 1.8 V plane. Design the geometry of the 1.8 V plane so that each balun supply or each set of two chokes is isolated from the other. This geometry can affect tansmitter to transmitter isolation. Figure 282 shows the layout configuration used on the ADRV9008-2 evaluation card.

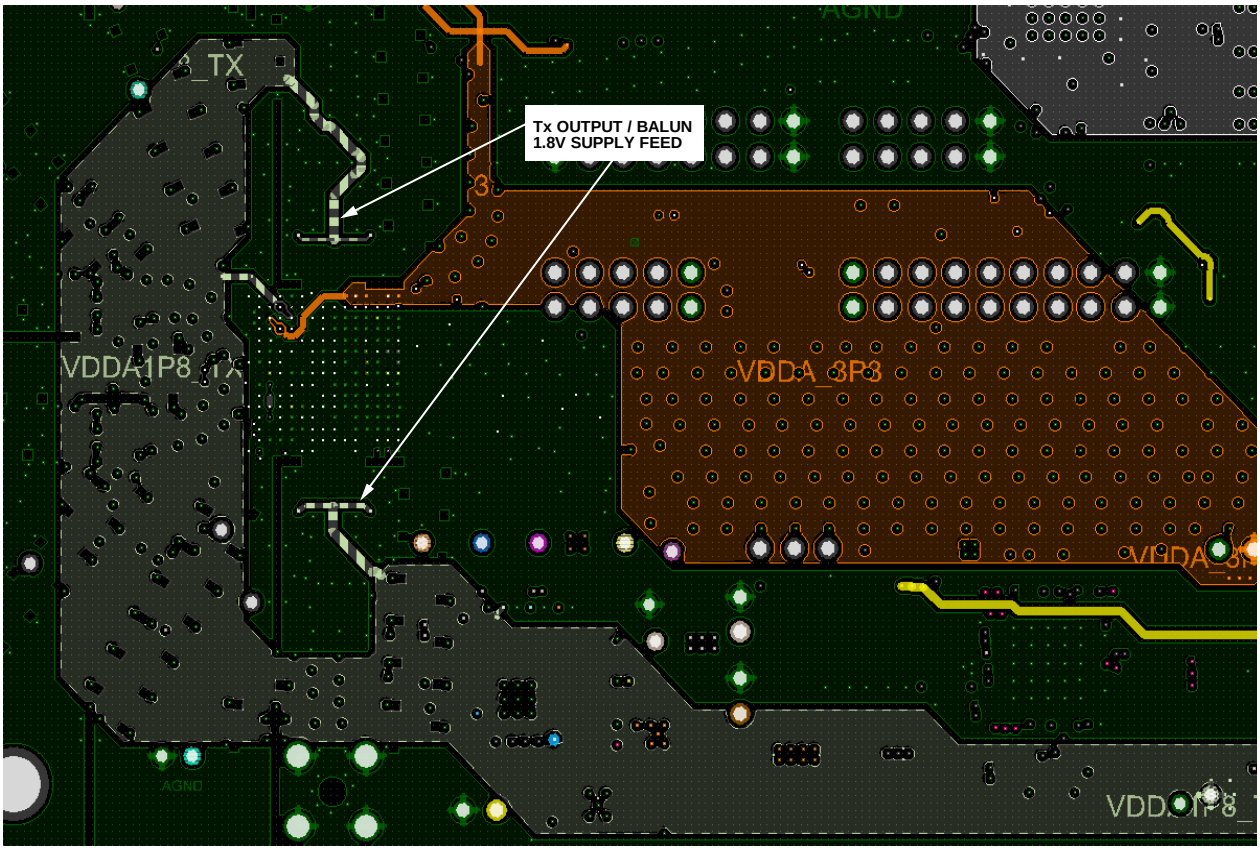


Figure 282. Transmitter Power Supply Planes (VDDA1P8_TX) on ADRV9008-2 Evaluation Card

The transmitter + and – pins must be biased with 1.8 V. This is accomplished on the evaluation board through dc chokes and decoupling capacitors as shown in Figure 283. Match both chokes and their layout to avoid potential current spikes. Difference in parameters between both chokes can cause unwanted emission at transmitter outputs. Place the decoupling caps that are near the transmitter balun as close as possible to the dc feed of the balun or the ground pin. Make its orientation perpendicular to the device so the return current forms as small a loop as possible with the ground pins surrounding the transmitter input. A combination network of capacitors is used to provide a very wide band and low impedance ground path and helps to eliminate transmitter spectrum spurs and dampen the transients.

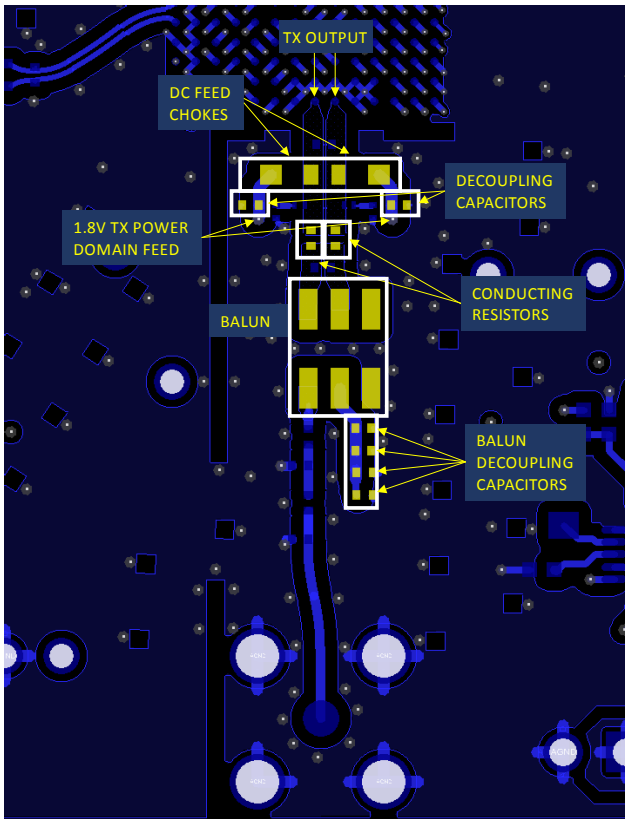


Figure 283. The Transmitter DC Chokes and Balun Feed Supply

JESD204B Trace Routing Recommendations

The ADRV9008-2 transceiver uses the JESD204B, high speed serial interface. To ensure optimal performance of this interface, keep the differential traces as short as possible by placing ADRV9008-2 as close as possible to the FPGA or BBP, and route the traces directly between the devices. Use a PCB material with a low dielectric constant (< 4) to minimize loss. For distances greater than 6 inches, use a premium PCB material such as RO4350B or RO4003C.

Routing Recommendations

Route the differential pairs on a single plane using a solid ground plane as a reference on the layers above and/or below these traces.

All JESD204B lane traces must be impedance controlled to achieve 50 Ω to ground. The differential pair should be coplanar and loosely coupled. An example of a typical configuration is 5 mil trace width and 15 mil edge to edge spacing, with the trace width maximized as shown in Figure 284.

Match trace widths with pin and ball widths while maintaining impedance control. If possible, use 1 oz. copper trace widths of at least 8 mil (200 µm). The coupling capacitor pad size must match JESD204B lane trace widths If trace width does not match pad size, use a smooth transition between different widths.

The pad area for all connector and passive component choices must be minimized due to a capacitive plate effect that leads to problems with signal integrity.

Reference planes for impedance controlled signals must not be segmented or broken for the entire length of a trace.

The REF_CLK_IN signal trace and the SYSREF signal trace are impedance controlled for Z0 = 50 Ω.

Stripline Transmission Lines vs. Microstrip Transmission Lines

Stripline has less singal loss and emits less electromagnetic interference than microstrip, but stripline requires the use of vias that add line inductance, increasing the difficulty of controlling the impedance.

Microstrip is easier to implement if the component placement and density allow for routing on the top layer. Microstrip makes controlling the impedance easier.

If the top layer of the PCB is used by other circuits or signals or if the advantages of stripline are more desirable over the advantages of microstrip, follow these recommendations:

- Minimize the number of vias.
- Use blind vias wherever possible to eliminate via stub effects, and use micro vias to minimize via inductance.
- When using standard vias, use maximum via length to minimize the stub size. For example, on an 8-layer board, use Layer 7 for the stripline pair.
- Place a pair of ground vias near each via pair to minimize the impedance discontinuity.

Route the JESD204B lines on the top side of the board as a differential 100 Ω pair (microstrip). For the customer evaluation board, the JESD204B differential signals are routed on inner layers of the board (Layer 5 and Layer 10) as differential 100 Ω pairs (stripline). To minimize potential coupling, these signals are placed on an inner layer using a via embedded in the component footprint pad where the ball connects to the PCB. The ac-coupling capacitors (100 nF) on these signals are placed near the connector and away from the chip to minimize coupling. The JESD204B interface can operate at frequencies of up to 12 GHz. Ensure that signal integrity from the chip to the connector is maintained.

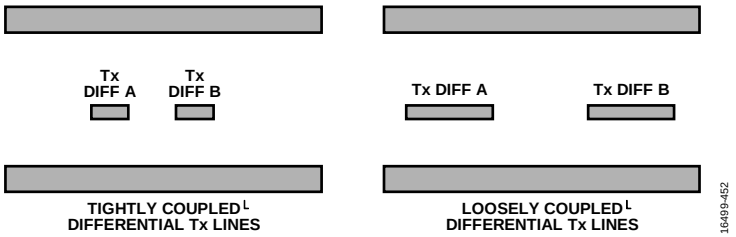


Figure 284. Routing JESD204B. Differential A and Differential B Correspond to Differential P Signals or N Signals (One Differential Pair)

ISOLATION TECHNIQUES USED ON THE ADRV9009 CUSTOMER CARD

Isolation Goals

Significant isolation challenges were overcome in designing the ADRV9008-2 customer card. The following isolation requirements were used to accurately evaluate the ADRV9008-2 transceiver performance:

- Transmitter to transmitter, 75 dB out to 6 GHz
- Transmitter to receiver, 65 dB out to 6 GHz
- Receiver to receiver, 65 dB out to 6 GHz
- Transmitter to observation receiver, 65 dB out to 6 GHz

To meet these isolation goals with significant margin, isolation structures were introduced.

Figure 285 shows the isolation structures used on the ADRV9008-2 customer evaluation card. These structures consist of a combination of slots and square apertures. These structures are present on every copper layer of the PCB stack. The advantage of using square apertures is that signals can be routed between the openings without affecting the isolation benefits of the array of apertures. When using these isolation structures, make sure to place ground vias around the slots and apertures.

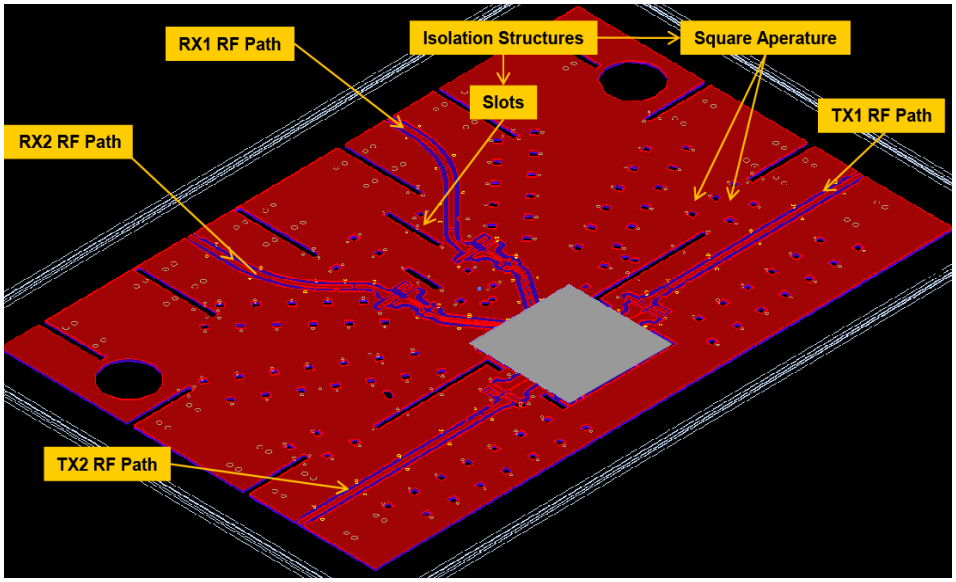


Figure 285. Isolation Structures on the ADRV9008-2 Customer Card

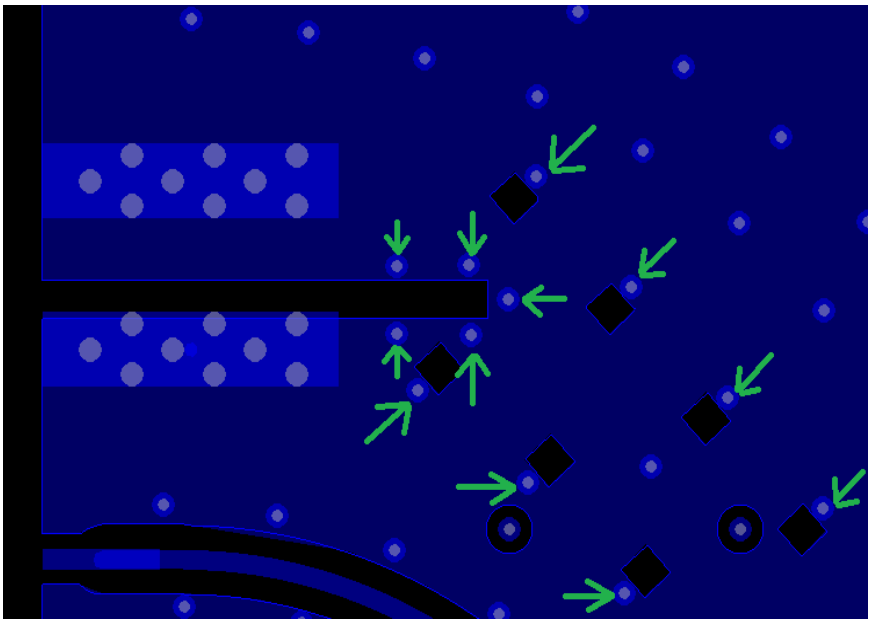


Figure 286. Current Steering Vias Placed Next to Isolation Structures

Figure 286 outlines the methodology used on the ADRV9008-2 evaluation card. When using slots, ground vias must be placed at the ends of the slots and along the sides of the slots. When using square apertures, at least one single ground via must be placed adjacent to each square. These vias must be through-hole vias from the top to the bottom layer. The function of these vias is to steer return current to the ground planes near the apertures.

For accurate slot spacing and square apertures layout, use simulation software when designing a PCB for the ADRV9008-2 transceiver. Spacing between square apertures must be no more than 1/10 of a wavelength. Calculate the wavelength using Equation 1:

$$wavelength\ (\text{m}) = \frac{300}{frequency\ (\text{MHz}) \times \sqrt{E_R}} \quad (1)$$

where E_R is the dielectric constant of the isolator material. For RO4003C material, microstrip structure (+ air) E_R = 2.8. For FR4-370HR material, stripline structure E_R = 4.1.

For example, if the maximum RF signal frequency is 6 GHz, and E_R = 2.8 for RO4003C material, microstrip structure (+ air), the minimum wavelength is approximately 29.8 mm.

To follow the 1/10 wavelength spacing rule, square aperture spacing must be 2.98 mm or less.

Isolation Between JESD204B Lines

The JESD204B interface uses eight line pairs that can operate at speeds of up to 12 GHz. When configuring the PCB layout, make sure these lines are routed according to the rules outlined in the JESD204B Trace Routing Recommendations section. In addition, use isolation techniques to prevent crosstalk between different JESD204B lane pairs.

Figure 287 shows a technique used on the ADRV9008-2 evaluation card that involves via fencing. Placing ground vias around each JESD204B pair provides isolation and decreases crosstalk. The spacing between vias is 1.2 mm.

Figure 287 shows the rule provided in Equation 1 JESD204B lines are routed on Layer 5 and Layer 10 so that the lines use stripline structures. The dielectric material used in the inner layers of the ADRV9008-2 customer card PCB is FR4-370HR.

For accurate spacing of the JESD204B fencing vias, use layout simulation software. Input the following data into Equation 1 to calculate the wavelength and square aperture spacing:

- Maximum JESD204B signal frequency is approximately 12 GHz.
- For FR4-370HR material, stripline structure, E_R = 4.1, the minimum wavelength is approximately 12.4 mm.

To follow the 1/10 wavelength spacing rule, spacing between vias must be 1.24 mm or less. The minimum spacing recommendation according to transmission line theory is 1/4 wavelength.

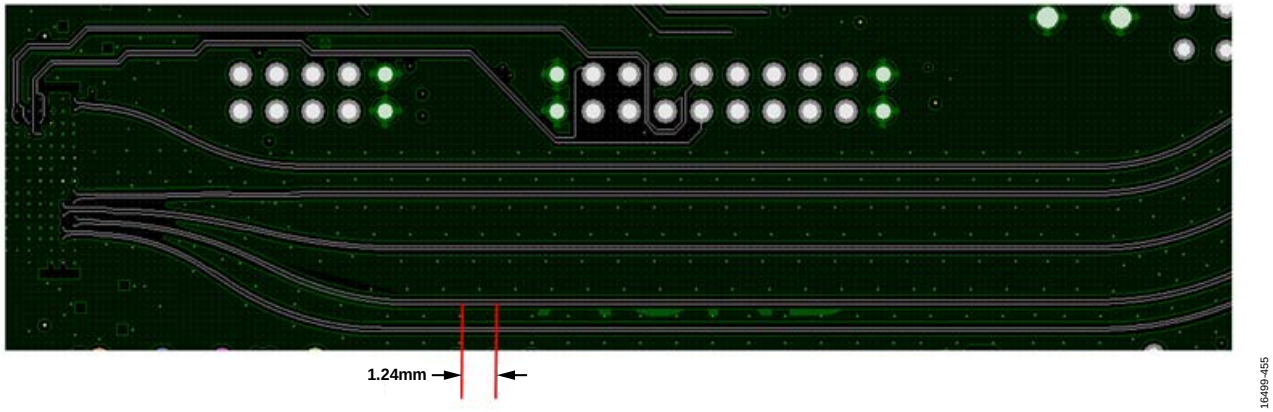


Figure 287. Via Fencing Around JESD204B Lines, PCB Layer 10

RF PORT INTERFACE INFORMATION

RF Port Interface Overview

This section details the RF transmitter and receiver interfaces for optimal device performance. This section also includes data for the anticipated ADRV9008-2 RF port impedance values and examples of impedance matching networks used in the evaluation platform. This section also provides information on board layout techniques and balun selection guidelines.

ADRV9008-2 is a highly integrated transceiver with transmit, receive, and observation (DPD) receive signal chains. External impedance matching networks are required on transmitter and receiver ports to achieve performance levels indicated on the data sheet.

Analog Devices recommends the use of simulation tools in the design and optimization of impedance matching networks. To achieve the closest match between computer simulated results and measured results, accurate models of the board environment, SMD components (including baluns and filters), and ADRV9008-2 port impedances are required.

RF Port Impedance Data

This section provides the port impedance data for all transmitters and receivers in the ADRV9008-2 integrated transceiver. Please note the following:

- Z0 is defined as 50 Ω.
- The ADRV9008-2 ball pads are the reference plane for this data.
- Single-ended mode port impedance data is not available. However, a rough assessment is possible by taking the differential mode port impedance data and dividing both the real and imaginary components by 2.
- Contact Analog Devices applications engineering for the impedance data in Touchstone format.

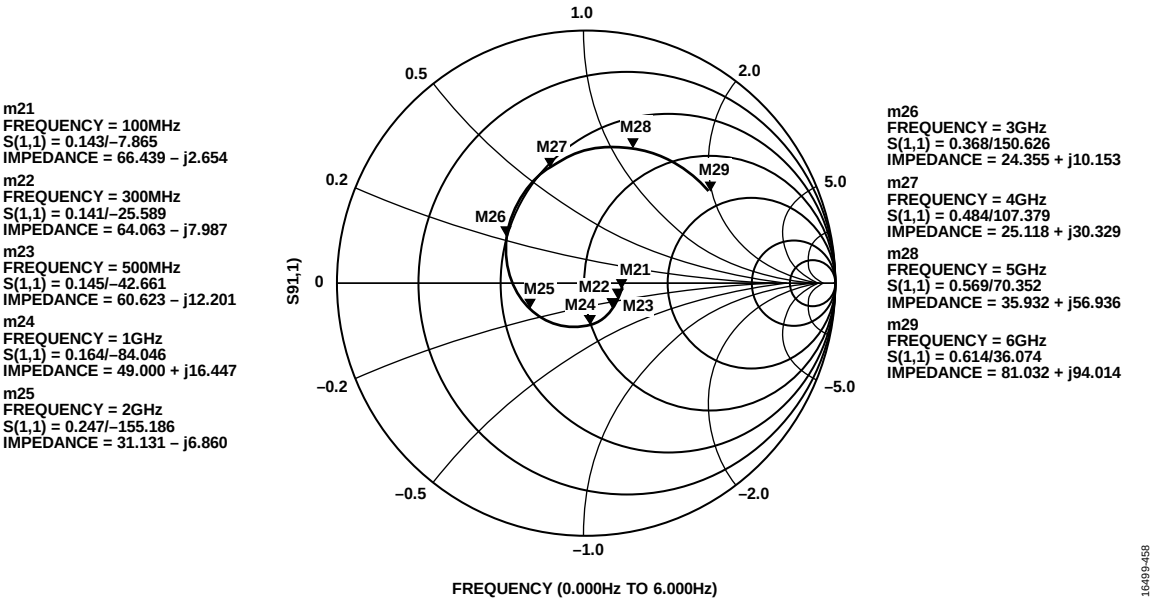


Figure 288. Transmitter 1 and Transmitter 2 SEDZ and PEDZ Data

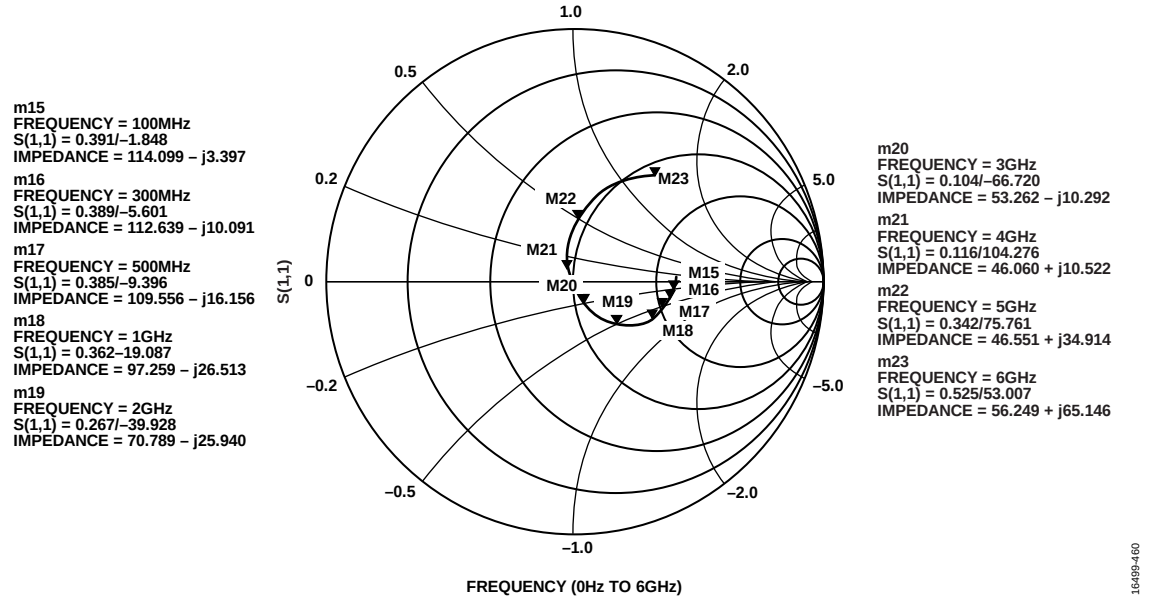


Figure 289. Observation Receiver 1 and Observation Receiver 2 SEDZ and PEDZ Data

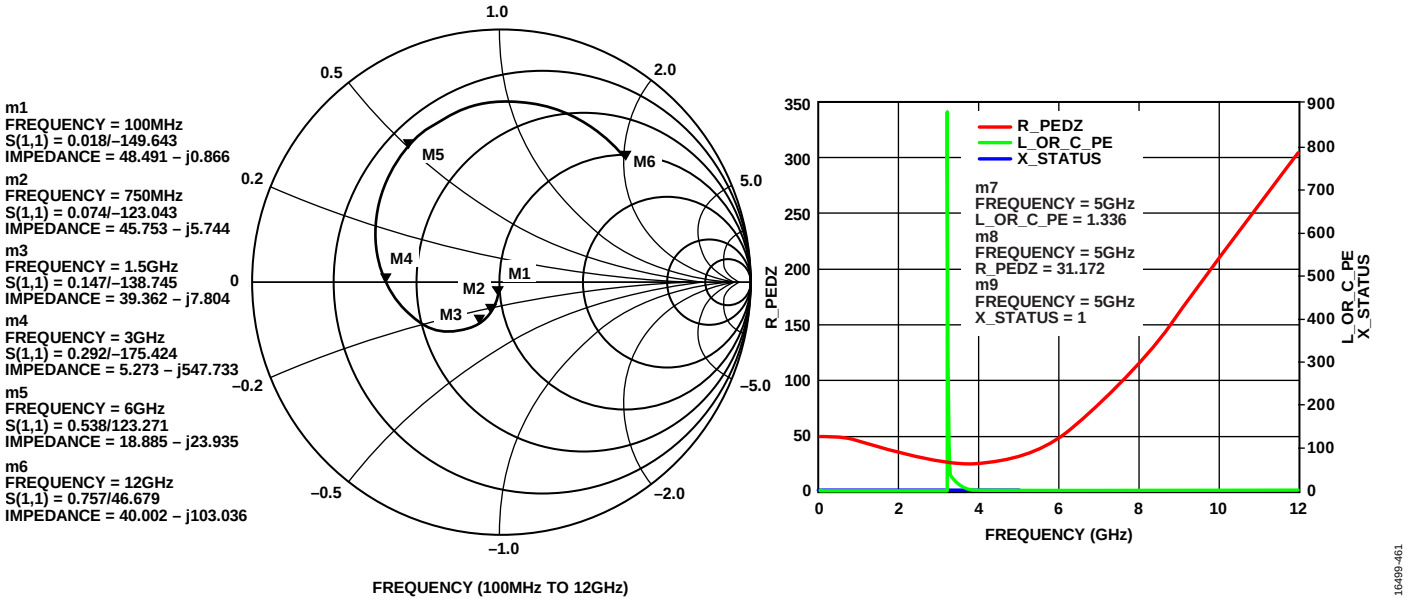


Figure 290. RF_EXT_LO_I/O± SEDZ and PEDZ Data

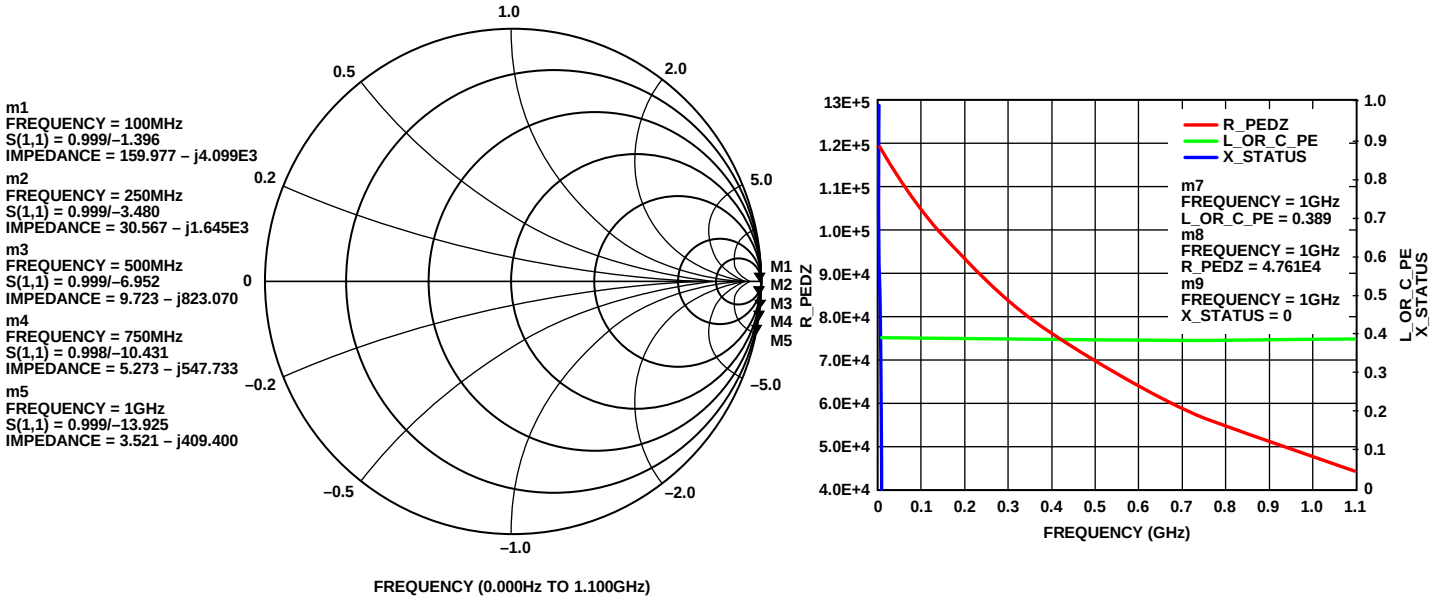


Figure 291. ADRV9008-2 REF_CLK_IN± SEDZ and PEDZ Data, on Average, the Real Part of the Parallel Equivalent Differential Impedance (R_P) = ~ 70 kΩ

Advanced Design System (ADS) Setup Using the DataAccessComponent and SEDZ File

Analog Devices supplies the port impedance as an **.s1p** file that can be downloaded from the ADRV9008-2 product page. This format allows simple interfacing to ADS by using the data access component. InFigure 292, Term1 is the single-ended input or output, and Term2 represents the differential input or output RF port on device. The pi on the single-ended side and the differential pi configuration on the differential side allow maximum flexibility in designing matching circuits. The pi configuration is suggested for all design layouts because the pi configuration can step the impedance up or down as needed with appropriate component population.

The mechanics of setting up a simulation for impedance measurement and impedance matching is as follows:

1. The data access component block reads the **rf port.s1p** file. This is the device RF port reflection coefficient.
2. The two equations convert the RF port reflection coefficient to a complex impedance. The result is the **RX_SEDZ** variable.
3. The RF port calculated complex impedance (RX_SEDZ) is utilized to define the **Term2** impedance.
4. Term2 is used in a differential mode, and **Term1** is used in a single-ended mode.
5. Setting up the simulation this way allows one to measure the S11, S22, and S21 of the three-port system without complex math operations within the display page.

For highest accuracy, EM modelling result of the PCB artwork and S-parameters of the matching components and balun must be used in the simulations.

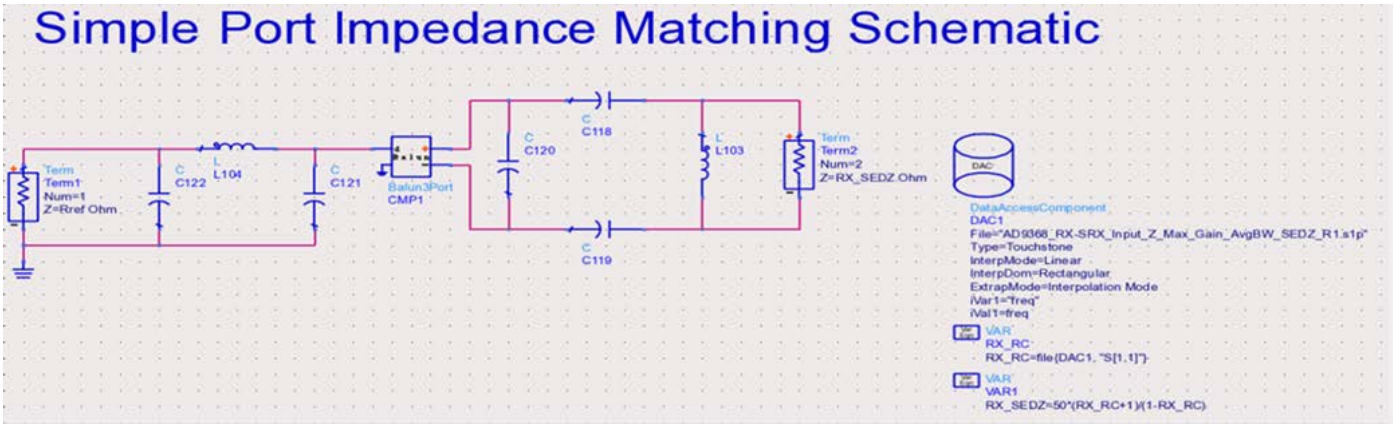


*Figure 292. Simulation Setup in ADS with SEDZ **.s1p** Files and DataAccessComponent*

Transmitter Bias and Port Interface

This section considers the dc biasing of the ADRV9008-2 transmitter outputs and how to interface to each transmitter port. The ADRV9008-2 transmitters operate over a range of frequencies. At full output power, each differential output side draws approximately 100 mA of dc bias current. The transmitter outputs are dc biased to a 1.8 V supply voltage using either RF chokes (wire wound inductors) or a transformer center tap connection.

Careful design of the dc bias network is required to ensure optimal RF performance levels. When designing the dc bias network, select components with low dc resistance to minimize the voltage drop across the series parasitic resistance element with either of the suggested dc bias schemes suggested in Figure 293. The R_{DCR} resistors indicate the parasitic elements. As the impedance of the parasitics increases, the voltage drop (ΔV) across the parasitic element increases, which causes the transmitter RF performance ($P_{O,1dB}$, $P_{O,MAX}$, and so on) to degrade. The choke inductance (L_C) must be at least 3× times higher than the load impedance at the lowest desired frequency so that it does not degrade the output power (see Table 10).

The recommended dc bias network is shown in Figure 294. This network has fewer parasitics and fewer total components.

Figure 295 through Figure 298 identify four basic differential transmitter output configurations. Except for in cases in which impedance is already matched, impedence matching networks (balun single-ended port) are required to achieve optimum device performance from the device. In applications in which the transmitter is not connected to another circuit that requires or can tolerate dc bias on the transmitter outputs, the transmitter outputs must be ac-coupled in because of the dc bias voltage applied to the differential output lines of the transmitter.

The recommended RF transmitter interface is shown in Figure 293 to Figure 298 featuring a center tapped balun. This configuration offers the lowest component count of the options presented.

Descriptions of the transmitter port interface schemes are as follows:

- In Figure 295, the center tapped transformer passes the bias voltage directly to the transmitter outputs.
- In Figure 296, RF chokes bias the differential transmitter output lines. Additional coupling capacitors (C_C) are added in the creation of a transmission line balun
- In Figure 297, RF chokes are used to bias the differential transmitter output lines and connect into a transformer
- In Figure 298, RF chokes bias the differential output lines that are ac-coupled into the input of a driver amplifier.

If a transmitter balun that requires a set of external dc bias chokes is selected, careful planning is required. It is necessary to find the optimum compromise between the choke physical size, choke dc resistance, and the balun low frequency insertion loss. In commercially available dc bias chokes, resistance decreases as size increases. As choke inductance increases, resistance increases. It is undesirable to use physically small chokes with high inductance because small chokes exhibit the greatest resistance. For example, the voltage drop of a 500 nH 0603 choke at 100 mA is roughly 50 mV.

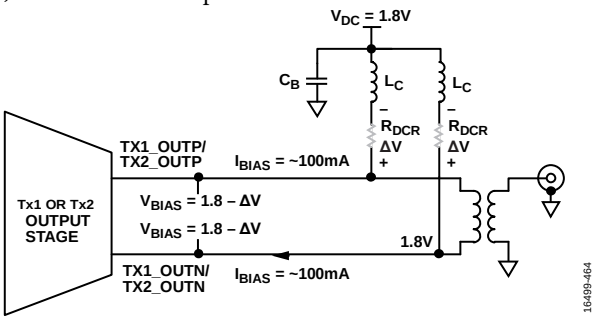


Figure 293. ADRV9008-2 RF DC Bias Configurations Depicting Parasitic Losses Due to Wire Wound Chokes

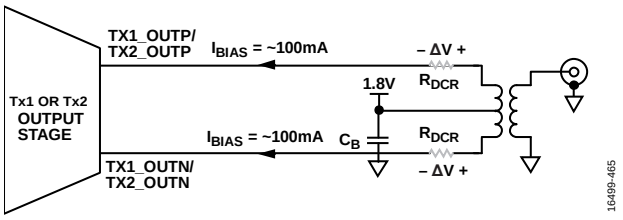


Figure 294. ADRV9008-2 RF DC Bias Configurations Depicting Parasitic Losses Due to Center Tapped Transformers

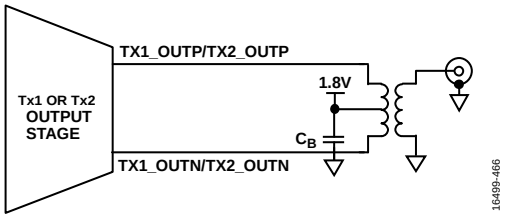


Figure 295. ADRV9008-2 RF Transmitter Interface Configurations

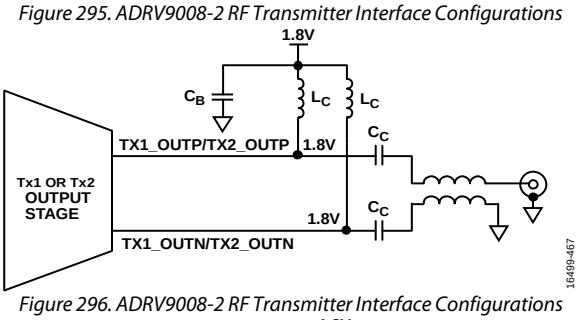


Figure 296. ADRV9008-2 RF Transmitter Interface Configurations

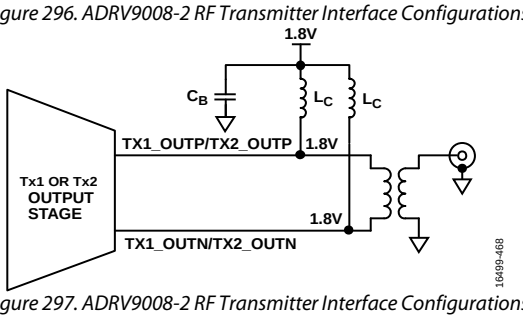


Figure 297. ADRV9008-2 RF Transmitter Interface Configurations

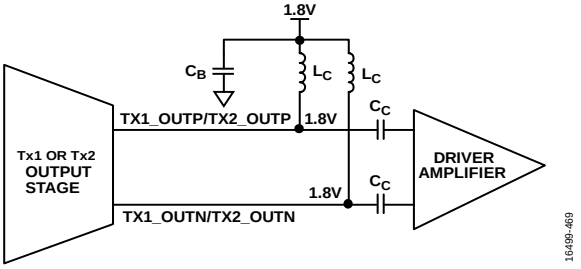


Figure 298. ADRV9008-2 RF Transmitter Interface Configurations

Table 10. Sample Wire Wound DC Bias Choke Resistance vs. Size vs. Inductance

Inductance (nH)	Resistance (Size: 0603)	Resistance (Size: 1206)
100	0.10	0.08
200	0.15	0.10
300	0.16	0.12
400	0.28	0.14
500	0.45	0.15
600	0.52	0.20

General Receiver Path Interface

The ADRV9008-2 has three types of receivers. These receivers include two main receive pathways (receiver 1 and receiver 2) and two observation, or DPD, receivers (observation receiver 1 and observation receiver 2). The receivers can support up to 200 MHz bandwidth, and the observation receivers can support up to 450 MHz bandwidth. The receiver channels and observation receiver channels are designed for differential use.

ADRV9008-2 receivers support a wide range of operation frequencies. In the case of the receiver channels and observation receiver channels, the differential signals interface to an integrated mixer. The mixer input pins have a dc bias of approximately 0.7 V and may need to be ac-coupled depending on the common-mode voltage level of the external circuit.

Important considerations for the receiver port interface are as follows:

- The device to be interfaced (filter, balun, T/R switch, external LNA, external PA, and so on).
- The receiver and observation receiver maximum safe input power is 23 dBm (peak).
- The receiver and observation receiver optimum dc bias voltage is 0.7 V bias to ground.
- The board design (reference planes, transmission lines, impedance matching, and so on).

Figure 299 and Figure 300 show possible differential receiver port interface circuits. The options in Figure 299 and Figure 300 are valid for all receiver inputs operating in differential mode, though only the receiver 1 signal names are indicated. Impedance matching may be necessary to obtain the performance levels.

Given wide RF bandwidth applications, SMD balun devices function well. Decent loss and differential balance are available in a relatively small (0603, 0805) package.

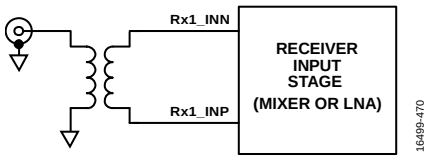


Figure 299. Differential Receiver Interface Using a Transformer

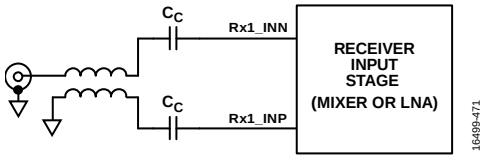


Figure 300. Differential Receiver Interface Using a Transmission Line Balun

Impedance Matching Network Examples

Impedance matching networks are required to achieve the ADRV9008-2 performance levels. This section provides example topologies and components used on the ADRV9008-2 customer evaluation boards.

Device models, board models, balun and SMD component models are required to build an accurate system level simulation. The board layout model can be obtained from an electromagnetic momentum (EM) simulator. The balun and SMD component models can be obtained from the device vendors or built locally. Contact Analog Devices applications engineering for ADRV9008-2 modeling details.

The impedance matching networks provided in this section have not been evaluated in terms of mean time to failure (MTTF) in high volume production. Consult with component vendors for long-term reliability concerns. Consult with balun vendors to determine appropriate conditions for dc biasing.

Figure 303 shows three elements in parallel marked do not install (DNI). However, only one set of SMD component pads is placed on the board. For example, R202, L202, and C202 components only have one set of SMD pads for one SMD component. Figure 303 shows that in a generic port impedance matching network, the shunt or series elements may be a resistor, inductor, or capacitor.

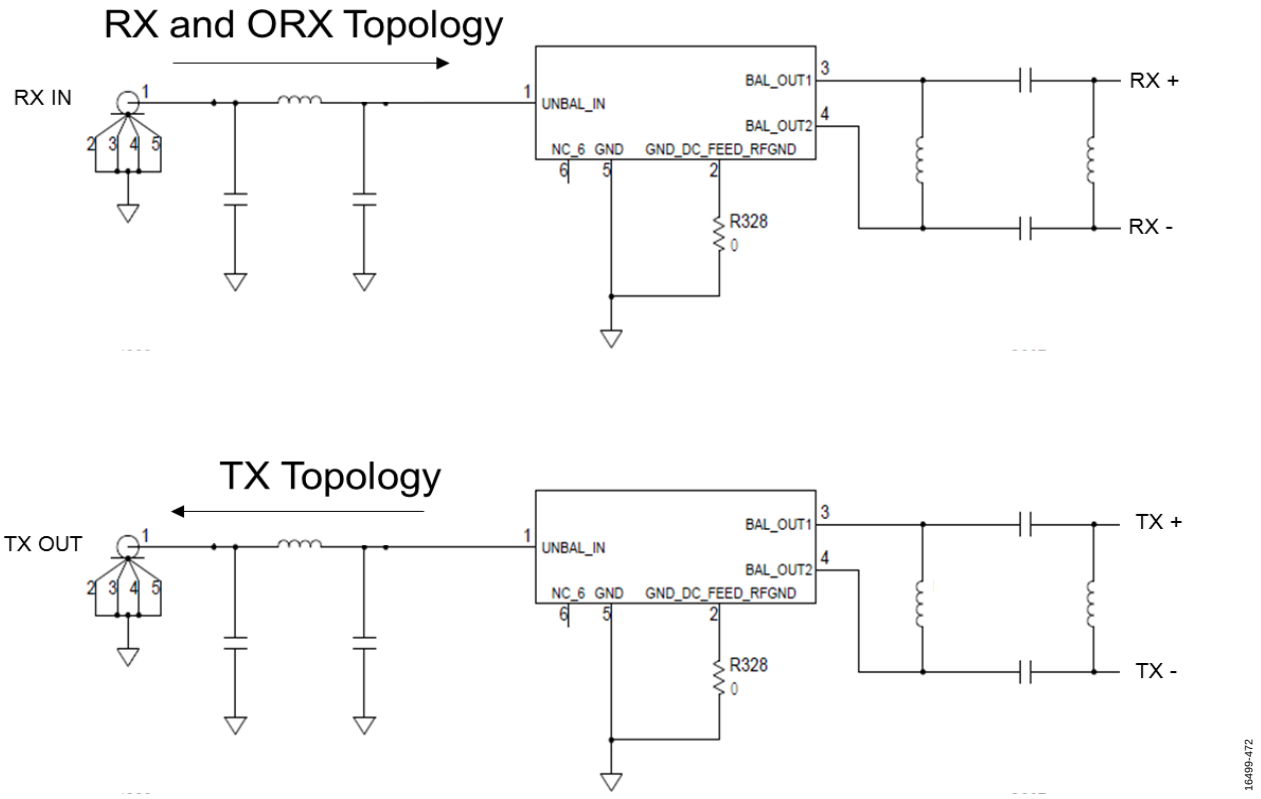


Figure 301. Impedance Matching Topology

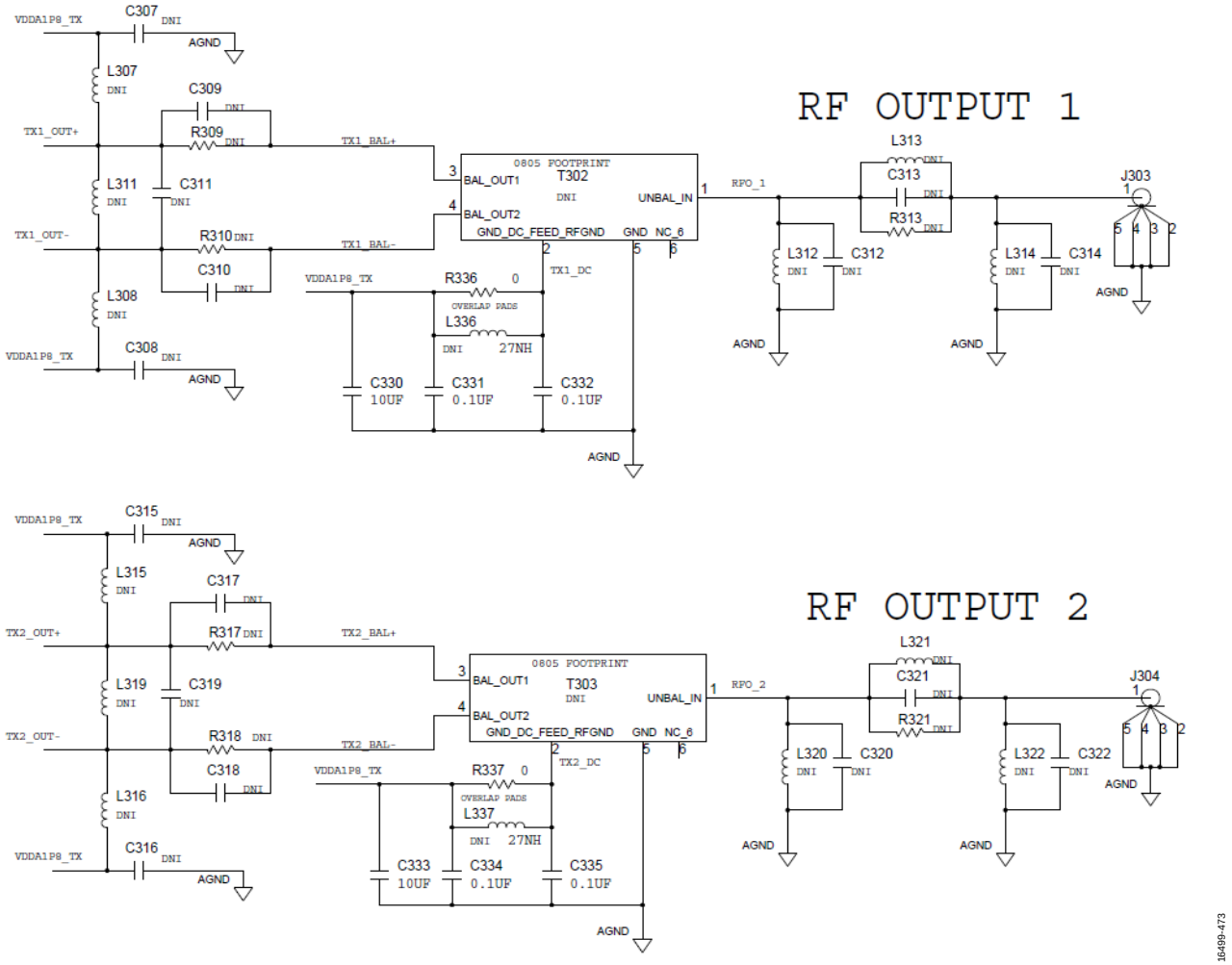


Figure 302. Transmitter 1 and Transmitter 2 Generic Matching Network Topology

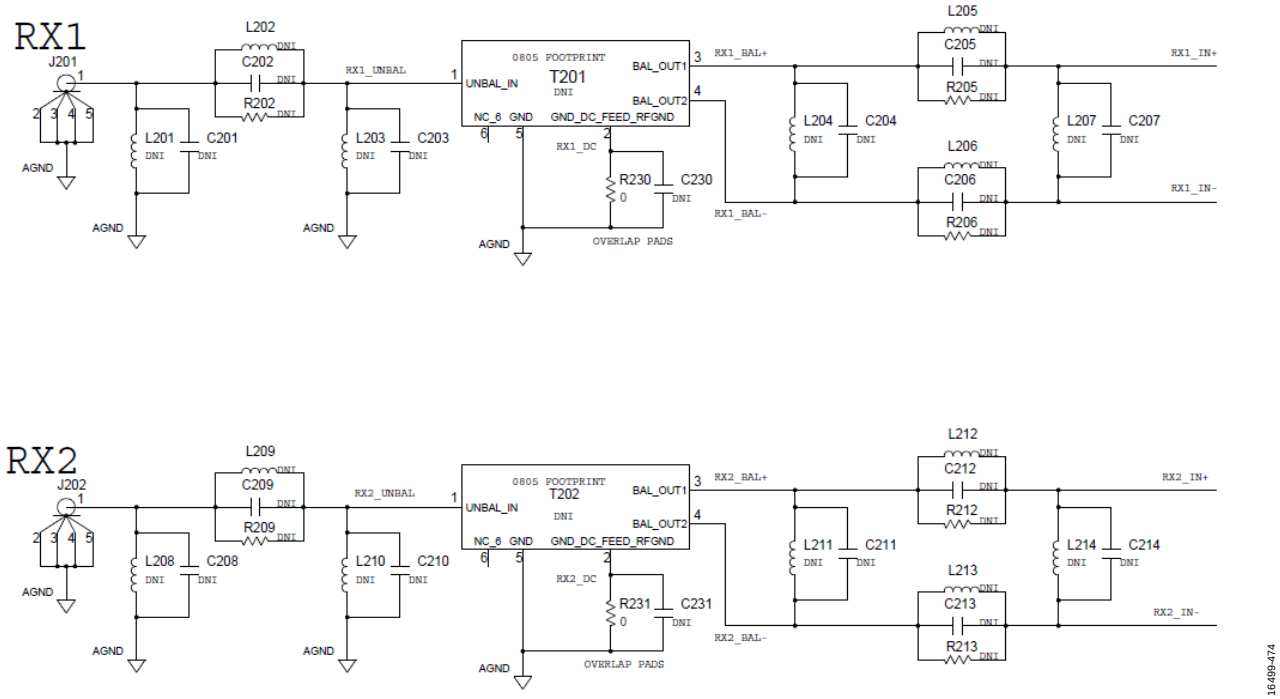


Figure 303. Rx1 and Rx2 Generic Matching Network Topology

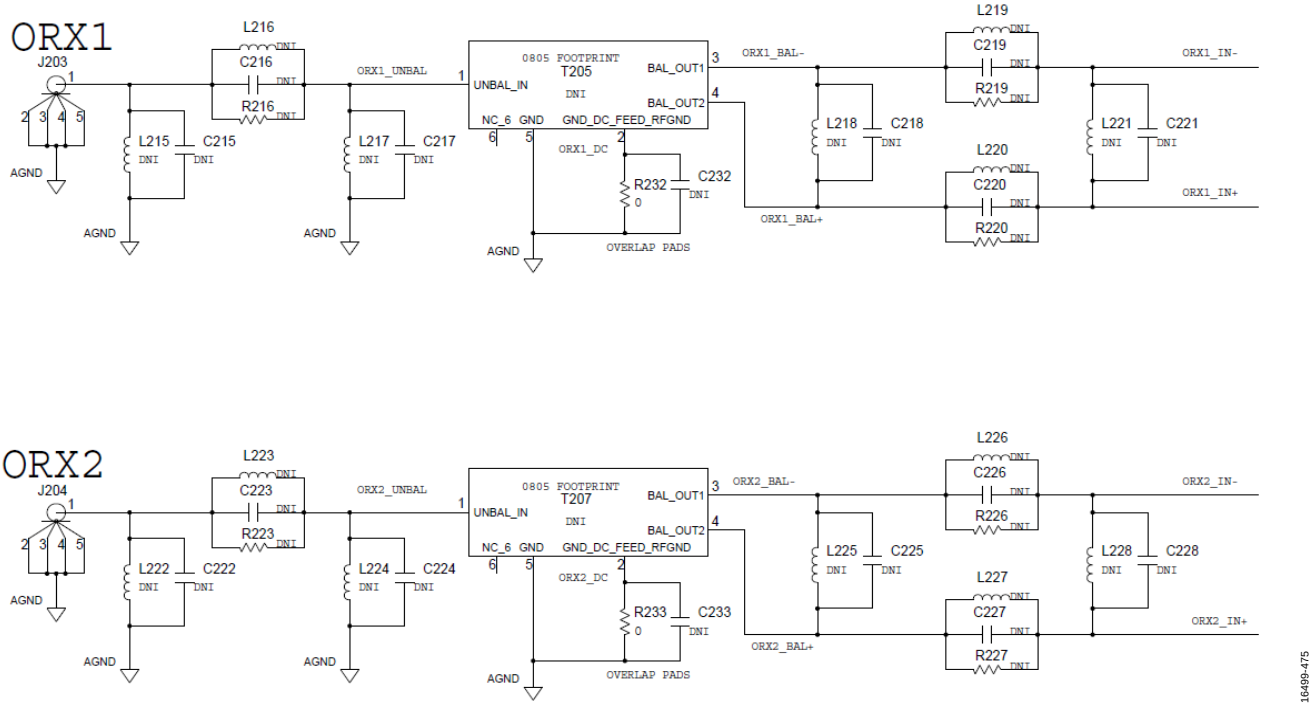


Figure 304. Observation Receiver 1 and Observation Receiver 2 Generic Matching Network Topology

Table 11 through Table 16 show the selected balun and component values used for three matching network sets. Refer to the ADRV9008-2 schematics for a wideband matching example that operates across the entire device frequency range with somewhat reduced performance.

The RF matching used in the ADRV9008-2 evaluation board allows the device to operate across the entire chip frequency range with slightly reduced performance. See the board support files included with the evaluation board software for component configuration and part numbers.

Table 11. Rx1 EVB Matching Components

Frequency Band	201	202	203	204	205, 206	207	T201
625 MHz to 2815 MHz	22 nH	12 pF	62 nH	180 nH	39 pF	91 nH	Johanson 1720BL15A0100
3400 MHz to 4800 MHz	Do not install	0 Ω	Do not install	18 nH	1.3 nH	0.4 pF	Anaren BD3150L50100AHF
5300 MHz to 5900 MHz	Do not install	0.6 nH	Do not install	Do not install	0.4 pF	4.3 nH	Johanson 5400BL15B200

Table 12. Rx2 EVB Matching Components

Frequency Band	208	209	210	211	212, 213	214	T202
625 MHz to 2815 MHz	22nH	12 pF	62 nH	180 nH	39 pF	91 nH	Johanson 1720BL15A0100
3400 MHz to 4800 MHz	Do not install	0 Ω	Do not install	18 nH	1.3 nH	0.4 pF	Anaren BD3150L50100AHF
5300 MHz to 5900 MHz	Do not install	0.6 nH	Do not install	Do not install	0.4 pF	4.3 nH	Johanson 5400BL15B200

Table 13. ORx1 EVB Matching Components

Frequency Band	215	216	217	218	219, 220	221	T205
625 MHz to 2815 MHz	Do not install	0 Ω	Do not install	56 nH	5.6 pF	180 nH	Johanson 1720BL15A0100
3400 MHz to 4800 MHz	0.3 pF	1.6 pF	2 nH	6.8 nH	1.7 nH	220 nH	Anaren BD3150L50100AHF
5300 MHz to 5900 MHz	100nH	6.8 pF	5.6 nH	Do not install	0.8 pF	1.5 nH	Johanson 5400BL15B200

Table 14. ORx2 EVB Matching Components

Frequency Band	222	223	224	225	226, 227	228	T207
625 MHz to 2815 MHz	Do not install	0 Ω	Do not install	56 nH	5.6 pF	180 nH	Johanson 1720BL15A0100
3400 MHz to 4800 MHz	0.3 pF	1.6 pF	2 nH	6.8 nH	1.7 nH	220 nH	Anaren BD3150L50100AHF
5300 MHz to 900 MHz	100 nH	6.8 pF	5.6 nH	Do not install	0.8 pF	1.5 nH	Johanson 5400BL15B200

Table 15. Tx1 EVB Matching Components [1]

Frequency Band	314	313	312	309, 310	311	T302	T302 PIN 2, Bypass Capacitor C332	C307, C308, L307, L308
625 MHz to 2815 MHz	22 nH	4.7 pF	43 nH	0 Ω	0.2 pF	Johanson 1720BL15B0050	33 pF	DNI
3400 MHz to 4800 MHz	DNI	0 Ω	DNI	2.7 nH	0.2 pF	Anaren BD3150L50100AHF	3.9 pF	DNI
5300 MHz to 5900 MHz	DNI	0 Ω	DNI	0.9 nH	8.2 nH	Johanson 5400BL14B100	1.8 pF	DNI

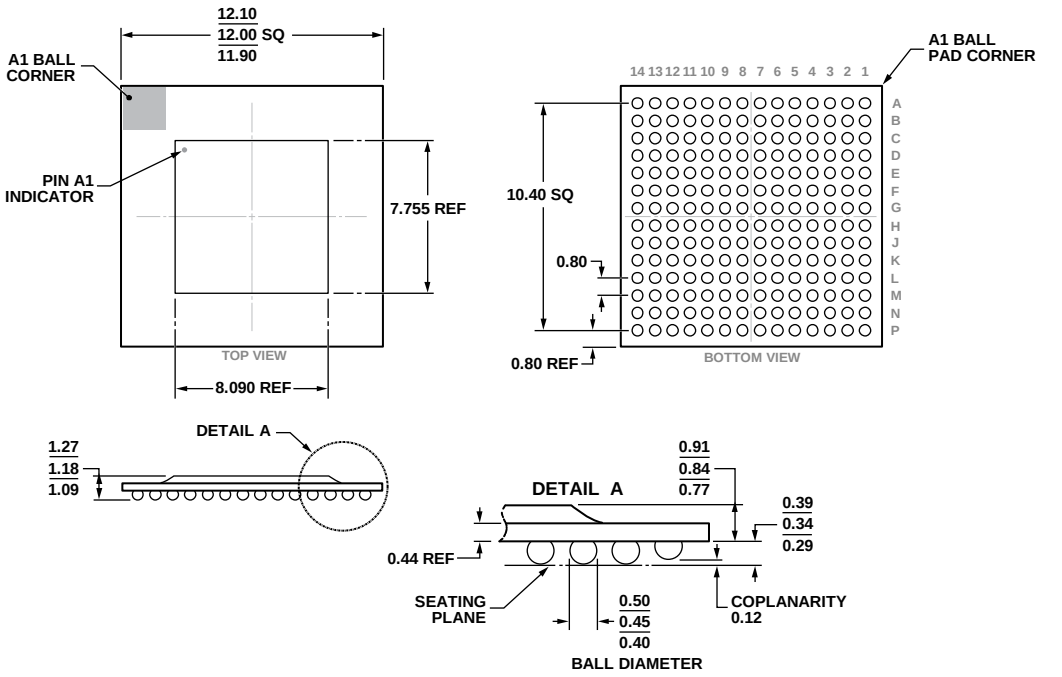
[1] These matches provide VDDA1P8_TX to the TXx_OUT+/- pins through the balun

Table 16. Tx2 EVB Matching Components [1]

Frequency Band	322	321	320		317, 318	319	T303	T303 PIN 2, Bypass Capacitor C335	C315, C316, L315, L316
625 MHz to 2815 MHz	22 nH	4.7 pF	43 nH		0 Ω	0.2 pF	Johanson 1720BL15B0050	33 pF	DNI
3400 MHz to 4800 MHz	DNI	0 Ω	DNI		2.7 nH	0.2 pF	Anaren BD3150L50100AHF	3.9 pF	DNI
5300 MHz to 5900 MHz	DNI	0 Ω	DNI		0.9 nH	8.2 nH	Johanson 5400BL14B100	1.8 pF	DNI

[1] These matches provide VDDA1P8_TX to the TXx_OUT+/- pins through the balun

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-275-GGAB-1.

Figure 305. 196-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-196-13)
Dimensions shown in millimeters

PR16833-0-6/18(PrA)