OptiMOS™-T Power-Transistor

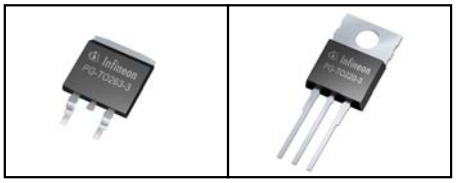
AEC Qualified

RoHS

Product Summary

V_{DS}	250	V
$R_{DS(on),max}$	100	mΩ
I_D	17	A

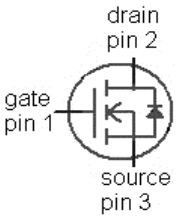
PG-TO263-3-2 PG-TO220-3-1



Features

- N-channel - Enhancement mode
- AEC qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green Product (RoHS compliant)
- 100% Avalanche tested

Type	Package	Marking
IPB17N25S3-100	PG-TO263-3-2	3N25100
IPP17N25S3-100	PG-TO220-3-1	3N25100



Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	T_C=25 °C, V_{GS}=10 V	17	A
		T_C=100°C, V_{GS}=10V[1)]	13.3	
Pulsed drain current[1)]	$I_{D,pulse}$	T_C=25°C	68	
Avalanche energy, single pulse[1)]	E_{AS}	I_D=5.4A	54	mJ
Avalanche current, single pulse	I_{AS}	-	5.4	A
Reverse diode dv/dt	dv/dt	-	6	kV/µs
Gate source voltage	V_{GS}	-	±20	V
Power dissipation	P_{tot}	T_C=25°C	107	W
Operating and storage temperature	T_j, T_{stg}	-	-55 ... +175	°C
IEC climatic category; DIN IEC 68-1	-	-	55/175/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics[1]						
Thermal resistance, junction - case	R_{thJC}	-	-	-	1.4	K/W
Thermal resistance, junction - ambient, leaded	R_{thJA}	-	-	-	62	
SMD version, device on PCB	R_{thJA}	minimal footprint	-	-	62	
		6 cm^2 cooling area[2]	-	-	40	
Electrical characteristics, at T_j=25 °C, unless otherwise specified						
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D= 1mA	250	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=54µA	2.0	3.0	4.0	
Zero gate voltage drain current	I_{DSS}	V_{DS}=250V, V_{GS}=0V	-	0.01	1	µA
		V_{DS}=250V, V_{GS}=0V, T_j=125°C[2]	-	1	100	
Gate-source leakage current	I_{GSS}	V_{GS}=20V, V_{DS}=0V	-	10	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=17A	-	85	100	mΩ

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics[1]						
Input capacitance	C_{iss}	V_{GS}=0V, V_{DS}=25V, f=1MHz	-	1133	1500	pF
Output capacitance	C_{oss}		-	480	625	
Reverse transfer capacitance	C_{rss}		-	11	23	
Turn-on delay time	$t_{d(on)}$	V_{DD}=125V, V_{GS}=10V, I_D=17A, R_G=3.3Ω	-	4.4	-	ns
Rise time	t_r		-	3.7	-	
Turn-off delay time	$t_{d(off)}$		-	7.5	-	
Fall time	t_f		-	1.2	-	
Gate Charge Characteristics[1), 3)]						
Gate to source charge	Q_{gs}	V_{DD}=200V, I_D=17A, V_{GS}=0 to 10V	-	5	7	nC
Gate to drain charge	Q_{gd}		-	2.4	4.8	
Gate charge total	Q_g		-	14	19	
Gate plateau voltage	$V_{plateau}$		-	4.6	-	V
Reverse Diode						
Diode continous forward current[1)]	I_S	T_C=25°C	-	-	17	A
Diode pulse current[1)]	$I_{S,pulse}$		-	-	56	
Diode forward voltage	V_{SD}	V_{GS}=0V, I_F=17A, T_j=25°C	-	0.9	1.3	V
Reverse recovery time[1)]	t_{rr}	V_R=125V, I_F=17A, di_F/dt=100A/µs	-	120	-	ns
Reverse recovery charge[1)]	Q_{rr}		-	525	-	nC

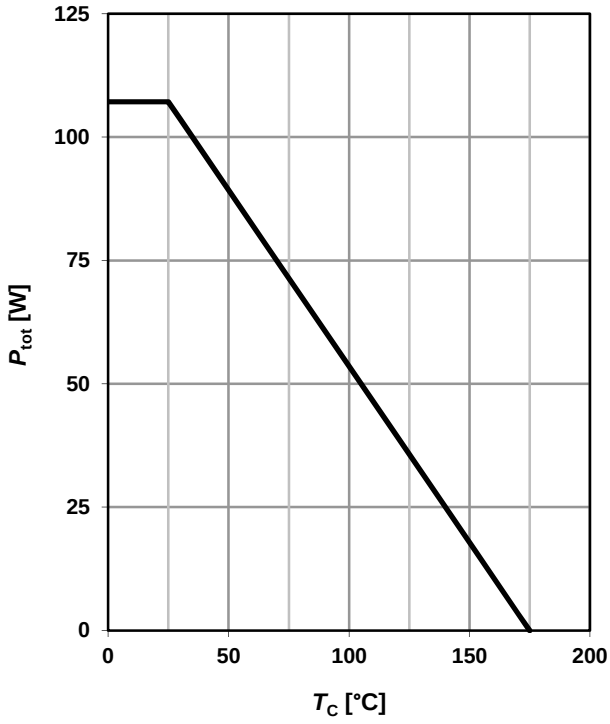
[1)] Defined by design. Not subject to production test.

[2)] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

[3)] Devices thermal performance determined according to EIA JESD 51-14 "Transient Dual Interface Test Method For The Measurement Of The Thermal Resistance"

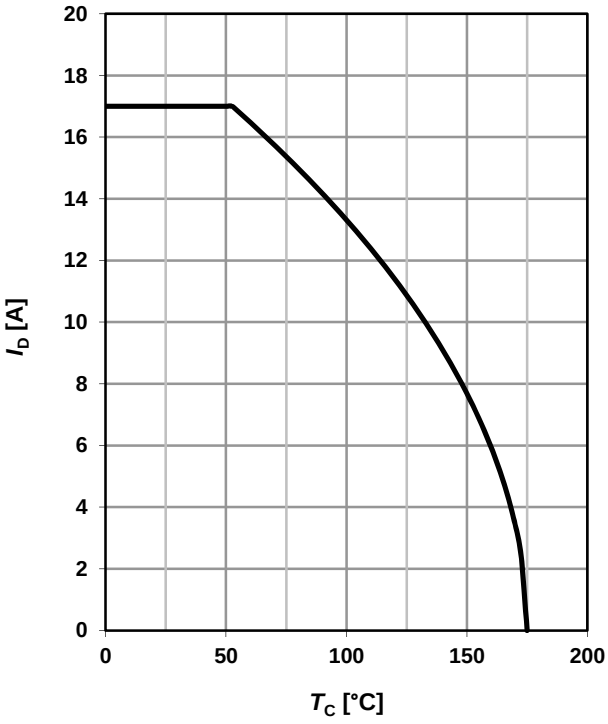
1 Power dissipation

$P_{tot} = f(T_C)$; $V_{GS} \geq 6$ V



2 Drain current

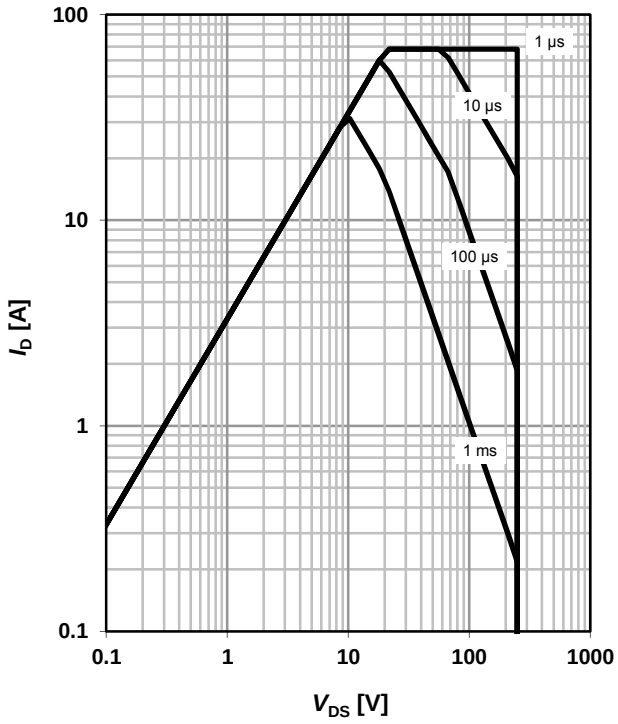
$I_D = f(T_C)$; $V_{GS} \geq 6$ V; SMD



3 Safe operating area

$I_D = f(V_{DS})$; $T_C = 25$ °C; $D = 0$; SMD

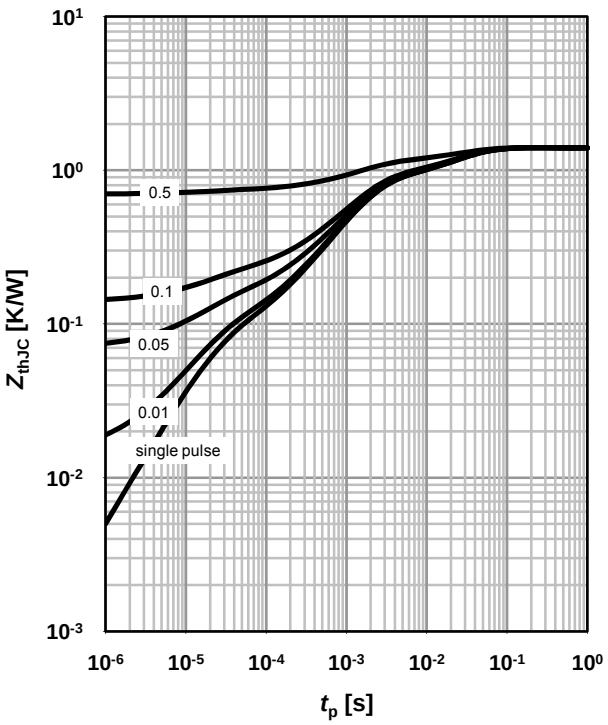
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJC} = f(t_p)$

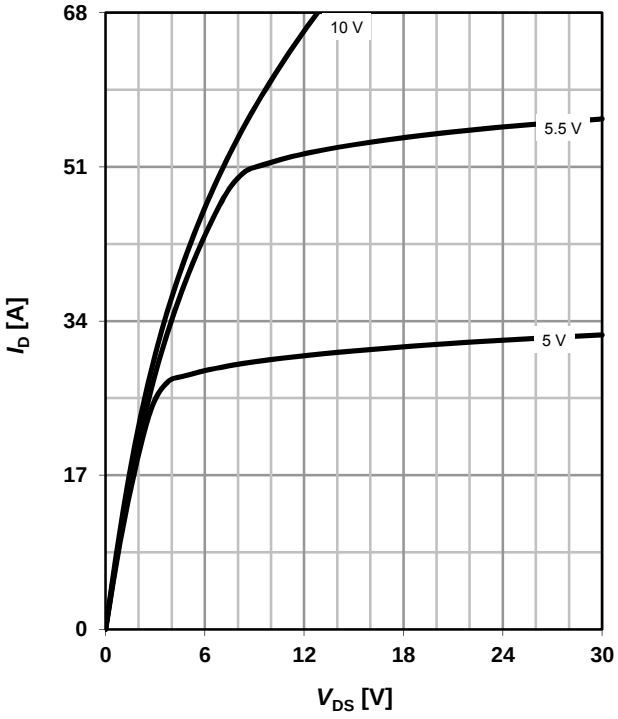
parameter: $D = t_p/T$



5 Typ. output characteristics

$I_D = f(V_{DS})$; $T_j = 25$ °C; SMD

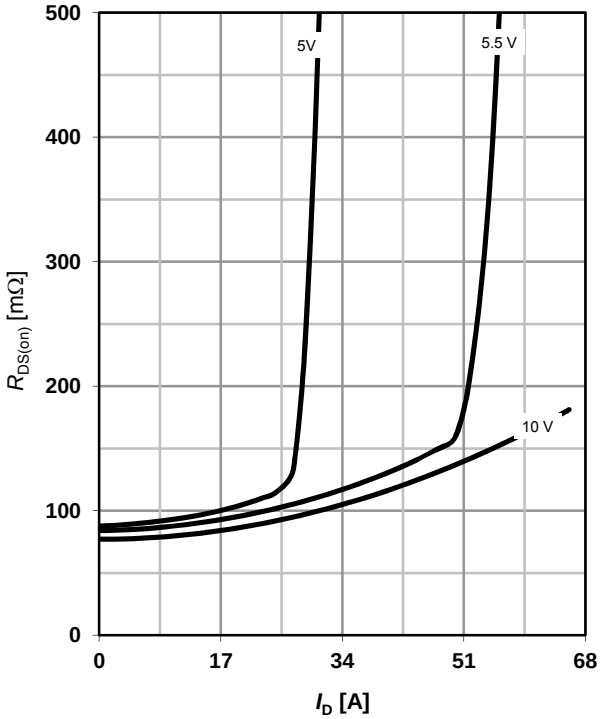
parameter: V_{GS}



6 Typ. drain-source on-state resistance

$R_{DS(on)} = f(I_D)$; $T_j = 25$ °C; SMD

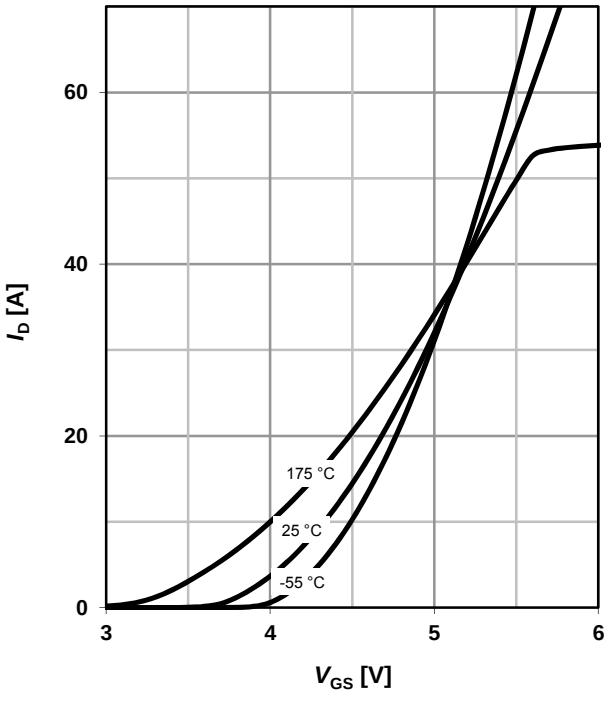
parameter: V_{GS}



7 Typ. transfer characteristics

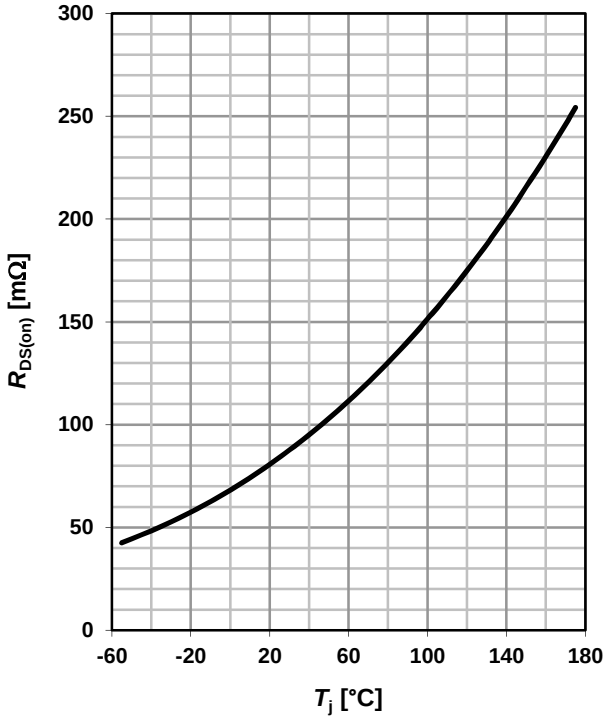
$I_D = f(V_{GS})$; $V_{DS} = 25$V

parameter: T_j



8 Typ. drain-source on-state resistance

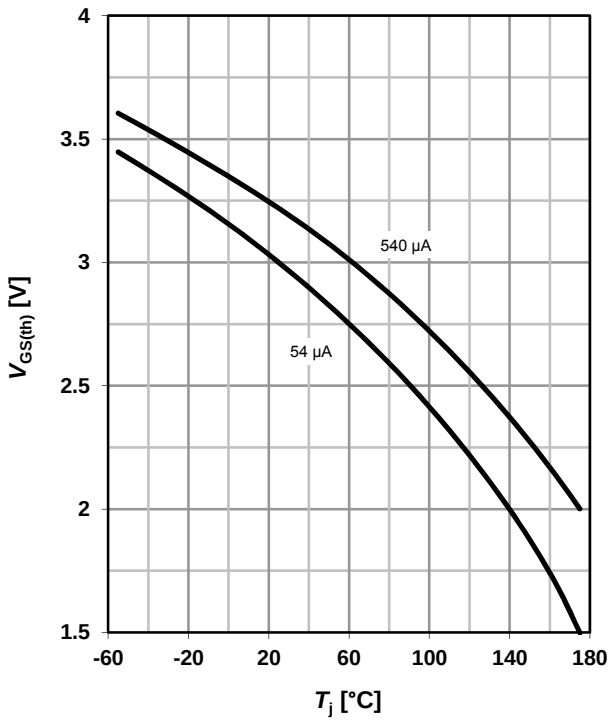
$R_{DS(on)} = f(T_j)$; $I_D = 17$ A; $V_{GS} = 10$ V; SMD



9 Typ. gate threshold voltage

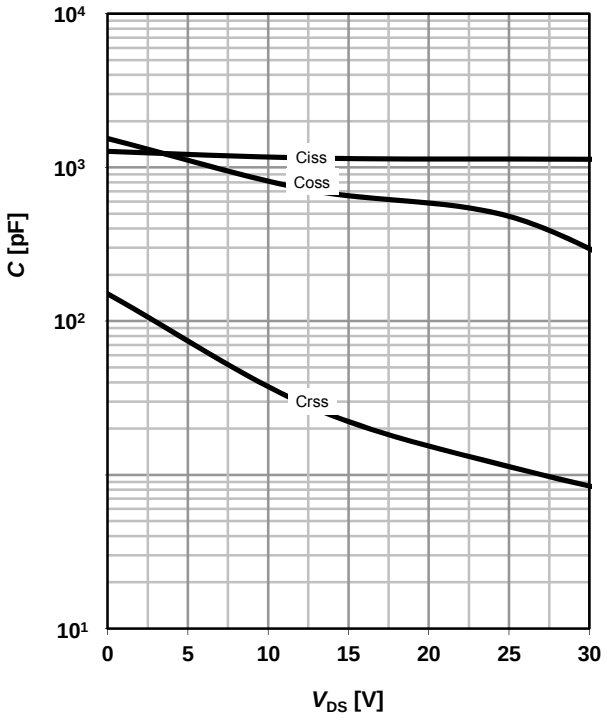
$V_{GS(th)} = f(T_j)$; $V_{GS} = V_{DS}$

parameter: I_D



10 Typ. capacitances

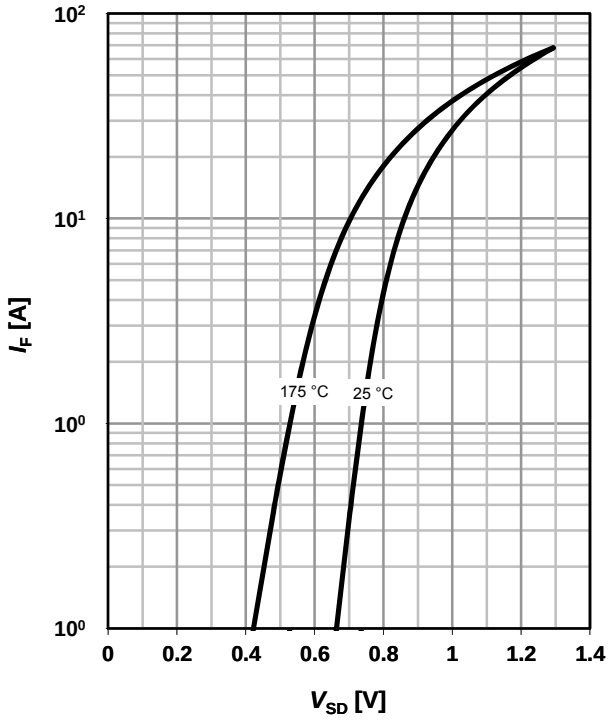
$C = f(V_{DS})$; $V_{GS} = 0$ V; $f = 1$ MHz



11 Typical forward diode characteristicis

IF = f(V_{SD})

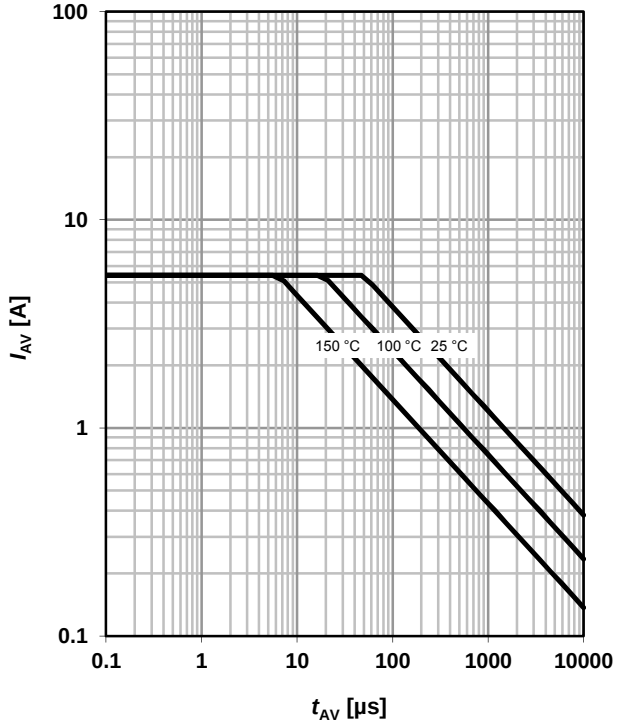
parameter: T_j



12 Avalanche characteristics

$I_{AS} = f(t_{AV})$

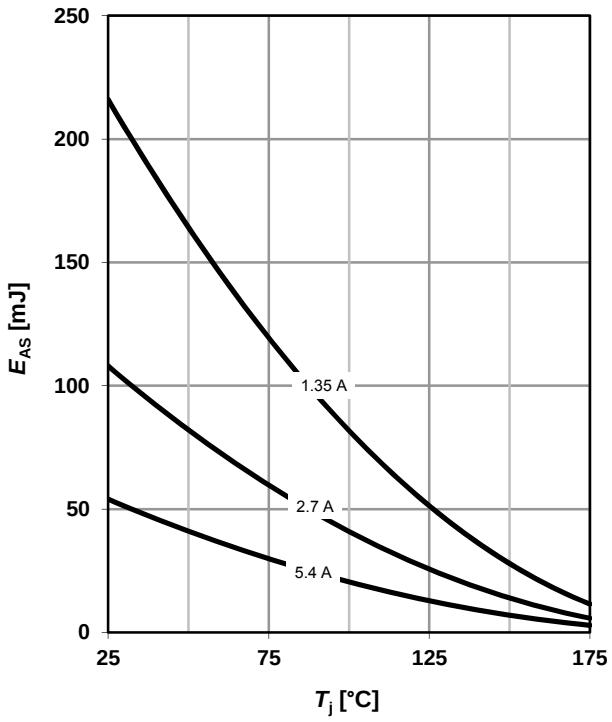
parameter: $T_{j(start)}$



13 Avalanche energy

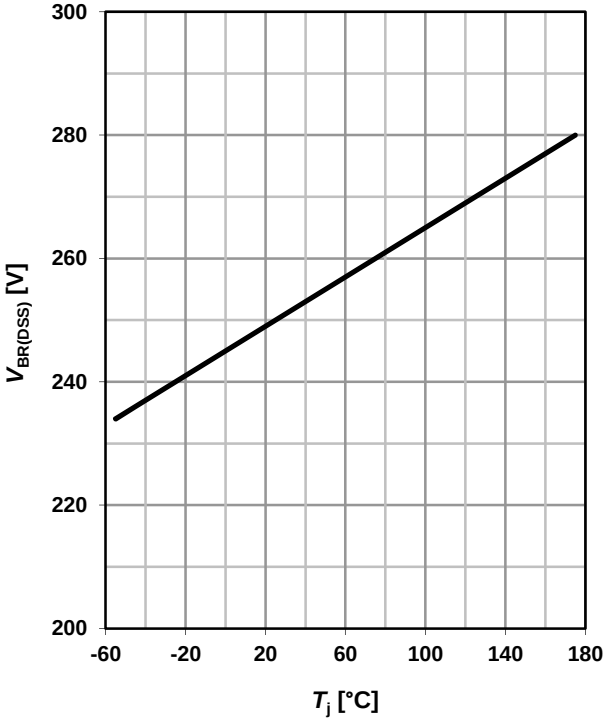
$E_{AS} = f(T_j)$

parameter: I_D



14 Drain-source breakdown voltage

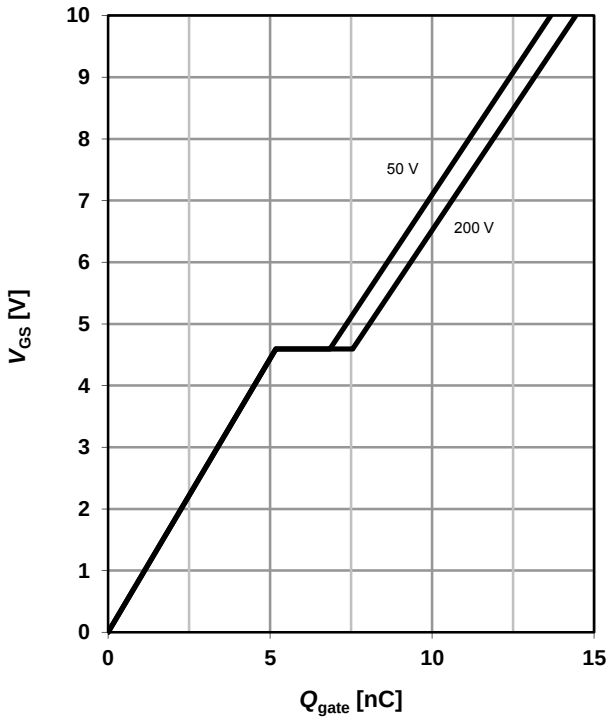
$V_{BR(DSS)} = f(T_j)$; $I_D = 1$ mA



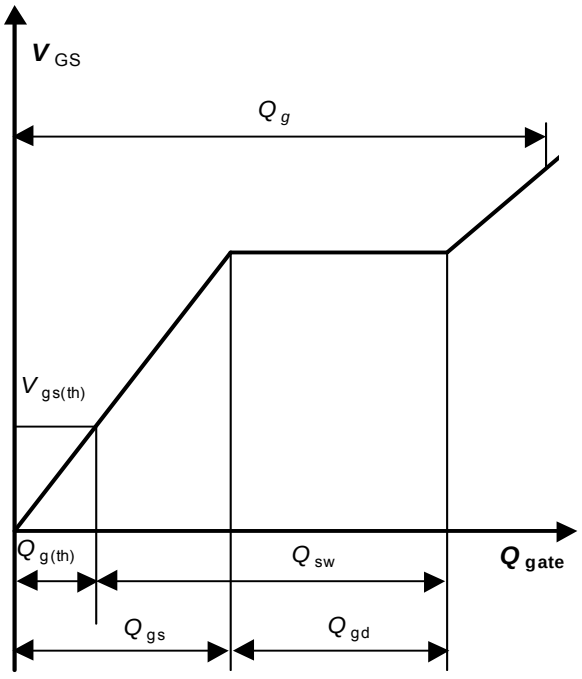
15 Typ. gate charge

$V_{GS} = f(Q_{gate})$; $I_D = 17$ A pulsed

parameter: V_{DD}



16 Gate charge waveforms



Published by
Infineon Technologies AG
81726 Munich, Germany

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If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

Revision History

Version	Date	Changes
Revision 1.0	18.10.2012	Final Data Sheet
Revision 1.1	12.05.2013	Update of diagram 5 and 6