



MICROCHIP PIC18F87J11 FAMILY

PIC18F87J11 Family Rev. A1 Silicon Errata

The PIC18F87J11 Family parts you have received conform functionally to the Device Data Sheet (DS39778B), except for the anomalies described below.

Any Data Sheet Clarification issues related to the PIC18F87J11 Family devices will be reported in a separate Data Sheet errata. Please check the Microchip web site for any existing issues.

The following silicon errata apply only to PIC18F87J11 Family devices with these Device/Revision IDs:

Part Number	Device ID	Revision ID
PIC18F66J11	0100 0100 010	0 0001
PIC18F66J16	0100 0100 011	0 0001
PIC18F67J11	0100 0100 100	0 0001
PIC18F86J11	0100 0100 111	0 0001
PIC18F86J16	0100 0101 000	0 0001
PIC18F87J11	0100 0101 001	0 0001

The Device IDs (DEVID1 and DEVID2) are located at addresses 3FFFFEh:3FFFFFh in the device's configuration space. They are shown in binary in the format "DEVID2 DEVID1".

1. Module: Voltage Regulator

If VDDCORE drops below approximately 2.45V while the on-chip core voltage regulator is enabled and operating in Voltage Tracking mode, the REGSLP bit (WDTCON <7>) will be automatically cleared. The REGSLP bit cannot be set again by firmware until VDDCORE rises back above the 2.45V approximate threshold.

Additionally, the REGSLP bit retains its previous state upon all Resets except POR.

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

2. Module: SRAM

Any access to SRAM – either in the form of read or write operations – will increase the current consumption of the device, depending on how often the SRAM is accessed. A small current increase is normal, but in this revision, the difference may be significant and of particular concern for low-power applications.

For further details, see Table 1.

TABLE 1: TYPICAL CURRENT CONSUMPTION

Case 1:			
Voltage Regulator Enabled Temperature = 25°C SEC_RUN mode using 32 kHz Timer1 crystal			
Condition	IDD (μA)	VDD (V)	
No RAM access ⁽¹⁾	59	3.3	
Typ RAM access ⁽²⁾	201	3.3	
Extreme RAM access ⁽³⁾	906	3.3	
Case 2:			
Voltage Regulator Disabled VDDCORE is tied to VDD Temperature = 25°C SEC_RUN mode using 32 kHz Timer1 crystal			
Condition	IDD (μA)	VDD (V)	VDDCORE (V)
No RAM access ⁽¹⁾	20	2.5	2.5
Typ RAM access ⁽²⁾	132	2.5	2.5
Extreme RAM access ⁽³⁾	723	2.5	2.5

- Note 1:** Code execution patterns where no instructions access SRAM.
- 2:** Code execution that accesses SRAM once every seven instruction cycles.
- 3:** Code execution where every instruction cycle executes an instruction that accesses SRAM.

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

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3. Module: Low-Voltage Detect

The LVDSTAT bit (WDTCON<6>) is not implemented in this revision of silicon.

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

4. Module: Oscillator Configurations (PLL)

When Phase Lock Loop (PLL) is enabled, if the PLL input frequency is higher than 8 MHz, there may be problems accessing the RAM.

Work around

Limit the PLL input frequency from 4 MHz to 8 MHz. This will cause the system clock to operate from 16 MHz to 32 MHz.

If it is necessary to run the device above 32 MHz, do not enable PLL and use the EC mode.

Date Codes that pertain to this issue:

All engineering and production devices.

REVISION HISTORY

Rev A Document (2/2007)

First revision of this document. Silicon issue 1 (Voltage Regulator), 2 (SRAM) and 3 (Low-Voltage Detect).

Rev B Document (9/2007)

Added silicon issue 4 (Oscillator Configurations – PLL).

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