SiT5022

220-625 MHz High Performance Differential (VC) TCXO

SiTime
The Smart Timing Choice™

Features

- Any frequency between 220 MHz and 625 MHz accurate to 6 decimal places
- LVPECL and LVDS output signaling types
- 0.6ps RMS phase jitter (random) over 12 kHz to 20 MHz bandwidth
- Frequency stability as low as ±5 ppm. Contact SiTime for tighter stability options
- Industrial and extended commercial temperature ranges
- Industry-standard packages: 3.2 x 2.5, 5.0 x 3.2 and 7.0 x 5.0 mm
- For frequencies lower than 220 MHz, refer to SiT5021 datasheet

Applications

- SATA, SAS, 10GB Ethernet, Fibre Channel, PCI-Express
- Networking, broadband, instrumentation

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Electrical Characteristics

Parameter and Conditions	Symbol	Min.	Typ.	Max.	Unit	Condition
LVPECL and LVDS, Common Electrical Characteristics						
Supply Voltage	Vdd	2.97	3.3	3.63	V	
		2.25	2.5	2.75	V	
		2.25	–	3.63	V	Termination schemes in Figures 1 and 2 - XX ordering code
Output Frequency Range	f	220	–	625	MHz	
Initial Tolerance	F_init	-2	–	2	ppm	At 25°C after two reflows
Stability Over Temperature	F_stab	-5	–	+5	ppm	Over operating temperature range at rated nominal power supply voltage and load. **Contact SiTime for tighter stability options.**
Supply Voltage	F_vdd	–	50	–	ppb	±10% Vdd
Output Load	F_load	–	0.1	–	ppm	15 pF ±10% of load
First Year Aging	F_aging1	-2.5	–	+2.5	ppm	25°C
10-year Aging	F_aging10	-5	–	+5	ppm	25°C
Operating Temperature Range	T_use	-40	–	+85	°C	Industrial
		-20	–	+70	°C	Extended Commercial
Pull Range	PR	±12.5, ±25, ±50			ppm	
Upper Control Voltage	VC_U	Vdd-0.1	–	–	V	All Vdds. Voltage at which maximum deviation is guaranteed.
Control Voltage Range	VC_L	–	–	0.1	V	
Control Voltage Input Impedance	Z_vc	100	–	–	kΩ	
Frequency Change Polarity	–	Positive slope			–	
Control Voltage -3dB Bandwidth	V_BW	–	–	8	kHz	
Input Voltage High	VIH	70%	–	–	Vdd	Pin 1, OE or $\overline{ST}$
Input Voltage Low	VIL	–	–	30%	Vdd	Pin 1, OE or $\overline{ST}$
Input Pull-up Impedance	Z_in	–	100	250	kΩ	Pin 1, OE logic high or logic low, or $\overline{ST}$ logic high
		2	–	–	MΩ	Pin 1, $\overline{ST}$ logic low
Start-up Time	T_start	–	6	10	ms	Measured from the time Vdd reaches its rated minimum value.
Resume Time	T_resume	–	6	10	ms	In Standby mode, measured from the time $\overline{ST}$ pin crosses
Duty Cycle	DC	45	–	55	%	Contact SiTime for tighter duty cycle
LVPECL, DC and AC Characteristics						
Current Consumption	Idd	–	61	69	mA	Excluding Load Termination Current, Vdd = 3.3V or 2.5V
OE Disable Supply Current	I_OE	–	–	35	mA	OE = Low
Output Disable Leakage Current	I_leak	–	–	1	µA	OE = Low
Standby Current	I_std	–	–	100	µA	$\overline{ST}$ = Low, for all Vdds
Maximum Output Current	I_driver	–	–	30	mA	Maximum average current drawn from OUT+ or OUT-
Output High Voltage	VOH	Vdd-1.1	–	Vdd-0.7	V	See Figure 1(a)
Output Low Voltage	VOL	Vdd-1.9	–	Vdd-1.5	V	See Figure 1(a)
Output Differential Voltage Swing	V_Swing	1.2	1.6	2.0	V	See Figure 1(b)
Rise/Fall Time	Tr, Tf	–	300	500	ps	20% to 80%, see Figure 1(a)
OE Enable/Disable Time	T_oe	–	–	115	ns	f = 220 MHz - For other frequencies, T_oe = 100ns + 3 period
RMS Period Jitter	T_jitt	–	1.2	1.7	ps	f = 266 MHz, VDD = 3.3V or 2.5V
		–	1.2	1.7	ps	f = 312.5 MHz, VDD = 3.3V or 2.5V
		–	1.2	1.7	ps	f = 622.08 MHz, VDD = 3.3V or 2.5V
RMS Phase Jitter (random)	T_phj	–	0.6	0.85	ps	f = 312.5 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdds

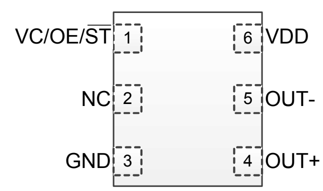
Electrical Characteristics (continued)

Parameter and Conditions	Symbol	Min.	Typ.	Max.	Unit	Condition
LVDS, DC and AC Characteristics						
Current Consumption	Idd	–	47	55	mA	Excluding Load Termination Current, Vdd = 3.3V or 2.5V
OE Disable Supply Current	I_OE	–	–	35	mA	OE = Low
Differential Output Voltage	VOD	250	350	450	mV	See Figure 2
Output Disable Leakage Current	I_leak	–	–	1	µA	OE = Low
Standby Current	I_std	–	–	100	µA	$\overline{ST}$ = Low, for all Vdds
VOD Magnitude Change	ΔVOD	–	–	50	mV	See Figure 2
Offset Voltage	VOS	1.125	1.2	1.375	V	See Figure 2
VOS Magnitude Change	ΔVOS	–	–	50	mV	See Figure 2
Rise/Fall Time	Tr, Tf	–	495	600	ps	20% to 80%, see Figure 2
OE Enable/Disable Time	T_oe	–	–	115	ns	f = 220 MHz - For other frequencies, T_oe = 100ns + 3 period
RMS Period Jitter	T_jitt	–	1.4	1.7	ps	f = 266 MHz, VDD = 3.3V or 2.5V
		–	1.4	1.7	ps	f = 312.5 MHz, VDD = 3.3V or 2.5V
		–	1.2	1.7	ps	f = 622.08 MHz, VDD = 3.3V or 2.5V
RMS Phase Jitter (random)	T_phj	–	0.6	0.85	ps	f = 312.5 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdds

Pin Description

Pin	Map	Functionality	
1	VC/OE/$\overline{ST}$	V Control	Voltage control
		Output Enable	H or Open: specified frequency output L: output is high impedance
		Standby	H or Open: specified frequency output L: Device goes to sleep mode. Supply current reduces to I_std.
2	NC	NA	No Connect; Leave it floating or connect to GND for better heat dissipation
3	GND	Power	VDD Power Supply Ground
4	OUT+	Output	Oscillator output
5	OUT-	Output	Complementary oscillator output
6	VDD	Power	Power supply voltage

Top View



Absolute Maximum

Attempted operation outside the absolute maximum ratings may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Min.	Max.	Unit
Storage Temperature	-65	150	°C
VDD	-0.5	4	V
Electrostatic Discharge (HBM)	–	2000	V
Soldering Temperature (follow standard Pb free soldering guidelines)	–	260	°C

Thermal Consideration

Package	θJA, 4 Layer Board (°C/W)	θJC, Bottom (°C/W)
7050, 6-pin	142	27
5032, 6-pin	97	20
3225, 6-pin	109	20

Environmental Compliance

Parameter	Condition/Test Method
Mechanical Shock	MIL-STD-883F, Method 2002
Mechanical Vibration	MIL-STD-883F, Method 2007
Temperature Cycle	JESD22, Method A104
Solderability	MIL-STD-883F, Method 2003
Moisture Sensitivity Level	MSL1 @ 260°C

Waveform Diagrams

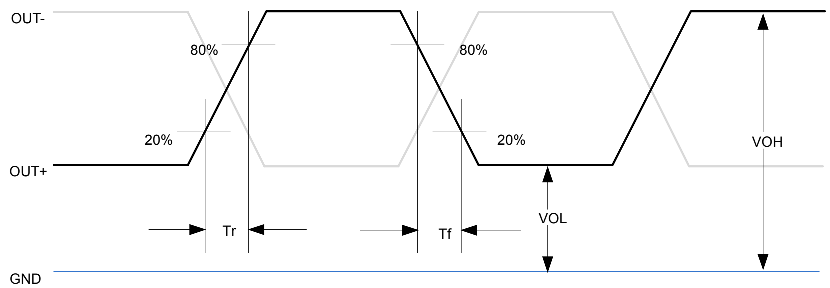


Figure 1(a). LVPECL Voltage Levels per Differential Pin (OUT+/OUT-)

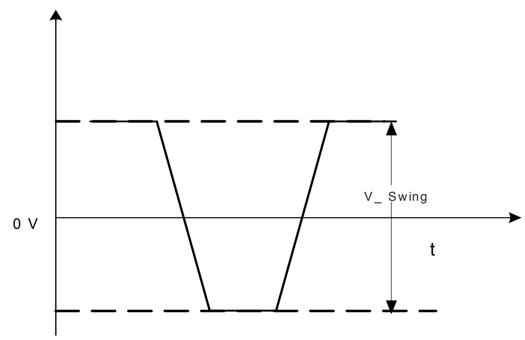


Figure 1(b). LVPECL Voltage Levels Across Differential Pair

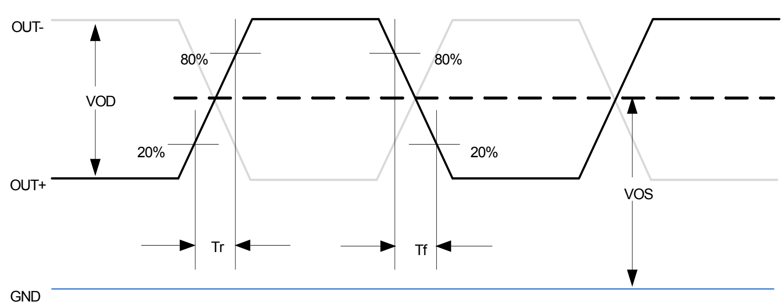


Figure 2. LVDS Voltage Levels per Differential Pin (OUT+/OUT-)

Termination Diagrams

LVPECL:

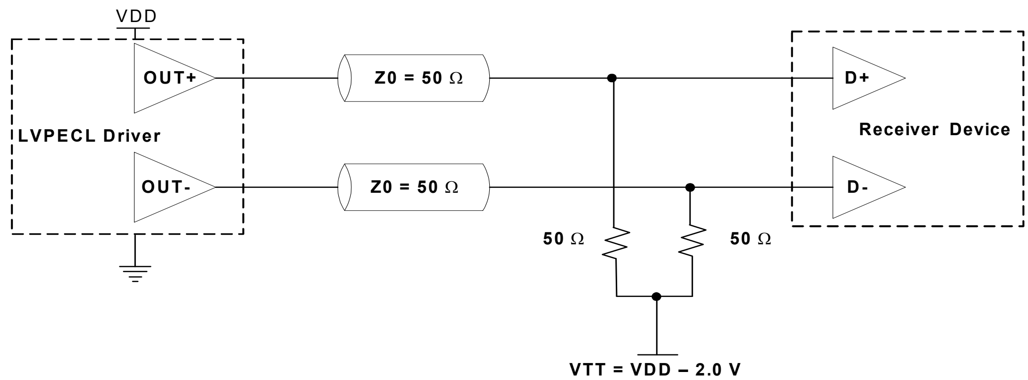


Figure 3. LVPECL Typical Termination

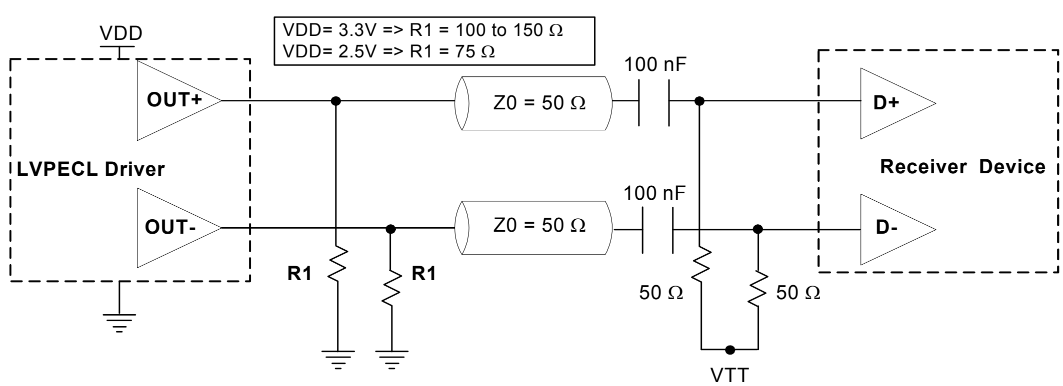


Figure 4. LVPECL AC Coupled Termination

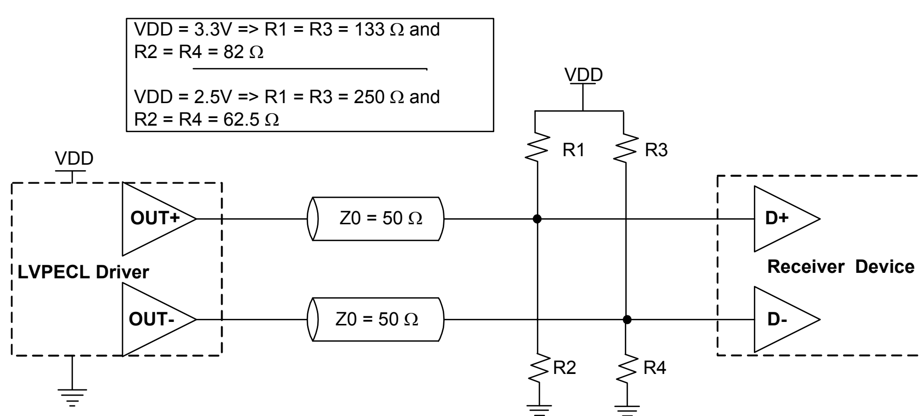


Figure 5. LVPECL with Thevenin Typical Termination

LVDS:

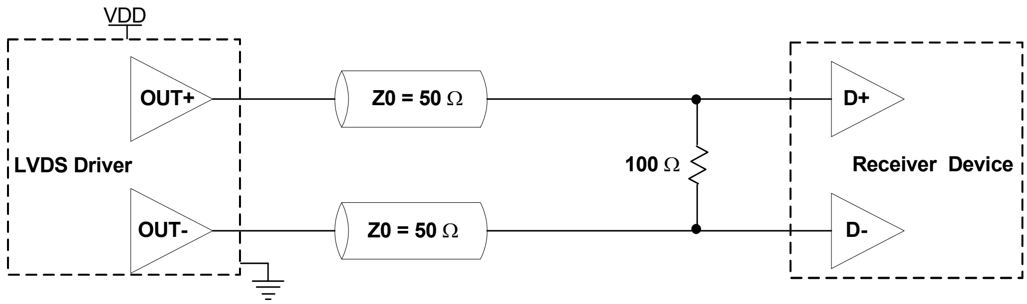
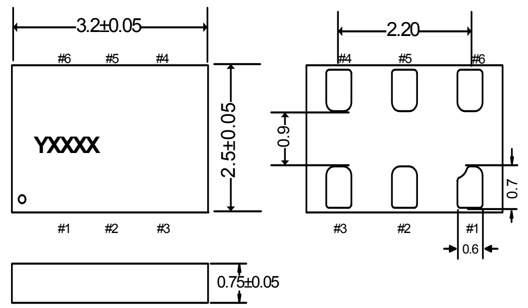
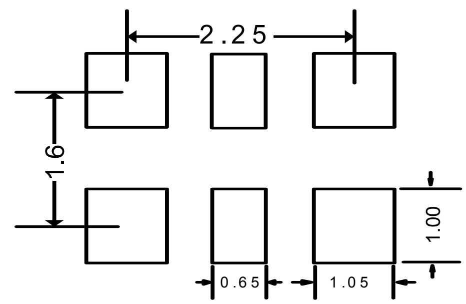


Figure 6. LVDS Single Termination (Load Terminated)

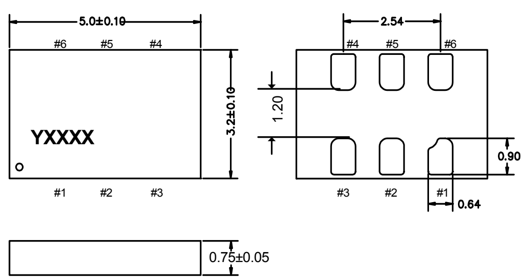
Dimensions and Patterns

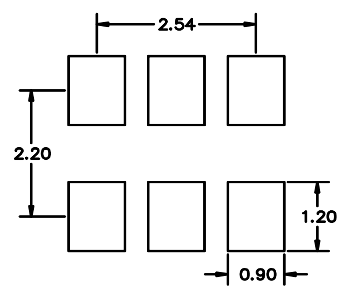
Package Size – Dimensions (Unit: mm)[1]	Recommended Land Pattern (Unit: mm)[2]
3.2 x 2.5x 0.75 mm	



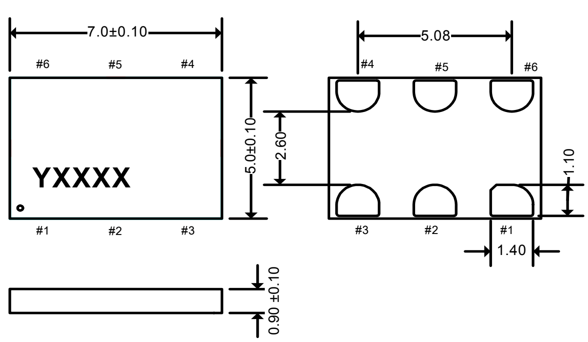


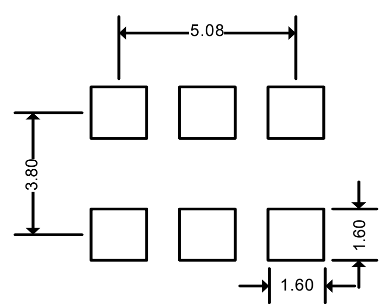
Package Size – Dimensions (Unit: mm)[1]	Recommended Land Pattern (Unit: mm)[2]
5.0 x 3.2 x 0.75 mm	





Package Size – Dimensions (Unit: mm)[1]	Recommended Land Pattern (Unit: mm)[2]
7.0 x 5.0x 0.90 mm	

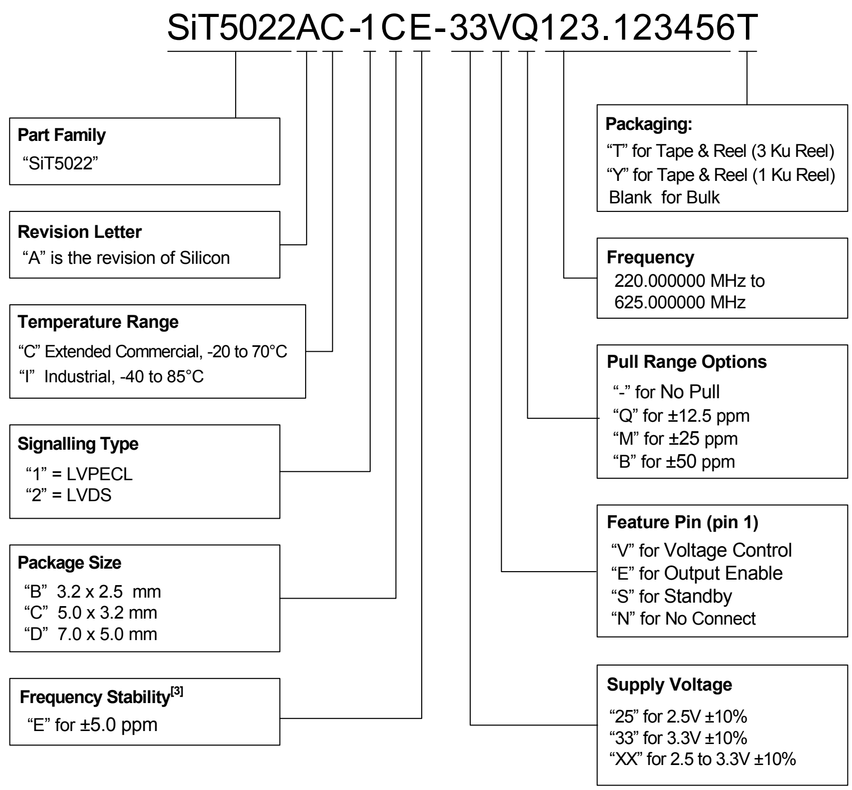




Notes:

1. Top Marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of “Y” will depend on the assembly location of the device.
2. A capacitor of value 0.1 µF between Vdd and GND is recommended.

Ordering Information



Note:

6. Contact SiTime for tighter stability options.

Frequencies Not Supported

Range 1: From 251.000001 MHz to 263.999999 MHz
Range 2: From 314.000001 MHz to 422.999999 MHz
Range 3: From 502.000001 MHz to 527.999999 MHz

Ordering Codes for Supported Tape & Reel Packing Method

Device Size	12 mm T&R (3ku)	12 mm T&R (1ku)	12 mm T&R (250u)	16 mm T&R (3ku)	16 mm T&R (1ku)	16 mm T&R (250u)
7.0 x 5.0 mm	–	–	–	T	Y	X
5.0 x 3.2 mm	T	Y	X	–	–	–
3.2 x 2.5 mm	T	Y	X	–	–	–

Additional Information

Document	Description	Download Link
Manufacturing Notes	Tape & Reel dimension, reflow profile and other manufacturing related info	http://www.sitime.com/component/docman/doc_download/85-manufacturing-notes-for-sitime-oscillators
Qualification Reports	RoHS report, reliability reports, composition reports	http://www.sitime.com/support/quality-and-reliability
Performance Reports	Additional performance data such as phase noise, current consumption and jitter for selected frequencies	http://www.sitime.com/support/performance-measurement-report
Termination Techniques	Termination design recommendations	http://www.sitime.com/support/application-notes
Layout Techniques	Layout recommendations	http://www.sitime.com/support/application-notes

Revision History

Version	Release Date	Change Summary
1.2	8/20/13	Original
1.3	12/16/13	Added input specifications, LVPECL/LVDS waveforms, packaging T&R options
1.4	12/11/14	Modified Thermal Consideration values and Pin Configuration table (pin 1) and drawing
1.5	11/12/15	• Revised stability over temperature and first year aging values in the electrical characteristics table • Revised frequency stability option

Supplemental Information

The Supplemental Information section is not part of the datasheet and is for informational purposes only.

Silicon MEMS Outperforms Quartz

Silicon MEMS Outperforms Quartz

The Smart Timing Choice™

Best Reliability

Silicon is inherently more reliable than quartz. Unlike quartz suppliers, SiTime has in-house MEMS and analog CMOS expertise, which allows SiTime to develop the most reliable products. Figure 1 shows a comparison with quartz technology.

Why is SiTime Best in Class:

- SiTime's MEMS resonators are vacuum sealed using an advanced EpiSeal™ process, which eliminates foreign particles and improves long term aging and reliability
- World-class MEMS and CMOS design expertise

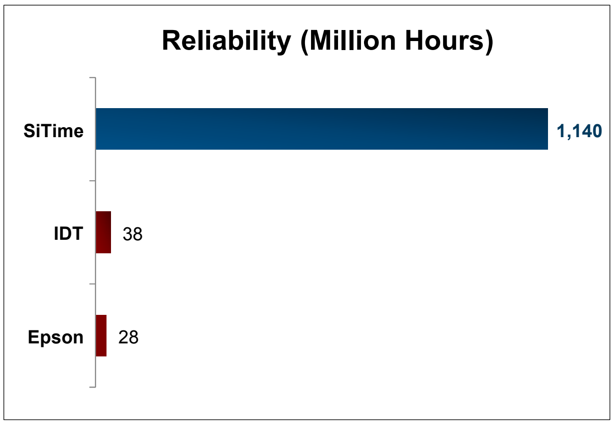


Figure 1. Reliability Comparison[1]

Best Aging

Unlike quartz, MEMS oscillators have excellent long term aging performance which is why every new SiTime product specifies 10-year aging. A comparison is shown in Figure 2.

Why is SiTime Best in Class:

- SiTime's MEMS resonators are vacuum sealed using an advanced EpiSeal process, which eliminates foreign particles and improves long term aging and reliability
- Inherently better immunity of electrostatically driven MEMS resonator

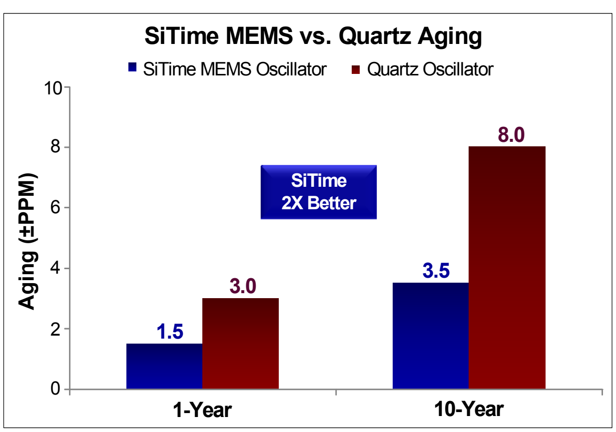


Figure 2. Aging Comparison[2]

Best Electro Magnetic Susceptibility (EMS)

SiTime's oscillators in plastic packages are up to 54 times more immune to external electromagnetic fields than quartz oscillators as shown in Figure 3.

Why is SiTime Best in Class:

- Internal differential architecture for best common mode noise rejection
- Electrostatically driven MEMS resonator is more immune to EMS

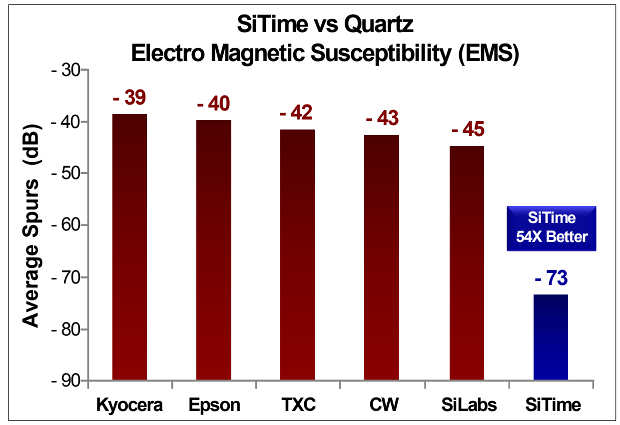


Figure 3. Electro Magnetic Susceptibility (EMS)[3]

Best Power Supply Noise Rejection

SiTime's MEMS oscillators are more resilient against noise on the power supply. A comparison is shown in Figure 4.

Why is SiTime Best in Class:

- On-chip regulators and internal differential architecture for common mode noise rejection
- Best analog CMOS design expertise

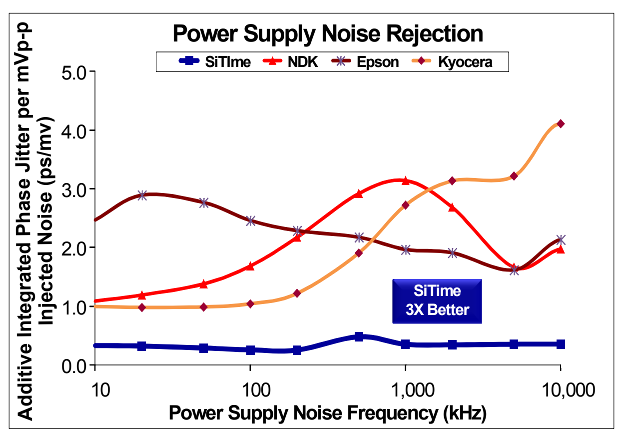


Figure 4. Power Supply Noise Rejection[4]

Silicon MEMS Outperforms Quartz

Best Vibration Robustness

High-vibration environments are all around us. All electronics, from handheld devices to enterprise servers and storage systems are subject to vibration. Figure 5 shows a comparison of vibration robustness.

Why is SiTime Best in Class:

- The moving mass of SiTime's MEMS resonators is up to 3000 times smaller than quartz
- Center-anchored MEMS resonator is the most robust design

Best Shock Robustness

SiTime's oscillators can withstand at least 50,000 *g* shock. They all maintain their electrical performance in operation during shock events. A comparison with quartz devices is shown in Figure 6.

Why is SiTime Best in Class:

- The moving mass of SiTime's MEMS resonators is up to 3000 times smaller than quartz
- Center-anchored MEMS resonator is the most robust design

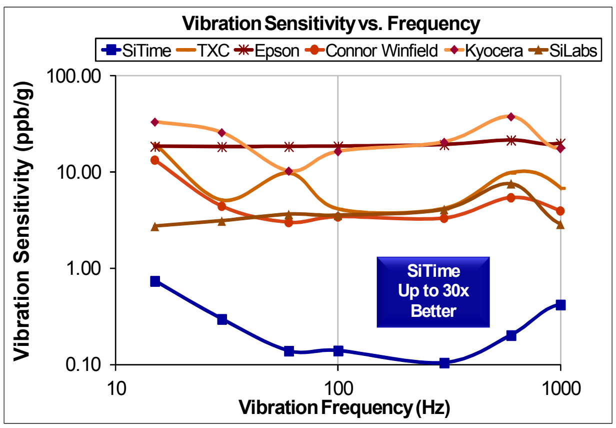


Figure 5. Vibration Robustness[5]

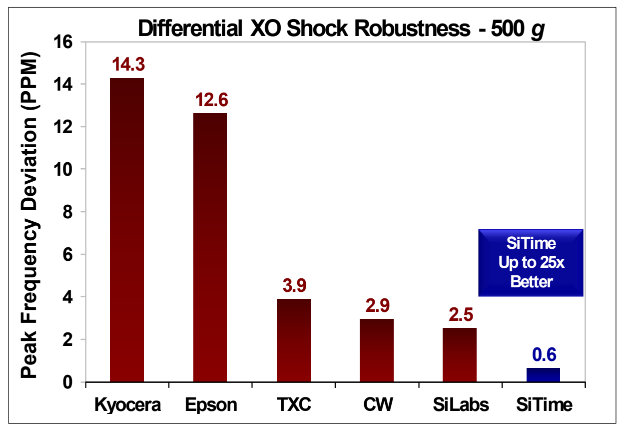


Figure 6. Shock Robustness[6]

Notes:

1. Data Source: Reliability documents of named companies.
2. Data source: SiTime and quartz oscillator devices datasheets.
3. Test conditions for Electro Magnetic Susceptibility (EMS):
   - According to IEC EN61000-4.3 (Electromagnetic compatibility standard)
   - Field strength: 3V/m
   - Radiated signal modulation: AM 1 kHz at 80% depth
   - Carrier frequency scan: 80 MHz – 1 GHz in 1% steps
   - Antenna polarization: Vertical
   - DUT position: Center aligned to antenna

   Devices used in this test:
   SiTime, SiT9120AC-1D2-33E156.250000 - MEMS based - 156.25 MHz
   Epson, EG-2102CA 156.2500M-PHPAL3 - SAW based - 156.25 MHz
   TXC, BB-156.250MBE-T - 3rd Overtone quartz based - 156.25 MHz
   Kyocera, KC7050T156.250P30E00 - SAW based - 156.25 MHz
   Connor Winfield (CW), P123-156.25M - 3rd overtone quartz based - 156.25 MHz
   SiLabs, Si590AB-BDG - 3rd overtone quartz based - 156.25 MHz
4. 50 mV pk-pk Sinusoidal voltage.

   Devices used in this test:
   SiTime, SiT8208AI-33-33E-25.000000, MEMS based - 25 MHz
   NDK, NZ2523SB-25.6M - quartz based - 25.6 MHz
   Kyocera, KC2016B25M0C1GE00 - quartz based - 25 MHz
   Epson, SG-310SCF-25M0-MB3 - quartz based - 25 MHz
5. **Devices used in this test:** same as EMS test stated in Note 3.
6. Test conditions for shock test:
   - MIL-STD-883F Method 2002
   - Condition A: half sine wave shock pulse, 500-g, 1ms
   - Continuous frequency measurement in 100 μs gate time for 10 seconds

   Devices used in this test: same as EMS test stated in Note 3
7. Additional data, including setup and detailed results, is available upon request to qualified customers. Please contact productsupport@sitime.com.

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1. Does the Electrical Characteristics table provide complete information? ◯ Yes ◯ No

If No, what parameters are missing?

____

2. Is the organization of this document easy to follow? ◯ Yes ◯ No

If "No," please suggest improvements that we can make:

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3. Is there any application specific information that you would like to see in this document? (Check all that apply)

☐ EMI ☐ Termination recommendations ☐ Shock and vibration performance ☐ Other

If "Other," please specify:

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4. Are there any errors in this document? ◯ Yes ◯ No

If "Yes", please specify (what and where):

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